



US006140226A

# United States Patent [19]

Grill et al.

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[45] Date of Patent: **Oct. 31, 2000**

[54] **DUAL DAMASCENE PROCESSING FOR SEMICONDUCTOR CHIP INTERCONNECTS**

5,882,996 3/1999 Dai ..... 438/597

### FOREIGN PATENT DOCUMENTS

905768 3/1999 European Pat. Off. .

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[75] Inventors: **Alfred Grill**, White Plains; **John Patrick Hummel**, Millbrook; **Christopher Vincent Jahnes**, Monsey; **Vishnubhai Vitthalbhai Patel**, Yorktown Heights; **Katherine Lynn Saenger**, Ossining, all of N.Y.

[57] **ABSTRACT**

[73] Assignee: **International Business Machines Corporation**, Armonk, N.Y.

The present invention relates to lithographic methods for forming a dual relief pattern in a substrate, and the application of such methods to fabricating multilevel interconnect structures in semiconductor chips by a Dual Damascene process in which dual relief cavities formed in a dielectric are filled with conductive material to form the wiring and via levels. The invention comprises a twice patterned single mask layer Dual Damascene process modified by the addition of an easy-to-integrate sidewall liner to protect organic interlevel and intralevel dielectrics from potential damage induced by photoresist stripping steps during lithographic rework. The invention further comprises a method for forming a dual pattern hard mask which may be used to form dual relief cavities for use in Dual Damascene processing, said dual pattern hard mask comprising a first set of one or more layers with a first pattern, and a second set of one or more layers with a second pattern.

[21] Appl. No.: **09/126,212**

[22] Filed: **Jul. 30, 1998**

### Related U.S. Application Data

[60] Provisional application No. 60/071,628, Jan. 16, 1998.

[51] Int. Cl.<sup>7</sup> ..... **H01L 21/4763**

[52] U.S. Cl. .... **438/637; 438/701; 438/638**

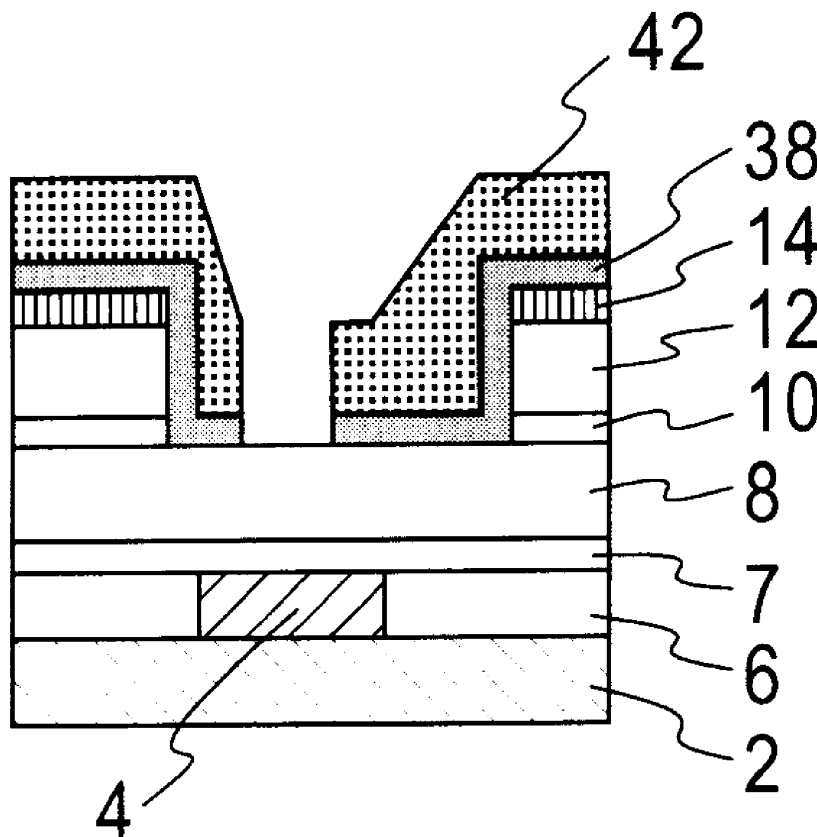
[58] Field of Search ..... 438/637, 636, 438/700, 701, 702, 638, 640

### [56] References Cited

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5,604,156 2/1997 Chung et al. .

**48 Claims, 8 Drawing Sheets**



PRIOR ART

Fig. 1A

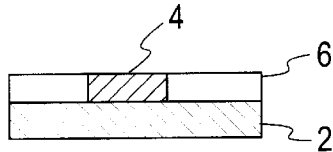


Fig. 1B

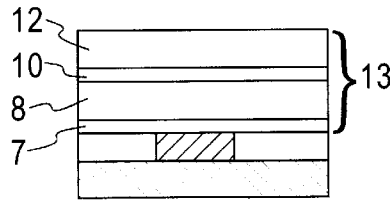


Fig. 1C

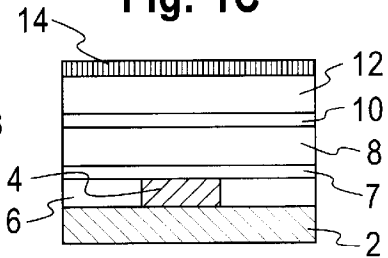


Fig. 1D

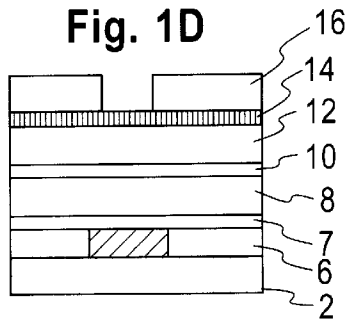


Fig. 1E

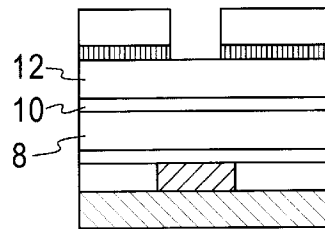


Fig. 1F

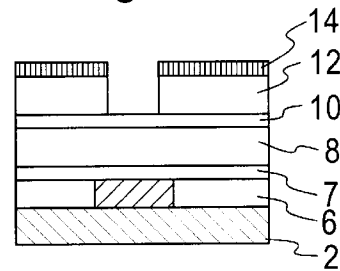


Fig. 1G

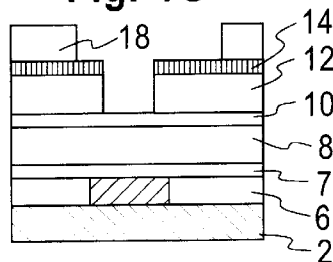


Fig. 1H

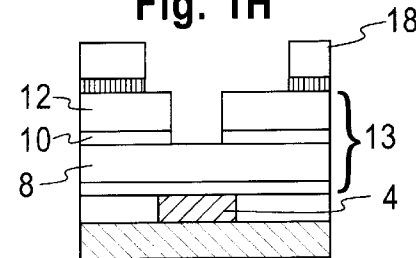


Fig. 1I

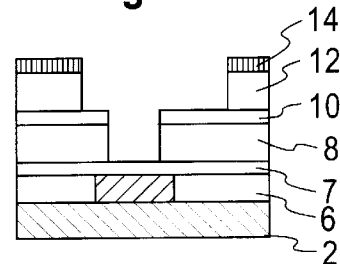


Fig. 1J

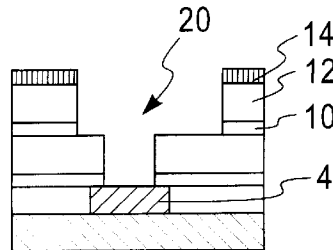


Fig. 1K

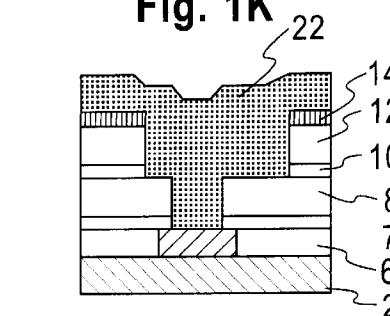


Fig. 1L

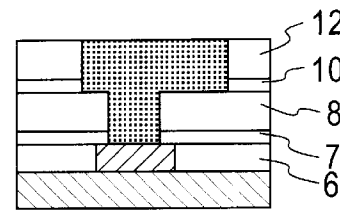


Fig. 2A

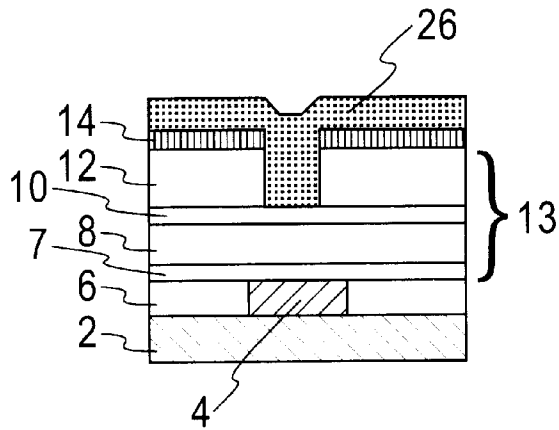


Fig. 2B

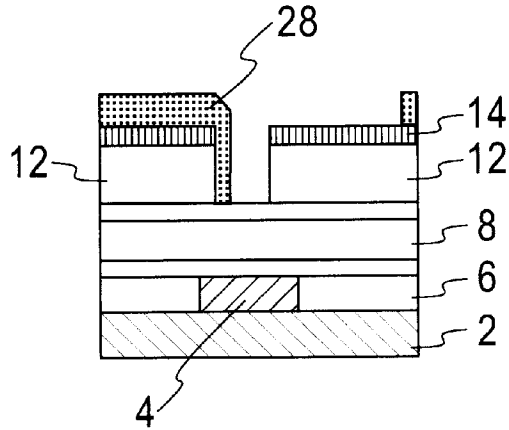


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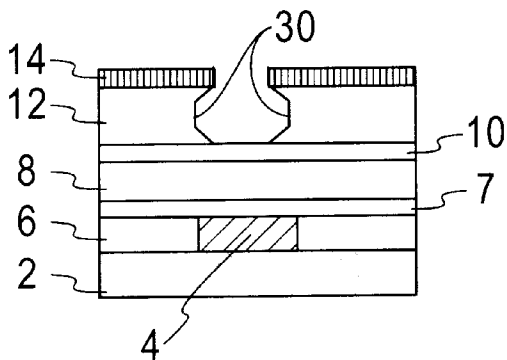
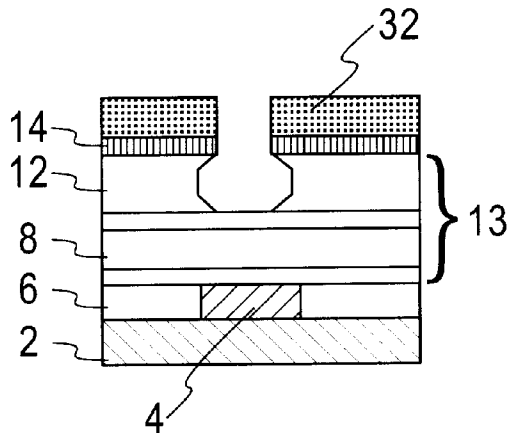


Fig. 2D



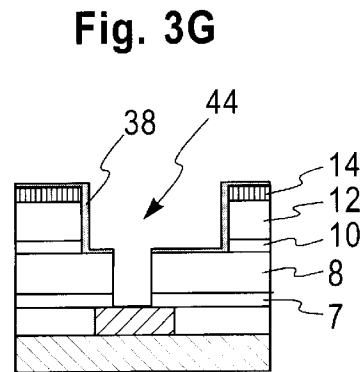
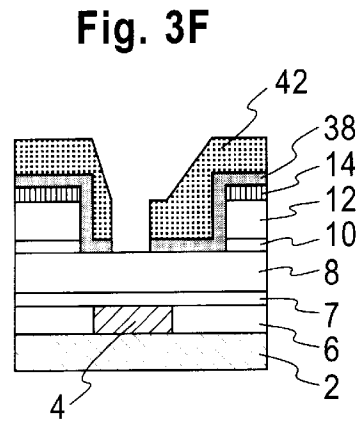
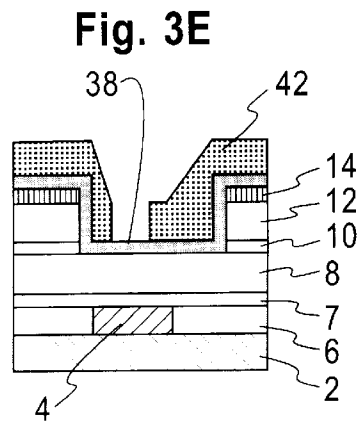
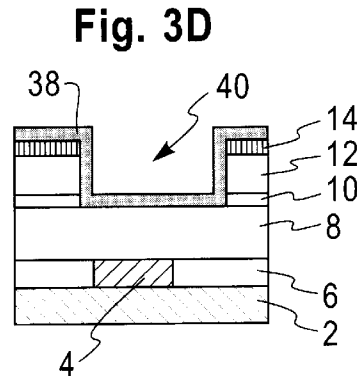
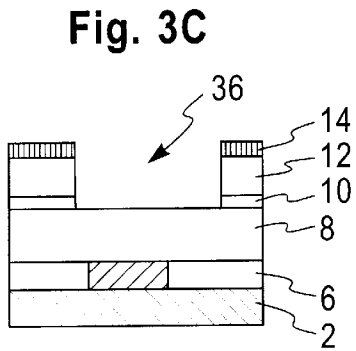
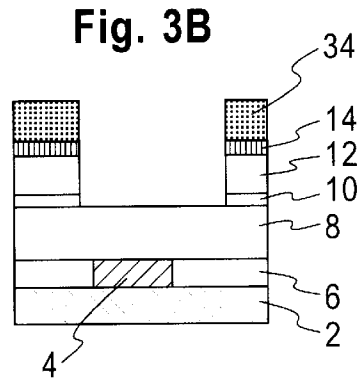
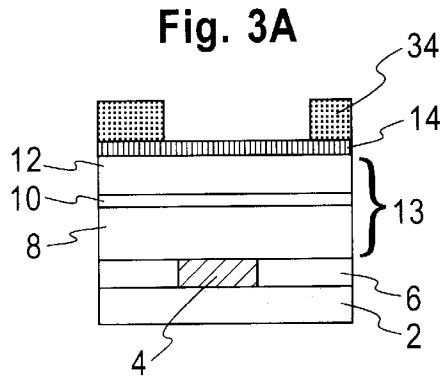


Fig. 4A

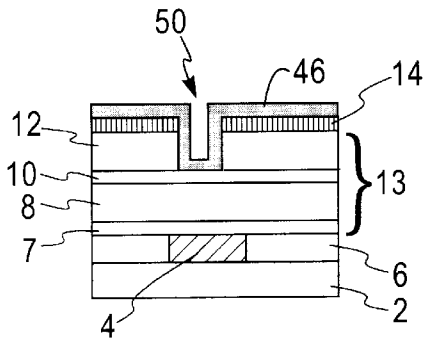


Fig. 4B

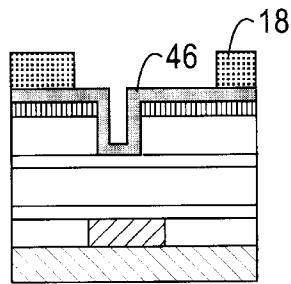


Fig. 4C

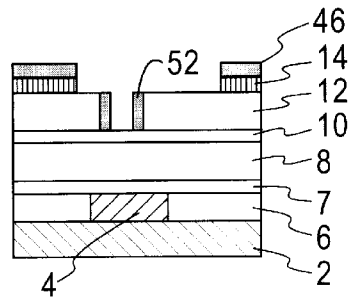


Fig. 4D

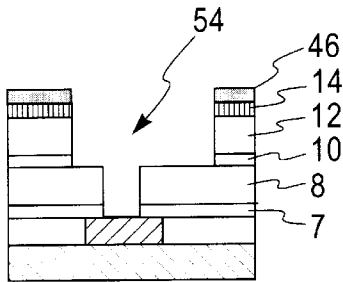


Fig. 4E

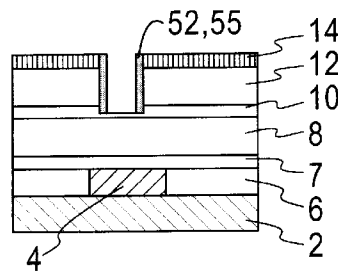
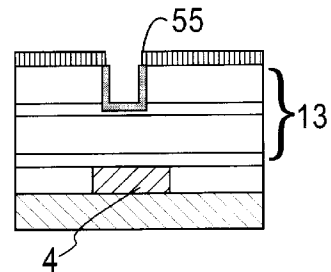


Fig. 4F



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