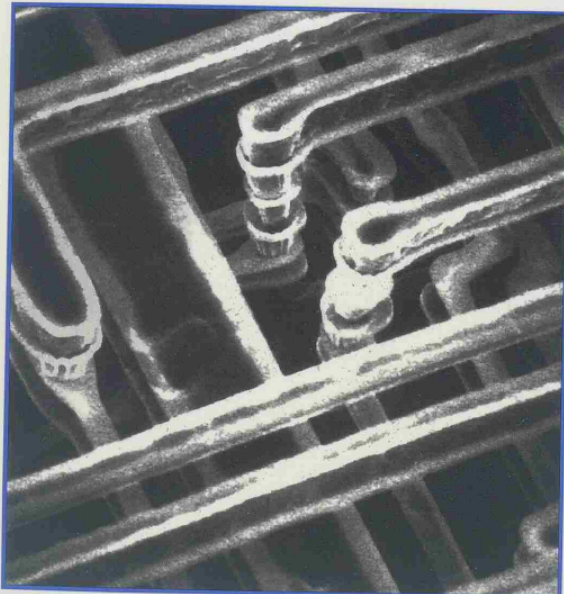
Proceedings of the

IITC International Interconnect Technology Conference



June 1-3, 1998

Hyatt Regency Airport Hotel, San Francisco, California

The IITC is sponsored by the IEEE Electron Devices Society. Its goal is to provide a forum for professionals in semiconductor processing, academia and equipment development to present and discuss exciting new science and technology.

Sponsored by the IEEE Electron Devices Society

Proceedings of the

IEEE 1998 INTERNATIONAL INTERCONNECT TECHNOLOGY CONFERENCE

Hyatt Regency Hotel
San Francisco, CA

June 1 - 3, 1998

The IITC is sponsored by the IEEE Electron Devices Society. Its goal is to provide a forum for professionals in semiconductor processing, academia and equipment development to present and discuss exciting new science and technology.

1998 International Interconnect Technology Conference
Digest of Technical Papers

Papers have been printed without editing as received from the authors.

Copyright and Reprint Permissions: Abstracting is permitted with credit to the source. Libraries are permitted to photocopy beyond the limit of U.S. Copyright law for private use of patrons those articles in this volume that carry a code at the bottom of the first page, provided the per-copy fee indicated in the code is paid through the Copyright Clearance Center, 222 Rosewood Drive, Danvers, MA 01923. For other copying, reprint or republication permission, write to IEEE Copyrights Manager, IEEE Service Center, 445 Hoes Lane, P.O. Box 1331, Piscataway, NJ 08855-1331. All rights reserved.
Copyright © 1998 by the Institute of Electrical and Electronics Engineers, Inc.

PRINTED IN THE UNITED STATES OF AMERICA

TK 7871
.85
.I5795
1998

Additional copies may be ordered from:
IEEE Order Dept.
445 Hoes Lane
Piscataway, NJ 08855
TEL: (800) 678-4333

IEEE Catalog Number: 98EX102
ISBN: 0-7803-4285-2 (Softbound)
ISBN: 0-7803-4286-0 (Microfiche)
Library of Congress: 97-80205

97-80205

TECHNICAL SESSIONS

Monday, June 1

PLENARY SESSION

8:15 **Welcome**
Robert Havemann, General Conference Chair

8:30 / 1.1 **Interconnection Challenges and the National Technology Roadmap for Semiconductors** 3
C.S. Chang, K.A. Monnig and M. Melliar-Smith, SEMATECH, Austin, TX

9:05 / 1.2 **IP Revolution and Multi-level Metallization** 7
Susumu Kohyama, Corporate Director and President, Toshiba Corporation

9:40 / 1.3 **Industry Challenges for System-on-a-Chip** 10
Davoud Samani, Vice President, Semiconductor Group, Siemens AG

SESSION 2: INTERCONNECT TECHNOLOGY TRENDS

Co-Chairs: James Meindl and Hans-Joachim Barth

10:30 / 2.1 **Invited - On-Chip Interconnects - Giga Hertz and Beyond** 15
K. Lee, Hewlett-Packard, Palo Alto, CA

10:55 / 2.2 **Spiral and Solenoidal Inductor Structures on Silicon Using Cu-Damascene Interconnects** 18
D.C. Edelstein and J.N. Burghartz, IBM, Yorktown Heights, NY

11:20 / 2.3 **Characteristics of Integrated Dipole Antennas on Bulk, SOI, and SOS Substrates for Wireless Communication** 21
K. Kim and K.K. O, University of Florida, Gainesville, FL

SESSION 3: INTERCONNECT RELIABILITY I

Co-chair: Konrad Hieber

2:30 / 3.1 **Invited - Incubation, Time-Dependent Drift and Saturation During Al-Si-Cu Electromigration: Modeling and Implications for Design** 27
A. Witvrouw*, P. Roussel*, G. Beyer*, J. Proost*, K. Maex*, *IMEC, Leuven, Belgium, and **INSYS, K.U., Leuven, Belgium

2:55 / 3.2 **Molecular Dynamics Simulation of Al Grain Boundary Diffusion for Electromigration Failure Analysis** 30
T. Shinzawa and T. Ohta, NEC Corp., Kanagawa, Japan

3:20 / 3.3 **Plasma Damage Mechanisms in Via Fabrication** 33
J. Werking, W. Brennan* and G. Bersuker, SEMATECH, Austin, TX and *Advanced Micro Devices, Austin, TX

SESSION 4: INORGANIC LOW K DIELECTRIC INTEGRATION

Co-chairs: Michael Thomas and Nobuo Hayasaka

4:00 4.1 — 4:00 **A Manufacturable Embedded Fluorinated SiO_2 for Advanced 0.25 μm CMOS VLSI Multilevel Interconnect Applications** — 39
C.S. Pai, A.N. Velaga*, W.S. Lindenberger, W.Y.-C. Lai, K.P. Cheung, F.H. Baumann, C.P. Chang, C.T. Liu, R. Liu, P.W. Diodato, J.I. Colonell, H. Vaidya, S.C. Vitkavage*, J.T. Clemens and F. Tsubokura**, Lucent Technologies, Murray Hill, NJ, *Orlando, FL and **NEC Corporation, Kanagawa, Japan

4:25 4.2 — **Highly Reliable Low-ε (3.3) SiOF HDP-CVD for Subquarter-Micron CMOS Applications** — 42
T. Fukuda, T. Hosokawa, E. Sasaki, and N. Kobayashi, Hitachi, Ltd., Tokyo, Japan

4:50 4.3 — **Integration of Unlanded Via in a Non-Etchback SOG Direct-on-Metal Approach in 0.25 Micron CMOS Process** — 45
T. Gao*, B. Coenegrachts*, J. Waeterloos*, G. Beyer*, H. Meynen*, M. Van Hove* and K. Maex*,**, IMEC, Leuven, Belgium and **INSYS, K.U., Leuven, Belgium

5:15 4.4 — **Suppressing Oxidization of Hydrogen Silsesquioxane Films by Using H_2O Plasma in Ashing Process** — 48
E. Tamaoka, T. Ueda, N. Aoi and S. Mayumi, Matsushita Electronics Corp., Kyoto, Japan

Tuesday, June 2

SESSION 5: IMPACT ON CIRCUIT PERFORMANCE

Co-chairs: Krishna Saraswat and Genda Hu

8:30 5.1 — **Invited - Impact of Interconnect on Circuit Design Performance** — 53
J-P. Schoellkopf, SGS-Thomson, Crolles, France

8:55 5.2 — 8:55 **Minimum Repeater Count, Size, and Energy Dissipation for Gigascale Integration (GSI) Interconnects** — 56
J.C. Eble, V.K. De*, D.S. Wills and J.D. Meindl, Georgia Institute of Technology, Atlanta, GA and *Intel Corp., Hillsboro, OR

9:20 5.3 — **Low-k Dielectrics Influence on Crosstalk: Electromagnetic Analysis and Characterization** — 59
C. Cregut, G. Le Carval* and J. Chilo, PFT-CEM, St Martin d'Heres, France and *LETI/CEA, Grenoble, France

9:45 5.4 — **Advanced Wiring RC Delay Issues for sub-0.25-micron Generation CMOS** — 62
A.K. Stamper, M.B. Fuselier and X. Tian, IBM Microelectronics, Essex Junction VT

SESSION 6: CHEMICAL MECHANICAL POLISHING

Co-chairs: Gary Ray and Michel Brillouet

10:25 6.1 **An Integrated Characterization and Modeling Methodology for CMP Dielectric Planarization** — 67
D. Ouma, D. Boning, J. Chung, G. Shinn, L. Olsen* and J. Clark*, Massachusetts Institute of Technology, Cambridge, MA and *Texas Instruments, Inc., Dallas, TX

10:50 6.2 **Chemical Mechanical Polishing of Aluminum for the .18 μm Dual Damascene Process** — 70
S. Kordic, C.A.H. Mutsaers, H. Lifka and M.N. Webster, Philips Research, Eindhoven, The Netherlands

11:15 6.3 **A New Theory for CMP with Soft Pads** — 73
F. G. Shi, B. Zhao* and S.-Q. Wang**, University of California, Irvine, CA, *Rockwell Semiconductor Systems, Newport Beach, CA and ** AlliedSignal Advanced Microelectronic Materials, Sunnyvale, CA

11:40 6.4 **Control of Dielectric Chemical Mechanical Polishing (CMP) Using an Interferometry Based Endpoint Sensor** — 76
S. J. Fang, A. Barda*, T. Janecko*, W. Little, D. Outley*, G. Hempel*, S. Joshi, B. Morrison, G.B. Shinn and M. Birang*, Texas Instruments, Dallas, TX and *Applied Materials, Santa Clara, CA

SESSION 7: ADVANCED INTERCONNECT PROCESSES

Co-chair: Robin Cheung

2:30 7.1 **Solid Phase Replacement Process for Multilevel High-Aspect Ratio Al Fill Applications** — 81
A. Sakata, J. Wada, T. Katata, N. Hayasaka and K. Okumura, Toshiba Corp., Yokohama, Japan

2:55 7.2 **Inorganic ARC for 0.18μm and Sub-0.18μm Multilevel Metal Interconnect** — 84
W.W. Lee, Q. He, G. Xing, A. Singh, E. Zielinski, K. Brennan, G. Dixit, K. Taylor, C.-S. Liang, J.D. Luttmer and B. Havemann, Texas Instruments, Dallas, TX

3:20 7.3 **Dielectric Anti-Reflection Coating Application in a 0.175 μm Dual-Damascene Process** — 87
G.Y. Lee, Z.G. Lu, D.M. Dobuzinsky*, X.J. Ning, and G. Costrini*, Siemens Microelectronics, Inc. and *IBM Microelectronics, Hopewell Junction, NY

SESSION 8: SILICIDES AND DIFFUSION BARRIERS

Co-chairs: George Cumming and Robert Wolters

4:00 8.1 **A Dual SALICIDE Process Scalable to Sub-0.25-μm CMOS Technologies** — 93
X.W. Lin, M. Weling and D. Pramanik, VLSI Technology, Inc., San Jose, CA

4:25 8.2 **Comparison of PECVD-WNx and CVD-TiN Films for the Upper Electrode of Ta_2O_5 Capacitors** — 96
B.-L. Park, M.-B. Lee, K.-J. Moon, H.-D. Lee, H.-K. Kang and M.-Y. Lee, Samsung Electronics Co. Ltd., Kyungki, Korea

4:50 8.3 **Performance and Manufacturability of the Co/Ti (Cap) Silicidation Process for 0.25μm MOS-Technologies** 99
A. Lauwers, P. Besser**, M. de Potter, E. Kondoh, N. Roelandts, A. Steegen, M. Stucchi and K. Maex*, IMEC, Leuven, Belgium, *IMEC & INSYS, K. U., Leuven, Belgium, and **Advanced Micro Devices, Sunnyvale, CA

5:15 8.4 **Low Temperature Processing of Conformal TiN by ACVD (Advanced Chemical Vapor Deposition) for Multilevel Metallization in High Density ULSI Devices** 102
S.B. Kang, Y.S. Chae, M.Y. Yoon, H.S. Leem, C.S. Park, S.I. Lee, and M.Y. Lee, Samsung Electronics Co. Ltd., Kyungki, Korea

Wednesday, June 3

SESSION 9: INTERCONNECT RELIABILITY II

Co-chairs: Mark Kushner and Hans-Joachim Barth

8:30 9.1 **Invited - Barrier/Seed Layer Requirements for Copper Interconnects** 107
S. S.Wong, C. Ryu, H. Lee, A. Loke, K-W. Kwon, S. Bhattacharya*, R. Eaton*, R. Faust, R. Mikkola*, J. Mucha* and J. Ormando*, Stanford University, Stanford, CA and SEMATECH, Austin, TX

8:55 9.2 **Electromigration Behaviour of 0.3 μm Damascene vs. Plasma-Etched Interconnects: A Lifetime and Drift Analysis** 110
J. Proost*, H. Li*, B. Brijs*, A. Witvrouw*, K. Maex*,**, *IMEC and **INSYS, K.U., Leuven, Belgium

9:20 9.3 **Stacked Film Structured Dependence of Electro- migration in Al-Cu Interconnect Terminated with W Plug** 113
S. Matsumoto, R. Etoh, T. Ohtsuka, T. Kouzaki* and S. Ogawa, Matsushita Electronics Corp., Kyoto, Japan and *Matsushita Techno Research Inc., Osaka, Japan

9:45 9.4 **Effects of W-Plug Via Arrangement on Electromigration Lifetime of Wide Line Interconnects** 116
S. Skala and S. Bothra, VLSI Technology, Inc., San Jose, CA

10:10 9.5 **Uniform (111) Textured Cu CVD on Vacuum Annealed Cu Seed Layer** 119
K. Ueno, A. Sekiguchi* and A. Kobayashi*, NEC Corp., Kanagawa, Japan and *Anelva Corp., Tokyo, Japan

SESSION 10: ORGANIC LOW K MATERIALS

Co-chair: Robert Geffken, IBM

10:50 10.1 **Integration and Reliability Issues for Low Capacitance Air-Gap Interconnect Structures** 125
B.P. Shieh, L.C. Bassman, D.-K. Kim, K.C. Saraswat, M.D. Deal, J.P. McVittie, R.S. List*, S. Nag* and L. Ting*, Stanford University, Stanford, CA and *Texas Instruments, Dallas, TX

11:15 10.2 **The Effect of Thermal Cycling on a-C:F,H Low Dielectric Constant Films Deposited by ECR Plasma Enhanced Chemical Vapor Deposition** 128
J. A. Theil, G. Kooi, F. Mertz, G. Ray and K. Seaward, Hewlett-Packard Co., Palo Alto, CA

11:40 10.3	**Integration of Organic Low-k Material with Cu-Damascene Employing Novel Process** M. Ikeda, H. Kudo, R. Shinohara, F. Shimpuku, M. Yamada and Y. Furumura, Fujitsu Ltd., Kawasaki, Japan	131

SESSION 11: ALUMINUM DUAL DAMASCENE

Co-chairs: Mehdi Moussavi and Nobuyoshi Kobayashi

1:00 11.1	**A Novel Low Temperature CVD/PVD Al Filling Process for Producing Highly Reliable 0.175 µm Wiring/0.35µm Pitch Dual Damascene Interconnections in Gigabit Scale DRAMS** L.A. Clevenger, G. Costrini, D.M. Dobuzinsky, R. Filippi, J. Gambino, M. Hoinkis, L. Gignac, J.L. Hurd, R.C. Iggulden, C. Lin, R. Longo, G.Z. Lu, J. Ning, J.F. Nuetzel, R. Ploessl, K. Rodbell, M. Ronay, R.F. Schnabel, D. Tobben, S.J. Weber, L. Chen*, S. Chiang*, T. Guo*, R. Mosely*, S. Voss*, and L. Yang*, IBM/Siemens DRAM Development Alliance, Hopewell Junction, NY and *Applied Materials Corporation, Santa Clara, CA	137
1:25 11.2	**Comparative Study of W-plug, Al-plug and Al-Dual Damascene for 0.18 µm ULSI Multilevel Interconnect Technologies** K. Kikuta, T. Takewaki, Y. Kakuhara, K. Fujii, and Y. Hayashi, NEC Corp., Kanagawa, Japan	140
1:50 11.3	**High Performance Al Dual Damascene Process with Elevated Double Stoppers** N. Nakamura, M. B. Anand, J. Wada, Y. Oikawa, T. Katata, K. Shiba and H. Shibata, Toshiba Corp., Kanagawa, Japan	143
2:15 11.4	**Aluminum Dual Damascene Interconnects with Low-k Intra/Inter-Level Dielectric for Reduced Capacitance and Low Cost** B. Zhao, D. Feiler, Q.Z. Liu, C.H. Nguyen, M. Brongo, J. Kuei, V. Ramanathan, J. Wu, H. Zhang, M. Rumer*, M.A. Biberger*, V. Sachan** and D. James**, Rockwell Semiconductor Systems, Newport Beach, CA, *Novellus Systems, Palo Alto, CA, and **Rodei, Newark, DE	146

SESSION 12: COPPER INTERCONNECT

Co-chairs: Betsy Weitzman and Yuji Furumura

2:55 12.1	**Invited - Copper Dual Damascene for Sub-0.25um CMOS** J. Heidenreich*, D. Edelstein, R. Goldblatt, W. Cote, C. Uzoh, N. Lustig, T. McDevitt*, A. Stamper*, A. Simon, J. Dukovic, P. Andriacacos, R. Washnik, H. Rathore, T. Katsetos, P. McLaughlin, S. Luce*, and J. Slattery*, IBM Semiconductor R&D Center, Hopewell Junction, NY and *IBM Microelectronics, Essex Junction, VT	151
3:20 12.2	**Integration Aspects for Damascene Copper Inter-connect in Low K Dielectric** V. Blaschke, G. Bersuker, R. Muralidhar, M. Breen, R. Mikkola, J. Mucha, B. Fowler, M. Marsden, A. Wang, S. Dempsey, A. Schmidt and K. Monnig, SEMATECH, Austin, TX	154
3:45 12.3	**Growth Morphology of Electroplated Copper: Effect of Seed Material and Current Density** C.H. Seah, S. Mridha and L.H. Chan*, Nanyang Technological University, Singapore and *Chartered Semiconductor Manufacturing, Ltd., Singapore	157

4:10 12.4	**Impact of Low Pressure Long Throw Sputtering Method on Submicron Copper Metallization** T. Saito, N. Ohashi, J. Yasuda, J. Noguchi, T. Imai, K. Sasajima, K. Hiruma, H. Yamaguchi and N. Owada, Hitachi Ltd., Tokyo, Japan	160
4:35 12.5	**CVD Cu Process Integration for Sub-0.25 μm Technologies** J. Zhang, D. Denning, G. Braeckelmann, R. Venkatraman, R. Fiordalice and E. Weitzman, Motorola Inc., Austin, TX	163
5:00 12.6	**Self-Annealing of Electrochemically Deposited Copper Films in Advanced Interconnect Applications** T. Ritzdorf, L. Graham, S. Jin*, C. Mu* and D. Fraser*, Semitool, Inc., Kalispell, MT and *Intel Corp., Santa Clara, CA	166
5:25 12.7	**A Novel Cu-Plug Formation Using High Pressure Reflow Process** K. Maekawa, T. Yamamura*, T.Fukada, A. Ohsaki and H. Miyoshi, Mitsubishi Electric Corp., Hyogo, Japan and *Ryoden Semiconductor System Engineering Corp., Japan	169

POSTER SESSION I

P1.1	**Effects of PECVD Deposition Fluxes on the Spatial Variation of Thin Film Density of As-Deposited SiO2 Films in Interconnect Structures**, K. Lee, M. Deal, J. McVittie, J. Plummer and K. Saraswat, Stanford University, Stanford, CA	175
P1.2	**Modeling of Metal-over-Silicon Microstrip Interconnections: The Effect of SiO2 Thickness on Slow-Wave Losses**, L. Wang, Y.L. Le Coz, R.B. Iverson and J.F. McDonald, Rensselaer Polytechnic Institute, Troy, NY	178
P1.3	**Application of Charge Based Capacitance Measurement (CBCM) Technique in Interconnect Process Development**, S. Bothra, G.A. Rezvani, H. Sur, M. Farr, and J.N. Shenoy, VLSI Technology, Inc., San Jose, CA	181
P1.4	**Stochastic Interconnect Network Fan-Out Distribution Using Rent's Rule**, P. Zarkesh-Ha, J.A. Davis, W. Loh* and J.D. Meindl, Georgia Institute of Technology, Atlanta, GA and *LSI Logic Corp., Milpitas, CA	184
P1.5	**Robustness of Self-Aligned Titanium Silicide Process: Improvement in Yield of Silicided Devices with APM Cleaning Step**, C.W. Lim*,**, K.H. Lee**, K.L. Pey**, H. Gong*, A.J. Bourdillon*, S.K. Lahiri*, *National University of Singapore and **Chartered Semiconductor Manufacturing Ltd., Singapore	187
P1.6	**The Effects of Stress on the Formation of Titanium Silicide**, S.L. Cheng, H.Y. Huang, Y.C. Peng L.J. Chen, B.Y. Tsui*, C.J. Tsai**, S.S. Guo** and K.H. Yu**, National Tsing Hua University, *ERSO/ITRI, and **National Chung Hsing University, Taiwan, ROC	190
P1.7	**Correlation of Film Thickness and Deposition Temperature with PAI and the Scalability of Ti-SALICIDE Technology to Sub-0.18μm Regime**, C. S.Ho, R.P.G. Karunasiri, S.J. Chua, K.L. Pey*, S.Y. Soh*, K. H. Lee*, and L. H. Chan*, National University of Singapore and *Chartered Semiconductor Manufacturing Ltd., Singapore	193
P1.8	**Interconnect Material and CMP Process Change Effects on Local Interconnect Planarity**, J. Mendonca, C. Dang, C. Pettinato, J. Cope, H. Garcia, J. Saravia, J. Farkas, D. Watts, and J. Klein, Motorola, Inc., Austin, TX	196
P1.9	**One Step Effective Planarization of Shallow Trench Isolation**, H-W. Chiou and L-J. Chen, ERSO/ITRI, Taiwan, ROC	199
P1.10	**Nitrogen Effect on Post-Nucleation Tungsten CVD Film Growth**, R. Petri, H. Hauf*, D. Berenbaum*, J.C. Favreau*, P. Mazet, ATMEL and *Applied Materials, Rousset, France	202

P1.11	**Laser Programmable Metallic Vias**, J.B. Bernstein, W. Zhang and C.H. Nicholas, University of Maryland, College Park, MD	205
P1.12	**New Via Formation Process for Suppressing the Leakage Current Between Adjacent Vias for Hydrogen Silicate Based Inorganic SOG Intermetal Dielectric**, N. Oda, T. Usami, T. Yokoyama, A. Matsumoto, K. Mikagi, H. Gomi, and I. Sakai, NEC Corp., Kanagawa, Japan	208
P1.13	**Study on the Stability of HDP-SiOF Film and IMD Application for 0.25μm LSI Device**, H.J. Shin, S.J. Kim, B.J. Kim, H.K. Kang and M.Y. Lee, Samsung Electronics Co., Kyungki, Korea	211
P1.14	**Chemical Vapor Deposition and Physical Vapor Deposition of Metal/Barrier Binary Stacks on Polytetrafluorethylene Low-k Dielectric**, R. Talevi, S. Nijsten, H. Gundlach, A. Knorr, K. Kumar. Z. Bian, T. Rosenmayer*, A.E. Kaloyeros and R.E. Geer, State University of New York, Albany, NY and *W.L. Gore and Assoc., Eau Claire, WI	214
P1.15	**Integration of Low k Spin-on Polymer (SOP) Using Electron Beam Cure for Non-Etch-Back Application**, J.C.M. Hui, Y. Xu, C.Y. Foong, L. Marvin, L. Charles, L.Y. Shung, A. Inamdar*, J. Yang*, J. Kennedy*, M. Ross* and S.-Q. Wang, Chartered Semiconductor Manufacturing Ltd., Singapore and *AlliedSignal, Inc., Santa Clara, CA	217
P1.16	**A Novel Wholly Aromatic Polyether as an Interlayer Dielectric Material**, T. Tanabe, K. Kita, M. Maruyama, K. Sanechika, M. Kuroki and N. Tamura, Asahi Chemical Industry Co., Ltd., Shizuoka, Japan	220
P1.17	**A Method for Improving the Adhesion of PE-CVD SiO_2 to Cyclotene™ 5021 Polymeric Interlayer Dielectric**, E.O. Shaffer II, M.E. Mills, D.D. Hawn, J.C. Liu* and J.P. Hummel*, The Dow Chemical Co., Midland, MI and *IBM, Hopewell Junction, NY	223
P1.18	**Two-Step Planarized Al-Cu PVD Process Using Long Throw Sputtering Technology**, T.-K. Ku, H.-C. Chen, Y. Mizusawa*, N. Motegi*, T. Kondo*, S. Toyoda*, C. Wei**, J. Chen** and L.-J. Chen, ERSO/ITRI, Taiwan, ROC, *ULVAC Japan, Ltd., Japan, and **ULVAC Taiwan Branch, Taiwan, ROC	226
P1.19	**0.60 μm Pitch Metal Integration in 0.25μm Technology**, J.R.D. DeBord, V. Jayaraman, M. Hewson, W. Lee, S. Nair, H. Shimada, V.L. Linh, J. Robbins, A. Sivasothy, Texas Instruments Inc., Dallas, TX	229
P1.20	**Study of Cu Contamination During Copper Integraton in a Dual Damascene Architecture for Sub-Quarter Micron Technology**, J. Torres, J. Palleau, P. Motte*, F. Tardif** and H. Bernard*, FT/CNET, Meylan, France, *SGS-Thomson Microelectronics, Crolles, France and **CEA/LETI, Grenoble, France	232
P1.21	**Development of Cu Etch Process for Advanced Cu Interconnects**, Y. Ye, D. Ma, A. Zhao, P. Hsieh, W. Tu, X. Deng, G. Chu, C. Mu*, J. Chow*, P. Moon* and S. Sherman*, Applied Materials Inc., Santa Clara, CA and *Intel Corp., Santa Clara, CA	235

POSTER SESSION II

P2.1	**Measurement and Modeling of High-Speed Interconnect-Limited Digital Ring Oscillators: The Effect of Dielectric Anisotropy**, A. Garg, Y. L. Le Coz, H.J. Greub, J.F. McDonald, and R.B. Iverson*, Rensselaer Polytechnic Institute, Troy, NY and *Random Logic Corporation, Fairfax, VA	241
P2.2	**A Case Study of RC Effects to Circuit Performance**, C.S. Pai, P.W. Diodato and R. Liu, Bell Laboratories, Lucent Technologies, Murray Hill, NJ	244
P2.3	**Modeling Microstructure Development in Trench-Interconnect Structures**, J. Sanchez, Jr. and P. R. Besser*, The University of Michigan, Ann Arbor, MI and *Advanced Micro Devices, Sunnyvale, CA	247
P2.4	**SAP – A Program Package for Three-Dimensional Interconnect Simulation**, R. Sabelka and S. Selberherr, Institute for Microelectronics, Vienna, Austria	250

REDACTED

P2.5	**Estimating Interconnect Performance for a New National Technology Roadmap for Semiconductors**, R. Mangaser and K. Rose, Rensselaer Polytechnic Institute, Troy, NY	253
P2.6	**Tantalum Silicide Sputtering Target Material for Amorphous Ta-Si-N Diffusion Barrier for Cu Metallization**, E. Ivanov, Tosoh SMD Inc., Grove City, OH	256
P2.7	**Thermal Stability of WSi_2 Polycide Structures for 1Gbit DRAMs**, J.P. Gambino, M. Weybright, J. Faltermeier and A. Domenicucci, IBM Microelectronics, Hopewell Junction, NY	259
P2.8	**Ionized Metal Plasma Deposition of Titanium and Titanium Nitride for Deep Contact Applications**, B.Y. Yoo, Y.-H. Park, H.-D. Lee, J.H. Kim, H.-K. Kang, M.Y. Lee, H.G. Wang*, K.-S. Lee*, J. Van Gogh*, C.-H. Chu*, S. Lai*, W. McClintock*, S. Edelstein* and F. Chen*, Samsung Electronics Co. Ltd., Kyungki-Do, Korea and *Applied Materials, Santa Clara, CA	262
P2.9	**Titanium-Related Emission Signals for Endpoint Detection During Via Etch Process**, C.H. Low, W.S. Chin, M.S. Zhou*, S.T. Loong*, and L. Chan*, National University of Singapore and *Chartered Semiconductor Manufacturing Ltd., Singapore	265
P2.10	**Etch/Metallization Process Sequence Integration - Impact of Al Texture on Al Etch Performance,** C. Yan, J. Stokes, S. Arias, Y. Ye, D. Ma, L. Chen, S. Subrahmanyan, H. Zhang, S. McArthur, N. Khurana and R. Mosely, Applied Materials, Inc. Santa Clara, CA	268
P2.11	**Integration Aspects of Flowfill and Spin-on-Glass Process for Sub-0.35μm Interconnects**, S. Penka, W. Robl*, R. Strenz*, and P. Baumgartner*, Siemens AG, Munich and *Regensburg, Germany	271
P2.12	**Characterization of the HDP-CVD Oxide as Interlayer Dielectric Material for Sub-quarter Micron CMOS**, J.W. Kim, J.B. Lee, J.G. Hong, B.K. Hwang, S.T. Kim and M. S. Han, Samsung Electronics Co., Ltd., Kyungki, Korea	274
P2.13	**Integration Study of Benzocyclobutene with CVD-Based Aluminum Metallization**, H. Gundlach. A. Knorr, S. Nijsten, K. Kumar, Z. Bian, R. Talevi, E.O. Shaffer*, A.E. Kaloyeros and R.E. Geer, State University of New York, Albany, NY and *The Dow Chemical Co., Midland, MI	277
P2.14	**Adhesion of Fluorinated Amorphous Carbon to Various Materials**, T.W. Mountsier and J.A. Samuels, Novellus Systems, Inc., San Jose, CA	280
P2.15	**An Oxide Cap Process for a PTFE-Based IC Dielectric**, T. Rosenmayer, J. Hammes, J. Bartz and P. Spevack, W.L. Gore & Assoc., Inc., Eau Claire, WI	283
P2.16	**A New Low Dielectric Constant Siloxane Polymer: Accuspin® T-24**, N.P. Hacker, L.K. Figge, V. Flores and S.P. Lefferts, AlliedSignal Advanced Microelectronic Materials, Sunnyvale, CA	286
P2.17	**Analysis of Blech Product Threshold in Passivated AlCu Interconnections**, L. Arnaud, G. Tartavel, P. Waltz and L. Ulmer, CEA-G / LETI, Grenoble, France	289
P2.18	**Characterization and Integration of Hollow Cathode Magnetron Sputtered Ti/TiN with Low Pressure Al Planarization**, K.F. Lai, L.M. Tam and Q. Lu, Novellus Systems, Palo Alto, CA	292
P2.19	**Comparison of Barrier Materials and Deposition Processes for Copper Integration**, M. Moussavi, Y. Gobil, L. Ulmer, L. Perroud, P. Motte***, J. Torres*, F. Romagna*, M. Fayolle, J. Palleau*, and M. Plissonnier**, LETI/CEA, Grenoble, *France Telecom, Meylan, **Applied Materials France, Meylan, and ***SGS Thomson Microelectronics, Crolles, France	295
P2.20	**Characterization of the Cu/Barrier Metal Interface for Copper Interconnects**, T. Nogami, J. Romero, V. Dubin, D. Brown and E. Adem, Advanced Micro Devices, Inc., Sunnyvale, CA	298
P2.21	**CVD Copper Metal for Poly-Si Thin Film Transistor**, S. He and T. Nguyen, Sharp Microelectronics Technology Inc., Camas, WA	301

Comparison of Barrier Materials and Deposition Processes for Copper Integration

M. Moussavi, Y. Gobil, L. Ulmer, L. Perroud, P. Motte***, J. Torrès*, F. Romagna*, M. Fayolle, J. Palleau* and M. Plissonnier**

LETI (CEA Technologies Avancées). DMEL-CEA/G - 17, rue des Martyrs - 38054 Grenoble cedex 9, France
*FRANCE TELECOM , CNETT/CNS, BP 98, 38243 Meylan cedex, France
**Applied Materials France 11B, chemin de la Dhuy, 38246 Meylan cedex, France
***SGS Thomson Microelectronics 850 rue Jean Monnet, 38926 Crolles cedex, France

Abstract

This paper reports the investigation of MOCVD (Metal Organic Chemical Vapor Deposition) TiN, and IMP (Ionized Metal Plasma) Ta and TaN thin films as barrier layers for copper metallization. Evaluation of both deposition techniques including step coverage, Cu adhesion, Cu diffusion and selectivity regarding Cu-CMP process have been performed. Successful implementation with copper metallization in high aspect ratio line and via patterns is reported.

Introduction

As circuit integration density continuously increases, interconnection size is predicted to decrease both in vertical and lateral dimensions. Unfortunately, intrinsic properties of the materials currently used for interconnection such as resistivity and electromigration performance do not allow an optimal scaling. This explains the growing interest in copper for overcoming limitations of the conventional aluminium based alloys (1,2). The two most critical aspects for integration of copper metallization are the optimal choice of diffusion barrier material - the Cu diffusion in the active areas resulting into degradation of the devices- and diffusion barrier material and copper deposition techniques. The barrier layer should meet stringent requirements : the thickness has to be small enough to not impact interconnect resistance while still acting as a good barrier against Cu diffusion. Several barrier materials have been reported as good candidates. TiN barrier, currently used with Al-based metallization, has shown convenient results (3). However other papers suggest that Tantalum and Tantalum nitride could be the best choice. In this work a comprehensive comparison of the TiN, Ta and TaN performance was carried out with regards to Cu integration. A variety of solutions have been developed to deposit copper : Ionized Metal Plasma, CVD, combination of these techniques and the new electroplating method.

Experimental

A. Barrier Materials

An Applied Materials Endura system using IMP (Ionized Metal Plasma) was used to deposit Ta and TaN barriers. Prior to film deposition, wafers were degassed at 350°C and sputter cleaned using a standard AMAT PCII reactor. CVD TiN was performed in P5000 reactor using TDMAT precursor with successive steps of deposition and plasma treatments.

B. Copper Deposition Equipment

IMP copper used as a seed layer was deposited on an Endura system. The Chemical Vapor Deposition of copper was performed in a Precision 5000 AMAT cluster tool. Two CVD chambers are available, one for copper deposition and the second for TiN-CVD. Copper was therefore deposited on TiN barrier, without vacuum break between TiN. The cluster equipment allows a clean and reproducible TiN/Cu interface. Copper Electroplating on various seed layers was performed on a Semitool Equinox system using pulsed current in order to achieve uniform films with high deposition rates up to 400 nm/min.

C. Chemical Mechanical Polishing

Polishing experiments were carried out on a PRESI MECAPOL 550 polisher, using a RODEL IC1000 pad stacked on a SUBA IV pad. The slurry is alumina-based and has to be mixed with hydrogen peroxide oxidizer prior to use (5).

Copper and barrier removal rates (RR) were determined by polishing respectively Cu, TiN, Ta and TaN blanket wafers. Barrier layer selectivities were calculated by the following formula: Selectivity = Copper RR / Barrier RR.

Planarization performance was investigated on topological wafers with copper line widths and oxide spaces varying from 0.3μm to 100μm.

0-7803-4285-2/98/$10.00 © 1998 IEEE

Results

A. Barrier Materials

Materials properties and barriers performance of IMP Ta, IMP TaN, CVD TiN films were extensively characterized The main results are summarized in Table 1. Stress was measured on 500nm thick film for IMP Ta and TaN and on 60nm thick film for CVD TiN. Tensile stress are measured on IMP films while the stress is compressive in CVD TiN film.

To evaluate barrier efficiency against Cu diffusion, 500nm of CVD copper was deposited on barriers (10nm IMPTa or TaN and 40nm TiN); Cu contamination in silicon was determined by SIMS after annealing at 450°C. On account of the different barrier thicknesses, the efficiency are similar for the three materials. For CMP application, selectivity between barrier and copper was evaluated on blanket wafers.

Properties	IMPTa	IMPTaN	CVDTiN
Resistivity	170μΩ.cm	250μΩ.cm	130 μΩ.cm
Stress	+350MPa	+1500MPa	-750MPa
Barrier performance	6E16at/cm3	6E17at/cm3	1E17at/cm3
Conformity (0.3μ line) side wall / bottom	20% / 40%	40% / 40%	100%/1 00%
CMP selectivity vs Cu	23	20	1

Table 1: Barrier characteristics

Step coverage was determined by SEM observations on patterned wafers with lines of 0.3 to 100μm widths.

Step coverage of CVD TiN is 100% whatever the pattern size. Figure 1 presents the variations of bottom and side-wall coverage of IMP Ta and IMP TaN. When increasing line width, bottom coverage increases up to 100% while side wall coverage remains around 20%.

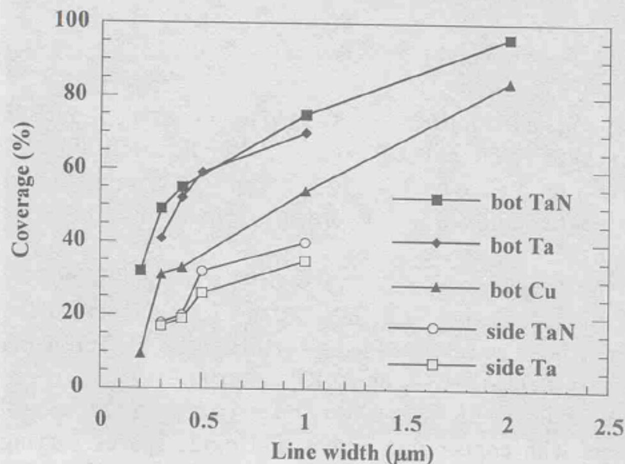


Figure 1: Coverage for IMP Ta, IMP TaN and IMP Cu vs line width

Figure 2 represents a SEM cross-section of 0.3μm line with 40nm thick IMP TaN layer. The IMP technique is efficient to achieve a continuous coverage of the barrier layer, even at the corners.

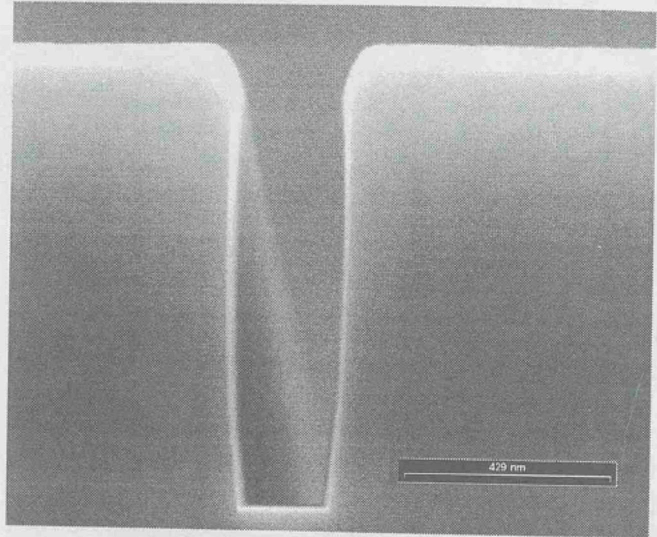


Figure 2: Coverage of IMP Ta film in 0.3μm line

B. Copper Deposition Processes

Copper deposition in high aspect ratio (3:1) trenches and vias was performed either by using Cu CVD alone or by combining a thin Cu liner with Cu electroplating for pattern filling.

In this work, pure Cu(hfac)(TMVS) was chosen as precursor for the CVD deposition. The detail of the process have been reported previously (4). Very conformal process was therefore available to achieve a void-free filling of the interconnect patterns. The nucleation step was also optimized in order to obtain very thin continuous seed layers. Good adhesion of Cu CVD with the underlying barrier material was obtained by using an in-situ treatment performed in the deposition equipment.

The electroplated copper films showed a void-free gap filling with a good resistivity of 1.9 μΩ.cm, and an adhesion compatible with CMP requirements. Figure (3) shows such film as deposited, and after CMP.

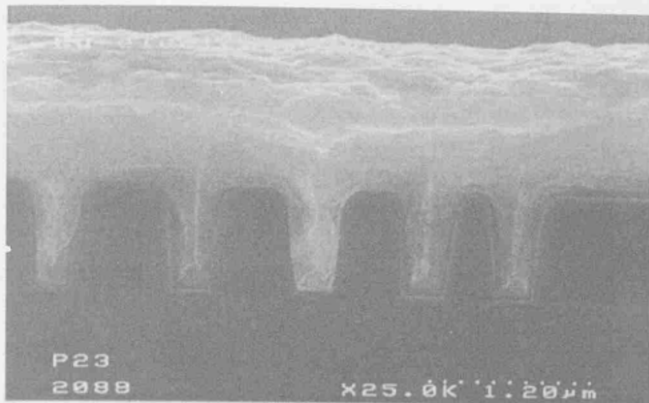


Figure 3a. As deposited Electroplated copper

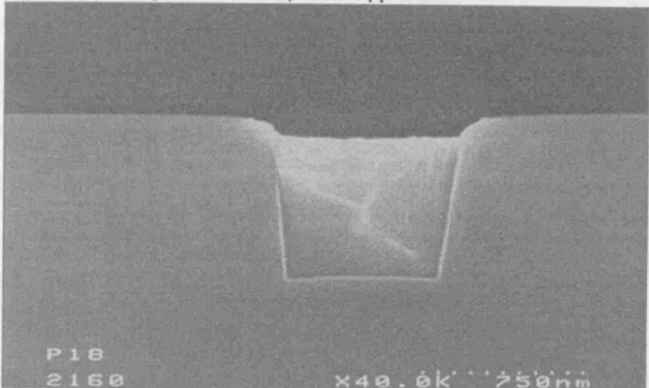


Figure3b. Electroplated Copper Film after CMP

C. Chemical Mechanical Polishing

Barrier versus copper selectivity determined on full sheet wafers are reported on table 1. Unlike TiN, Ta and TaN removal rates are much lower than copper removal rate.
The elimination of these barrier layers was investigated on topological wafers. The 40nm TiN layer was entirely removed while keeping acceptable copper dishing and oxide erosion effects. The high selectivity of Ta and TaN barrier layers was confirmed on topological wafers. To quantitatively determine this effect, a thick Ta barrier layer (100nm) was used. After polishing using the same conditions than for the TiN barrier layer, the remaining Ta barrier thickness was measured by SEM. As shown on figure 4, less than 5nm of the barrier layer were removed, demonstrating the excellent CMP stop layer capability of Ta material.

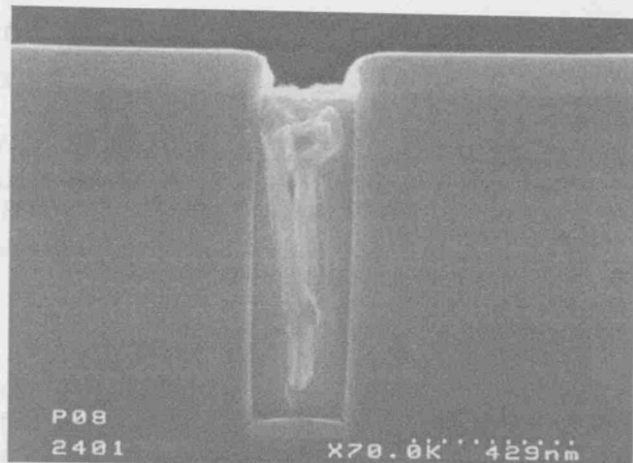


Figure 4. Copper CMP with Ta barrier
(0.3 µm line width / 0.3 µm oxide space)

Conclusion

A variety of solutions for 0.25µm copper interconnect technology have been developed. Complete via filling was achieved by combination of CVD and IMP techniques, and by electroplating deposition. A comprehensive comparison of TiN, Ta and TaN materials as barrier layers for copper metallization has been carried out, as these three materials proved to block copper diffusion. TiN was suitable for usual CMP process, involving removal of the entire metal stack during polishing. Ta and TaN barriers showed excellent CMP stop layer capabilities. Therefore, these new materials can lead to a novel CMP approach, in which the barrier layer is used to prevent from oxide erosion.

Acknowledgment

This work has been carried out within the GRESSI Consortium between CEA-LETI and France Telecom-CNET. The authors would like to thank B. Chin, T-Y Yao, L. Chen and M. Bakli from Applied Materials for their active contribution.

References

1. D.Edelstein et al, "Full copper wiring in a sub-0.25µm CMOS ULSI technology", Proc. IEEE IEDM, 1997, pp. 773-776
2. S.Venkatesan et al, "A high performance 1.8V, 0.20mm CMOS technology with copper metallization", Proc. IEEE IEDM, 1997, pp. 769-772
3. C. Marcadal et al, "OMCVD TiN diffusion barrier for copper contact an via and line", Proc. VMIC, 1997, pp. 405-410
4. C. Marcadal et al, "OMCVD Copper process for dual damascene metallization", Proc. VMIC, 1997, pp. 93-98
5. M. Fayolle and F. Romagna, "Copper CMP evaluation : planarization issues", Proc. Materials for Advanced Metallization Conference, Villard de Lans France, 1997, pp. 135-141