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(54) **TAILORED BARRIER LAYER WHICH PROVIDES IMPROVED COPPER INTERCONNECT ELECTROMIGRATION RESISTANCE**

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(58) **Field of Search** 204/192.15, 192.17, 204/192.22, 192.25; 438/652, 656, 660

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(57) **ABSTRACT**

Disclosed herein is a barrier layer structure useful in forming copper interconnects and electrical contacts of semiconductor devices. The barrier layer structure comprises a first layer of TaN_x which is applied directly over the substrate, followed by a second layer of Ta. The TaN_x/Ta barrier layer structure provides both a barrier to the diffusion of a copper layer deposited thereover, and enables the formation of a copper layer having a high <111> crystallographic content so that the electromigration resistance of the copper is increased. The TaN_x layer, where x ranges from about 0.1 to about 1.5, is sufficiently amorphous to prevent the diffusion of copper into the underlying substrate, which is typically silicon or a dielectric such as silicon dioxide. The thickness of the TaN_x and Ta layers used for an interconnect depend on the feature size and aspect ratio; typically, the TaN_x layer thickness ranges from about 50 Å to about 1,000 Å, while the Ta layer thickness ranges from about 20 Å to about 500 Å. For a contact via, the permissible layer thickness on the via walls must be even more carefully controlled based on feature size and aspect ratio; typically, the TaN_x layer thickness ranges from about 10 Å to about 300 Å, while the Ta layer thickness ranges from about 5 Å to about 300 Å. The copper layer is deposited at the thickness desired to suit the needs of the device. The copper layer may be deposited using any of the preferred techniques known in the art. Preferably, the entire copper layer, or at least a "seed" layer of copper, is deposited using physical vapor deposition techniques such as sputtering or evaporation, as opposed to CVD or electroplating. Since the crystal orientation of the copper is sensitive to deposition temperature, and since the copper may tend to dewet/delaminate from the barrier layer if the temperature is too high, it is important that the copper be deposited and/or annealed at a temperature of less than about 500° C., and preferably at a temperature of less than about 300° C.

7 Claims, 2 Drawing Sheets

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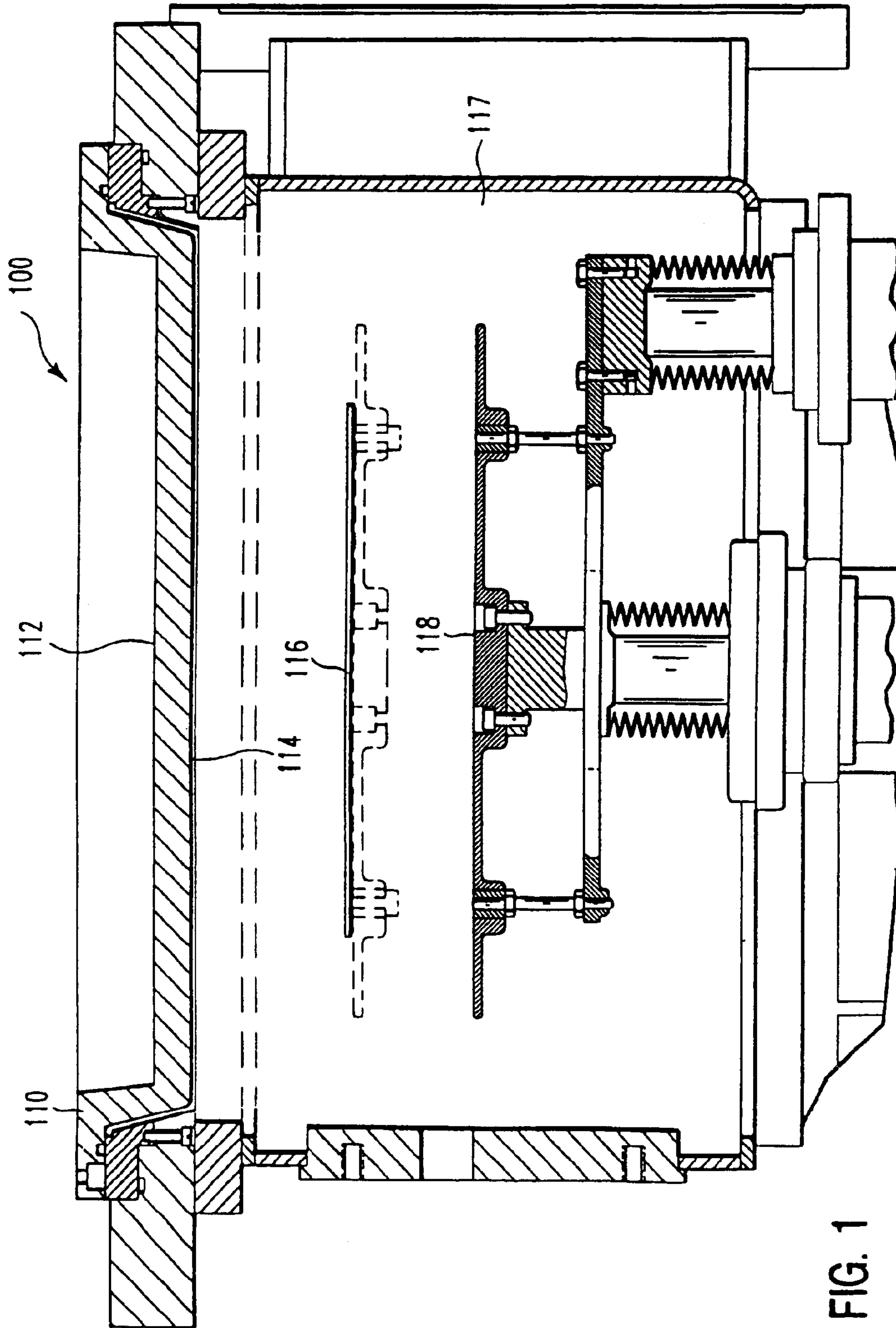

FIG. 1

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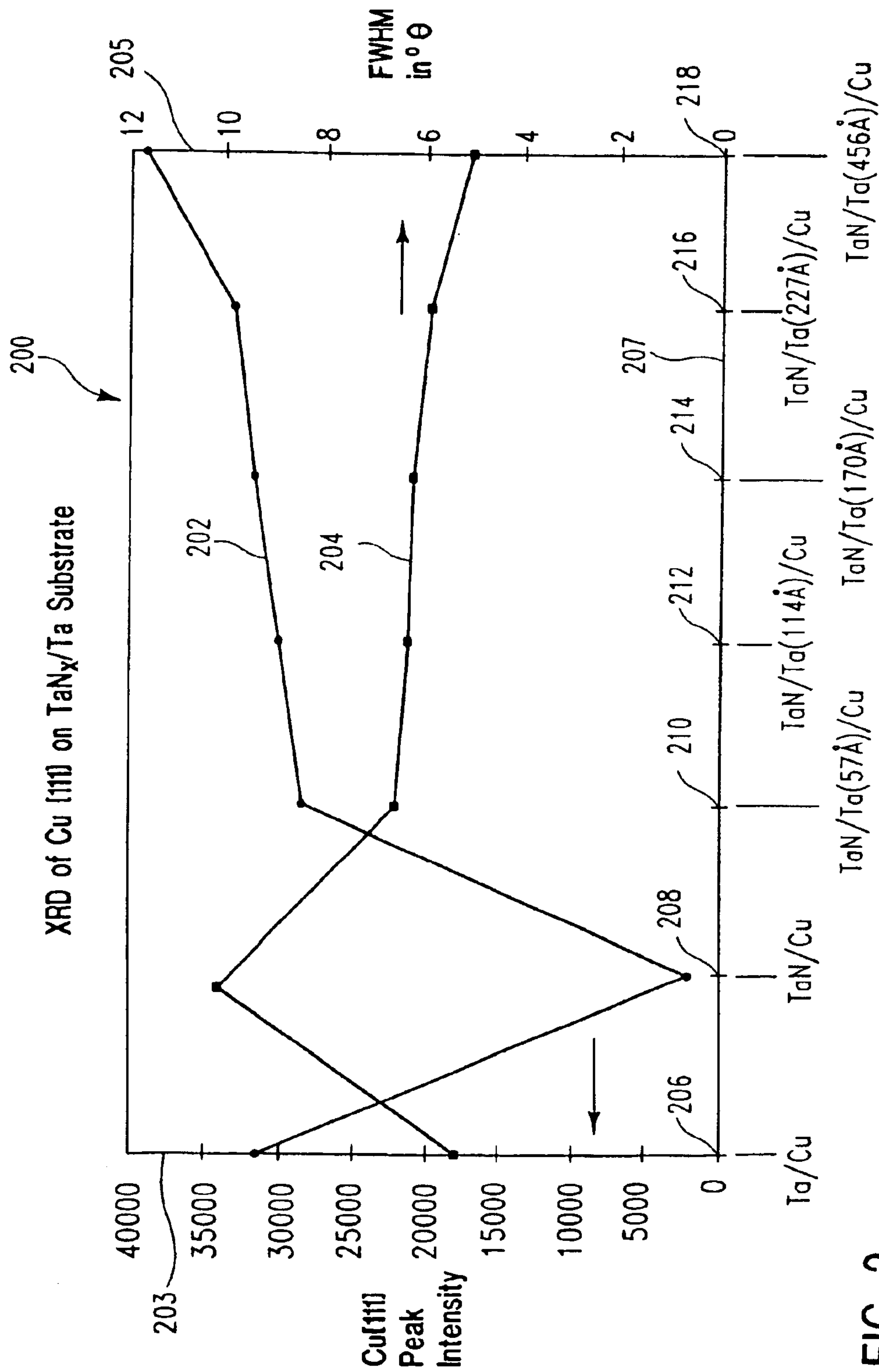

FIG. 2

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TAILORED BARRIER LAYER WHICH PROVIDES IMPROVED COPPER INTERCONNECT ELECTROMIGRATION RESISTANCE

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention pertains to a particular TaN_x/Ta barrier/wetting layer structure which increases the degree of {111} crystal orientation in an overlying copper layer, thereby providing improved electromigration resistance of the copper.

2. Brief Description of the Background Art

As microelectronics continue to miniaturize, interconnection performance, reliability, and power consumption has become increasingly important, and interest has grown in replacing aluminum alloys with lower-resistivity and higher-reliability metals. Copper offers a significant improvement over aluminum as a contact and interconnect material. For example, the resistivity of copper is about 1.67 $\mu\Omega$cm, which is only about half of the resistivity of aluminum.

There are two principal competing technologies under evaluation by material and process developers working to enable the use of copper. The first technology is known as damascene technology. In this technology, a typical process for producing a multilevel structure having feature sizes (i.e., width of the aperture) in the range of 0.5 micron (μm) or less would include: blanket deposition of a dielectric material; patterning of the dielectric material to form openings; deposition of a diffusion barrier layer and, optionally, a wetting layer to line the openings; deposition of a copper layer onto the substrate in sufficient thickness to fill the openings; and removal of excessive conductive material from the substrate surface using chemical-mechanical polishing (CMP) techniques. The damascene process is described in detail by C. Steinbruchel in "Patterning of copper for multilevel metallization: reactive ion etching and chemical-mechanical polishing", *Applied Surface Science* 91 (1995)139–146.

The competing technology is one which involves the patterned etch of a copper layer. In this technology, a typical process would include deposition of a copper layer on a desired substrate (typically a dielectric material having a barrier layer on its surface); application of a patterned hard mask or photoresist over the copper layer; pattern etching of the copper layer using wet or dry etch techniques; and deposition of a dielectric material over the surface of the patterned copper layer, to provide isolation of conductive lines and contacts which comprise various integrated circuits.

Typically, the copper layer can be applied using sputtering techniques well known in the art. The sputtering of copper provides a much higher deposition rate than evaporation or CVD (chemical vapor deposition) and provides a purer copper film than CVD.

In integrated circuit interconnect structures where copper is the material used to form conductive lines and contacts, it is recognized that copper diffuses rapidly into adjacent layers of SiO_2 and silicon and needs to be encapsulated. Gang Bai et al. in "Copper Interconnection Deposition Techniques and Integration", 1996 Symposium on VLSI Technology, Digests of Technical Papers (0-7803-3342-X/ 96 IEEE) describe the effectiveness of Ta, TiN, W and Mo

annealed in UHV (ultra high vacuum) after copper deposition provided the best barrier layer. Sputtered copper appeared to be preferable over CVD copper and over electroplated copper, although all the data for electroplated copper was not available at the time of presentation of the paper.

U.S. Pat. No. 4,319,264 of Gangulee et al., issued Mar. 9, 1982 and titled "Nickel-gold-nickel Conductors For Solid State Devices" discusses the problem of electromigration in solid state devices. In particular, the patent discusses the application of direct current over particular current density ranges which induces motion of the atoms comprising the thin film conductor, the effect known as electromigration. Electromigration is said to induce crack or void formation in the conductor which, over a period of time, can result in conductor failure. The rate of electromigration is said to be dependent on the current density imposed on the conductor, the conductor temperature, and the properties of the conductor material. In high current density applications, potential conductor failure due to electromigration is said to severely limit the reliability of the circuit. In discussing the various factors affecting performance of the conductive materials, grain structure is mentioned as being important. (In order to obtain adequate lithographic line width resolution, it is recommended that the film be small grained, with a grain size not exceeding about one-third of the required line width.) Uniformity of grain size and preferred crystallographic orientation of the grains are also said to be factors which promote longer (electromigration limited) conductor lifetimes. Fine grained films are also described as being smoother, which is a desirable quality in semiconductor applications, to lessen difficulties associated with covering the conductor with an overlayer.

U.S. Pat. No. 5,571,752 to Chen et al., issued Nov. 5, 1996, discloses a method for patterning a submicron semiconductor layer of an integrated circuit. In one embodiment describing an aluminum contact, titanium or titanium nitride having a thickness of between approximately 300 and 2,000 Å is formed by sputter deposition to reach the bottom of a contact opening. Finally, a second conductive layer, typically aluminum, is applied over the surface of the conformal conductive layer. The aluminum is sputtered on, preferably at a temperature ranging between approximately 100° C. and 400° C. This method is said to make possible the filling of contact openings having smaller device geometry design requirements by avoiding the formation of fairly large grain sizes in the aluminum film.

As described in U.S. patent application Ser. No. 08/824,911, of Ngan et al., filed Mar. 27, 1997 and commonly assigned with the present invention, efforts have been made to increase the <111> crystallographic content of aluminum as a means of improving electromigration of aluminum. In particular, the <111> content of an aluminum layer was controlled by controlling the thickness of various barrier layers underlying the aluminum layer. The underlying barrier layer structure was Ti/TiN/TiN_x, which enabled aluminum filling of high aspect vias while providing an aluminum fill exhibiting the high degree of aluminum <111> crystal orientation. The Ti/TiN/TiN_x barrier layer was deposited using IMP (ion metal plasma) techniques, and the barrier layer thicknesses were as follows. The thickness of the first layer of Ti ranges from greater than about 100 Å to about 500 Å (the feature geometry controls the upper thickness limit). The thickness of the TiN second layer ranges from greater than about 100 Å to less than about 800 Å

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titanium to about 100 atomic percent titanium) ranges from about 15 Å to about 500 Å. A Ti/TiN/TiN_x barrier layer having this structure, used to line a contact via, is described as enabling complete filling of via with sputtered warm aluminum, where the feature size of the via or aperture is about 0.25 micron or less and the aspect ratio ranges from about 5:1 to as high as about 6:1.

Subsequently, in U.S. Pat. No. 5,882,399, of Ngan et al., issued Mar. 16, 1999, the inventors disclose that to maintain a consistently high aluminum <111> crystal orientation content of an interconnect during the processing of a series of semiconductor substrates in a given process chamber, it is necessary to form the first deposited layer of the barrier layer to a minimal thickness of at least about 150 Å, to compensate for irregularities in the crystal orientation which may be present during the initial deposition of this layer when the process chamber is initially started up (and continuing for the first 7–8 wafers processed). Ngan et al. teach that in the case of a copper conductive layer, it may also be necessary that the first layer of a barrier layer structure underlying the copper layer have a minimal thickness of at least about 150 Å, to enable a consistent crystal orientation within the copper layer during the processing of a series of wafers in a semiconductor chamber.

SUMMARY OF THE INVENTION

We have discovered that tantalum nitride (TaN_x) is a better barrier layer for copper than tantalum (Ta). However, copper deposited directly over TaN_x does not exhibit a sufficiently high degree of <111> crystal orientation to provide the desired copper electromigration characteristics. We have developed a barrier layer structure comprising a layer of Ta overlying a layer of TaN_x which provides both a barrier to the diffusion of a copper layer deposited thereover, and enables the formation of a copper layer having a high <111> crystallographic content, so that copper electromigration resistance is increased.

The TaN_x layer, where x ranges from about 0.1 to about 1.5, is sufficiently amorphous to prevent the diffusion of copper into underlying silicon or silicon oxide surfaces. The desired thickness for the TaN_x layer is dependent on the device structure. For a typical interconnect, the TaN_x layer thickness ranges from about 50 Å to about 1,000 Å. For a contact, the TaN_x layer, the thickness on the wall of a contact via ranges from about 10 Å to about 300 Å, depending on the feature size. The TaN_x layer is preferably deposited using standard reactive ion sputtering techniques at a substrate temperature ranging from about 20° C. to about 500° C. However, ion deposition sputtering techniques may be used to deposit this layer.

The Ta layer deposited over the TaN_x layer has a desired thickness ranging from about 5 Å to about 500 Å, wherein the thickness is preferably greater than about 20 Å, depending on the feature size. The Ta layer is preferably deposited using standard ion sputtering techniques at a substrate temperature ranging from about 20° C. to about 500° C. However, ion deposition sputtering techniques may be used to deposit this layer.

The copper layer is deposited at the thickness desired to suit the needs of the device. The copper layer may be deposited using any of the preferred techniques known in the art. Preferably, the entire copper layer or at least a "seed" layer of copper is deposited using physical vapor deposition techniques such as sputtering or evaporation, as opposed to temperature of the copper either during deposition or during subsequent annealing processes not be higher than about 500° C. Preferably, the maximum temperature is about 300° C.

We have also developed a method of producing a copper interconnect structure comprising a copper layer deposited over a barrier layer structure of the kind described above, comprising a Ta layer overlying a TaN_x layer, where the Cu <111> crystallographic content is at least 70% of the Cu <111> crystallographic content which can be obtained by depositing the copper layer over a pure Ta barrier layer which is about 500 Å thick. The method comprises the steps of:

a) depositing a first layer of TaN_x having a thickness ranging from greater than about 50 Å to about 1,000 Å;

b) depositing a second layer of Ta having a thickness ranging from about 5 Å to about 500 Å over the surface of the first layer of TaN_x; and

c) depositing a third layer of copper over the surface of the second layer of Ta, wherein at least a portion of the third layer of copper is deposited using a physical vapor deposition technique, and wherein the substrate temperature at which the third layer of copper is deposited is less than about 500° C.

Further, we have developed a method of producing a copper-comprising contact via structure comprising a copper layer deposited over a barrier layer structure of the kind described above, comprising a Ta layer overlying a TaN_x layer; wherein the Cu <111> crystallographic content is at least 70% of the Cu <111> crystallographic content which can be obtained by depositing said copper layer over a pure Ta barrier layer which is about 300 Å thick. The method comprises the steps of:

a) depositing a first layer of TaN_x having a thickness ranging from greater than about 10 Å to about 300 Å;

b) depositing a second layer of Ta having a thickness ranging from about 5 Å to about 300 Å over the surface of said first layer of TaN_x; and

c) depositing a third layer of copper over the surface of the second layer of Ta, wherein at least a portion of the third layer of copper is deposited using a physical vapor deposition technique, and wherein the substrate temperature at which the third layer of copper is deposited is less than about 500° C.

In the method of producing a copper-comprising contact structure described above, a least a portion of the first layer of TaN_x, or the second layer of Ta, or the third layer of Cu, or at least a portion of more than one of these three layers may be deposited using ion-deposition sputtering, where at least a portion of the sputtered emission is in the form of ions at the time the emission reaches the substrate surface, and where, typically 10% or more of the sputtered emission is in the form of ions at the time the emission reaches the substrate surface.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** shows a schematic of a cross sectional view of a sputtering chamber of the kind which can be used to deposit the barrier layer of the present invention.

FIG. **2** shows a graph representative of the copper <111> crystal orientation on a TaN_x/Ta barrier layer as a function of the thickness of the Ta layer, with the TaN_x layer held constant at about 500 Å.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

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