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United States Patent [19]

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Wetzel et al.

[45] **Date of Patent:** Jul. 6, 1999

[54] **METHOD OF FORMING A SEMICONDUCTOR DEVICE HAVING DUAL INLAID STRUCTURE**

OTHER PUBLICATIONS

[75] Inventors: **Jeffrey T. Wetzel; John J. Stankus**, both of Austin, Tex.

B. Luther et al., "Planar Copper-Polyimide Back End of the Line Interconnections for ULSI Devices", Jun. 8-9, 1993 VMIC Conference, Catalog No. 93ISMIC-102, pp. 15-21.

[73] Assignee: **Motorola, Inc.**, Schaumburg, Ill.

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[21] Appl. No.: **08/921,293**

[57] ABSTRACT

[22] Filed: **Aug. 29, 1997**

A method for forming semiconductor device (1) that includes providing a substrate (10) having a metal interconnect (12), depositing a via interlevel dielectric (ILD) layer (20) over the substrate (10) and the metal interconnect (12), etching the via ILD layer (20) to form a via (30) over the metal interconnect (12), depositing a trench ILD layer (32) over the via ILD layer (20) and the via (30), etching the trench ILD layer (32) to form a trench (40), the trench (40) being contiguous with the via (12), and depositing a metal (44) so as to fill the via (30) and the trench (40), and provide electrical connection with the metal interconnect (12).

[51] **Int. Cl.⁶** **H01L 21/4763**

[52] **U.S. Cl.** **438/618; 438/622; 438/623; 438/624; 438/627; 438/628; 438/634; 438/638**

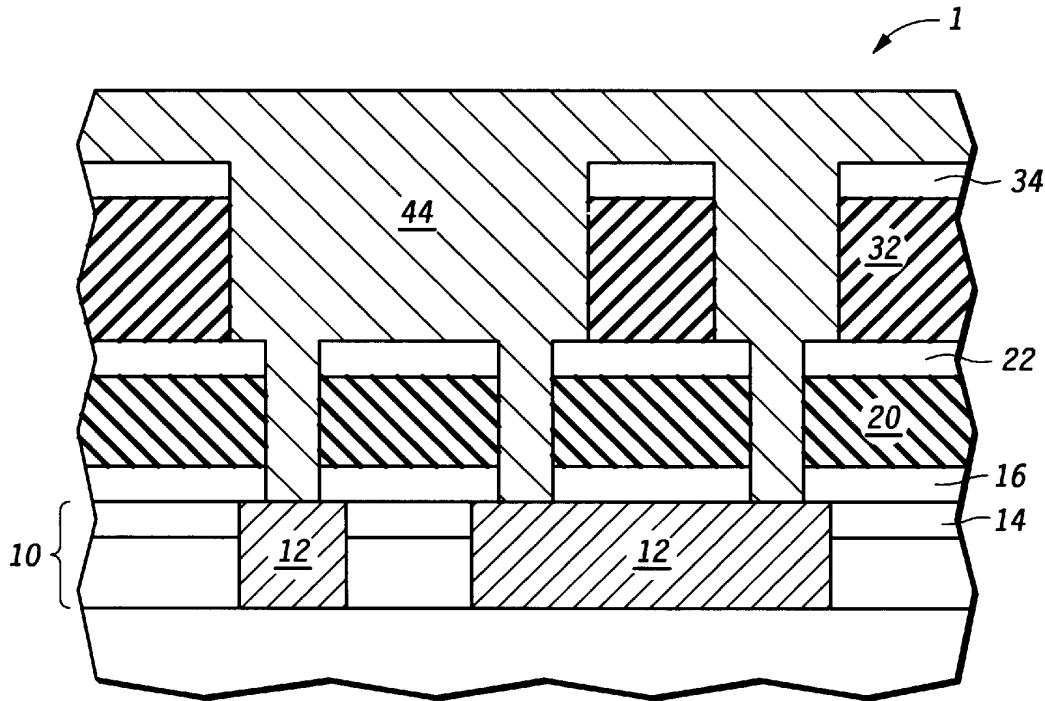
[58] **Field of Search** **438/618, 622, 438/623, 624, 627, 628, 634, 638**

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26 Claims, 4 Drawing Sheets



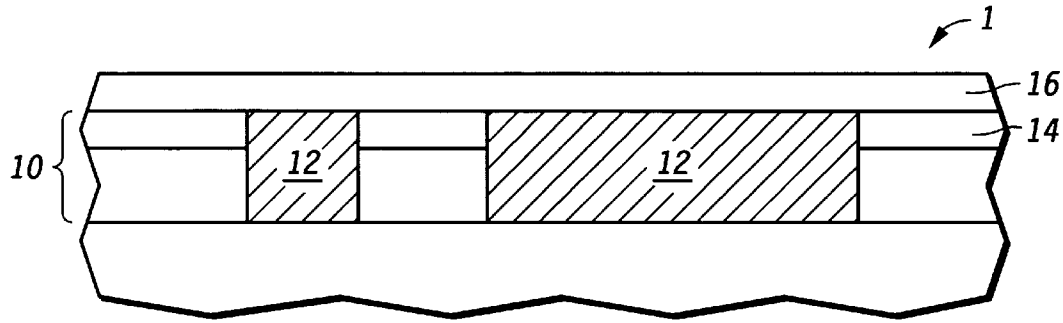


FIG. 1

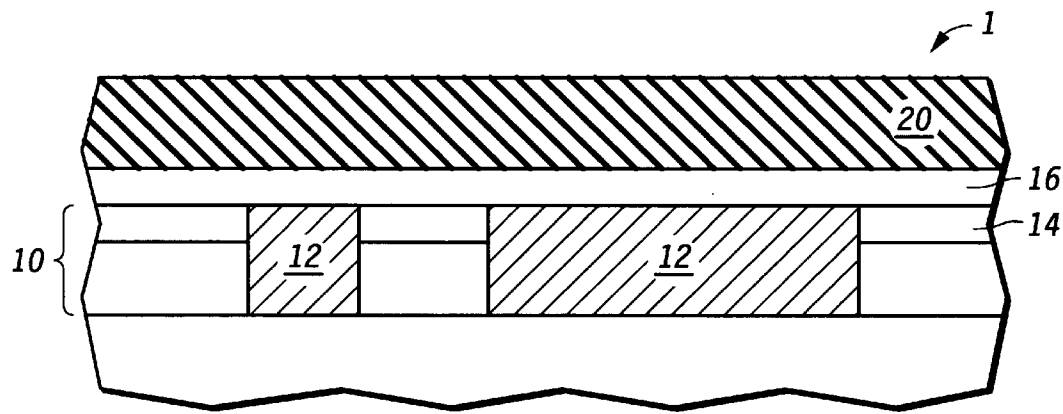


FIG. 2

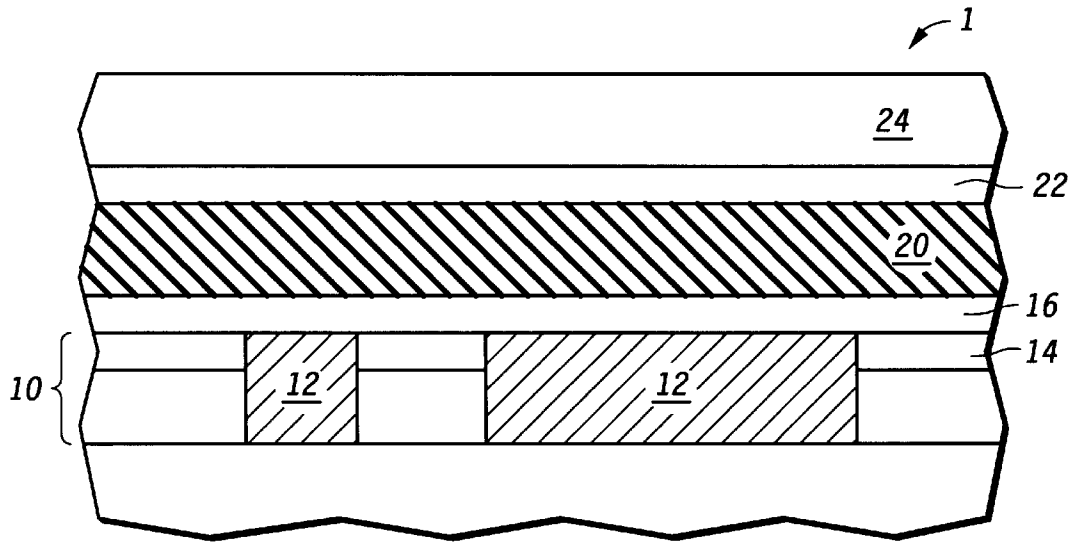


FIG. 3

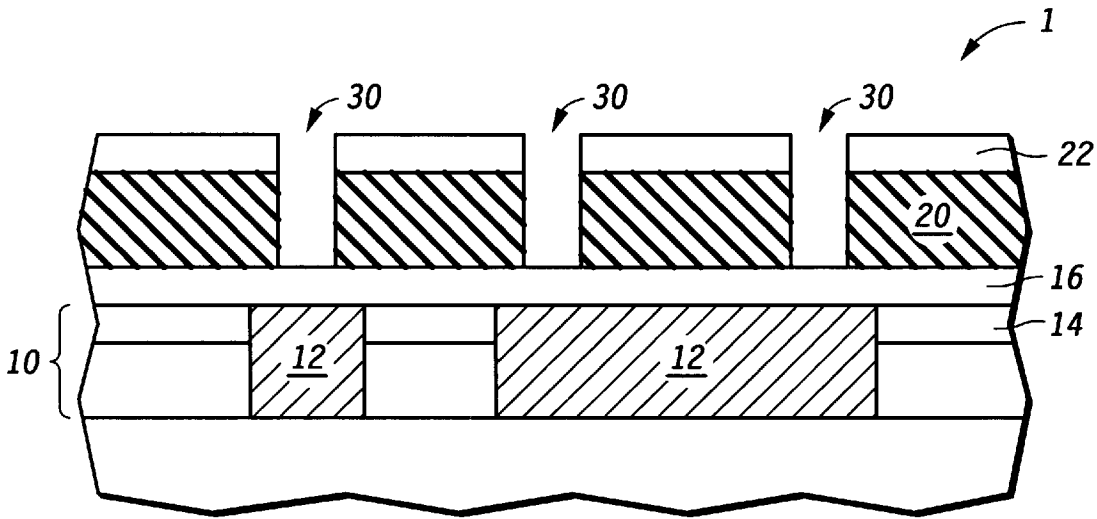


FIG. 4

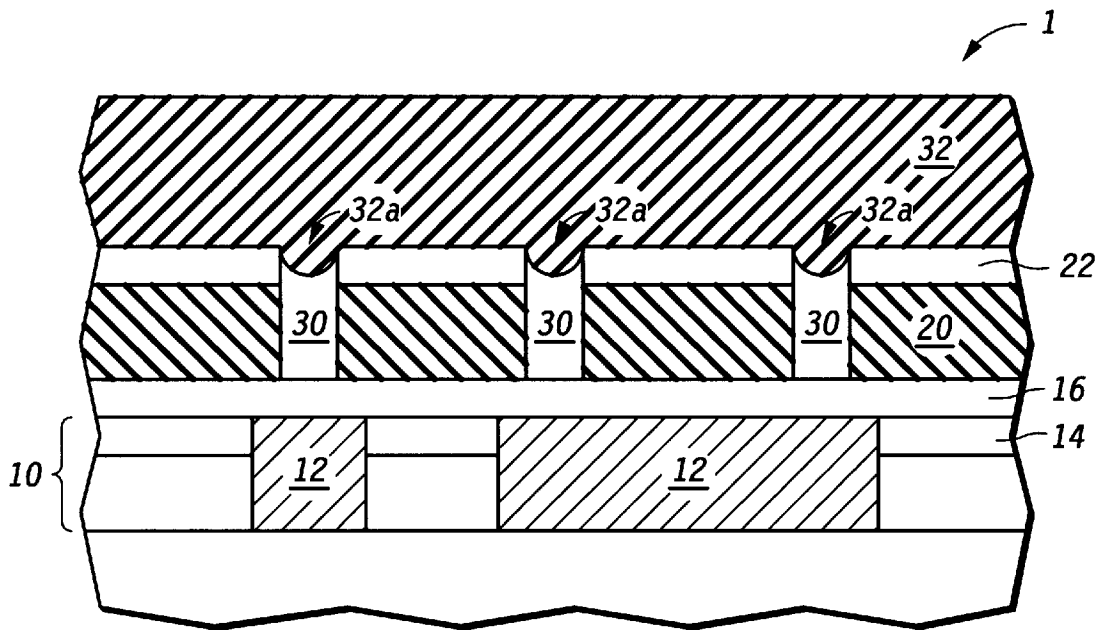


FIG. 5

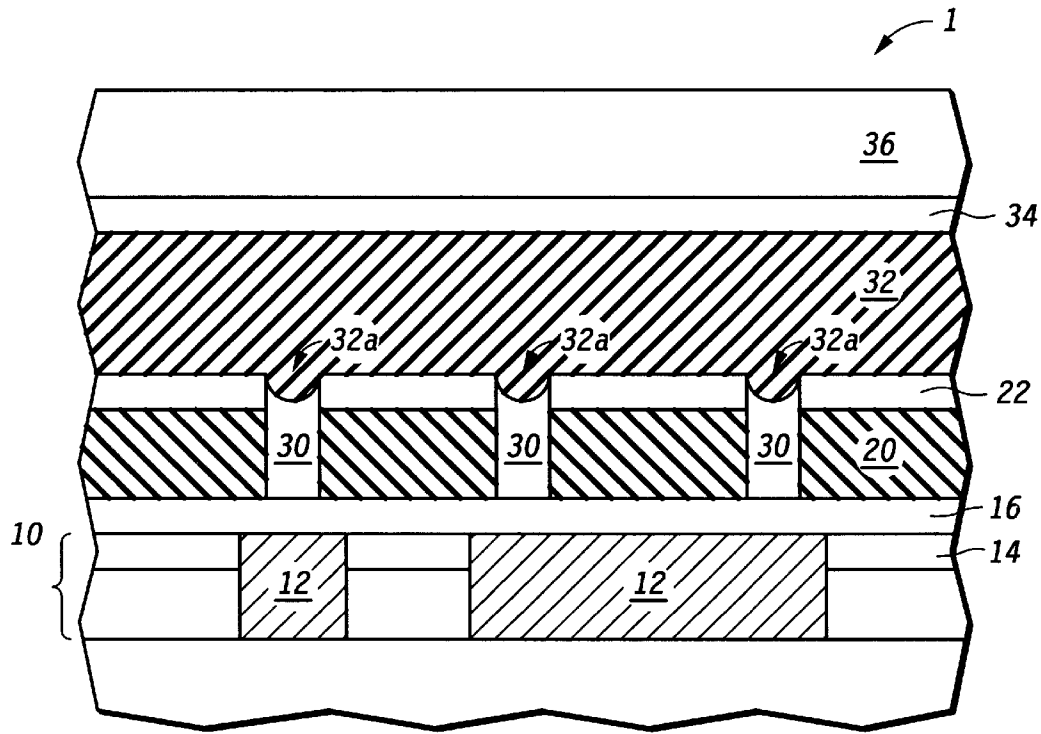


FIG. 6

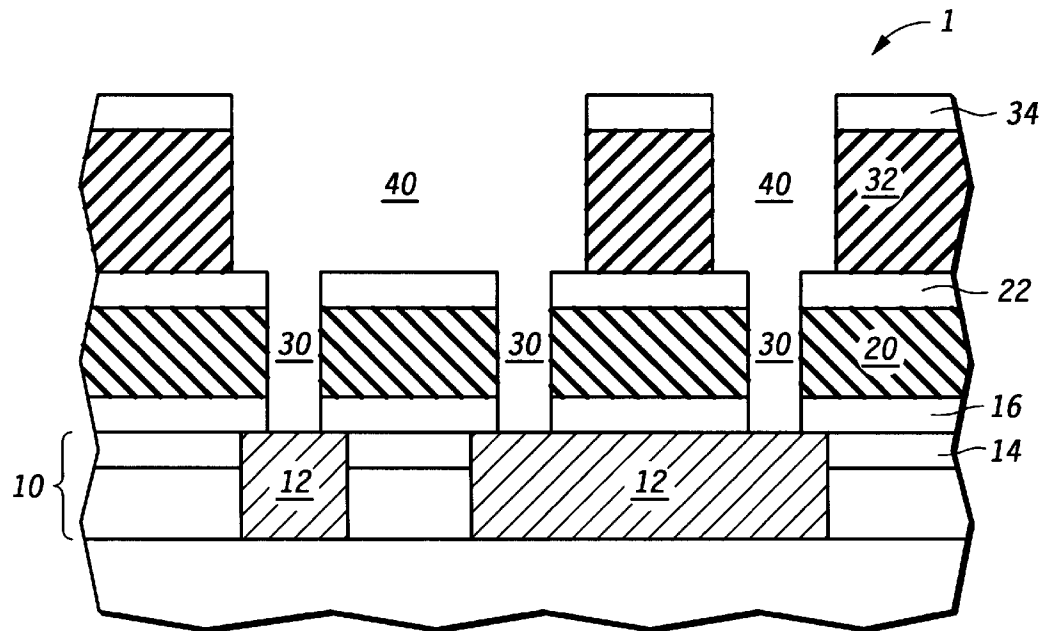


FIG. 7

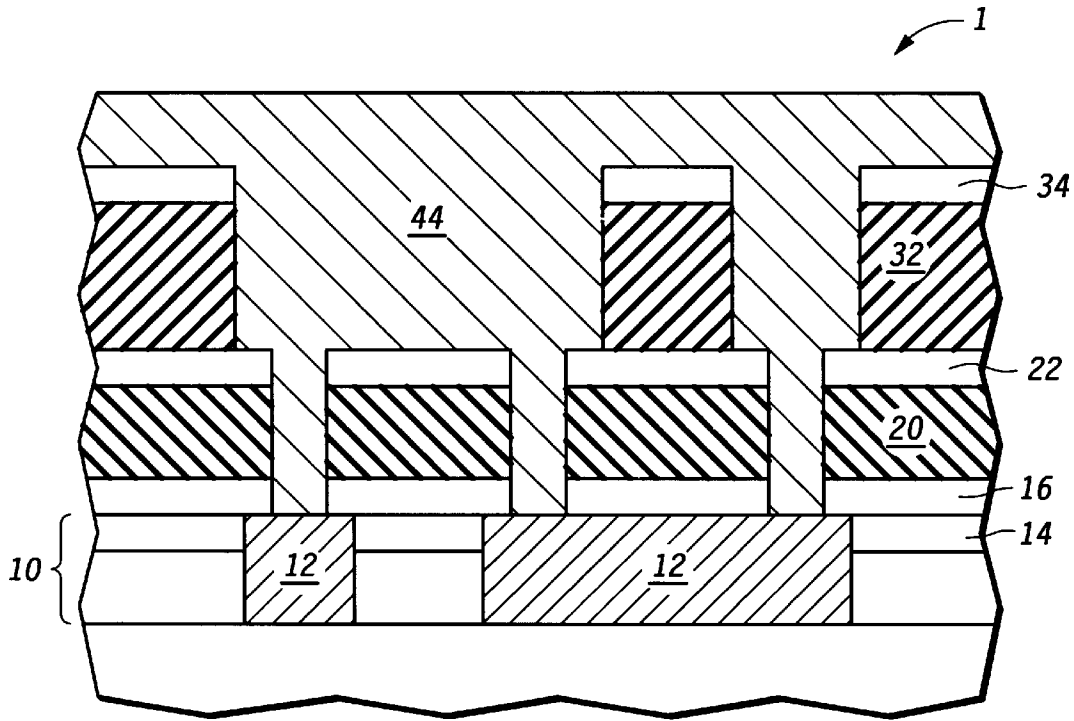


FIG. 8

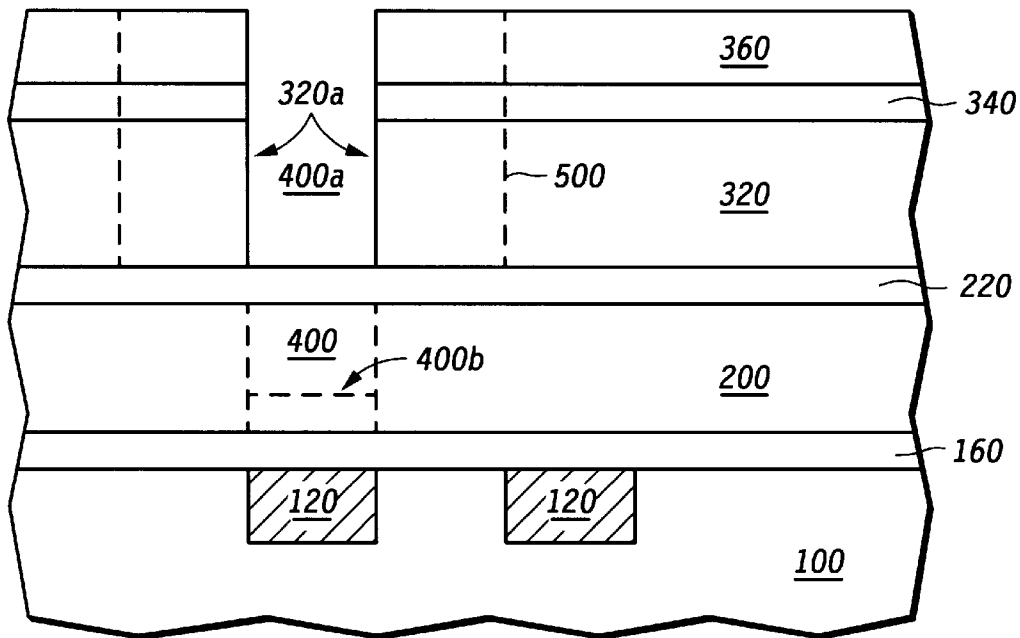


FIG. 9
-PRIOR ART-

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