



US006100184A

United States Patent [19]

[11] Patent Number: **6,100,184**

Zhao et al.

[45] Date of Patent: **Aug. 8, 2000**

- [54] **METHOD OF MAKING A DUAL DAMASCENE INTERCONNECT STRUCTURE USING LOW DIELECTRIC CONSTANT MATERIAL FOR AN INTER-LEVEL DIELECTRIC LAYER**
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- [73] Assignees: **Sematech, Inc.**, Austin, Tex.; **Lucent Technologies Inc.**, Murray Hill, N.J.

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[21] Appl. No.: **08/914,995**

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[22] Filed: **Aug. 20, 1997**

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[51] Int. Cl.⁷ **H01L 21/4763**

[52] U.S. Cl. **438/638**; 438/622; 438/623; 438/627; 438/643; 438/636; 438/637; 438/638; 438/648; 438/653; 438/656; 438/672; 438/685; 438/687; 438/902

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[58] Field of Search 438/622, 623, 438/627, 637, 638, 639, 640, 666, 668.6, 672, 643, 678, 685, 902, 629, 636, 648, 653, 656, 687

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Primary Examiner—John F. Niebling
Assistant Examiner—David A. Zarneke

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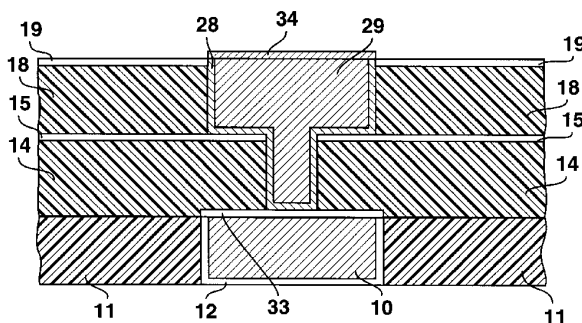
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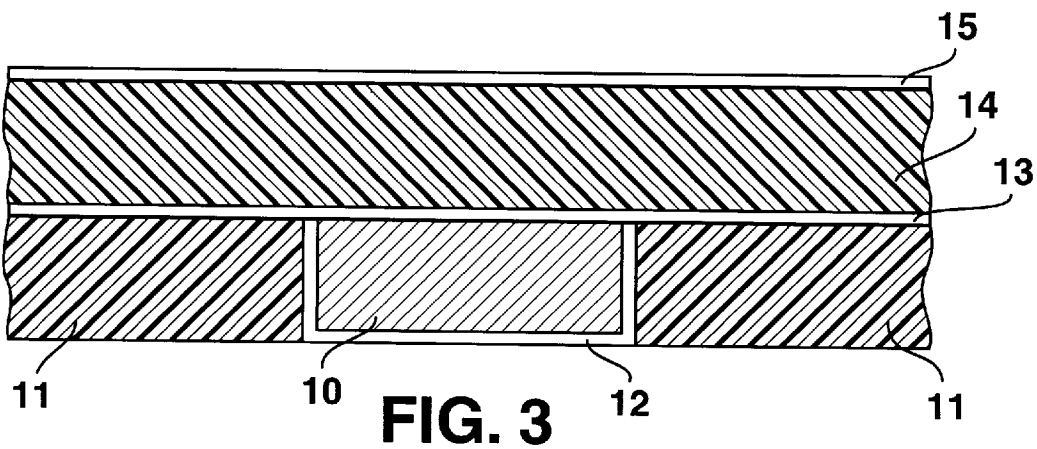
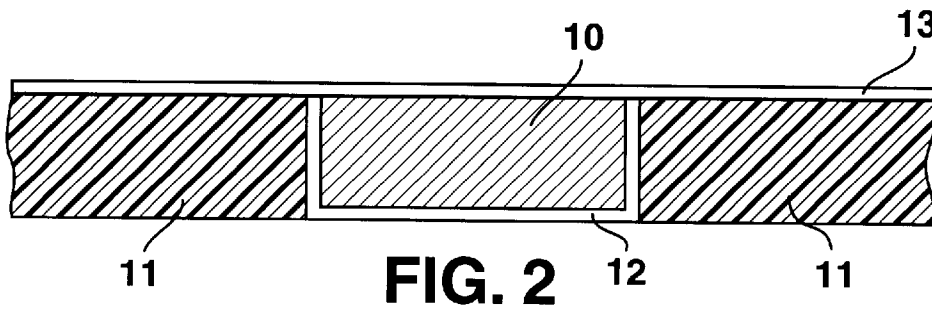
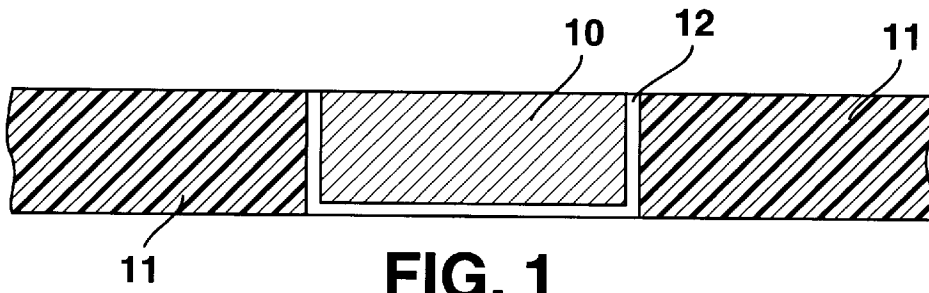
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[57] ABSTRACT

A technique for fabricating a dual damascene interconnect structure using a low dielectric constant material as a dielectric layer or layers. A low dielectric constant (low-ε) dielectric material is used to form an inter-level dielectric (ILD) layer between metallization layers and in which via and trench openings are formed in the low-ε ILD. The dual damascene technique allows for both the via and trench openings to be filled at the same time.

12 Claims, 6 Drawing Sheets





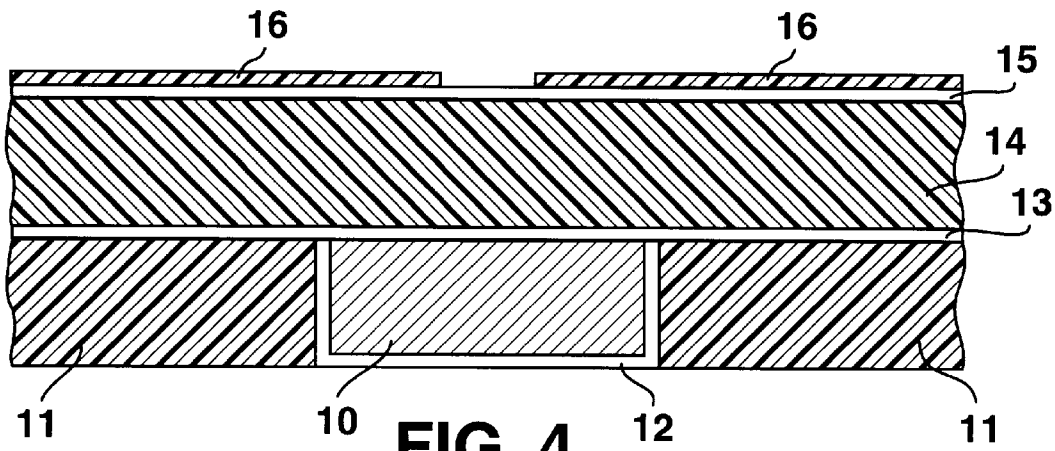


FIG. 4

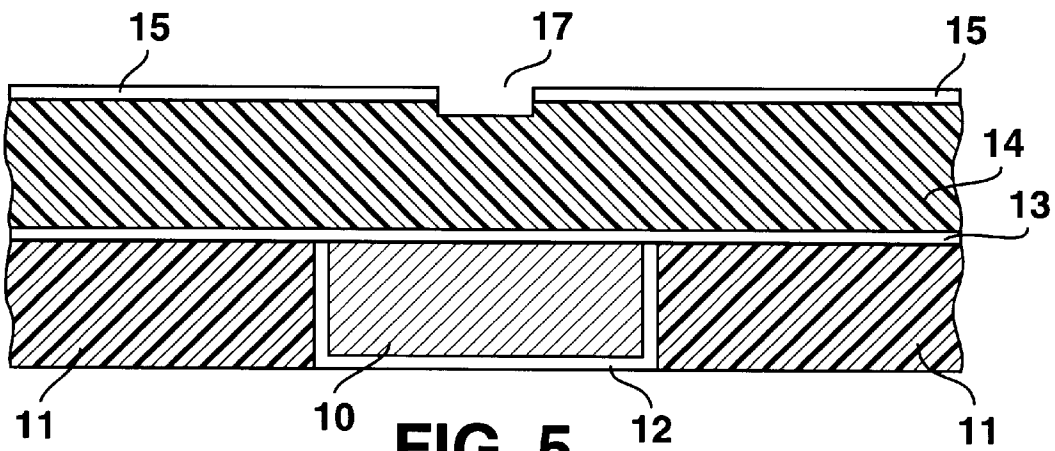


FIG. 5

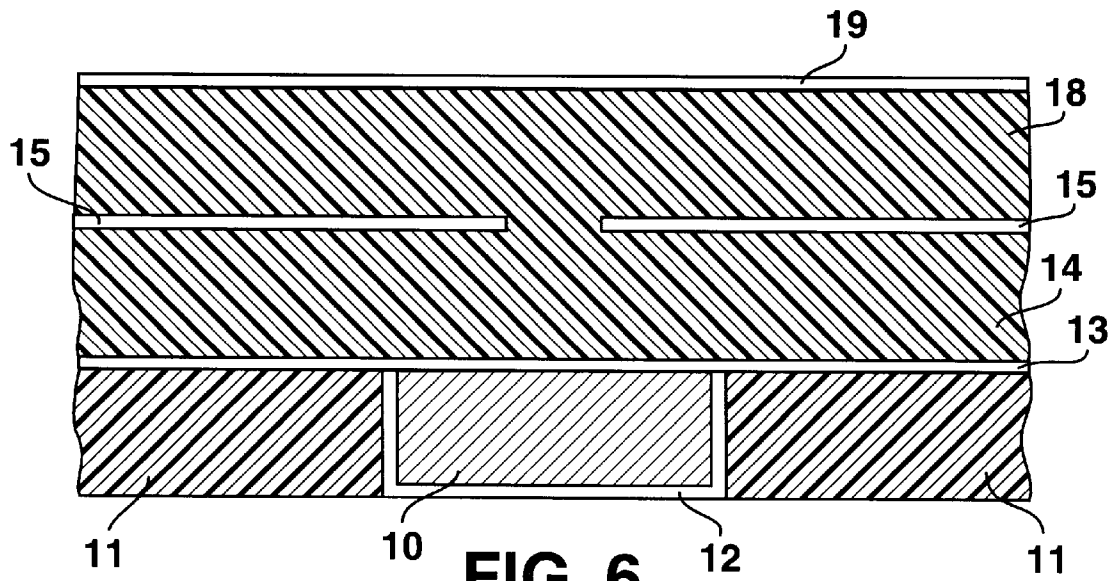


FIG. 6

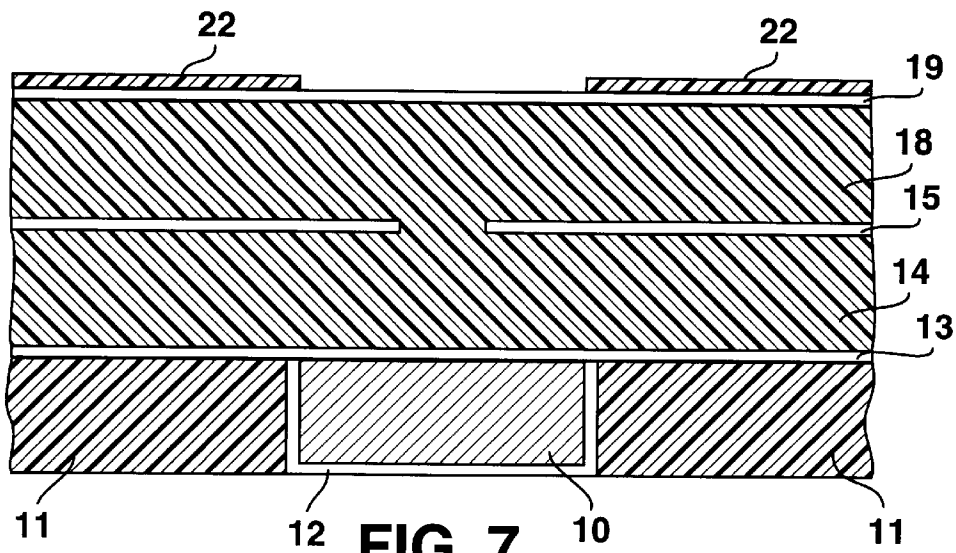


FIG. 7

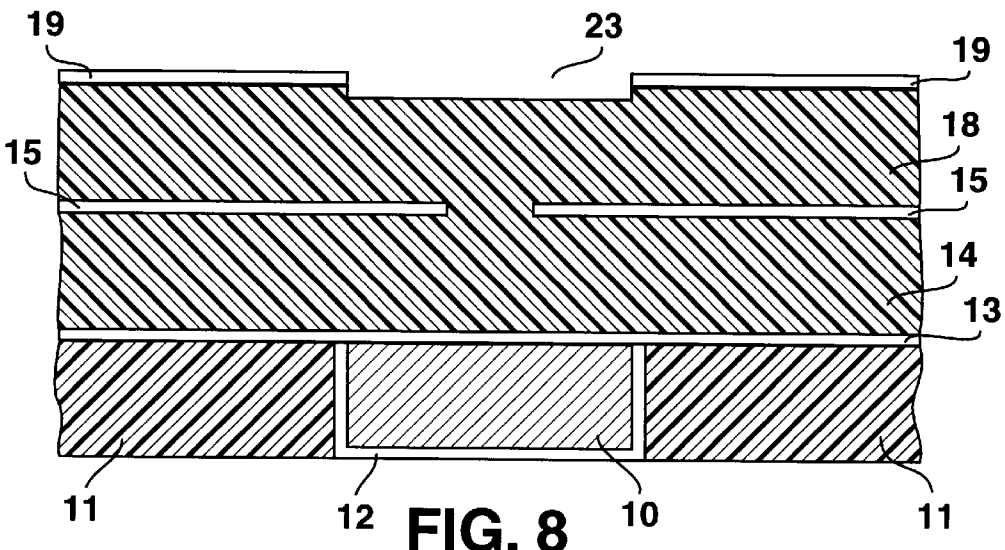


FIG. 8

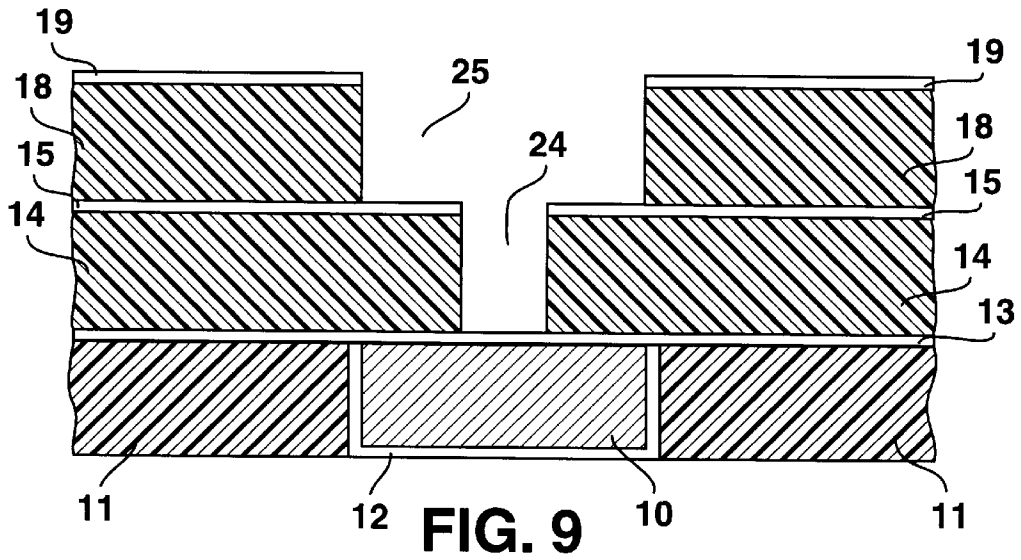
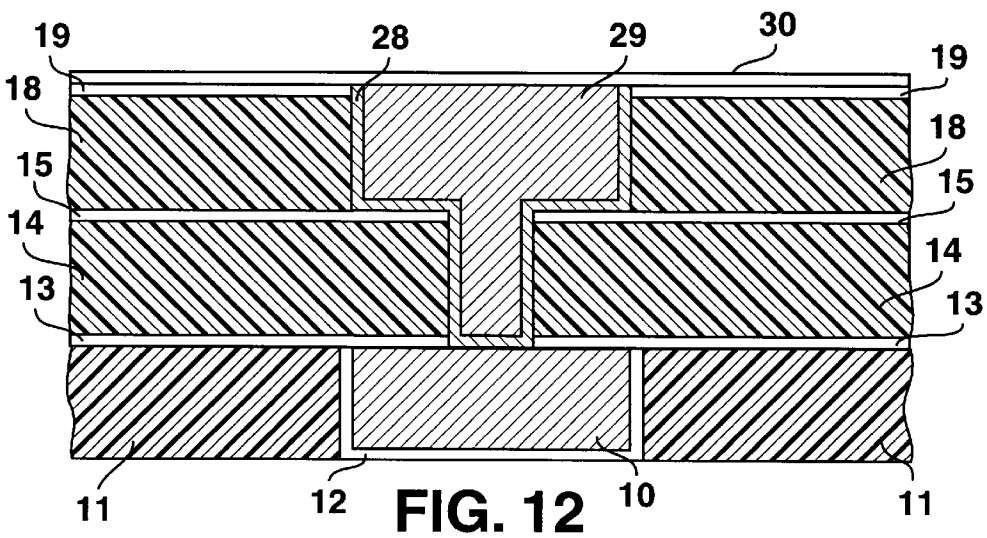
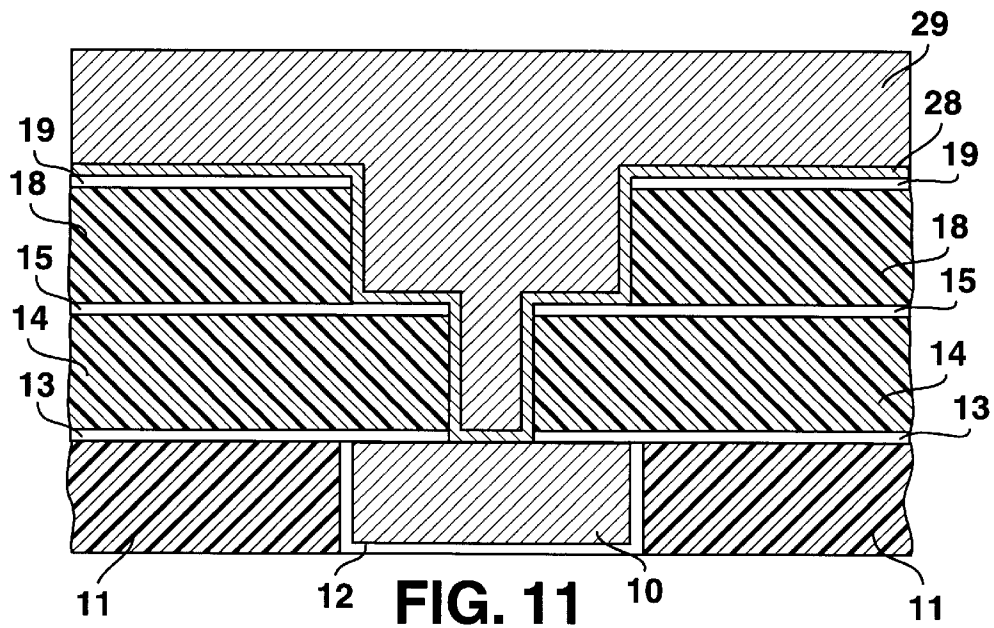
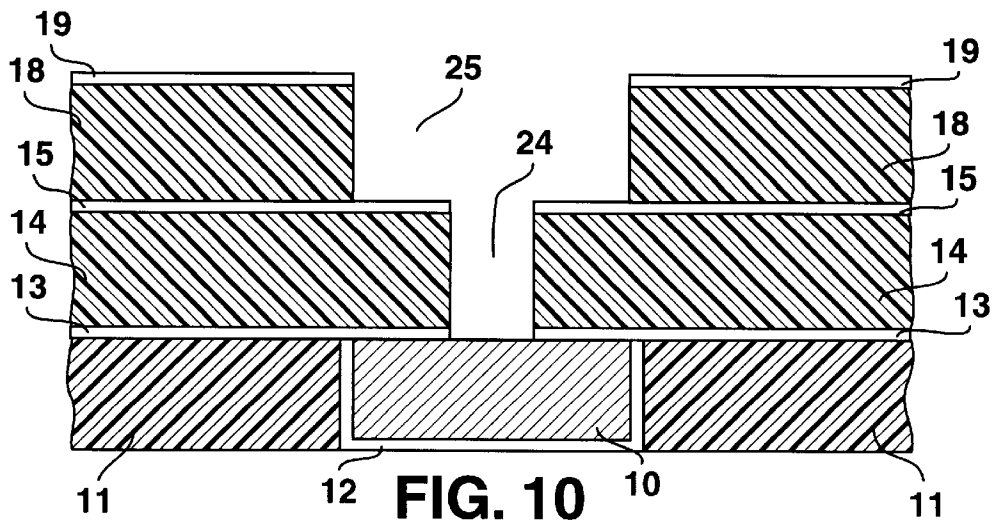


FIG. 9



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