Monolithic Spiral Inductors Fabricated Using a VLSI Cu-Damascene Interconnect Technology and Low-Loss Substrates

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Abstract

This paper presents spiral inductor structures optimized in a Cu-damascene VLSI interconnect technology with use of silicon, high-resistivity silicon (HRS), or sapphire substrates. Quality factors (Q) of 40 at 5.8 GHz for a 1.4 nH-inductor and 13 at 600 MHz for a 80 nH-inductor have been achieved.

Introduction

The integration of spiral inductors is one of the most challenging tasks for the realization of monolithic rf transceivers on silicon substrates. Maximum quality-factors (Q_{max}) up to 24 were obtained by employing five levels of Al interconnects, as presented at last year's IEDM (1). While this result was based on standard silicon processing, the adoption of a low-resistive metal like gold, (2), or copper (Cu), (3), and of low-loss substrates such as high-resistivity silicon (HRS), (2), sapphire (Al_2O_3), or silicon-on-insulator with a thick buried oxide (SOI) give promise to increase the Q even more and to enter the domain governed by discrete inductors. In this paper, we present the results of a rigorous optimization of monolithic inductors by employing the technology options given with advanced silicon process technology.

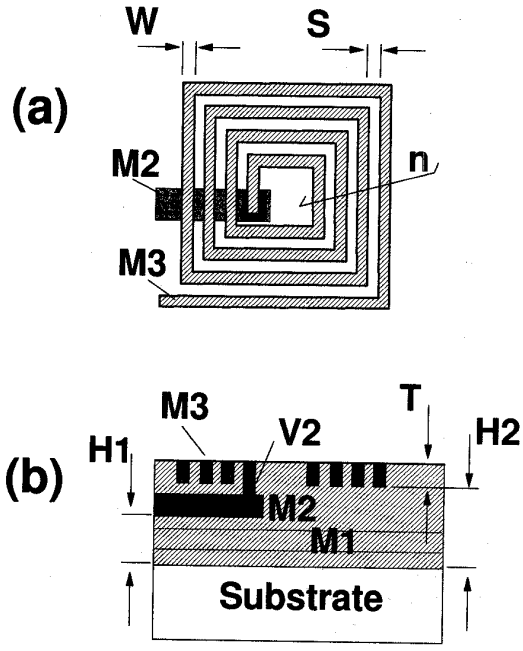

Fig. 1 Spiral inductor structure in (a) plan view and (b) cross-section. The spiral coil was built using the M3 metal layer, and the underpass was at M2; the layer M1 was not used.

Fabrication Process

A three-level Cu-damascene process with 2.5 µm-thick Cu-interconnects and oxide (SiO_2) isolation, which was similar to the technology described in (3), was developed to build spiral inductor structures at the upper two metal levels (M2 and M3 in Fig. 1). The spiral coil was built at M3, and the underpass contact was at M2. The first metal level was not fabricated in our experiments. The metal layer M2 was formed in a single-damascene step, while both the vias V2 and the metal layer M3 were fabricated in one dual-damascene process step (Fig. 2). A liner film, which acts as a diffusion barrier and adhesion promoter, was deposited prior to the metal. The dual-damascene process involved two cycles of lithography and dry-etching, one Cu-deposition step, removal of the metal overburden through chemical-mechanical polishing (CMP), and electroless capping of the exposed Cu-surface. The Cu-resistivity in the metal layers and the vias was about 1.9 µΩ-cm.

Three different types of substrates were used (Cu1, Cu2, and Cu3 in Table I). One set of test devices was built on conventional 10 Ω-cm silicon wafers (Cu1). A second series of inductors used HRS wafers that were diced from floatzone silicon rods (Cu2). A third group of devices was built on sapphire substrates, as used in silicon-on-saphire (SOS) technology (Cu3).

For comparisons, two Al-interconnect processes with three (Al1, (4)) or five (Al2, (1)) metal levels, which have been used in our previous experiments, are described in Table I as well. The lateral dimensions of some of the inductors that

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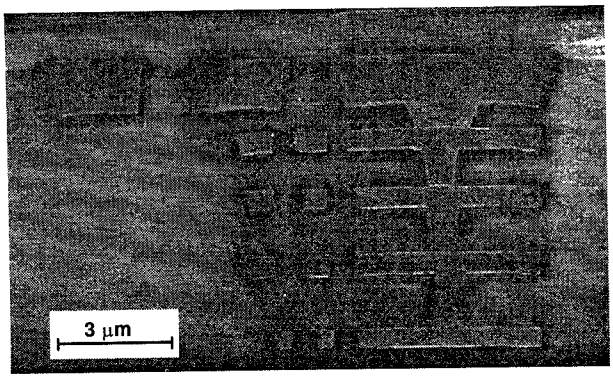

Fig. 2 Cross-sectional SEM of a five-level Cu-damascene interconnect structure with oxide isolation. (Note that the structure is illustrated to demonstrate the VLSI capability of the process; the dimensions of metal layers, vias, and oxide isolation are different from the ones used for the inductor fabrication.)

were fabricated are listed in Table II. According to the two different area sizes, the inductors are grouped in two types, the LA-type and the LB-type. The LB-type structures were the same as the ones used in (1). It is important to note that the Cu-damascene process is capable of providing a metal pitch as required for VLSI circuits, even though the inductor structures fabricated here had coarse dimensions (Fig. 2).

Results and Discussion

One-port S-parameter measurements were performed for inductor characterization (Fig. 3). Measurements up to 20 GHz were carried out on-wafer using high-frequency probes. The calibration procedure included de-embedding of the on-chip contact pad capacitance and the contact resistance. The error in de-embedding the contact resistance was not more than 0.2 Ω.

The inductances and Q-factors of the devices LA2 and LB2 as a function of frequency are shown in Fig. 4 and Fig. 5. The inductor LB2, fabricated by using the three level Cu-interconnect process (spiral coil at M3, underpass at M2,

TABLE I
PARAMETERS OF THE INTERCONNECT PROCESSES

	Metal Layers in Coil	Metal Thickness (T) and Type	Substrate Resistivity and Type	Underpass/ Substrate Spacing (H1)	Coil/ Substrate Spacing (H2)
Al1	M3	2 µm	10 Ω-cm	3.6 µm	5.7 µm
Al2	M3/M4/M5	4 µm	10 Ω-cm	4.5 µm	7.0 µm
Cu1	M3	2.5 µm	10 Ω-cm	4.5 µm	6.5 µm
Cu2	M3	2.5 µm	HRS	4.5 µm	6.5 µm
Cu3	M3	2.5 µm	Sapphire	4.5 µm	6.5 µm

TABLE II
DIMENSIONS OF THE TEST INDUCTORS

	LA2	LA4	LB2	LB5	LB8
Area (µm²)	500x500	500x500	226x226	226x226	226x226
No. turns (n)	16	8	3	4	6
Wire Width (W)	9 µm	22 µm	18 µm	16 µm	12 µm
Wire Space (S)	4 µm	4 µm	18 µm	10 µm	4 µm

M1 not used), but a standard silicon substrate (Cu1), had a Q_{max} that came close to the one achieved with the five-level Al-structure (Al2), as shown in Table III. The comparison of Cu1 and Al2 indicated that a single, 2.5 µm-thick Cu-layer can nearly substitute for three shunted Al-layers to form the spiral coil structure. The Q_{max} of Cu1 was ~1.7x greater than in a comparable three-level metal Al structure (Al1). With use of a HRS substrate, the Q_{max} was raised to 30, and for a sapphire substrate even to 40, which represents an improvement of 1.7x over the Q_{max} of 24 published in (1) and a 3.8x increase over the three-level metal process Al1.

It becomes apparent from Fig. 4 that the slope of Q at low frequency depends to first order on the dc resistance of the spiral coil and on the inductance and is therefore similar for the three cases. The comparison of the inductor, which was fabricated by using the process Cu1, to those built with the

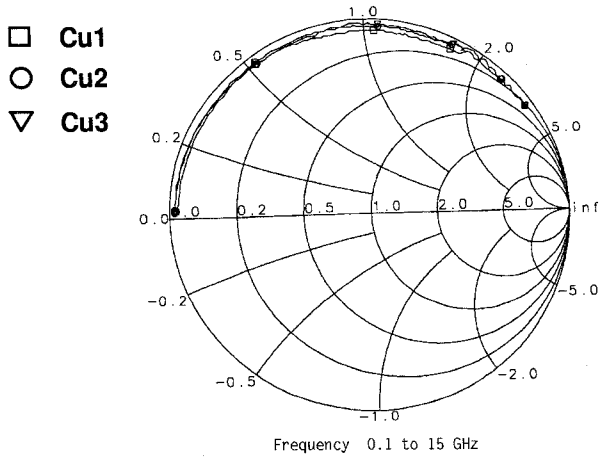

Fig. 3 Smith chart with measured S_{11} parameters of LB2-structures fabricated by using the processes Cu1, Cu2, and Cu3.

low-loss substrate processes Cu2 and Cu3 shows that the improved substrate quality leads to significantly higher Q_{max}-values but also to a shift of the Q_{max} to a higher frequency. The frequency dependence of the inductance and the Q can be modeled with good accuracy by using the lumped-element model in Fig. 6, as obvious from the example

in Fig. 7. In the model, an ideal inductance L_S, a coil resistance R_S, an inter-wire capacitance C_P, oxide capacitances C_{OX}, and bulk resistances R_B are considered (4).

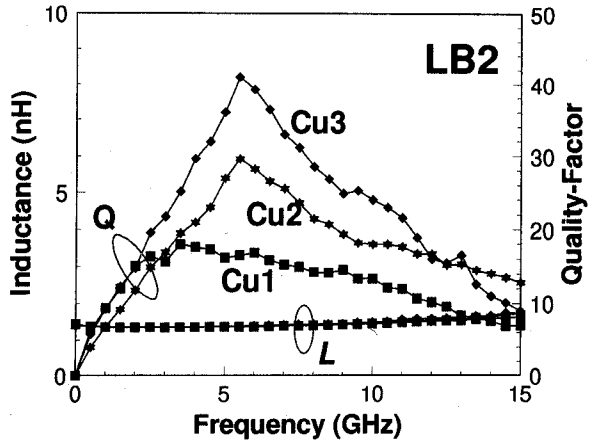

Fig. 4 Inductances and quality factors as functions of frequency for LB2-structures fabricated by using processes Cu1, Cu2, and Cu3.

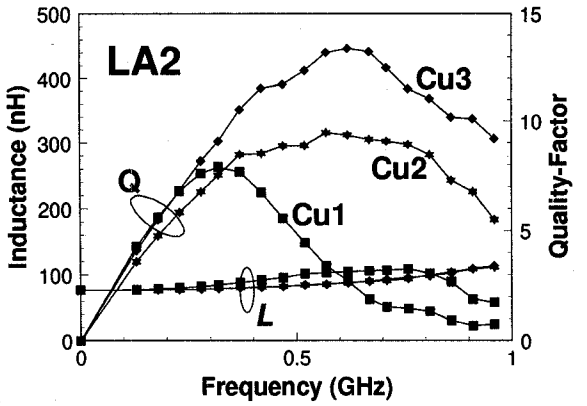

Fig. 5 Inductances and quality-factors as functions of frequency for LA2-structures fabricated by using the processes Cu1 Cu2, and Cu3.

The element parameters describing the inductor LB2 are listed in Table IV for the processes Cu1, Cu2, and Cu3. Their values reflect the process differences: the parameters L_S, R_S, and C_P depend mainly on the lateral dimensions. Since the lateral inductor layout was identical for the three cases, those values were very similar. The comparison of the values obtained for the processes Cu1 and Cu2 shows that the different bulk resistivities are properly reflected while the oxide capacitance remained the same. The oxide capacitance was significantly reduced for the sapphire substrate (Cu3) compared to the results with the silicon substrates (Cu1 and Cu2).

TABLE III
ELECTRICAL CHARACTERISTICS OF THE INDUCTORS

	LB2			LB5			LB8		
	Rdc (Ω)	L0 (nH)	Qmax at f/ GHz	Rdc (Ω)	L0 (nH)	Qmax at f/ GHz)	Rdc (Ω)	L0 (nH)	Qmax at f/ GHz
Al1	1.7	1.35	10.6/ 3.7	2.35	2.15	8.8/ 3.8	4.46	4.9	7.2/ 2.3
Al2	0.65	1.45	24/ 2.3	1.04	2.13	16/ 2.0	2.05	5.1	11.5/ 1.8
Cu1	0.75	1.35	18/ 3.7	0.93	2.13	14/ 3.5	1.76	4.9	11/ 2.1
Cu2	1.05	1.4	30/ 5.2	1.15	2.2	25/ 4.1	2.38	4.95	16/ 4.3
Cu3	0.67	1.39	40/ 5.8	1	2.15	33/ 5.6	1.9	4.95	17/ 4.1

	LA2			LA4		
	Rdc (Ω)	L0 (nH)	Qmax at f/ GHz	Rdc (Ω)	L0 (nH)	Qmax at f/ GHz
Al1	32.1	86	3.0/ 0.3	4.8	16.9	5.4/ 1.0
Al2	---	---	---	---	---	---
Cu1	13.9	80	8.0/ 0.3	2.8	16.3	10/ 0.5
Cu2	16.8	80	9.4/ 0.6	3.4	16.3	14/ 1.4
Cu3	14.9	80	13/ 0.6	3	16.2	17.5/ 1.9

A similar degree of improvement with the low-loss substrate processes Cu2 and Cu3 was observed for the other two inductors of the same area size, LB5 and LB8, which had been discussed last year as well ((1), Table III). Greater increases were achieved for *large-area* structures (LA2 and LA4), as obvious from Table III. Even though the Q_{max} becomes typically smaller at large inductance values (1),(2) a Q_{max} of 13 at 600 MHz was measured for a 80 nH-inductor fabricated by using the process Cu3.

Fig. 7 shows the Q_{max} values drawn *versus* the inductances for all inductors fabricated by using the processes Cu1-Cu3. It is first obvious from the results that the reduction in substrate losses translates into a higher Q_{max} over the entire range of inductances. For each inductor area size (LA-type or LB-type) there is an obvious trend that small inductances combine with a high Q_{max} and *vice-versa*. The slope of Q_{max} versus inductance, however, is larger for the small-area LB-type structures compared to the LA-type, so that beyond 5 nH inductance the LA-inductor structures provide the higher Q_{max}. This indicates that, besides the process technology improvement discussed in the bulk of this paper, also the lateral inductor geometry must be carefully optimized to achieve the highest possible Q_{max}.

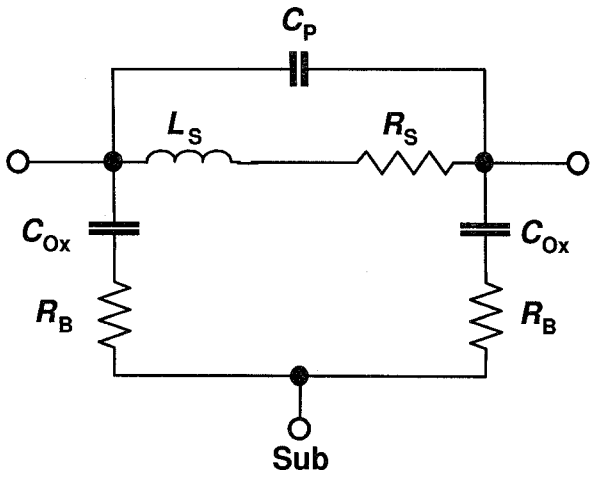

Fig. 6 Lumped-element model of the inductors

TABLE IV
LUMPED-ELEMENT PARAMETERS OF INDUCTORS LB2

	R_S (Ω)	L_S (nH)	C_P (pF)	C_{OX} (pF)	R_B (Ω)
Cu1	0.75	1.25	0.02	0.25	550
Cu2	1.05	1.32	0.03	0.25	1800
Cu3	0.8	1.32	0.03	0.02	1400

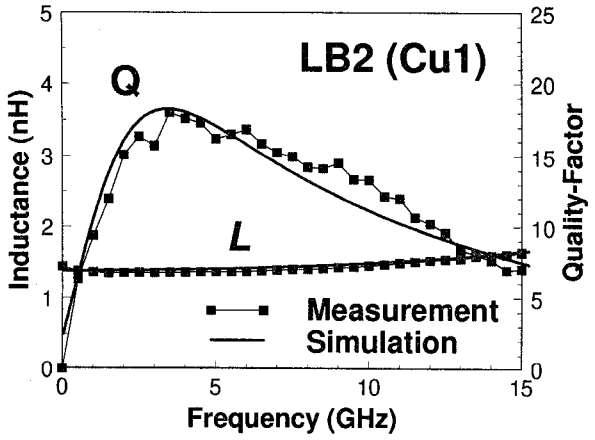

Fig. 7 Measured inductance and Q-factor as a function of frequency in comparison to the simulated characteristics derived from the lumped-element model in Fig. 6 with values from Table IV.

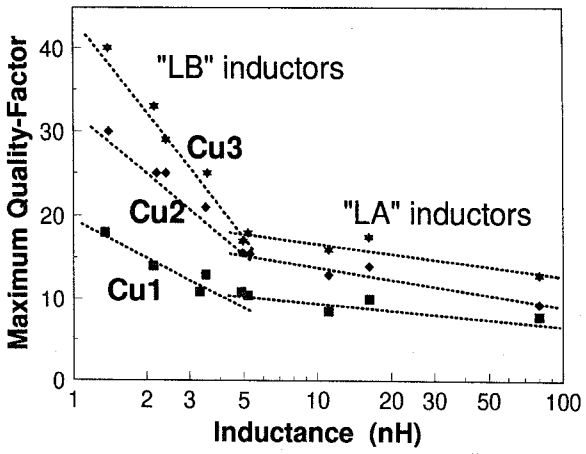

Fig. 7 Maximum quality-factors drawn *versus* the inductances of different spiral inductors. LB-type inductors have an area of 226x226 μm²; the area of LA-type devices is 500x500 μm². (The figure includes the results from inductors which are not listed in Tables II and III.

Conclusions

Very high quality factors were achieved for inductors fabricated in silicon technology by using Cu-damascene interconnects and low-loss substrates. It should be noted that the best results were achieved with sapphire substrates that can be used in a silicon-on-sapphire (SOS) configuration for circuit fabrication. Similar results are likely achievable with the use of SOI substrates that have a very thick buried oxide. The use of HRS-substrates may be more transparent to main-stream VLSI fabrication processes, and also for this option a considerable increase of the inductor-Q compared to a standard silicon substrate was indicated by our experimental results.

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