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United States Patent [19]

Aoyama et al.

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[54] **SEMICONDUCTOR DEVICE HAVING A WIRING LAYER WITH A BARRIER LAYER**

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[73] Assignee: **Kabushiki Kaisha Toshiba**, Kawasaki, Japan

[21] Appl. No.: **330,998**

[22] Filed: **Oct. 28, 1994**

[30]   **Foreign Application Priority Data**

Oct. 29, 1993	[JP]	Japan	5-272784
Mar. 15, 1994	[JP]	Japan	6-070156
Sep. 19, 1994	[JP]	Japan	6-249984

[51] **Int. Cl.**^{6} H01L 23/535; H01L 29/41; H01L 29/43

[52] **U.S. Cl.** 257/751; 257/752; 257/760; 257/763; 257/764; 257/762; 257/915

[58] **Field of Search** 257/750–753, 257/759, 760, 762, 773, 763, 764, 915

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[57]   **ABSTRACT**

A semiconductor device comprises a semiconductor substrate in which a semiconductor element is formed, an interlayer insulating film formed on the semiconductor substrate, an insulating barrier layer, formed on the interlayer insulating film by plasma nitriding, for preventing diffusion of a metal constituting a wiring layer, a conductive barrier layer, formed on the insulating barrier layer, for preventing diffusion of the metal, and a wiring layer formed of the metal on the conductive barrier layer. A bottom portion of the wiring layer is protected by the conductive barrier layer and the insulating barrier layer. Therefore, the diffusion of the metal constituting the wiring layer can be surely prevented.
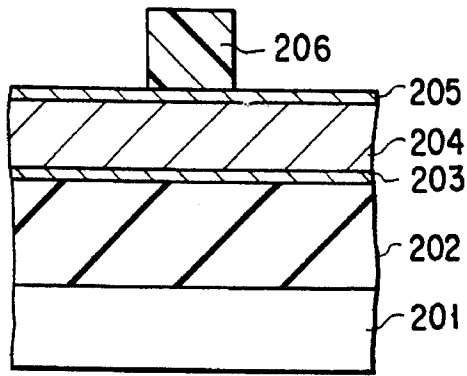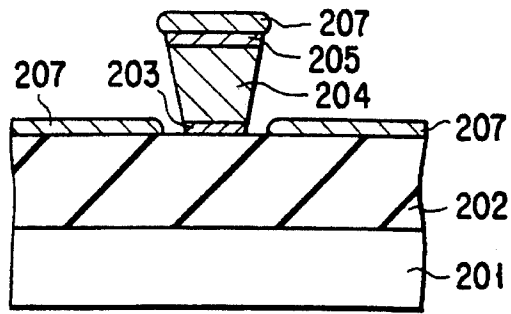
5 Claims, 35 Drawing Sheets
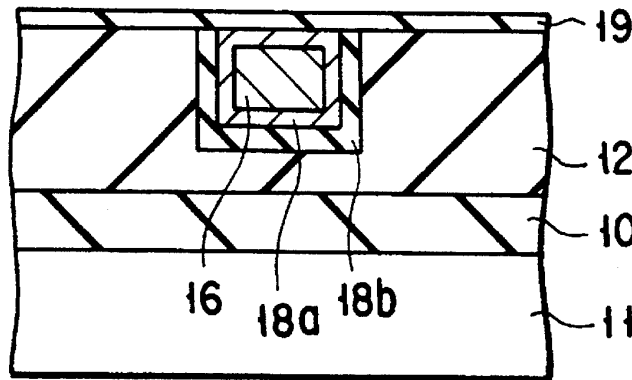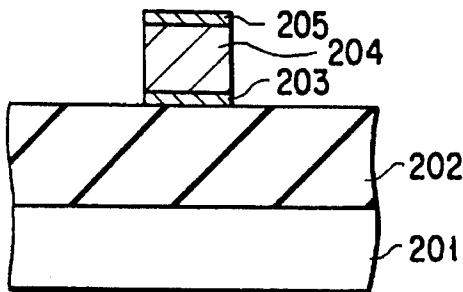
FIG. 1A   PRIOR ART
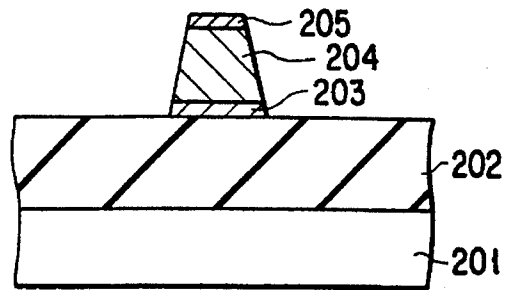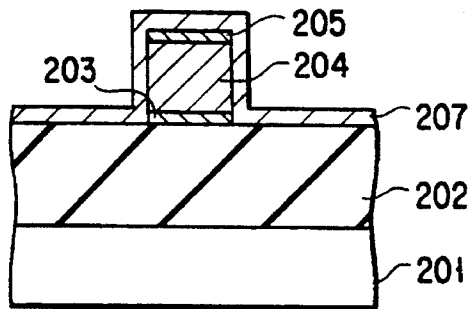
FIG. 2A   PRIOR ART

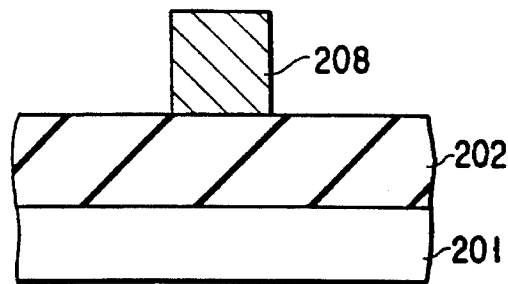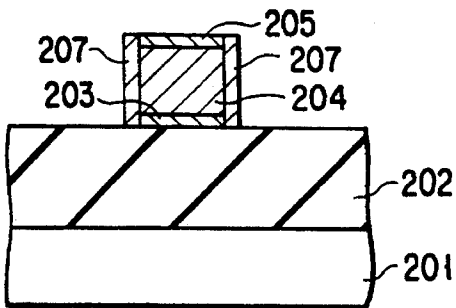FIG. 1B   PRIOR ART

FIG. 2B   PRIOR ART
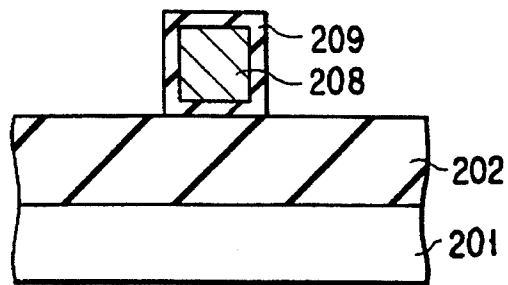
FIG. 1C   PRIOR ART

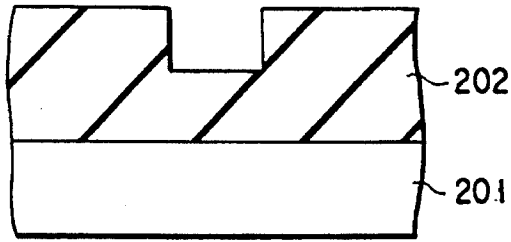FIG. 3A   PRIOR ART

FIG. 1D   PRIOR ART
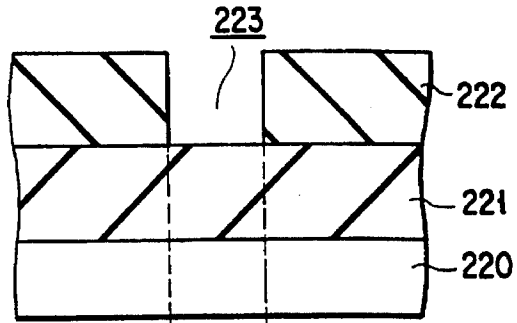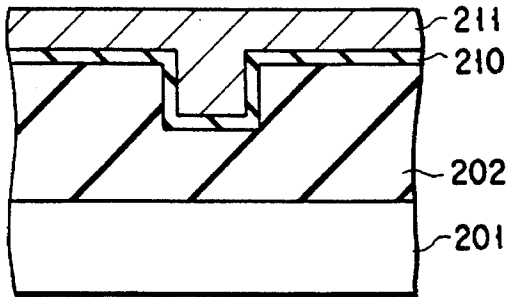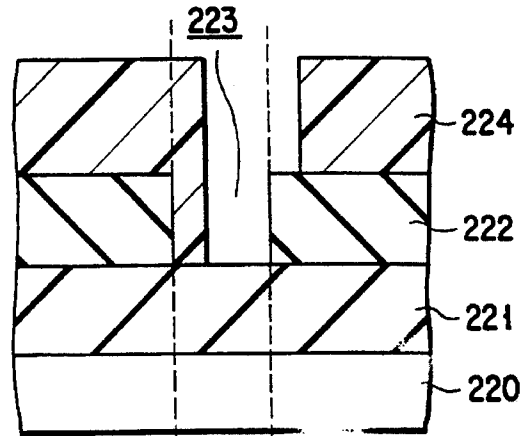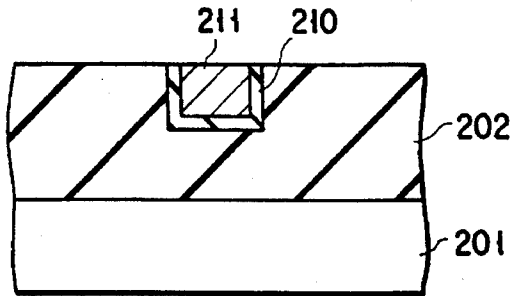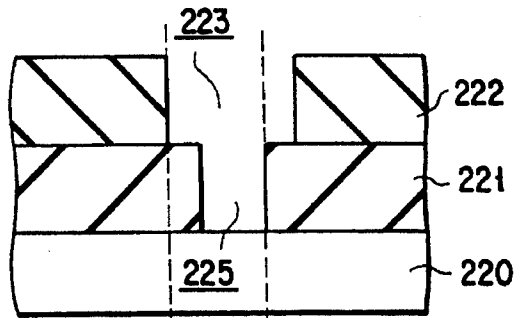
FIG. 3B   PRIOR ART

F I G. 4A PRIOR ART

F I G. 5A PRIOR ART

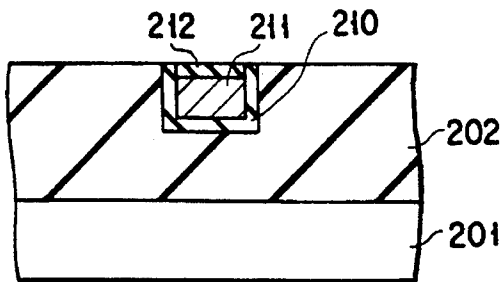F I G. 4B PRIOR ART

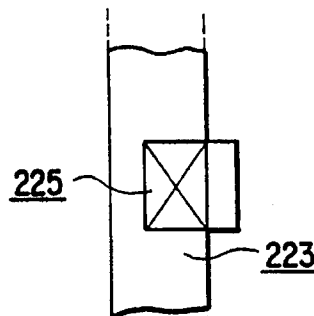
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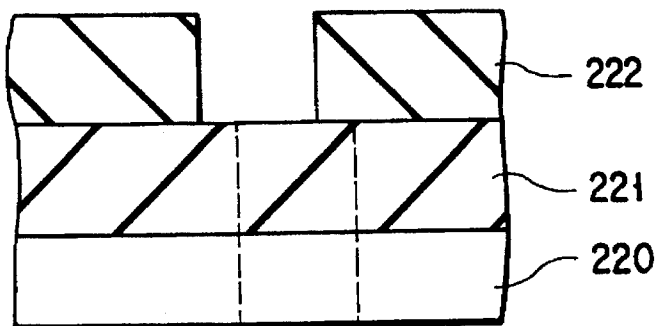

F I G. 4C PRIOR ART

F I G. 5C PRIOR ART

F I G. 4D PRIOR ART

F I G. 5D PRIOR ART

PRIOR ART

F I G. 6 A

— 222

— 221

— 220

PRIOR ART

F I G. 6 B

— 226

— 222

— 221

— 220

223

PRIOR ART

F I G. 6 C

— 222

— 221

— 220

225

225

PRIOR ART

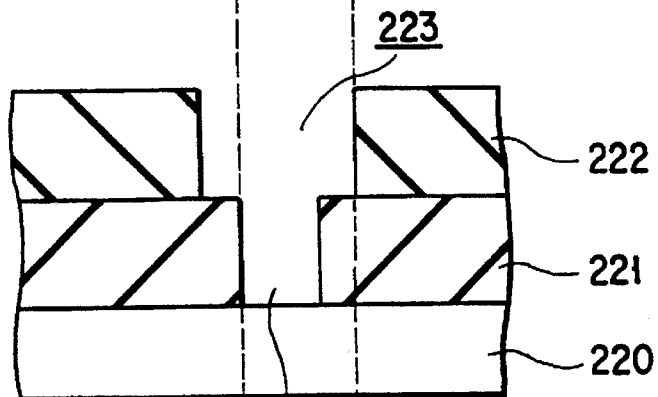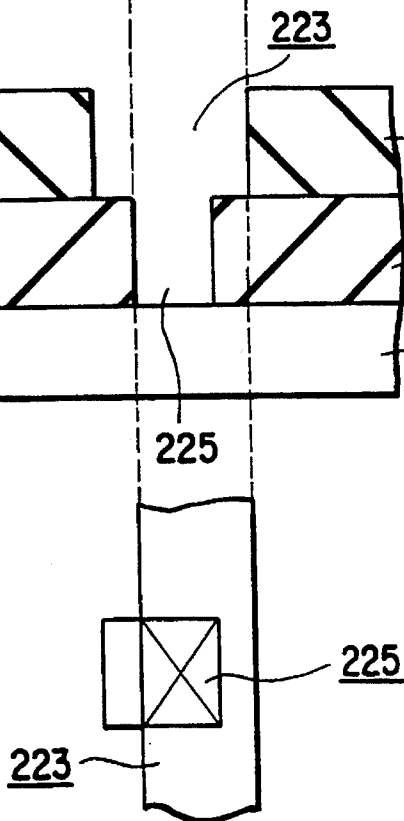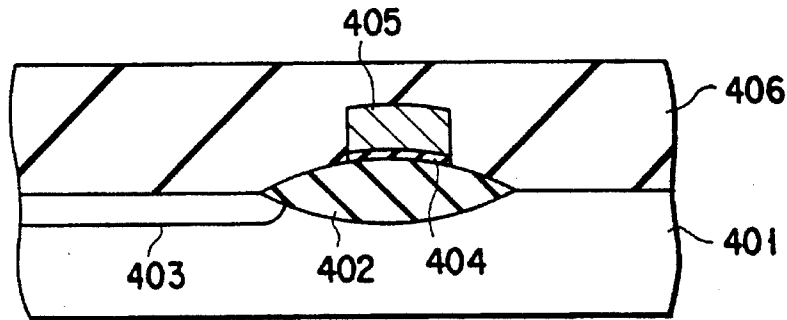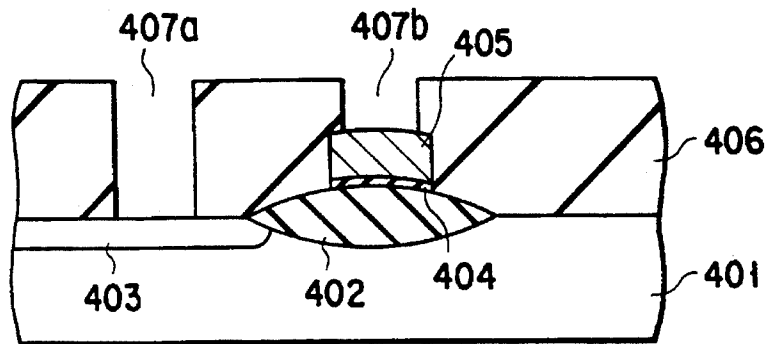F I G. 6 D

223
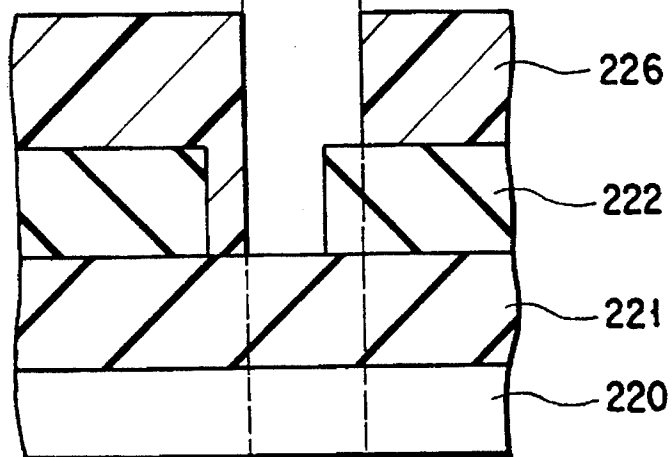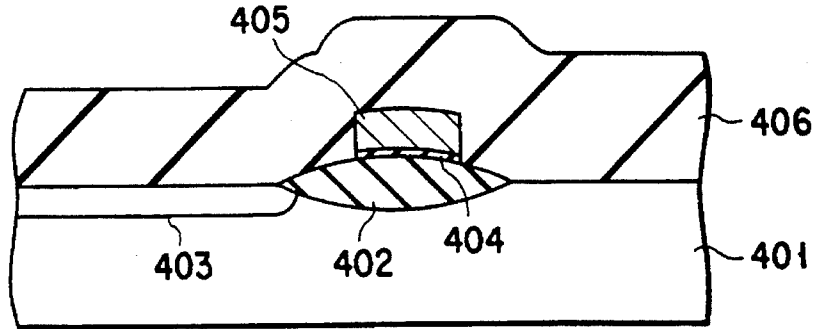
PRIOR ART
F I G. 7A
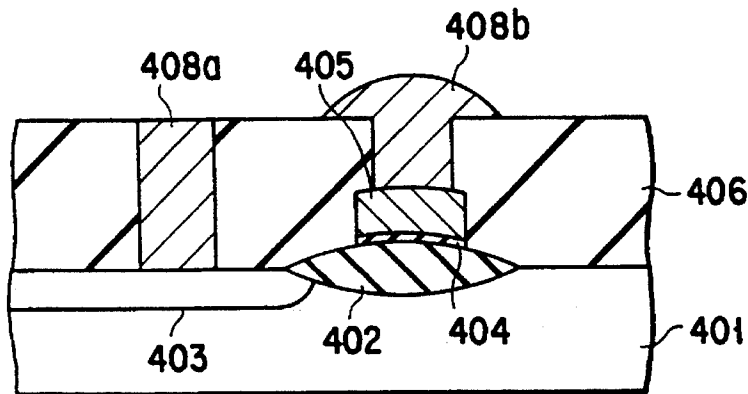
PRIOR ART
F I G. 7B

PRIOR ART
F I G. 7C

PRIOR ART
F I G. 7D

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