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United States Patent [19]

Ueda et al.

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[54] **SEMICONDUCTOR DEVICE WITH A FIELD-EFFECT TRANSISTOR HAVING A LOWER RESISTANCE IMPURITY DIFFUSION LAYER, AND METHOD OF MANUFACTURING THE SAME**

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[73] Assignee: **Matsushita Electric Industrial Co., Ltd.**, Osaka, Japan

[21] Appl. No.: **571,131**

[22] Filed: **Dec. 12, 1995**

Related U.S. Application Data

[63] Continuation-in-part of Ser. No. 340,341, Nov. 14, 1994, abandoned.

[30] **Foreign Application Priority Data**

Nov. 15, 1993 [JP] Japan 5-284820
Oct. 26, 1995 [JP] Japan 7-278546

[51] **Int. Cl.**[6] **H01L 21/265**

[52] **U.S. Cl.** **438/289**; 438/297; 438/301; 438/586; 438/691

[58] **Field of Search** ..... 437/40 R, 40 GS, 437/40 RG, 41 R, 41 GS, 44, 45, 187, 979, 228 POL, 29, 228 PL; 156/636.1, 645.1; 216/52; 148/DIG. 163; 438/289, 297, 301, 586, 691

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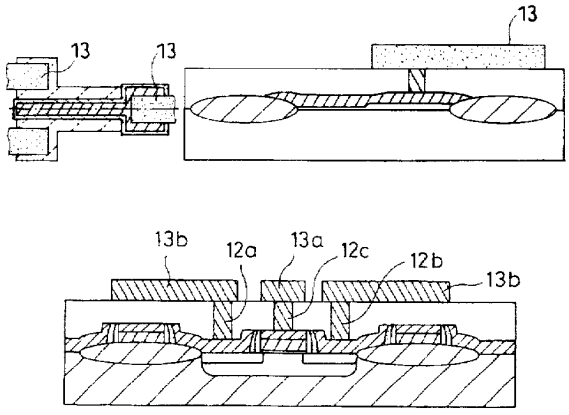
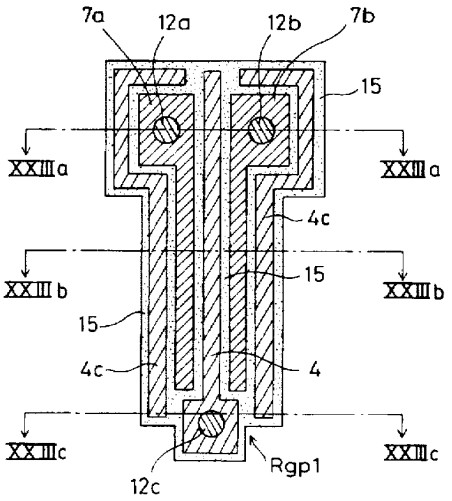
[57] **ABSTRACT**

There is formed an isolation which surrounds an active region of a semiconductor substrate. Formed over the active region and on the isolation, respectively, are a gate electrode and two gate interconnections on both sides thereof. Between the gate electrode and the gate interconnections are located two first interspaces each of which is smaller in width than a specified value and a second interspace which is larger in width than the specified value and interposed between the two first interspaces. In forming side walls on both side faces of the gate electrode and gate interconnections by depositing an insulating film on the substrate, the first interspaces are buried with the insulating film. Thereafter, a metal film is deposited on the substrate, followed by chemical mechanical polishing till the gate electrode, gate interconnections, and side walls become exposed. By the process, withdrawn electrodes from a source/drain region for contact with the active region is formed by self alignment, while the withdrawn electrodes are insulated from the gate electrode and gate interconnections by the side walls.

11 Claims, 27 Drawing Sheets





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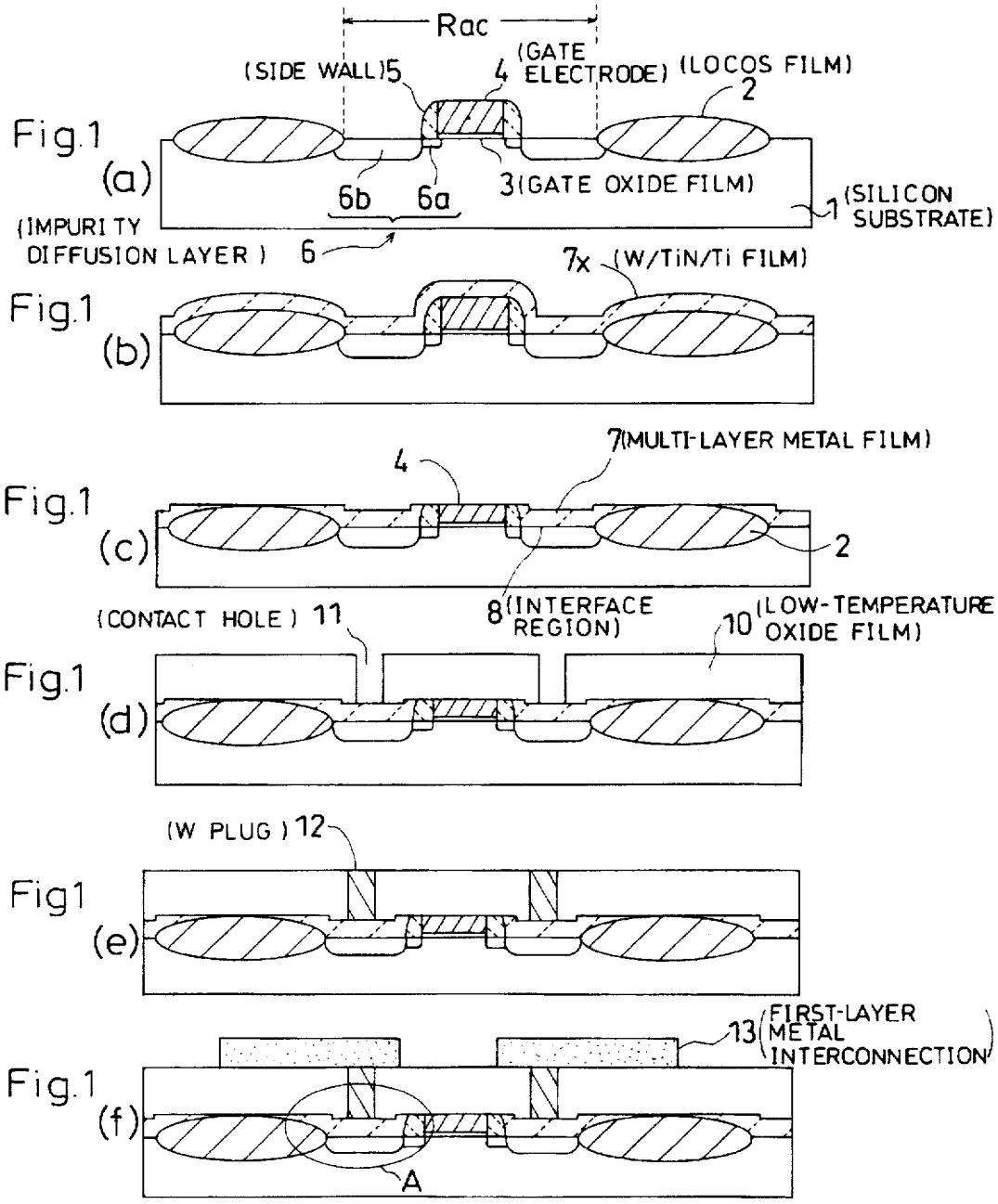

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Fig.2

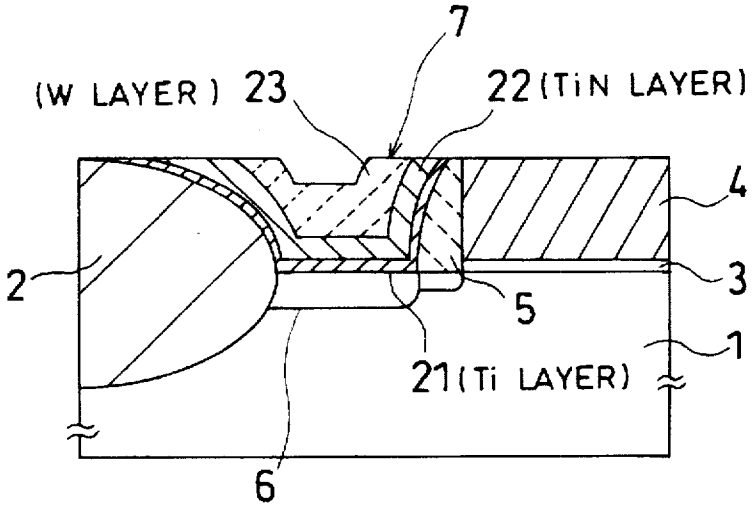
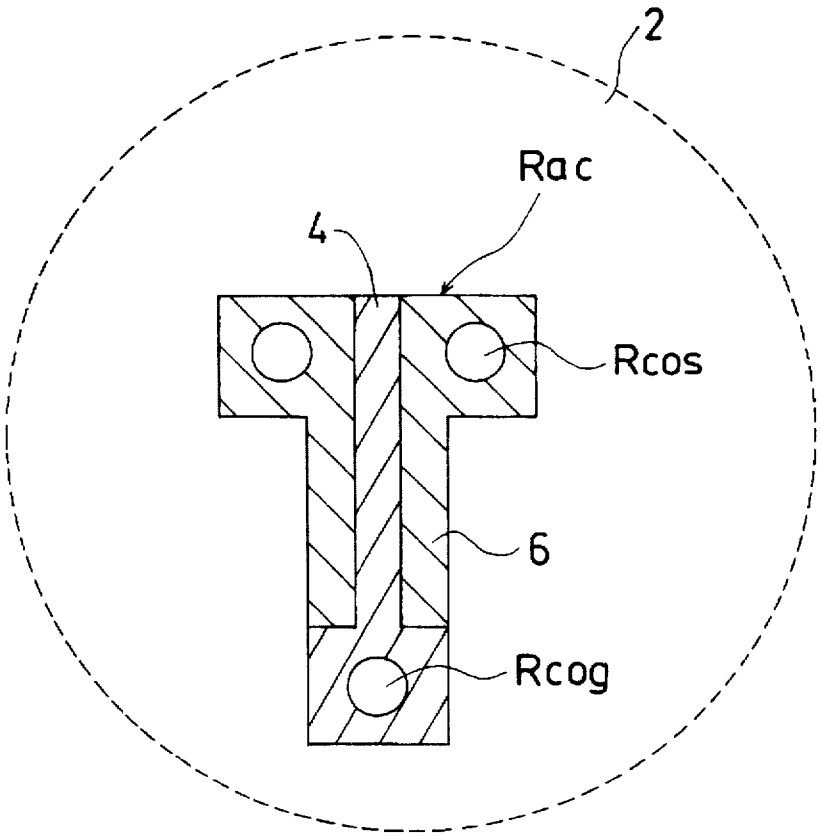


Fig.3



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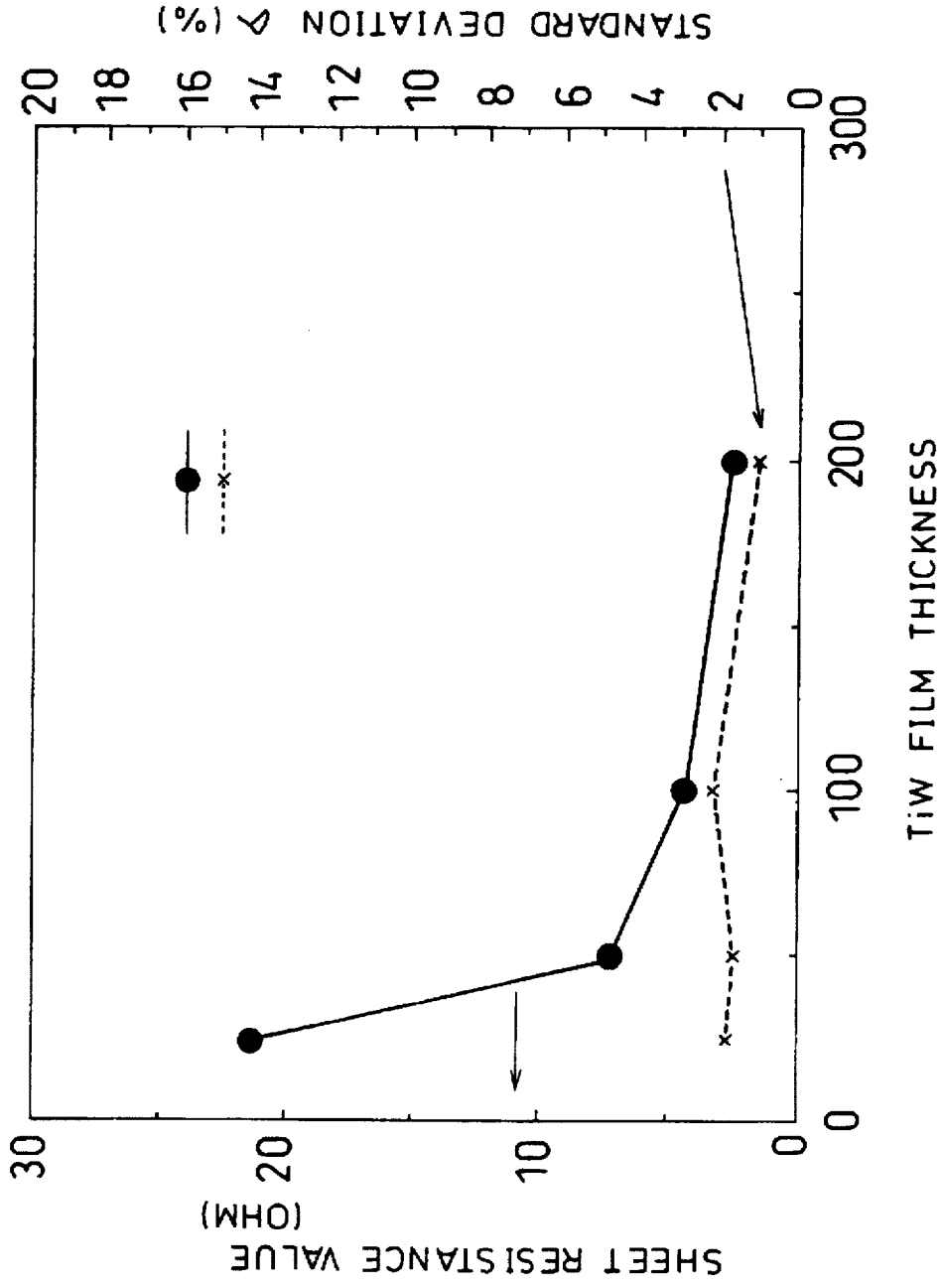

Fig.4

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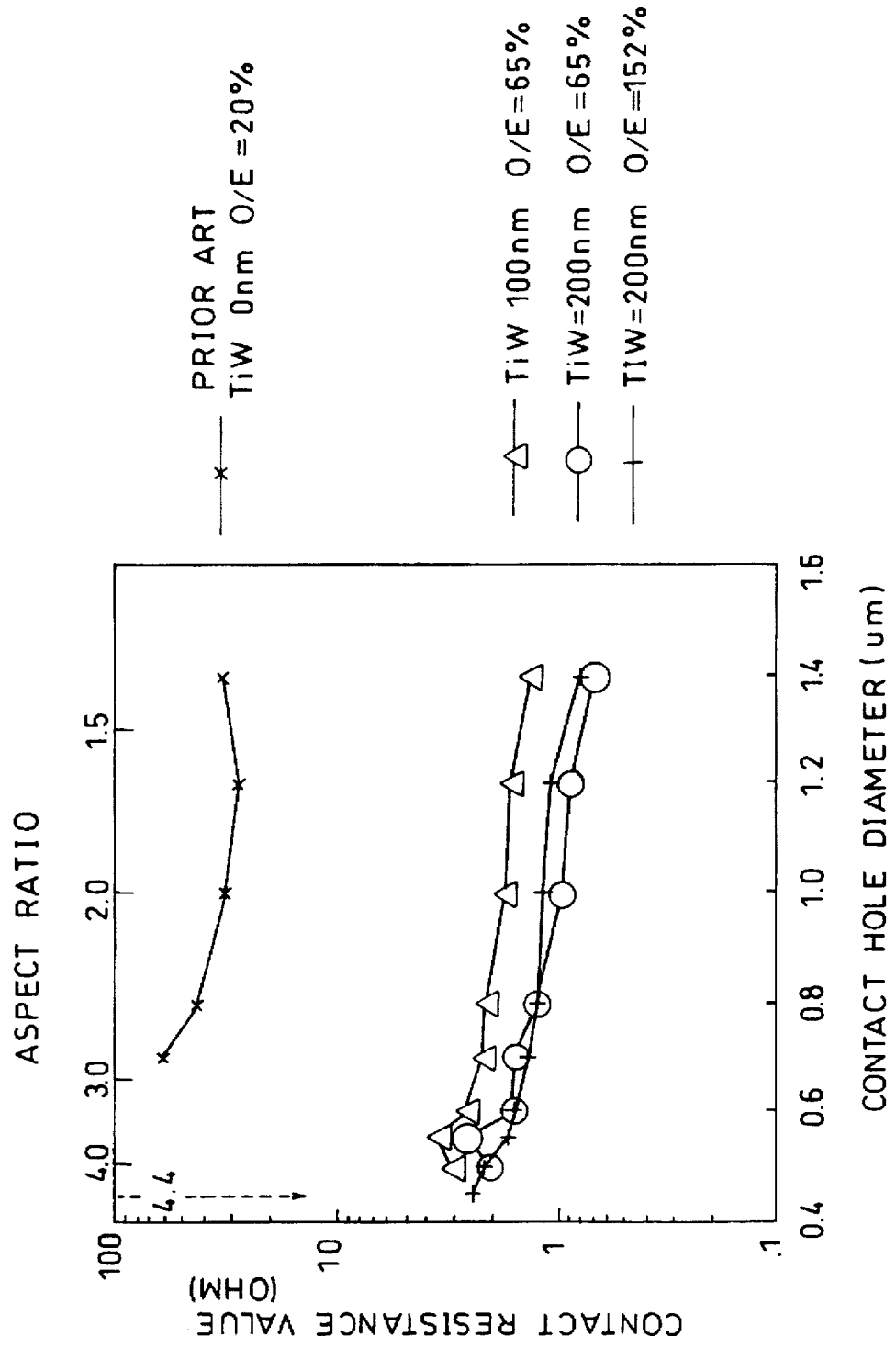
Fig.5



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