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Douglas

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[54] METHOD FOR FORMING LOCAL INTERCONNECTS USING SELECTIVE ANISOTROPY

[75] Inventor: **Monte A. Douglas,** Coppell, Tex.

[73] Assignee: **Texas Instruments Incorporated,** Dallas, Tex.

[21] Appl. No.: **402,944**

[22] Filed: **Sep. 5, 1989**

Related U.S. Application Data

[63] Continuation-in-part of Ser. No. 273,287, Nov. 17, 1988, Pat. No. 4,863,559, which is a continuation of Ser. No. 159,282, Feb. 22, 1988, Pat. No. 4,793,896.

[51] **Int. Cl.**^{5} **B44C 1/22;** C03C 15/00; C03C 25/06; C23F 1/02

[52] **U.S. Cl.** **156/643;** 156/646; 156/662; 156/659.1; 204/192.35

[58] **Field of Search** 156/643, 646, 652, 653, 156/655, 656, 657, 659.1, 662, 667; 204/192.32, 192.35, 192.37; 357/23.1, 65, 67; 437/180, 200, 228; 252/79.1

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Primary Examiner—William A. Powell
Attorney, Agent, or Firm—Rodney M. Anderson

[57] **ABSTRACT**

A method for etching titanium nitride local interconnects is disclosed. A layer of titaniun nitride is either formed as a by-product of the formation of titanium silicide by direct reaction or by deposition. The location of the interconnects is defined by patterning photoresist at the desired locations. A plasma etch using a chlorine-bearing agent such as CCl_4 as the etchant etches the titanium nitride anisotropically at those locations covered by photoresist, and isotropically elsewhere, so that filaments of the titanium nitride are removed without undercutting the photoresist mask. The etch is selective relative to the underlying material, such as a refractory metal silicide, refractory metals, or silicon, due to the passivation of the underlying material by the carbon atoms of the CCl_4. The selectivity, together with the selective anisotropy, even allows significant overetch of the material to remove the filaments without undercutting the masked interconnect material.

29 Claims, 4 Drawing Sheets

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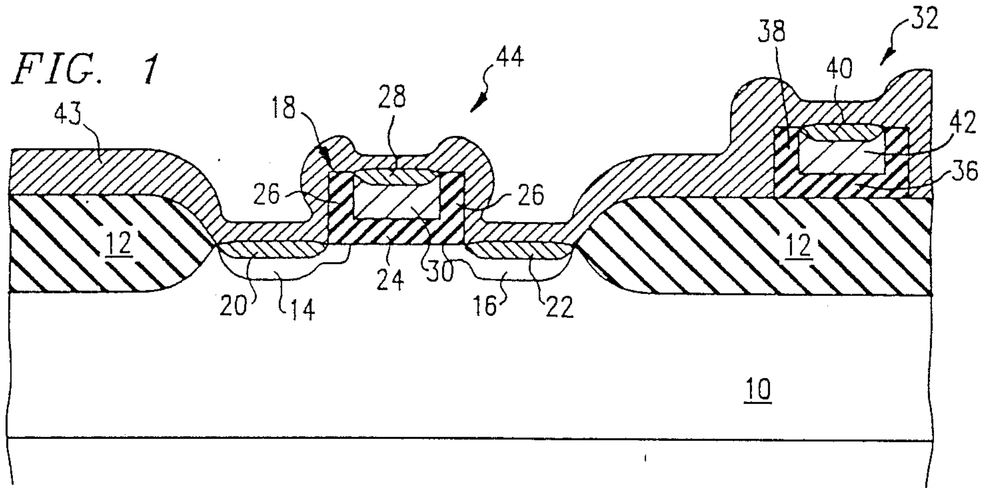

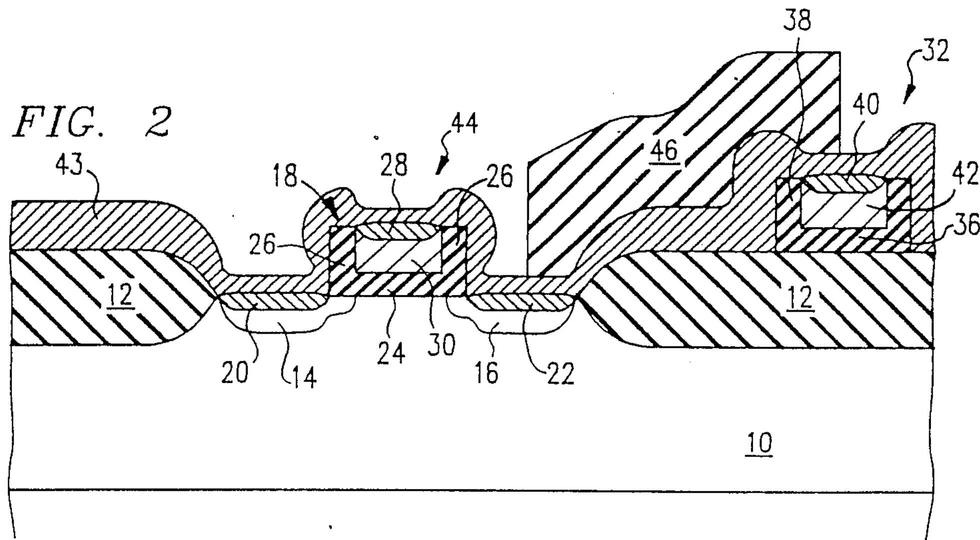

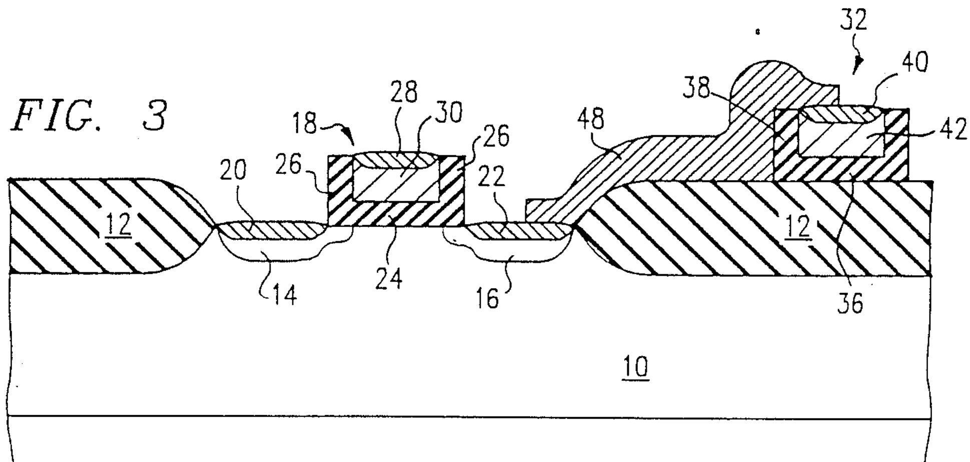

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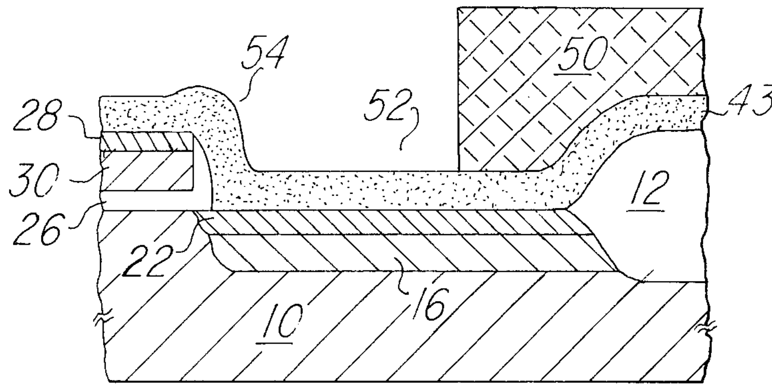

Fig. 4a

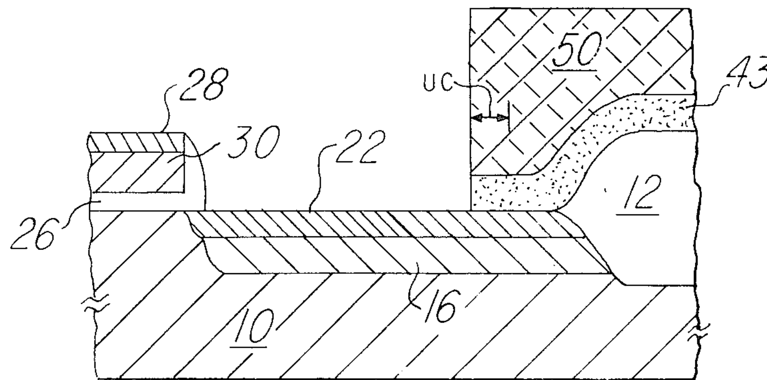

Fig. 4b

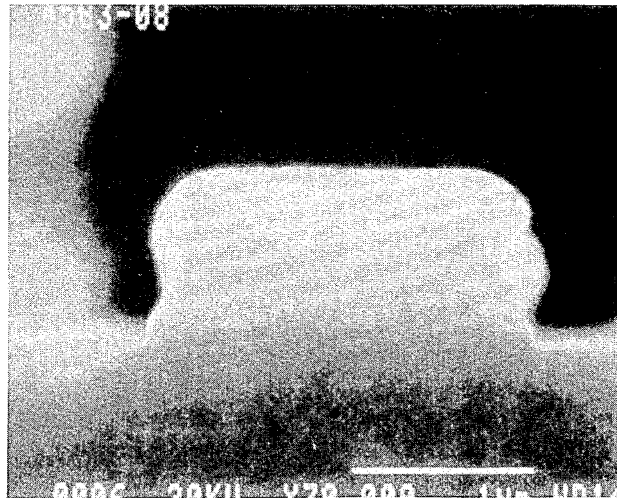

Fig. 5

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METHOD FOR FORMING LOCAL INTERCONNECTS USING SELECTIVE ANISOTROPY

This application is a continuation-in-part of application S.N. 273,287 filed Nov. 17, 1988, now U.S. Pat. No. 4,863,559, which is a continuation of application S.N. 159,282 filed Feb. 22, 1988, now U.S. Pat. No. 4,793,896 issued Dec. 27, 1988.

This invention relates in general to semiconductor devices, and in particular to an improved method for forming local interconnects using chlorine bearing agents.

BACKGROUND OF THE INVENTION

Increasing the number of levels of interconnects (both intra-level and inter-level) in integrated circuits provides additional routing capability, more compact layouts, better circuit performance and greater use of circuit design within a given integrated circuit surface area. A particularly useful level of connection is commonly called local interconnection, where neighboring diffused areas are connected to one another, and to neighboring polysilicon and metal lines.

For example, a conventional method for creating local interconnects uses metal interconnection of diffused regions to one another, as well as to other layers. The metal interconnection is formed by etching vias through a thick oxide layer to the locations to be interconnected. A conductor is then formed to fill the vias and make the connection. This method is limited, for purposes of reducing the area required for such connection, by the state of the technology of etching contact holes and the planarization of interlevel dielectrics. These limitations include the alignment tolerance of the vias to the underlying region to be connected, the size of the via required (and accordingly the size of the contact area in the underlying region) which can be reliably etched, and the step coverage of the conductor in filling the via and making good ohmic contact to the underlying region. Also, the additional layer of a metallic conductor across the dielectric contributes to a loss of planarization in subsequent levels.

An alternative method developed by Hewlett Packard and published at page 118 of the 1984 IEDM Proceedings uses additional patterned silicon to provide conductive silicide regions extending over the field oxide as desired. A layer of titanium is deposited over the substrate and, prior to the direct reaction of the titanium with the underlying silicon to form the silicide, a thin layer of silicon is patterned on top of the titanium metal to define an interconnect extending over a silicon dioxide region separating the two regions to be interconnected. Where this silicon layer remains, a silicide is formed during the reaction process extending over the oxides. This method requires the deposition and patterning of the additional layer of silicon to define the local interconnection. In addition, the resulting silicide strap provides a conduit through which typical n-type dopants such as phosphorous can diffuse, since titanium silicide is a very poor diffusion barrier to conventional semiconductor dopants. If a silicide strap is used to connect n-type regions to p-type regions, for example n-doped polysilicon to p-type diffusion, subsequent processing must be done at relatively low temperatures to minimize the counterdoping of the p-type region

with the n-type dopant through the silicide interconnect.

Another known method uses molybdenum metal as a local interconnect material. Molybdenum, however, also acts as a diffusion conduit through which phosphorus, used to dope n-type regions of the semiconductor device, can diffuse. The molybdenum interconnect therefore is not an effective local interconnect between n-type and p-type regions, as the p-type regions can be undesirably counterdoped by the phosphorous diffusing through the molybdenum, similarly as the silicide strap interconnect.

Another local interconnection method is disclosed in U.S. Pat. No. 4,675,073, issued to me on June 23, 1987, and assigned to Texas Instruments Incorporated, incorporated herein by this reference. As disclosed therein, the desired local interconnect is formed by patterning the residual titanium compound, for example titanium nitride, from the direct reaction forming titanium silicide cladding of the diffusions and polysilicon gates. The titanium nitride is sufficiently conductive so that it is useful to make local interconnections between neighboring regions. The disclosed process uses carbon tetrafluoride (CF_4) as the reactant in a plasma etch to remove the undesired titanium nitride faster than titanium silicide. This plasma etch using carbon tetrafluoride etches titanium nitride or titanium oxide at approximately twice the rate it removes titanium silicide. This technique also etches silicon oxides at twice the rate, and photoresist at five times the rate, as it etches titanium nitride or titanium oxide. Additionally, products of the etching process include solids that tend to adhere to the etching device. This requires extra maintenance and cleanup time that is nonproductive. Thus, a need has arisen for a method for producing a local interconnect with increased selectivity to the refractory metal compound of the local interconnect (e.g., titanium nitride or titanium oxide) relative to silicides, silicon oxides and photoresist, so that an additional layer of interconnection may be more consistently manufactured with precisely located interconnects and improved planarization compatible with sub-micron technology.

For purposes of forming such small feature sizes for the interconnect, it is well known that etches which are substantially anisotropic (i.e., directional) are preferred. Anisotropic etches provide improved control in fabrication, since the patterned masking material more closely defines the feature to remain after the etch; etches which are more isotropic tend, of course, to undercut the mask, requiring that the size of the patterned masking material be made larger than that of the desired feature in order to compensate for the line width loss resulting from the undercut.

However, substantially anisotropic etches can leave filaments of the material being etched. Such filaments tend to occur at locations where the etched material makes a step over surface topography. In the case of the local interconnect discussed above, such filaments can create a short circuit between conductive structures at the top of, and at the bottom of, a step where no such connection is desired. In addition, filaments may be present laterally, connecting two otherwise unconnected structures.

It should also be noted that the titanium nitride may be used as a gate material, especially in the case where it is deposited. Similar problems concerning the etch as described above will also affect the etch of such tita-

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nium gate electrodes, as well as other structures for which a conductive titanium compound may be used.

It is therefore an object of this invention to provide an etch for the residual material over insulating layers remaining from the direct react silicidation which is anisotropic at the locations where the masking layer is in place to define the interconnect, but which is isotropic elsewhere so that filaments of the interconnect material are removed.

It is a further object of this invention to provide such an etch which also has improved etch selectivity (i.e., an increased etch rate ratio) of the interconnect relative to underlying conducting layers.

It is a further object of the present invention to provide such an etch with improved selectivity to titanium nitride or titanium oxide with respect to titanium silicide, silicon dioxide and photoresist.

It is a further object of the present invention to provide such an etch which reduces the preventative maintenance and cleanup schedules and procedures by the use of a chlorine bearing agent as opposed to a flourine agent.

Other objects and advantages of the invention will become apparent to those of ordinary skill in the art having reference to the following specification in conjunction with the drawings.

SUMMARY OF THE INVENTION

The invention may be incorporated into a method for forming a local interconnect on a semiconductor surface. A dielectric layer of a prefabricated integrated circuit is covered with a conductive chemical compound of a refractory metal, such as titanium. The compound may be formed by deposition, or as a by-product of the silicidation of the refractory metal at locations where it is in contact with the underlying semiconductor. Photoresist is placed over this chemical compound layer to protect a specific portion thereof which will serve as an interconnect. A chlorine bearing agent is used to etch the exposed conductive chemical compound layer, which occurs in substantially an anisotropic manner at those locations where the photoresist is in place. At those locations where the photoresist is absent, the etch is substantially isotropic. Accordingly, the etch removes filaments which may otherwise remain upon clearing of the surfaces, without undercutting the photoresist mask. The chlorine bearing agent etches the conductive chemical compound at a greater rate than the underlying silicide, or other material used as a conductor.

BRIEF DESCRIPTION OF THE DRAWINGS

For a more complete understanding of the present invention, and for further advantages thereof, reference is now made to the following description taken in conjunction with the accompanying drawings in which:

FIG. 1 is a cross-sectional view of a partially fabricated integrated circuit with a titanium chemical compound formed over the entire surface;

FIG. 2 is a cross-sectional view of the device of FIG. 1 with patterned masking material added over the area to be protected;

FIG. 3 is a cross-sectional view of an integrated circuit with a local interconnect formed in accordance with the present invention.

FIGS. 4*a* and 4*b* are cross-sectional views of an integrated circuit with a local interconnect formed according to an alternate embodiment of the invention.

FIG. 5 is a cross-sectional SEM microphotograph illustrating the anisotropy of the etch described herein.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

FIG. 1 shows the first step utilizing the method of the preferred embodiment of the present invention, as directed to an integrated circuit wafer **44**. Wafer **44** contains a semiconducting substrate **10** formed of silicon. Field oxide **12**, preferably silicon dioxide (SiO_2), is grown or deposited in selected portions of the surface of the substrate **10** for isolation of active regions from one another according to the well known local oxidation (LOCOS) isolation technique; of course, other isolation techniques such as trench isolation may alternatively be used. The active transistors of the integrated circuit device are formed into the locations of the surface of substrate **10** not covered with field oxide **12**, such locations commonly called moat regions. In FIG. 1, a transistor **44** is shown having source and drain regions **14** and **16**, respectively, diffused into the moat region between two portions of field oxide **12**. Source and drain regions **14** and **16** are generally implanted and subsequently diffused after the placement of polysilicon gate electrode **30** over gate dielectric **24**, so that source and drain regions **14** and **16** are self-aligned relative to gate electrode **30**. As described in U.S. Pat. No. 4,356,623, issued Nov. 11, 1982 and assigned to Texas Instruments Incorporated, the incorporation of sidewall oxide filaments **26** along the side of gate electrode **30** provide for a graded junction, as shown in FIG. 1. FIG. 1 further illustrates a polysilicon layer **42** overlying field oxide **12** serving as an interconnect to another portion of the integrated circuit, for example extending to another moat region (not shown) and serving as the gate electrode for a transistor.

In this embodiment of the invention, source and drain regions **14** and **16**, and gate electrodes **30** and **42**, are clad with a refractory metal silicide such as titanium silicide. This cladding is performed by depositing a layer of the refractory metal, and subsequently heating the wafer **44** so that the metal directly reacts with the underlying silicon to form the silicide, as described in U.S. Pat. No. 4,384,301, issued on May 17, 1983 and assigned to Texas Instruments Incorporated. An example of the conditions for such direct reaction is heating the wafer **44** in a nitrogen and argon ambient at a temperature on the order of 675° C. Other methods of achieving the direct reaction may alternatively be used, for example, by use of a single-wafer Rapid Thermal Processor (RTP) where the wafer **44** is rapidly heated to the appropriate temperature for a sufficient amount of time to perform the direct reaction described above. It has been determined by physical analysis that the titanium silicide formed in this manner may not be stoichiometrically, or chemically, pure titanium silicide, but that measurable amounts of other materials such as silicon oxide and other oxides are also present in the film.

As described in said U.S. Pat. No. 4,675,073, where titanium is used as the refractory metal, as a result of the direct reaction process a layer of a conductive titanium compound covers the surface of the wafer **44**, including the silicide regions. Referring to FIG. 1, source region **14**, drain region **16**, and gate electrodes **28** and **42** are shown clad with titanium silicide film **20**, **22**, **28** and **40**, respectively. A layer **43** of residual material containing, for example, titanium nitride if the direct reaction is

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