LOCMOS, a new technology for complementary MOS circuits

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Although the good characteristics of complementary MOS transistors have been known for some time, they have been very little used in LSI (large-scale integration) circuits because of the complicated processes and the low packing density. Now that the LOCOS technique is available CMOS transistors can be used to produce LSI circuits with high packing density and good electrical characteristics.

A type of MOS-transistor circuit arrangement that has now been known for several years is the 'complementary MOST circuit' (CMOS). The circuit has been given this name because it contains both *N*- and *P*-channel MOS transistors. Such circuits can have significant advantages over conventional MOS circuits [1]. The most important advantage is the low current level in logic circuits, giving a low dissipation. This enables static logic to be produced that would encounter considerable problems of heat dissipation if made entirely with *N*-channel or *P*-channel MOS transistors [2].

We shall explain this with the example of an inverter circuit. *Fig. 1a* shows such a circuit, made from CMOS transistors. With a positive supply voltage V_{dd}, if a positive voltage V_i is applied to the input (logic state '1'), then the *N*-channel transistor becomes conducting while the *P*-channel transistor does not conduct. The output voltage is then zero (logic state '0'). If the voltage is now removed from the input ('0'), the *P*-channel transistor becomes conducting and the *N*-channel transistor is switched off. The output voltage is now V_{dd} ('1'). The two MOS transistors therefore behave as switches, and the current in the circuit is determined by the very small leakage current of the switched-off MOS transistor. The current has a larger value only temporarily, during the switching, when there is some dissipation.

By way of comparison fig. 1*b* shows an inverter circuit made up from *P*-channel transistors [3]. The supply voltage here is $-V_{dd}$. If no voltage is applied to the input ('0') the lower MOS transistor, the 'switching transistor', does not conduct but the upper one, the 'load transistor' does. The output voltage is then equal to the difference between the supply voltage and the threshold voltage V_{th} of the load transistor: $-V_{dd} + V_{th}$ ('1'). When a negative input voltage is

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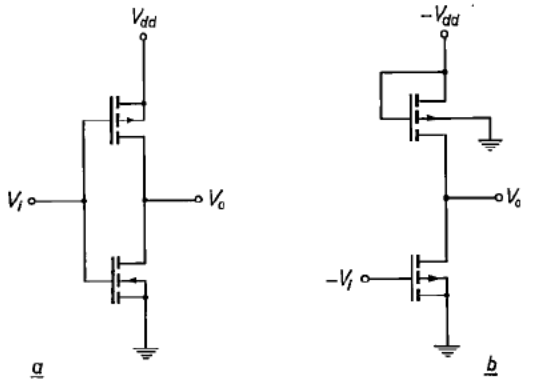

Fig. 1. *a*) An inverter circuit (schematic) consisting of an MOS transistor with a *P*-type channel *(above)* and another with an *N*-type channel *(below)*. The two gates are connected together, as are the two drains ('complementary' MOS transistors, CMOS for short). With a positive supply voltage V_{dd} and an input voltage V_i (logic state '1') the *N*-channel transistor conducts and the *P*-channel transistor does not. The output voltage V_o is now zero (logic state '0'). If $V_i = 0$ (state '0') the situation is reversed and the output voltage equals V_{dd} ('1'). The two transistors function as switches and in both states the only current in the circuit is the leakage current of one transistor.
b) Schematic circuit of an inverter circuit consisting of two *P*-channel MOS transistors, with the drain of one connected to the source of the other. With a negative supply voltage $-V_{dd}$ and a negative input voltage $-V_i$ ('1') both transistors conduct. The output voltage is then determined by the ratio of the channel resistances of the two transistors. If the channel resistance of the lower transistor, the 'switching transistor', is much smaller than that of the upper one, the 'load transistor', the output voltage is also very small ('0'). A current determined by the value of the channel resistances now flows in the circuit. If $V_i = 0$ (state '0'), the switching transistor does not conduct and the load transistor does. The output voltage is then equal to $-V_{dd} + V_{th}$ ('1'), where V_{th} is the threshold voltage of the load transistor. Only the leakage current of the switching transistor now flows in the circuit.

[1] MOS transistors and circuits have been discussed in detail in Philips tech. Rev. **31**, No. 7/8/9, 1970 (the MOST issue).
[2] In static logic the information content of a logic circuit is held for an unlimited time, while in dynamic logic it is lost in a relatively short time. See also L. M. van der Steen, Digital integrated circuits with MOS transistors, Philips tech. Rev. **31**, 277-285, 1970. The differences between static and dynamic shift registers are discussed in this article.
[3] A more detailed treatment of this circuit is given in the article mentioned in note [2].

applied the switching transistor conducts. The output voltage is now determined by the ratio of the channel resistances of the lower and upper transistors. If this ratio has a small value, the output voltage is also small ('0'). But in this state there is a difference from the CMOS circuit: a current mainly determined by the channel resistance of the load transistor now flows through the transistors, so that there is dissipation. While this current can indeed be made small by making the resistance of the channel high, this can only be done at the expense of switching speed. The advantage of a CMOS circuit is that the channel resistance values can be small, and hence the switching speeds high.

Other advantages of CMOS circuits compared with ordinary MOS circuits are the immunity to fluctuations in the supply voltage or in the input voltage. The sensitivity to input-voltage fluctuations is low because the input voltage at which the circuit changes over from one logic state to the other is equal to about half the supply voltage, while the actual transition takes place over a very small range of input voltage. It is also easy to make a CMOS circuit compatible with other logic circuits such as DTL (diode-transistor logic) and TTL (transistor-transistor logic).

All these advantages would make CMOS transistors very suitable for use in integrated circuits, were it not for the fact that with the same tolerances the packing density is smaller than for ordinary MOS transistors. This means that the CMOS technique will give only a low yield when applied in large-scale integration (LSI circuits). Extra process steps are also required for a CMOS circuit, which has an adverse effect on the yield.

It has now been found that marked reduction in surface area can be obtained by using the LOCOS technique [4] developed at Philips Research Laboratories, combined with a special technique for applying *P*-type regions. This process is controlled in such a way that LSI circuits can be made.

In the LOCOS technique a silicon substrate is coated with a layer of silicon nitride, which is used as a mask in a later oxidation of the silicon when a silicon-dioxide layer is formed at the places where the nitride has been removed. Most of this 'LOCOS' oxide sinks into the silicon and gives good separation between regions of different doping. It takes up far less space than the conventional isolation diffusion. The dimensions of a circuit can be made even smaller since contact window and metallization masking do not have to be kept a certain minimum distance from the isolation diffusion, but can extend right up to the LOCOS oxide. In addition, narrow uninterrupted metallized tracks can now be applied, since there are no large steps on the surface [illegible] technique is the low capacitance between the metallization and the silicon at the thick oxide layer; this enables fast switching speeds to be obtained.

We shall now describe the process used for making CMOS circuits by the LOCOS technique — we call the process the 'LOCMOS technique' — with the aid of *fig. 2*. The starting material is a wafer of *N*-type silicon whose surface has the ⟨100⟩ orientation. A surface with this orientation generally has very few surface states, and little charge appears in the oxide grown upon it; this gives a low and reproducible threshold voltage. The wafer is coated with a thin layer of silicon nitride, which is next removed at the places where the isolation oxide is to be formed, and the silicon is then oxidized until the oxide layer is 1.8 μm thick (fig. 2*a*). The next step is to remove the nitride at the places where the *P*-islands for the *N*-channel transistors have to appear; this is done by standard photo-etching techniques. After this *P*-type regions are produced at these places by a special technique (fig. 2*b*). In this technique the silicon is doped with boron in such a way that the boron concentration at the surface has the value necessary for good operation of the MOS transistor, while the maximum of the concentration profile is located about 1.5 μm beneath the surface. This approach prevents parasitic *N*-type channels from forming along the LOCOS oxide. With this method there is no need to use 'channel stoppers' — these are strongly doped regions included to counteract the formation of parasitic channels, and they take up a lot of space. After the *P*-diffusion the rest of the nitride is removed, and a thin oxide layer is formed thermally. A polycrystalline layer of silicon is then applied. Next the polycrystalline layer is doped with phosphorus to make it an *N*-type conductor, and a pattern is etched in it for the electrodes and a part of the interconnection pattern (fig. 2*c*); the doping is necessary to give a low series resistance of the conductors and hence a high switching speed. This treatment also gives a stable threshold voltage, since the phosphorous oxide produced binds sodium atoms and thus protects the silicon dioxide from atoms that are known to introduce mobile charge in the oxide. The next step in the process is to produce *P*-type sources and drains by boron diffusion at previously etched openings in the oxide layer (fig. 2*d*). The gates

[4] 'LOCOS' is an acronym from Local Oxidation of Silicon. A description is given in:
J. A. Appels, H. Kalter and E. Kooi, Some problems of MOS technology, Philips tech. Rev. **31**, 225-236, 1970;
J. A. Appels and M. M. Paffen, Local oxidation of silicon, new technological aspects, Philips Res. Repts. **26**, 157-165, 1971;
E. Kooi, J. G. van Lierop, W. H. C. G. Verkuijlen and R. de Werdt, LOCOS devices, Philips Res. Repts. **26**, 166-180, 1971.

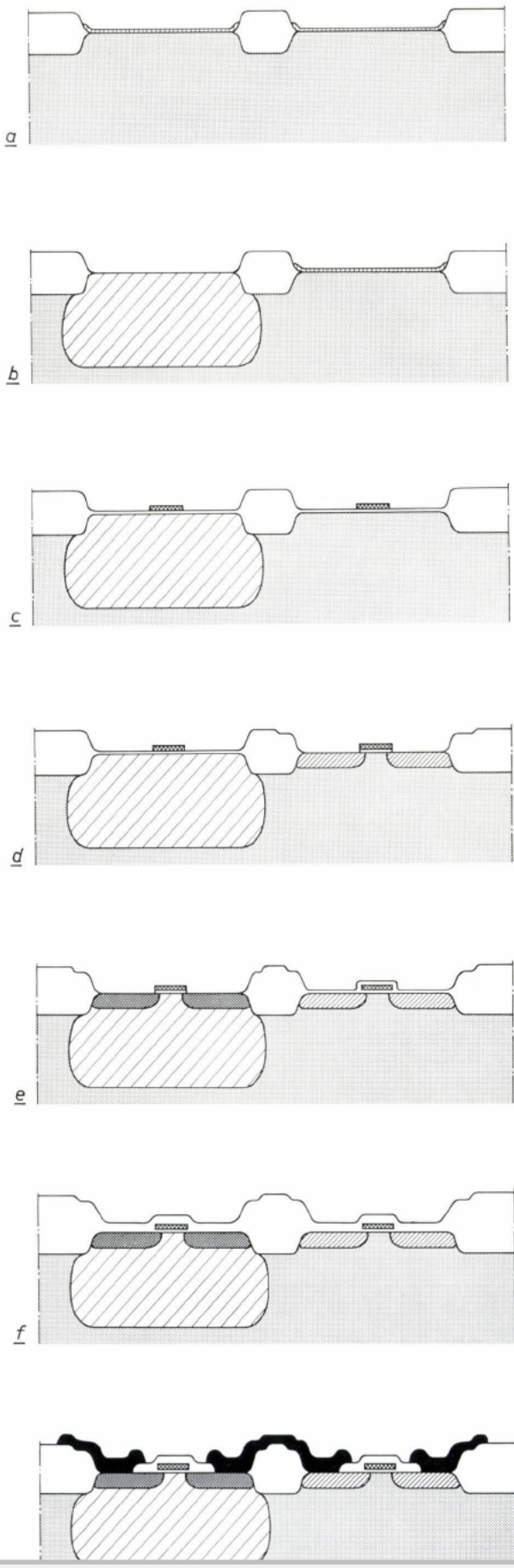

Fig. 2. The steps in the LOCMOS technique. *a*) The application of the LOCOS oxide. The *N*-type silicon is coated with silicon nitride in which openings are etched. The LOCOS oxide forms here as a result of an oxidation treatment. *b*) *P*-type regions for the *N*-channel transistors are made by diffusing boron through windows in the silicon-nitride layer. *c*) After removing the nitride, and forming a thin oxide layer on the silicon surface, a layer of polycrystalline silicon is applied. A pattern for the gates and their interconnections is etched in this layer. *d*) The sources and drains (P^+) for the *P*-channel transistors (*right*) are now formed by boron diffusion in the *N*-type regions, with the gates and the LOCOS oxide serving as a mask. *e*) The sources and drains (N^+) for the *N*-channel transistors (*right*) are now formed in a similar way by phosphorus diffusion in the *P*-type regions. *f*) An SiO_2 layer is next deposited pyrolitically, and openings are etched in the SiO_2 at the places where contact with the electrodes is required. *g*) An aluminium layer is then deposited by evaporation and the interconnection pattern for the circuit is etched in it.

and the LOCOS oxide serve as masks. Since these electrodes are small the stray capacitances are small, which also helps to give a high switching speed. After the boron diffusion a thin oxide is again formed on these regions. The *N*-type sources and drains are next produced in a similar treatment, with a phosphorus diffusion (fig. 2*e*). A silicon-dioxide layer is then deposited pyrolitically, and openings are etched in this to allow contact between the electrodes and the interconnection pattern (fig. 2*f*). Finally, a layer of aluminium is applied by vacuum evaporation and the interconnection pattern is formed in this by etching (fig. 2*g*).

The great saving in space obtained with the LOCMOS technique is demonstrated in *fig. 3*, which shows an inverter circuit made with this technique compared with the same circuit made with the conventional technique.

The LOCMOS process described here has been successfully applied in the manufacture of a number of integrated circuits. These include an inverter circuit, an 8-bit shift register and a static 256-bit random-access memory.

The inverter circuit has a delay time of 3 to 5 ns with a supply voltage of 5 V and an identical inverter circuit as load. Under similar conditions a conventional CMOS circuit has a delay time of at least 12 ns.

The 8-bit shift register has one series input and eight parallel outputs, which are all capable of driving one TTL input. This circuit operates up to a frequency of 10 MHz at a supply voltage of 5 V. The area occupied

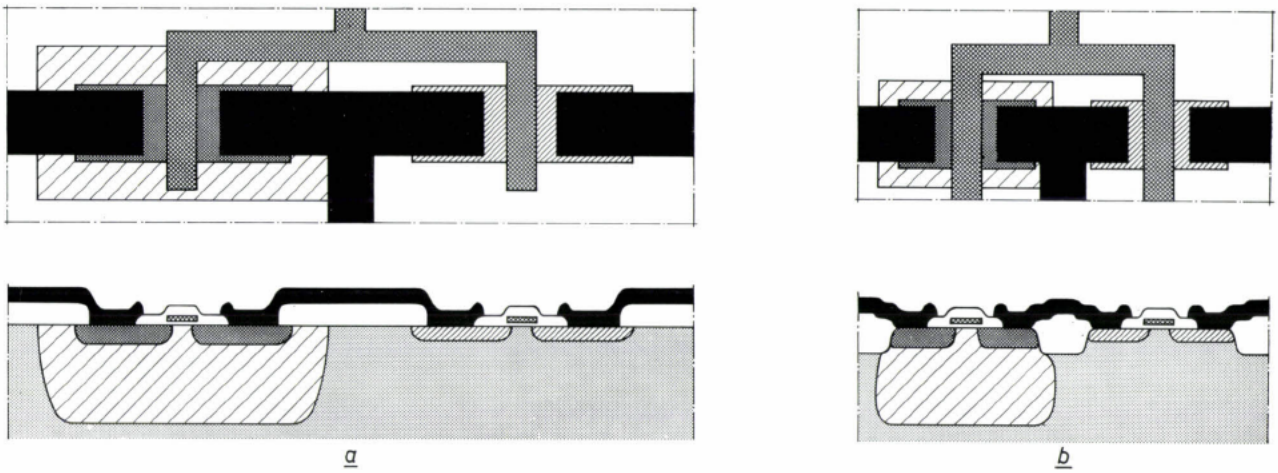

Fig. 3. Comparison of the dimensions of an inverter circuit made by the conventional process (*a*) and by the LOCMOS process (*b*). The structure is explained in fig. 2.

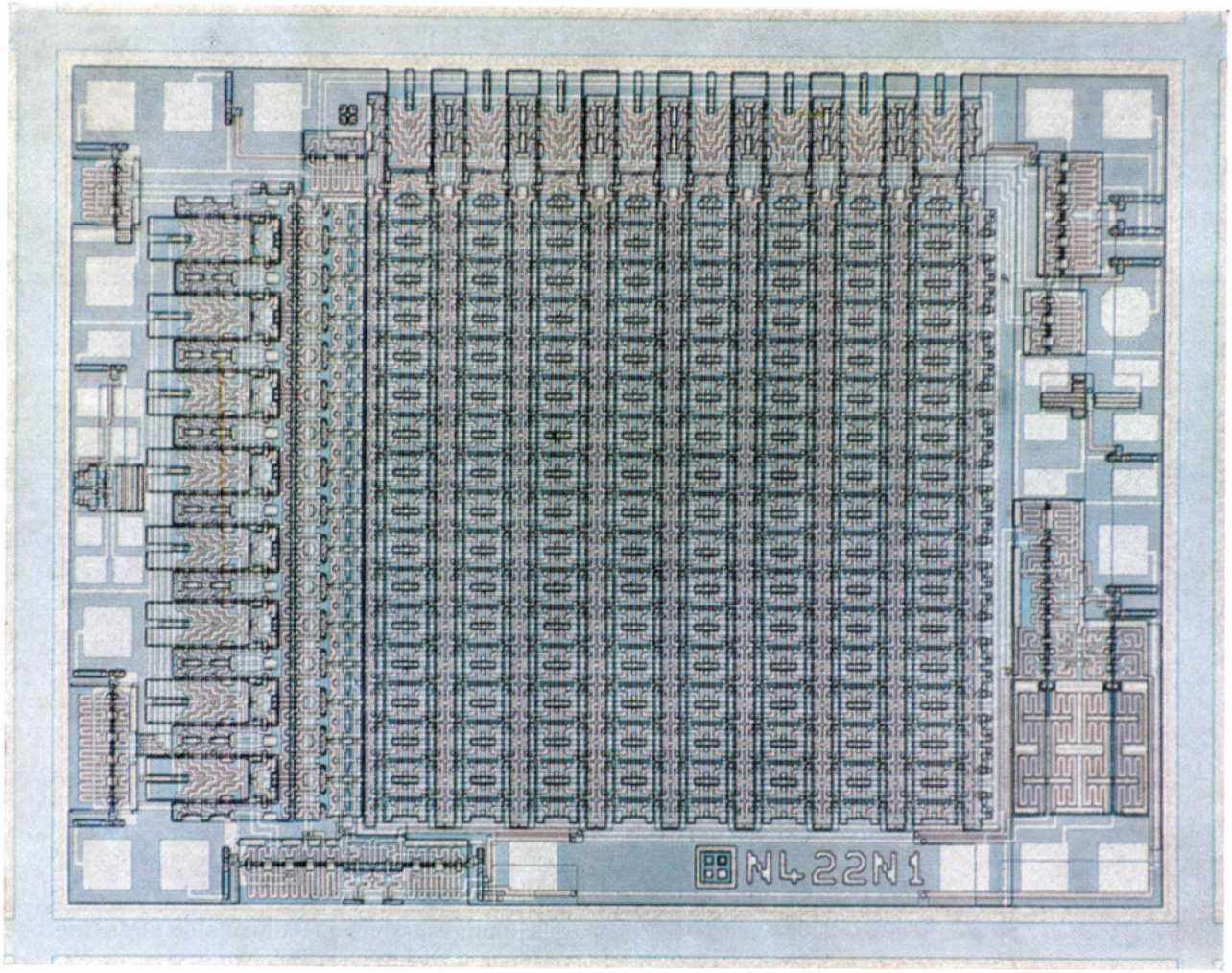

Fig. 4. A 256-bit static random-access memory made by the LOCMOS process. The circuit

circuit would occupy at least 5 mm².

The memory shown in *fig. 4*, occupies an area of 5 mm². The access time is 200 ns at a supply voltage of 5 V and is less than 100 ns if the supply voltage is increased to 10 V. The dissipation is extremely small. A similar circuit made without using the LOCOS technique would occupy more than 10 mm² and with a 5 V supply would have an access time of 600 ns.

These examples, particularly the last one, show that the use of the LOCOS technique has considerably increased the possibility of applying CMOS circuits in LSI.

Summary. Circuits with CMOS transistors have several good features, one of the most important being the low dissipation. It is however particularly difficult to apply them in LSI when conventional methods are used, partly because only low packing densities are obtainable. When the LOCOS technique is used, in which the silicon is locally oxidized by means of silicon-nitride masking, circuits can be made that have high packing densities and high switching speeds. Noteworthy features of this new LOCMOS technique are a special *P*-diffusion to produce a boron-concentration profile with a maximum *below* the silicon surface (to prevent parasitic *N*-channels from forming along the 'LOCOS oxide'), and the use of the LOCOS oxide and the interconnection pattern for the gates as masking for the formation of the sources and drains.

The article gives three examples of circuits made by the LOCMOS technique: an inverter circuit with a delay time of 3 to 5 ns, an 8-bit shift register occupying an area of 2.5 mm² and operating up to a frequency of 10 MHz, and a 256-bit static random-access memory with a surface area of 5 mm² and an access time of 100 to 200 ns.