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United States Patent [19]

Chau et al.

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[54] **TRANSISTOR WITH LOW RESISTANCE TIP AND METHOD OF FABRICATION IN A CMOS PROCESS**

[75] Inventors: **Robert S. Chau**, Beaverton; **Chia-Hong Jan**, Portland; **Chan-Hong Chern**, Portland; **Leopoldo D. Yau**, Portland, all of Oreg.

[73] Assignee: **Intel Corporation**, Santa Clara, Calif.

[*] Notice: This patent issued on a continued prosecution application filed under 37 CFR 1.53(d), and is subject to the twenty year patent term provisions of 35 U.S.C. 154(a)(2).

[21] Appl. No.: **08/581,243**

[22] Filed: **Dec. 29, 1995**

Related U.S. Application Data

[63] Continuation-in-part of application No. 08/363,749, Dec. 23, 1994, Pat. No. 5,710,450.

[51] **Int. Cl.**[7] **H01L 21/8238**

[52] **U.S. Cl.** **438/231**; 438/226; 438/233; 438/232; 438/305; 438/306; 438/586; 438/589; 438/576; 438/558; 438/561; 438/664

[58] **Field of Search** ..... 438/589–663, 438/664, 191, 226–223, 229, 230, 231, 232, 259, 270, 330, 301, 303, 305, 306, 586, 576, 558, 565, 581, 583, FOR 168, FOR 180, FOR 197, FOR 216, FOR 217, FOR 218, FOR 251, FOR 250, FOR 219; 148/DIG. 147, DIG. 19, DIG. 59; 257/288, 900

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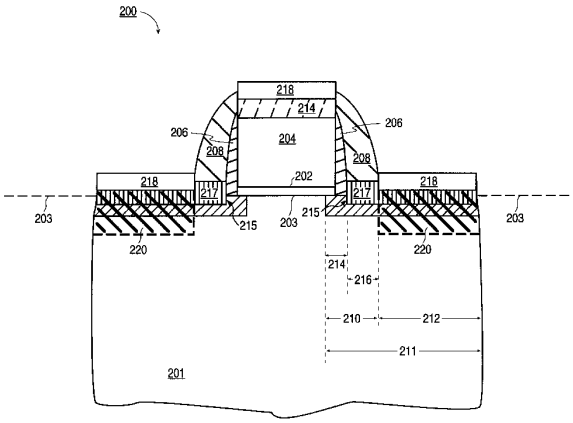
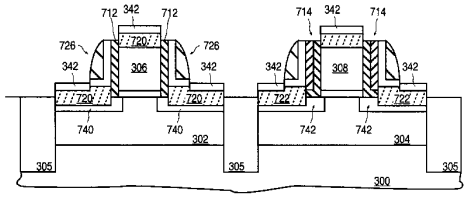
Primary Examiner—Long Pham
Attorney, Agent, or Firm—Blakely, Sokoloff, Taylor & Zafman LLP

[57] **ABSTRACT**

A novel transistor with a low resistance ultra shallow tip region and its method of fabrication in a complementary metal oxide semiconductor (CMOS) process. According to the preferred method of the present invention, a first gate dielectric and a first gate electrode are formed on a first portion of a semiconductor substrate having a first conductivity type, and a second gate dielectric and a said gate electrode are formed on a second portion of semiconductor substrate having a second conductivity type. A silicon nitride layer is formed over the first portion of the semiconductor substrate including the first gate electrode and over the second portion of the semiconductor substrate including the second gate electrode. The silicon nitride layer is removed from the second portion of the silicon substrate and from the top of the second gate electrode to thereby form a first pair of silicon nitride spacers adjacent to opposite sides of the second gate electrode. A pair of recesses are then formed in the second portion of the semiconductor substrate in alignment with the first pair of sidewall spacers. A selectively deposited semiconductor material is then formed in the recesses.

52 Claims, 13 Drawing Sheets





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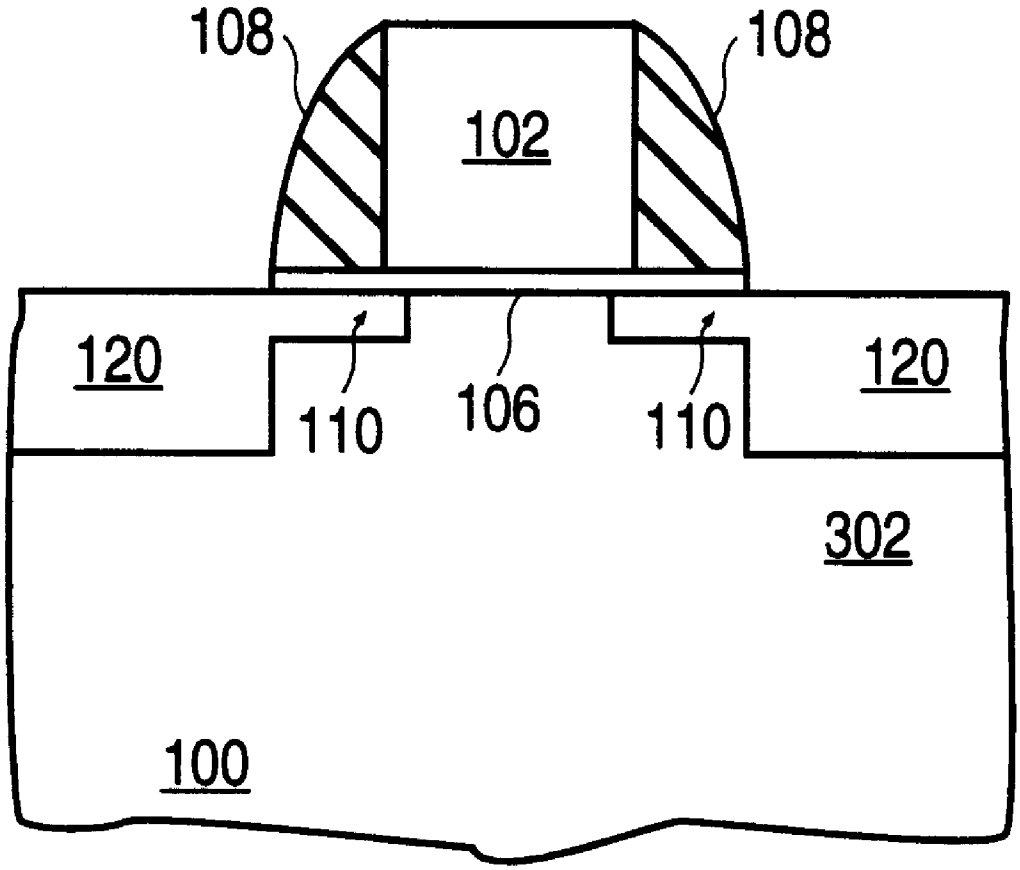

FIG. 1 (PRIOR ART)

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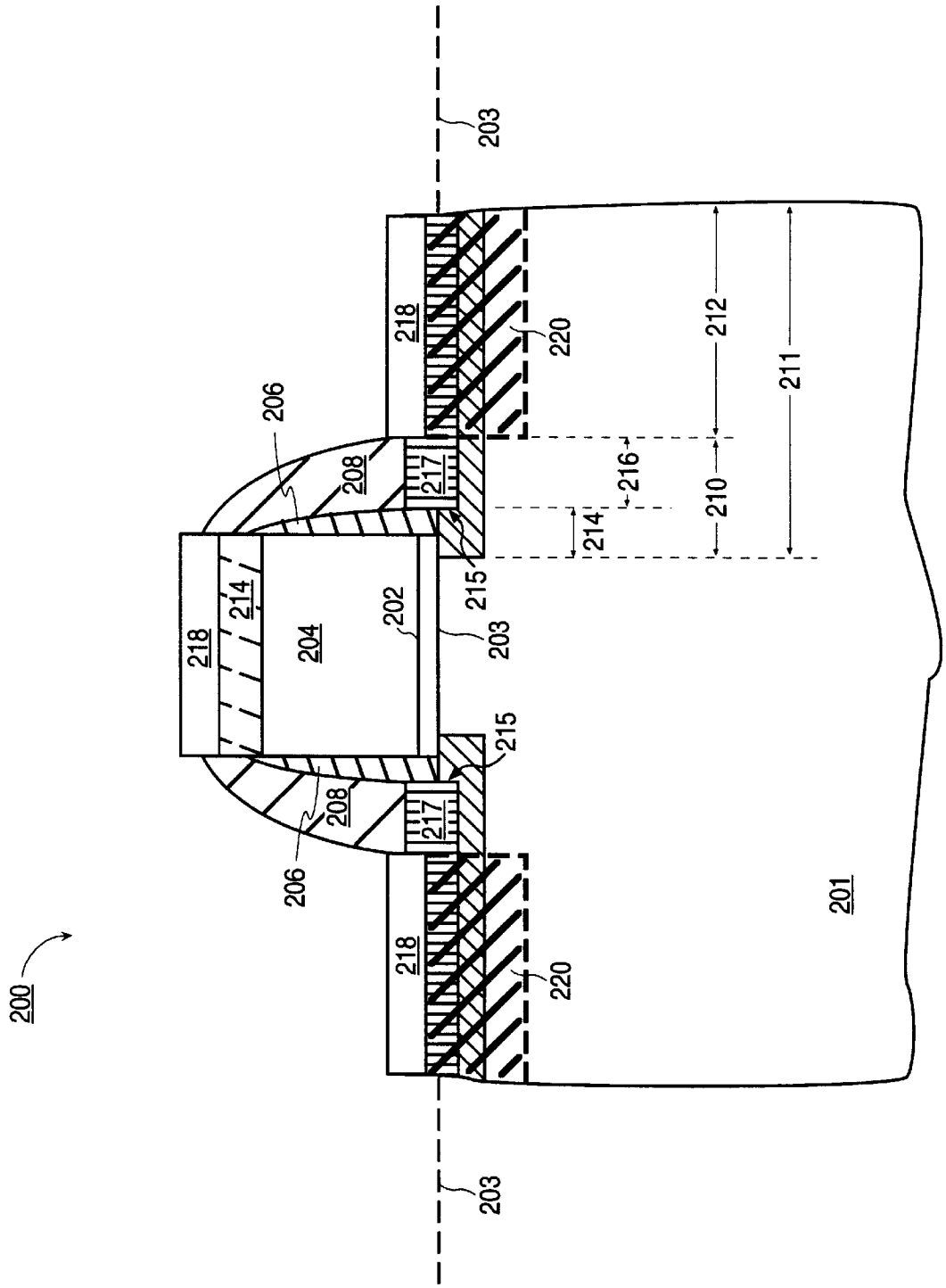

FIG. 2

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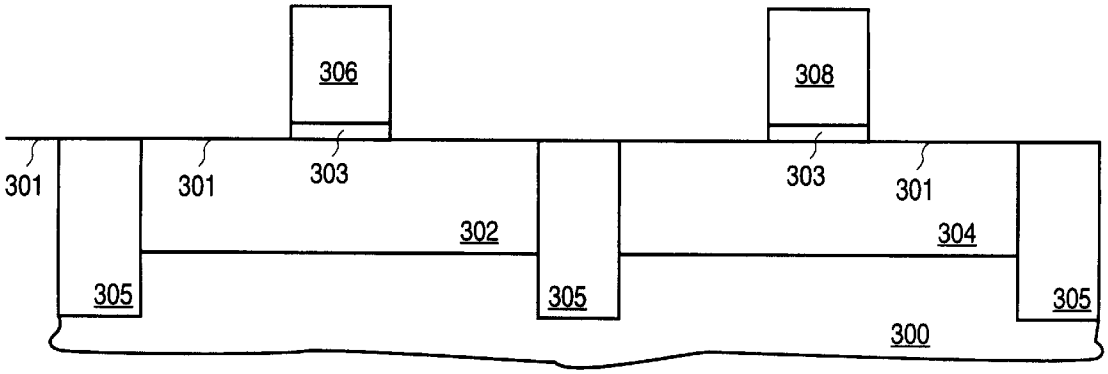

FIG. 3A

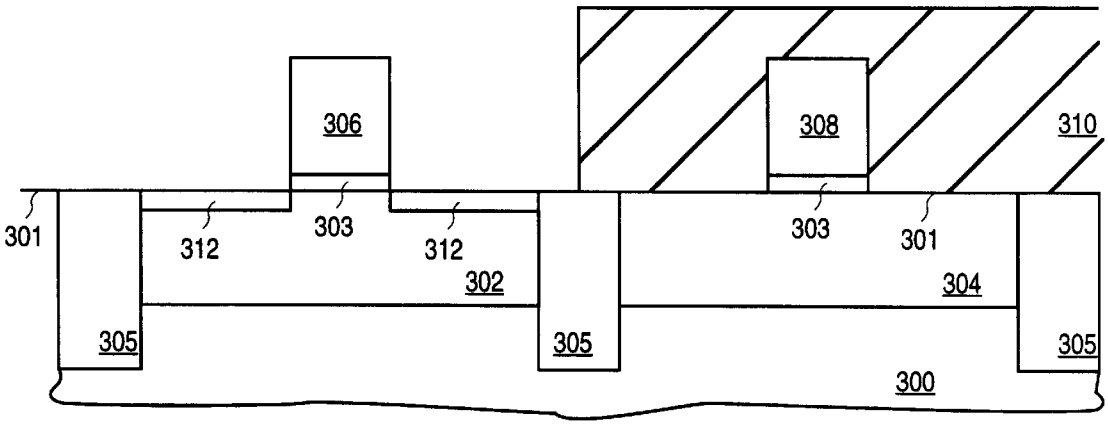

FIG. 3B

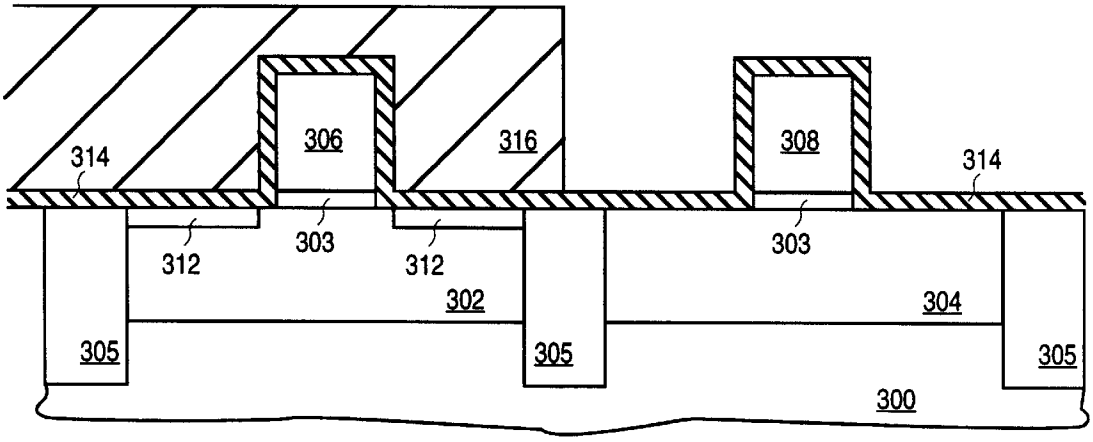

FIG. 3C

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