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United States Patent [19]

[11] **Patent Number:** **5,976,939**

Thompson et al.

[45] **Date of Patent:** **Nov. 2, 1999**

[54] **LOW DAMAGE DOPING TECHNIQUE FOR SELF-ALIGNED SOURCE AND DRAIN REGIONS**

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61-279129	12/1986	Japan	437/164
63-169047	7/1988	Japan	437/978
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[73] Assignee: **Intel Corporation**, Santa Clara, Calif.

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[21] Appl. No.: **08/498,028**

[22] Filed: **Jul. 3, 1995**

[57] **ABSTRACT**

[51] **Int. Cl.**⁶ **H01L 21/336**

[52] **U.S. Cl.** **438/305; 438/559; 438/563; 438/231**

[58] **Field of Search** 437/44, 405 W, 437/415 W, 164, 160, 161, 978; 148/DIG. 43; 438/305, 306, 307, 299, 301, 559, 563, 558, 562, 231, 230

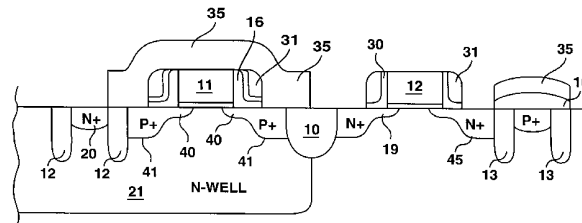
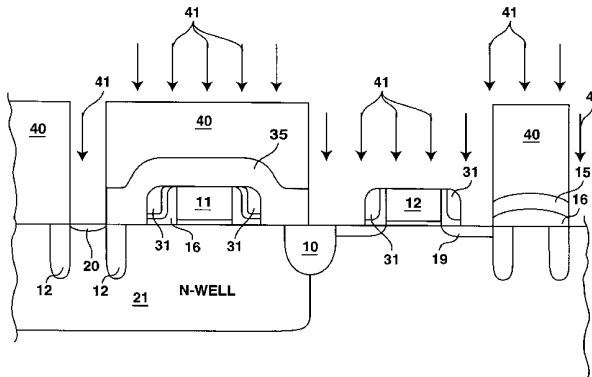
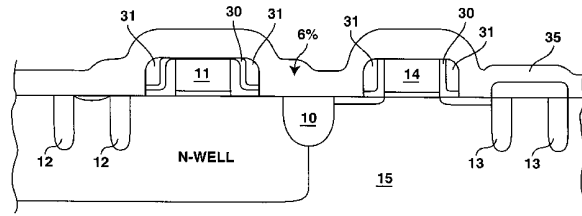
A process for fabricating a source and drain region which includes a more lightly doped source and drain tip region immediately adjacent to the gate and a more heavily doped main portion of the source and drain region spaced apart from the gate. A first layer of glass (2% BSG) is used to provide the source of doping for the tip region and a second layer of glass (6% BSG) is used to provide the dopant for the more heavily doped major portion of source and drain regions. Spacers are formed between the glass layers to define the tip region from the main portion of the source and drain regions.

[56] **References Cited**

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4 Claims, 4 Drawing Sheets



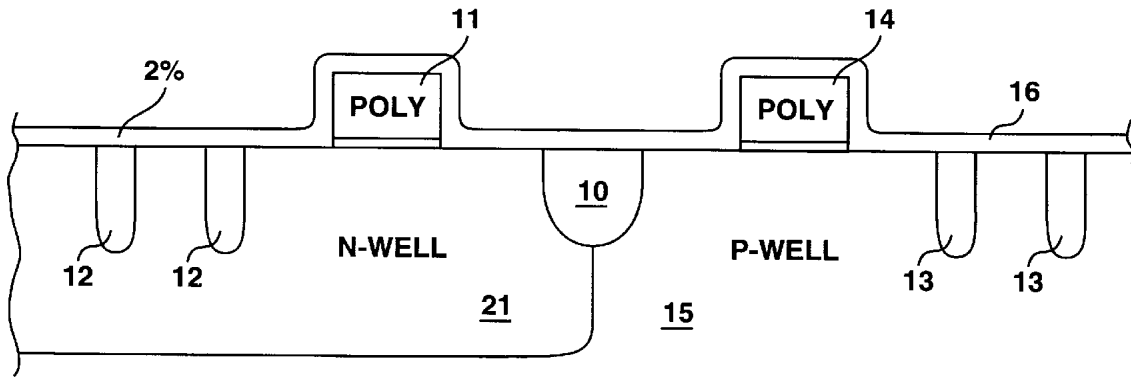


FIG. 1

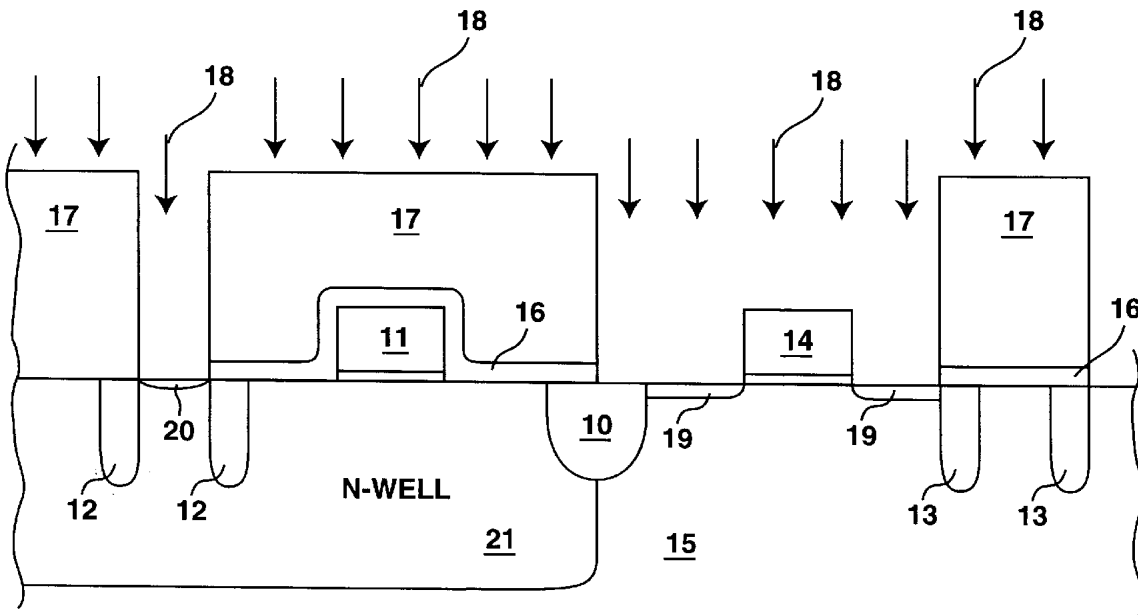


FIG. 2

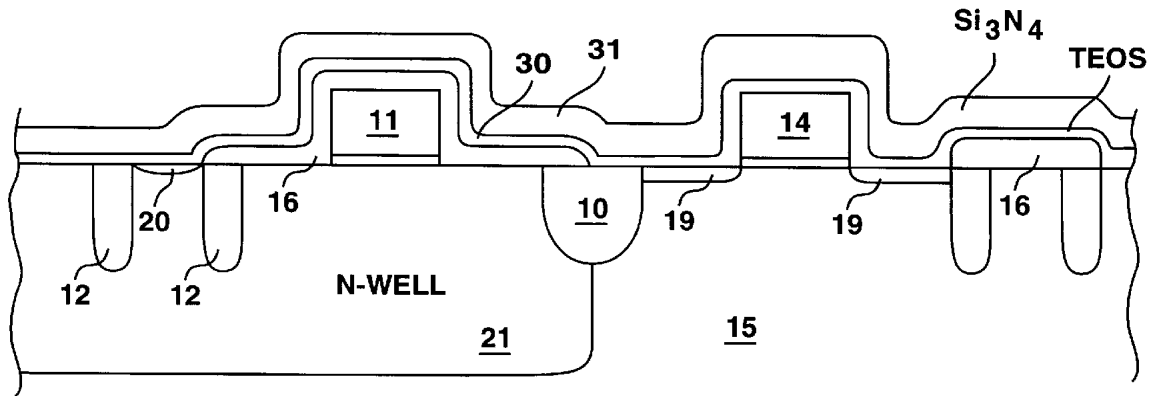


FIG. 3

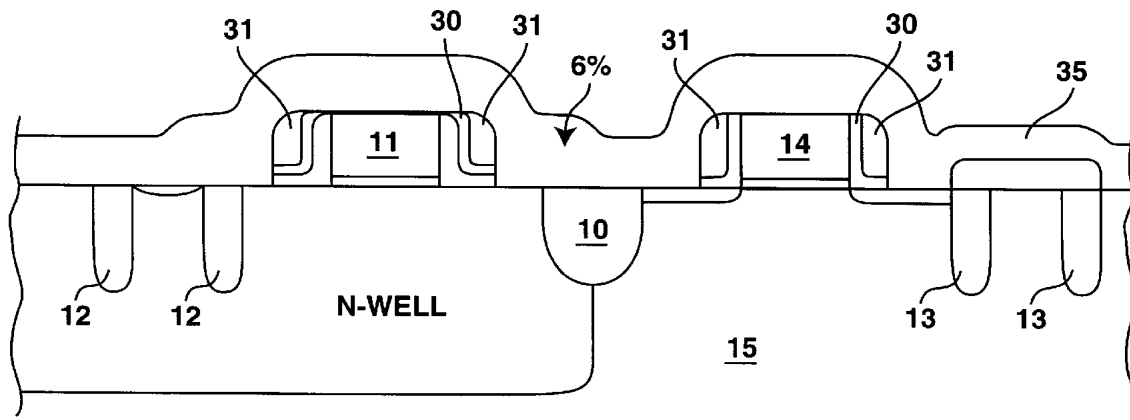


FIG. 4

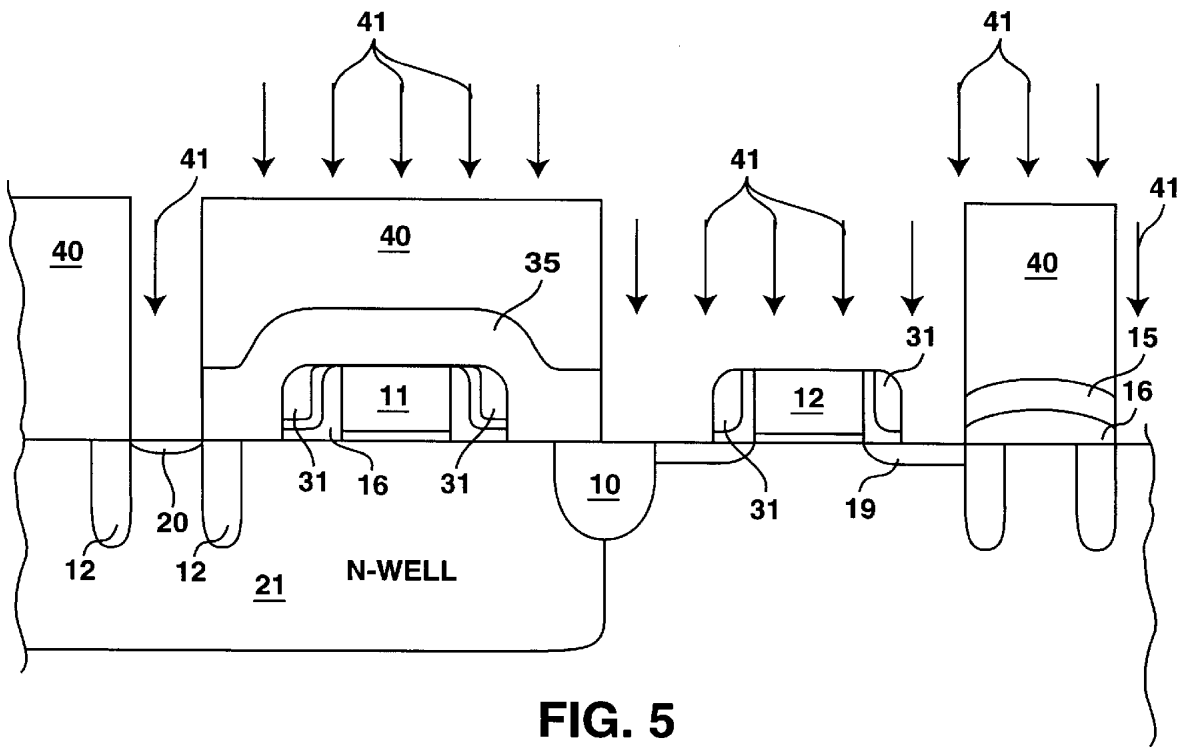


FIG. 5

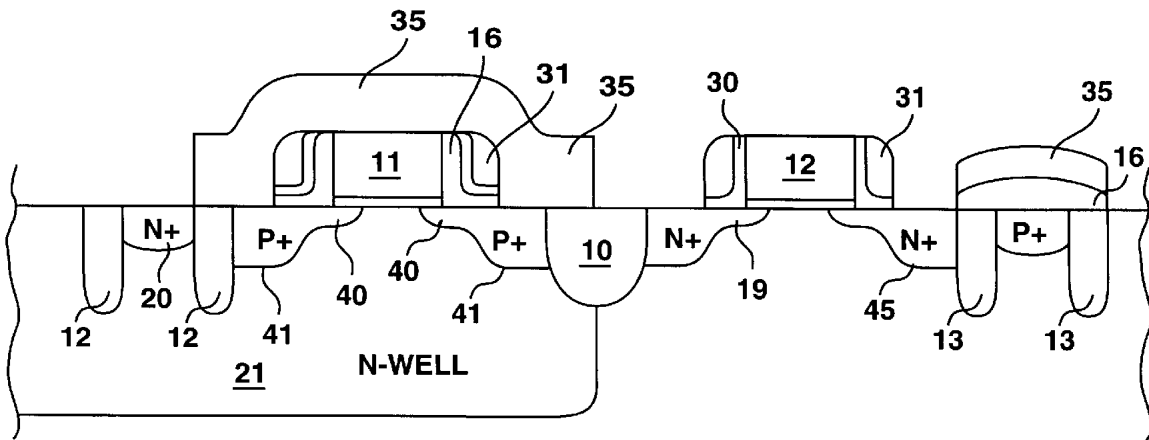


FIG. 6

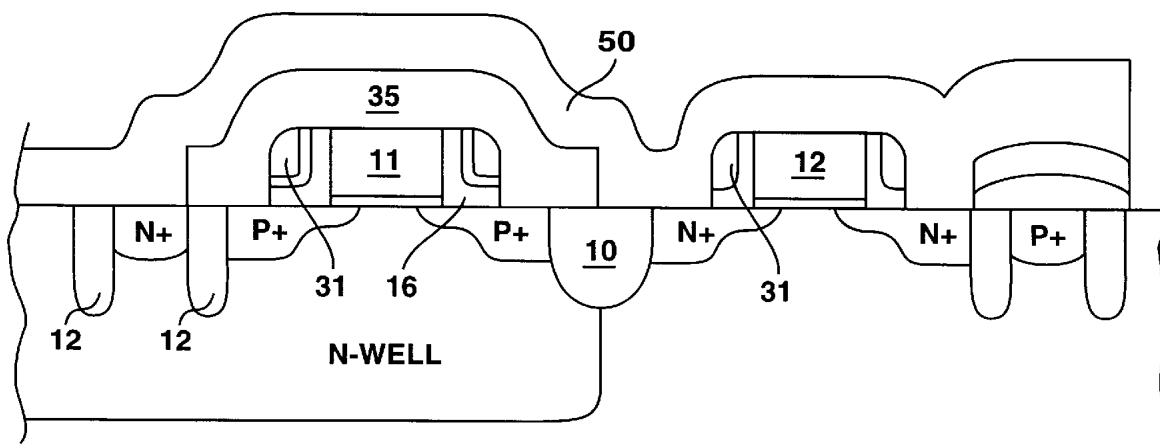


FIG. 7

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