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(12) **United States Patent**
Segawa et al.

(10) **Patent No.: US 7,126,174 B2**
(45) **Date of Patent: Oct. 24, 2006**

(54) **SEMICONDUCTOR DEVICE AND METHOD OF MANUFACTURING THE SAME**

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(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **10/995,283**

(22) Filed: **Nov. 24, 2004**

(65) **Prior Publication Data**

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Related U.S. Application Data

(62) Division of application No. 10/454,682, filed on Jun. 5, 2003, now Pat. No. 6,967,409, which is a division of application No. 09/902,157, filed on Jul. 11, 2001, now Pat. No. 6,709,950, which is a division of application No. 08/685,726, filed on Jul. 24, 1996, now Pat. No. 6,281,562.

(30) **Foreign Application Priority Data**

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Dec. 19, 1995 (JP) 7-330112

(51) **Int. Cl.**
H01L 29/76 (2006.01)

(52) **U.S. Cl.** **257/288**; 257/336; 257/E23.001

(58) **Field of Classification Search** 257/384, 257/336, 288, 333, 386, 389, 401, 396
See application file for complete search history.

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(74) *Attorney, Agent, or Firm*—McDermott Will & Emery LLP

(57) **ABSTRACT**

An isolation which is higher in a stepwise manner than an active area of a silicon substrate is formed. On the active area, an FET including a gate oxide film, a gate electrode, a gate protection film, sidewalls and the like is formed. An insulating film is deposited on the entire top surface of the substrate, and a resist film for exposing an area stretching over the active area, a part of the isolation and the gate protection film is formed on the insulating film. There is no need to provide an alignment margin for avoiding interference with the isolation and the like to a region where a connection hole is formed. Since the isolation is higher in a stepwise manner than the active area, the isolation is prevented from being removed by over-etch in the formation of a connection hole to come in contact with a portion where an impurity concentration is low in the active area. In this manner, the integration of a semiconductor device can be improved and an area occupied by the semiconductor device can be decreased without causing degradation of junction voltage resistance and increase of a junction leakage current in the semiconductor device.

20 Claims, 21 Drawing Sheets

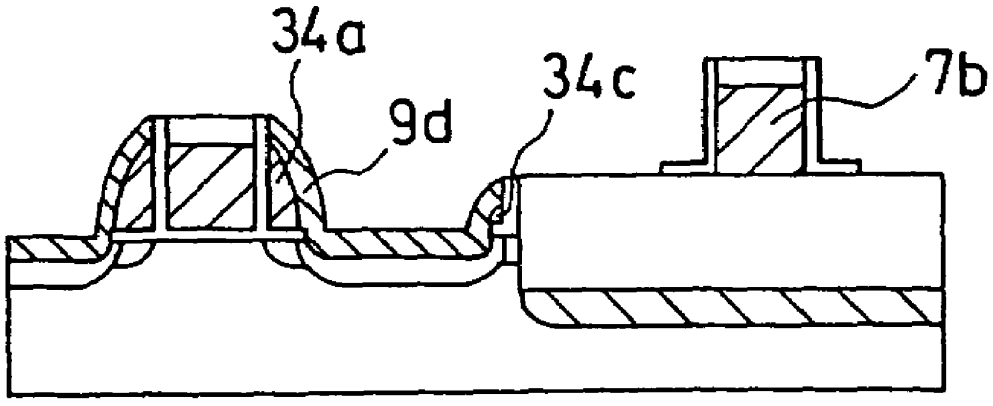

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FIG. 1(a)

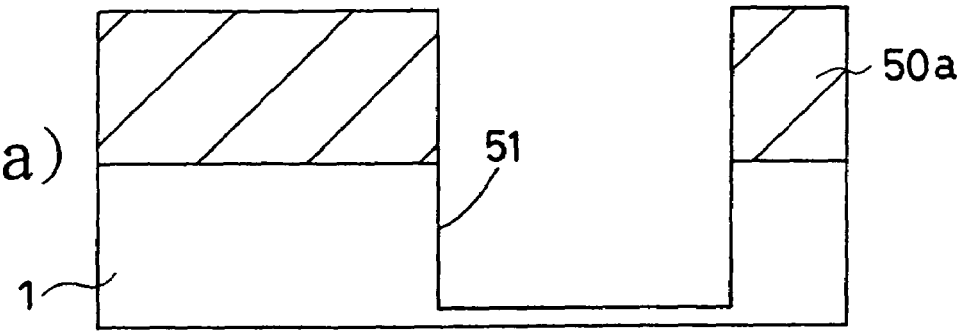


FIG. 1(b)

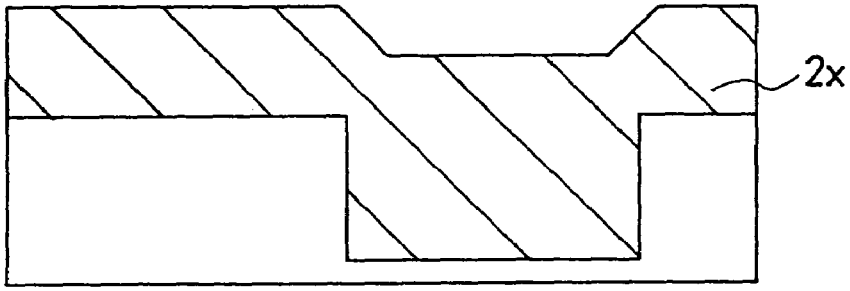


FIG. 1(c)

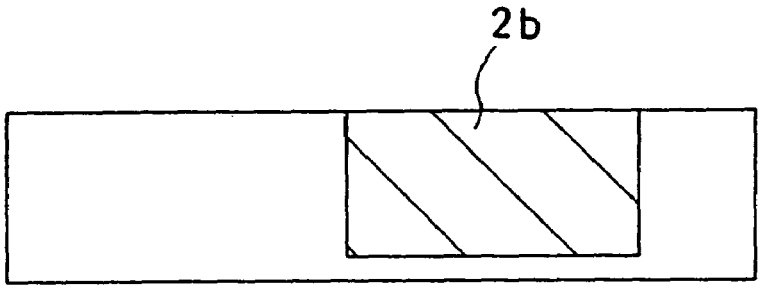


FIG. 1(d)

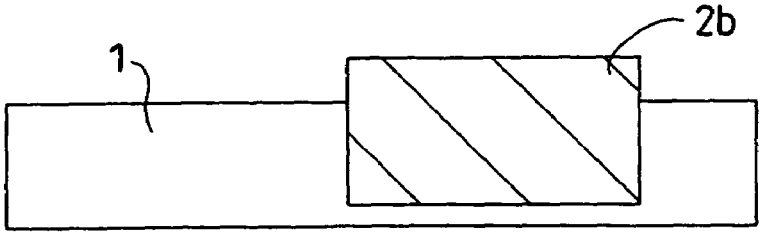


FIG. 2(a)

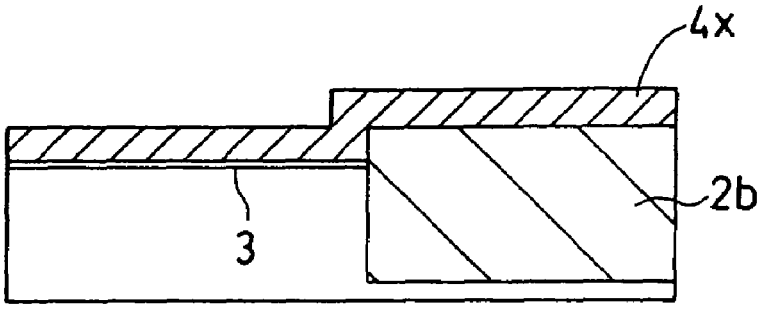
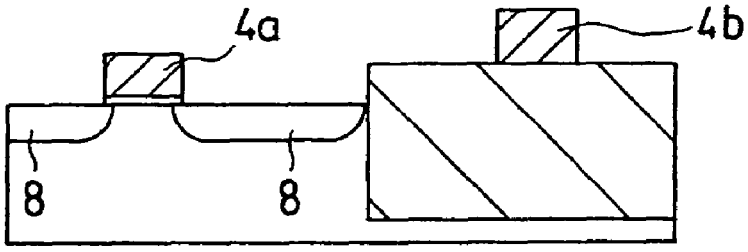


FIG. 2(b)



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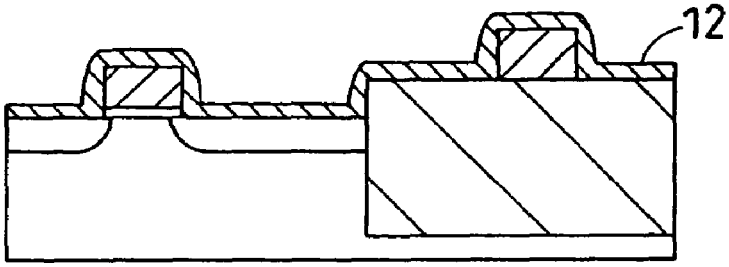

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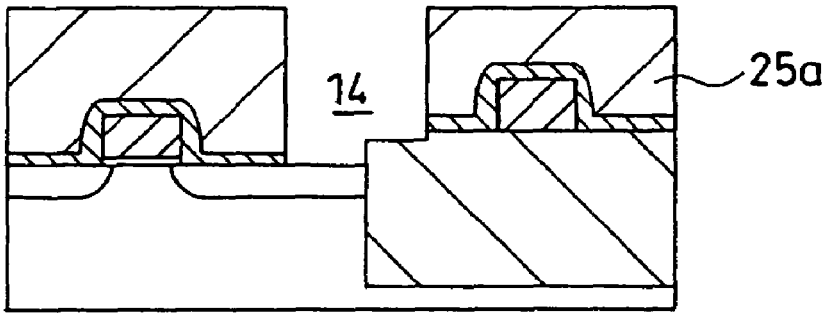


FIG. 2(e)

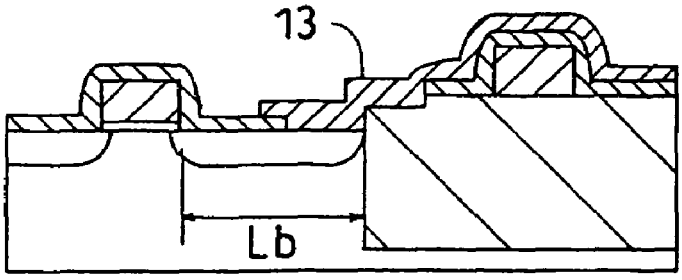


FIG. 3(a)

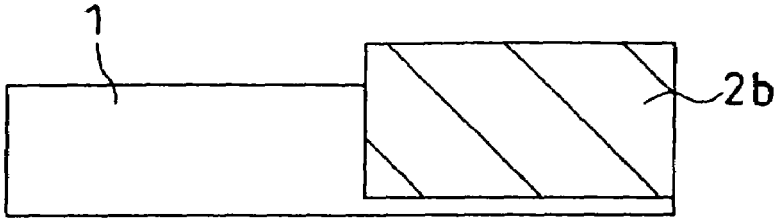


FIG. 3(b)

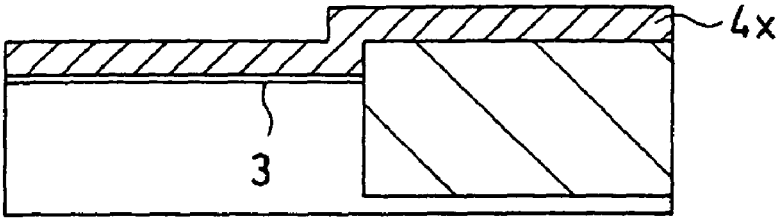


FIG. 3(c)

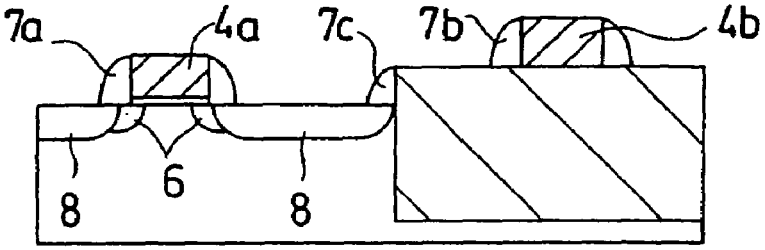


FIG. 3(d)

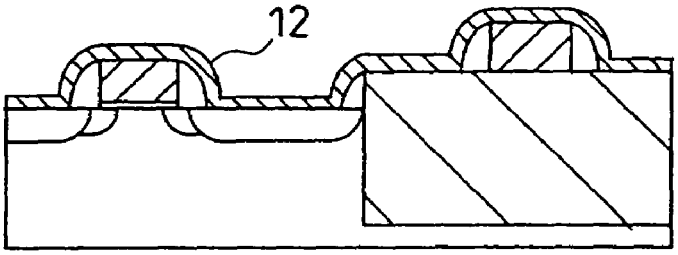


FIG. 3(e)

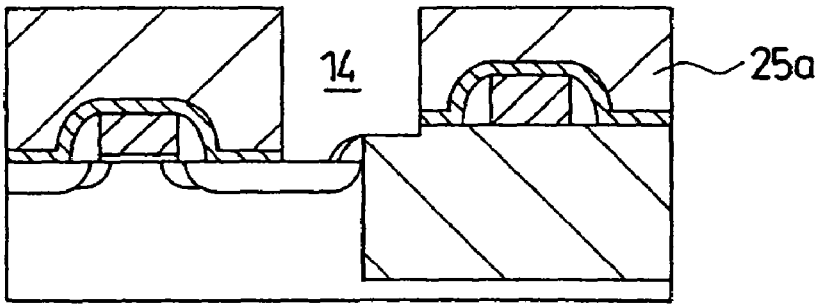
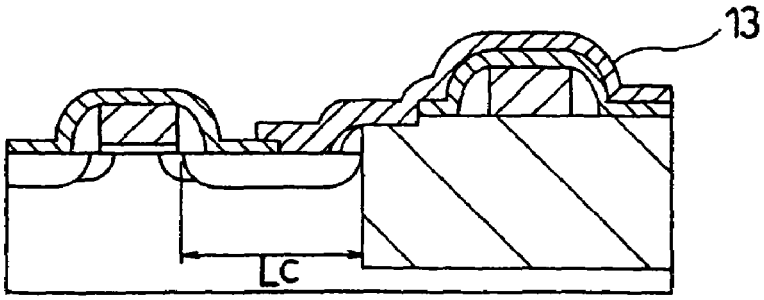


FIG. 3(f)



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