9th Annual
IEEE/SEMI®
Advanced Semiconductor Manufacturing Conference and Workshop

World Class Manufacturing

98

Bind //Abel

SEPTEMBER 23 – 25, 1998
THE FAIRMONT COPLEY PLAZA
BOSTON, MASSACHUSETTS USA

CONFERENCE SESSIONS

- YIELD MODELING & ANALYSIS
- OVERALL EQUIPMENT EFFICIENCY
- YIELD ENHANCEMENT STRATEGIES & TECHNIQUES
- HARNESSING & DEVELOPING WORKFORCE POTENTIAL
- INTERNATIONAL PERSPECTIVE
- CONTAMINATION FREE MANUFACTURING
- ADVANCED METROLOGY
- COST REDUCTION
- ADVANCED PROCESSING - PHOTO & ETCH
- ADVANCED PROCESSING - A NEW ERA OF INTERCONNECT TECHNOLOGY
- FACTORY AUTOMATION -WIP MANAGEMENT
- ADVANCED PROCESSING - ISOLATION AND DIELECTRIC ISSUES AT 0.18 MICRON
- FACTORY MODELING - SIMULATION

SPONSORED BY:

SEMI — Semiconductor Equipment and Materials International (SEMI)

IEEE *Networking the World™* — Institute of Electrical and Electronics Engineers, Inc. (IEEE)

EDS — IEEE Electron Devices Society

CPMT — IEEE Components, Packaging and Manufacturing Technology Society

ISSN: 1078-8743

IEEE CATALOG NUMBER 98CH36168

ASME proceedings (IEEE/SEMi Advanced Semiconductor
" manufacturing Conference and Workshop

Advanced Semiconductor
Manufacturing Conference and Workshop

World Class Manufacturing

IEEE/SEMI®

1998
IEEE/SEMI
Advanced
Semiconductor
Manufacturing
Conference
And Workshop

Theme – **Semiconductor Manufacturing: Meeting the Challenges of the Global Marketplace**

ASMC 98 PROCEEDINGS

The IEEE/SEMI Advanced Semiconductor Manufacturing Conference and Workshop is an annual forum that provides a venue for the presentation of methodologies, approaches and techniques required to achieve world class semiconductor manufacturing. A key role this conference plays is in promoting interaction among semiconductor professionals at all levels. The goal and objective of the conference are to assist in making the participating companies more knowledgeable of semiconductor production methods, encourage open communication between participants, and develop the strategic relationship between users and suppliers needed to achieve manufacturing excellence and improve global competitiveness.

September 23 – 25, 1998
Boston, Massachusetts, USA

1998 PROCEEDINGS
IEEE/SEMI ADVANCED SEMICONDUCTOR MANUFACTURING CONFERENCE AND WORKSHOP (ASMC)

PERMISSION TO REPRINT OR COPY:

PRINTED AND BOUND IN THE UNITED STATES OF AMERICA

Additional copies of these Proceedings may be purchased from:

SEMI
805 East Middlefield Road
Mountain View, CA 94043 USA
Phone: (650) 940-6971
http://www.semi.org

IEEE Service Center
445 Hoes Lane
Piscataway, NJ 08855-0060 USA
Phone: (732) 981-0060
In the US 1-800-678-IEEE
http://www.ieee.org

Refer to the IEEE Catalog Number, printed below:

IEEE Catalog Number;	98CH36168	
ISBN Number:	0-7803-4380-8	Softbound Edition
	0-7803-4381-6	Casebound Edition
	0-7803-4382-4	Microfiche Edition
ISSN:	1078-8743	

Layout, composition and compilation by
Semiconductor Equipment and Materials International (SEMI)

TABLE OF CONTENTS

Yield Modeling & Analysis

Overall Equipment Efficiency

Yield Enhancement Strategies & Techniques

† **Not available at time of printing**

Harnessing & Developing Workforce Potential

Poster Session

International Session

Contamination Free Manufacturing

Advanced Metrology

Cost Reduction

† **Not available at time of printing**

Advanced Processing/Photo & Etch

Advanced Processing/A New Era of Interconnect Technology

Factory Automation – WIP Management

Advanced Processing - Isolation and Dielectric Issue at 0.18μm

Factory Modeling/Simulation

Development of a Production Worthy Copper CMP Process

Kapila Wijekoon[a], Sourabh Mishra[a], Stan Tsai[a], Kumar Puntambekar[a], Madhavi Chandrachood[a], Fritz Redeker[a], Robert Tolles[a], Bingxi Sun[b], Liang Chen[b], Tony Pan[c], Ping Li[c], Savitha Nanjangud[a], Gregory Amico[a]
Applied Materials, 3050 Bowers Avenue, Santa Clara, CA 95054
and
Joe Hawkins, Theodore Myers, Rod Kistler, Vlasta Brusic, Shumin Wang, Isaac Cherian, Lisa Knowles, Colin Schmidt and Chris Baker
Cabot Corporation, MMD Division, 500 Commons Drive, Aurora, IL 60504

[a] CMP Division; [b] Metal Deposition Products Division; [c] Equipment Set Solution Division

Abstract

A chemical mechanical polishing (CMP) process for copper damascene has been developed and characterized on a second generation, multiple platen polishing tool. Several formulations of experimental copper slurries containing alumina abrasive particles were evaluated for their selectivity of copper to Ta, TaN and PETEOS film. The extent of copper dishing and oxide erosion of these slurries is investigated with various process parameters such as slurry flow rate, platen speed and wafer pressure. The amount of dishing and erosion is found to be largely dependent on process parameters as well as the slurry composition. It is shown that the extent of oxide erosion and copper dishing can be significantly reduced by using a two slurry copper polish process (one slurry to polish copper and another to polish barrier layers) in conjunction with an optical end-point detection system.

Introduction

The trend in semiconductor industry continues to move towards faster miniaturized integrated circuits for ever increasing device packing densities.[1-3] As device architectures are scaled down to submicrometer dimensions, RC delay of metal interconnects plays an important role on the device performance. In order to increase the switching speed, RC delay of metal interconnects must be reduced. Aluminum, interconnects widely used in present VLSI devices, raises reliability concerns with the shrinking device dimensions which rules out the possibility of using Al in future submicron devices. Because of the superior conductivity (resistivity of copper is about 1.7 μΩ-cm compared to 3.0 μΩ-cm for aluminum), higher resistance to electromigration (electromigration limit for copper is 10^7 A/cm^2 and that for aluminum is 10^6 A/cm^2) and reduced susceptibility to joule heating, copper is being considered as a potential candidate for the replacement of aluminum in future metal interconnects.[2] However, patterning copper via traditional dry etch techniques is problematic mainly due to lack of volatile copper compound formation at low temperatures. This difficulty can be overcome by following an alternative approach using metal inlay structures such as single and dual damascene in conjunction with chemical mechanical polishing (CMP).[4-6]

In a Damascene approach, the dielectric layer is patterned and etched using standard procedures. Barrier and copper films are then deposited on the patterned surface. Next, the copper surface topography is removed by CMP. Another challenge in copper technology is developing a good deposition technique for copper. A good barrier layer material is necessary to prevent diffusion of copper into silicon. The barrier layer must be thin to minimize the resistance of contact holes, vias and metal lines. In addition, the barrier layer must be able to be planarized with a CMP process. Materials such as Ta, TaN, and TiN are the most commonly studied barrier layers for copper and are planarized using CMP process. Although many techniques such as sputtering (PVD), chemical vapor deposition (CVD) and electro-chemical deposition (ECD) are currently being considered as film deposition options, further refinements of deposition parameters are necessary in order to obtain more uniform copper films.

Although CMP offers an attractive solution for implementing copper technology in integrated circuits, many challenges exist in developing a manufacturable copper CMP process. The key process issues which must be taken into account in developing a production worthy copper CMP process include control of within-wafer uniformity, wafer-to-wafer uniformity, copper dishing, oxide erosion, corrosion and post CMP

0-7803-4380-8/98/$10.00 1998 IEEE

cleaning.[7-11] In view of space limitations, this paper focuses only on the characterization of two key CMP process issues namely copper dishing and oxide erosion. In general, copper dishing is defined as the difference in height between the lowest point of a single copper line/bond pad (usually at the center of the structure) and the surrounding oxide film. Oxide erosion is defined as the difference in the oxide layer thickness within an array of line structures before and after CMP processing (Therefore, the total copper loss of a given feature during CMP is the sum of erosion and dishing).

Both copper dishing and oxide erosion can generate a significant amount of surface non-planarity which cause various process integration problems. They reduce the dielectric spacing and amount of copper in the interconnects, thus leading to increased interconnect resistance and deterioration of device performance. Hence, it is vital to develop a CMP process with minimum copper dishing and oxide erosion. The extent of copper dishing and oxide erosion is found to be heavily dependent on CMP consumables (slurry, pad), process parameters (wafer pressure, platen speed) as well as device features (line width, spacing). In this paper, we describe the reduction of dishing with the use of multiple polishing steps and multiple polishing slurries in conjunction with an optical end-point system.

Experimental Procedures

Copper CMP was carried out on Applied Materials Mirra® polisher using Titan™ polishing heads. The experiments were performed by using polyurethane pads and several experimental copper CMP slurries which use alumina abrasive particles. All slurries were provided by Cabot Corporation. Hydrogen peroxide oxidizer was added to each slurry and mixed well prior to polishing. Slurry was continuously agitated during the experiments. Wafer pressure was varied between 1.0 psi and 6.0 psi, platen speed was varied between 33 rpm to 143 rpm and slurry flow rate was varied between 75 ml/min and 220 ml/min. In every case the end-point was detected with the ISRM™ system. The Laser based ISRM module is embedded in the polishing platen. When the laser beam is incident on the film surface during polishing, the ISRM system probes the film surface, collects and processes data, and displays a real time signal. This process continues until a pre-set end point is reached. Data are collected only when the laser beam is incident on the film surface, therefore, the ISRM signal does not depend on process parameters such as platen velocity, down force, slurry flow rate or pad hardness.

The wafers used in this study contained test structures with different line widths and spacings. Copper deposition was carried out with either PVD, CVD and/or ECD techniques. The barrier layers were either Ta or TaN. In the case of a single slurry process the same slurry was used to polish copper and barrier layers. In the case of two-step copper polish process, one slurry was used to polish copper and the other slurry was used to polish the remaining barrier layers. Copper polishing was carried out on the first platen and the barrier layer was polished on the second platen. The buff and rinse step was accomplished on the third platen. In both cases, multiple polishing steps were used. During some of the single slurry processes, one or more polishing steps were carried out on the first platen and the rest of the steps were carried out on the second platen. Again one buff and rinse step was done on the third platen. All the erosion and dishing measurements were performed with a Tencor HRP200 high resolution profilometer.

Results and Discussion

The main contribution to copper dishing and oxide erosion comes from over-polishing, which is often necessary to assure complete removal of copper and barrier residues across the entire wafer. The uniformity variations of the copper thickness of the as deposited wafers can make the CMP step problematic. In the ideal case, one would like to fully planarize the copper layer before reaching the barrier layers. Depending on the slurry chemistry, the same slurry or a different slurry can be used to polish residual copper and the barrier layers thus creating a structure with metal inlaid in dielectric. Large differences in chemical reactivity of copper and tantalum result in dissimilar polishing rates of the two layers. In the case of single slurry processing, the barrier removal rate is significantly lower than that of copper. Hence, during barrier polishing, the exposed copper feature dishes due to continued chemical and mechanical action. Table I shows the copper removal rates and selectivities of copper to barrier layers for the slurries used in this study.

	Slurry A	Slurry B	Slurry C
Cu Removal Rate (Å/min)	7500	5900	169
Cu:Ta selectivity	47:1	30:1	~ 1:1
Cu:TaN selectivity	19:1	11:1	~ 1:2
Cu:PETEOS selectivity	137:1	207:1	~ 3:1

Table I. Copper removal rate and selectivity to barrier films for various copper CMP slurries at a platen speed of 43 rpm and a wafer pressure of 4.0 psi.

As shown in Table I, either slurry A or B can be used in the single slurry process since they have a high copper removal rate. Slurry C is well suited for clearing barrier layers since the copper removal rate in this slurry is comparable to barrier removal rates. An ideal single step slurry would polish Cu and the barrier film at similar removal rates (low selectivity to barrier) and would also have a very low removal rate for the field oxide (high selectivity to SiO_2). Additionally, such an ideal slurry would remove residual Cu and barrier without dishing Cu interconnects and eroding the dielectric layer.

The majority of the single slurry process discussed in the present work was carried out with slurry A. The dependence of the copper dishing and oxide erosion on the process parameters such as slurry flow rate, platen speed and wafer pressure was investigated with this slurry. In every case, end-point was detected with the ISRM system. All wafers were 10% over-polished after the end-point was detected. Figure 1 shows a end-point trace of a blanket copper film containing Ta barrier film.

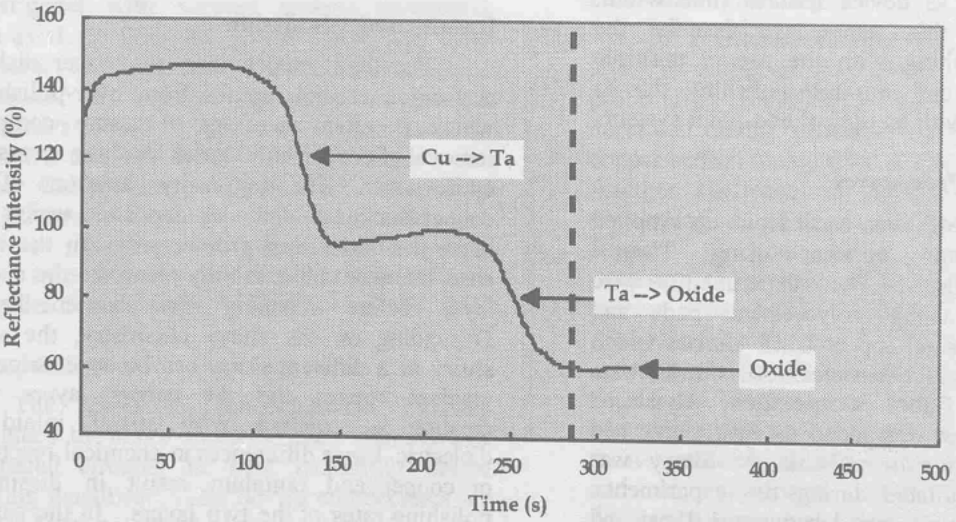

Figure 1. ISRM trace of a blanket copper film containing Ta barrier. End-point is shown by the dotted line.

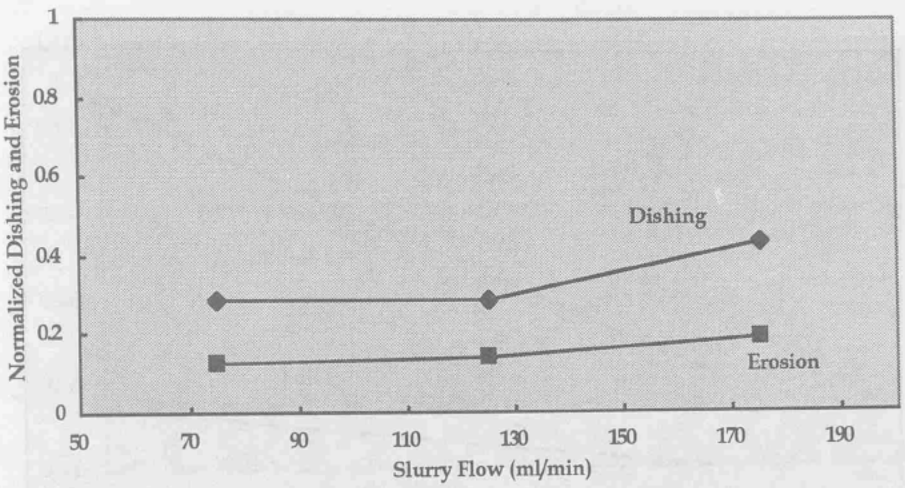

Figure 2. Dependence of copper dishing and oxide erosion on slurry (slurry A) flow rate. Platen speed and wafer pressure were held constant. Dishing was measured on a 50mm thick line (pitch 150mm) while erosion was measured at a 0.5mm thick line (pitch 1.0mm).

As shown in Figure 1, different interfaces of the film stack can be accurately detected with the end-point system. The amount of over-polish in a single slurry process is defined as the percent polish time after the end-point is reached. Figures 2-4 show the extent of copper dishing observed in a 50µm copper line and extent of oxide erosion observed in a 0.5µm feature as process parameters such as slurry flow rate, wafer pressure and platen speed are varied.

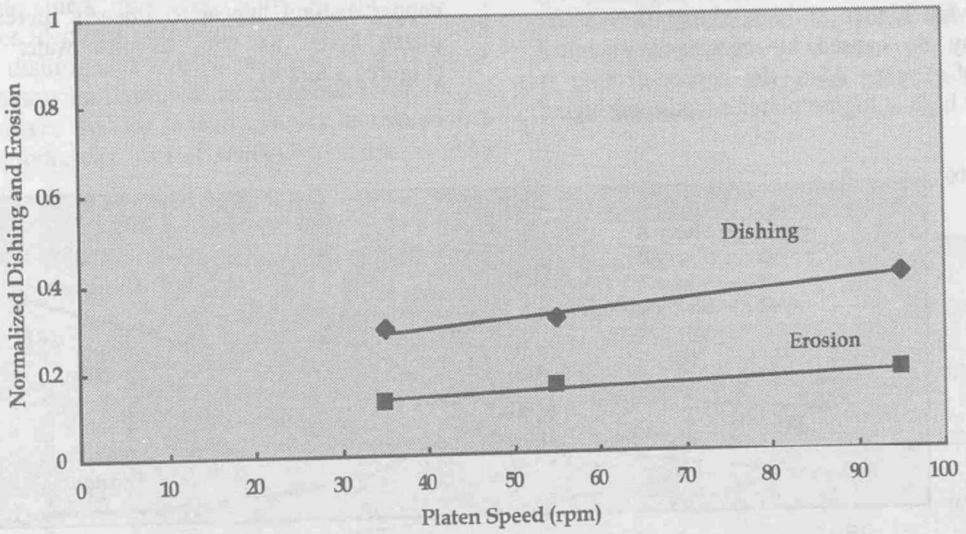

Figure 3. Dependence of copper dishing and oxide erosion on platen speed (slurry A). Slurry flow rate and wafer pressure were kept constant. Dishing was measured on a 50mm feature (pitch 150mm) while erosion was measured at 0.5mm line (pitch 1.0mm).

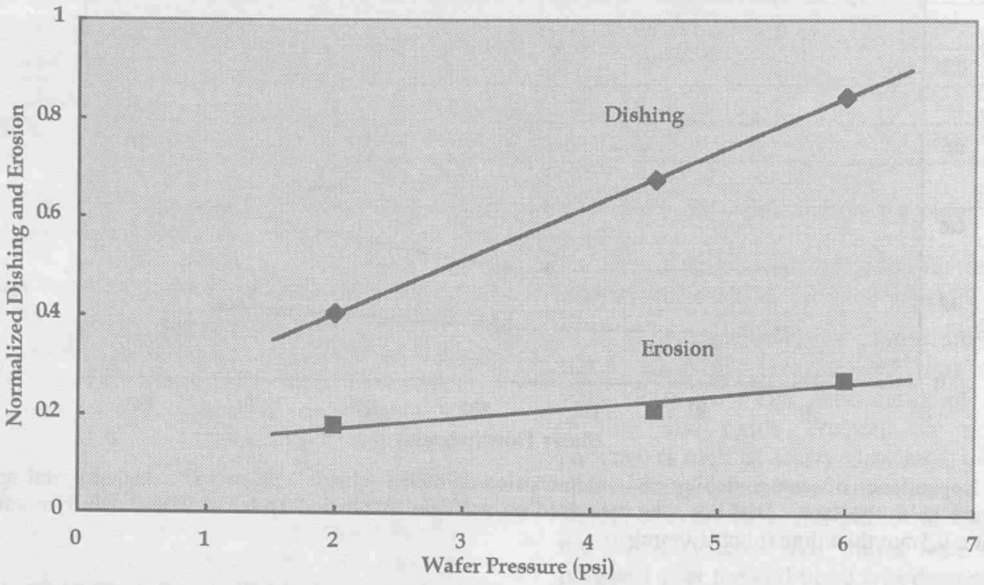

Figure 4. Dependence of copper dishing and oxide erosion on wafer pressure (slurry A). Platen speed and slurry flow rate were held constant. Dishing was measured on 50mm feature (pitch 150mm) while erosion was measured at 0.5mm line (pitch 1.0mm).

Data in Figure 2 show that copper dishing is somewhat higher at high slurry flow rates. This may be caused by continued chemical etching of copper. Also, the copper dishing is relatively high at higher platen speeds and higher wafer pressures. Both the oxide erosion and copper dishing appear to linearly increase with platen speed as well as the wafer pressure (Figures 3 and 4).

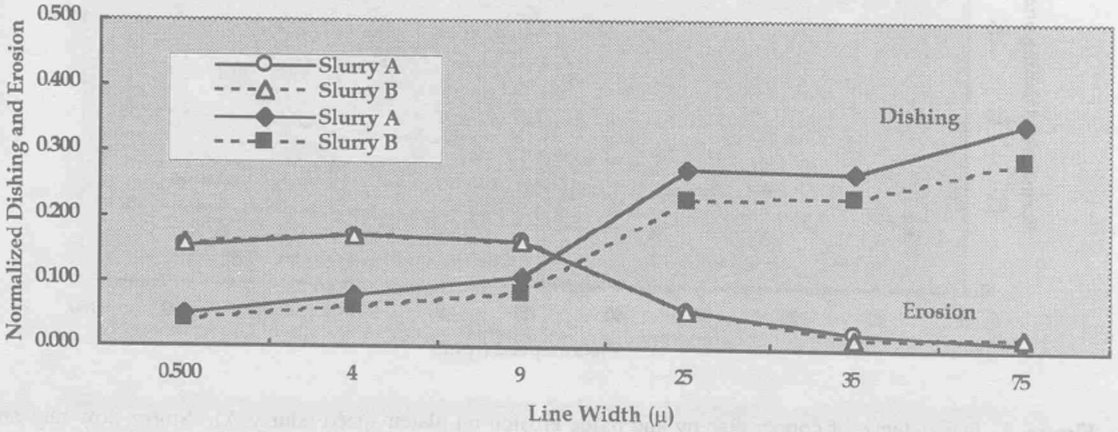

Figure 5. Comparison of copper dishing and oxide erosion of single slurry process under identical experimental conditions (slurry A and slurry B). Copper dishing on slurry B is relatively smaller compared to that of slurry A. Both slurries have similar oxide erosion performance.

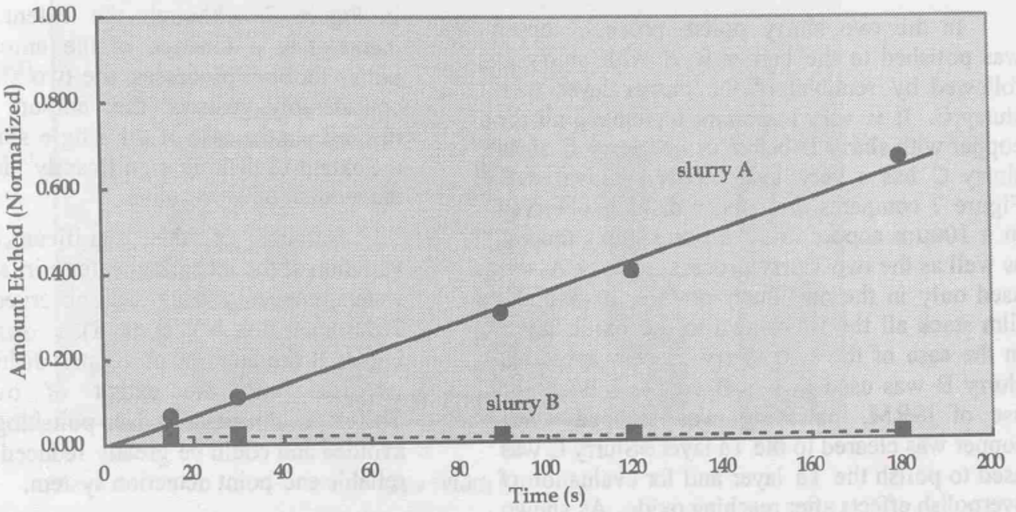

Figure 6. Static copper etch rate at room temperature (slurry A and Slurry B).

In order to improve the dishing in a single slurry process, another slurry formulation (slurry B) was evaluated. Figure 5 compares the extent of dishing and erosion observed with single slurry processes (slurry A and slurry B) under identical polishing conditions. It is seen that dishing and erosion performance of slurry B is somewhat improved as compared to slurry A. Improved dishing in slurry B may be related to a low static etch rate of slurry B (Figure 6). As shown in Figure 6, static copper etch rate of slurry A is considerably higher than that of slurry B. Therefore, slurry B reduces static etching during the barrier removal and over-polish, leading to lower copper dishing levels. Because of the improved dishing performance of slurry B (compared to slurry A), slurry B was selected as the first step slurry for the two-slurry process evaluations.

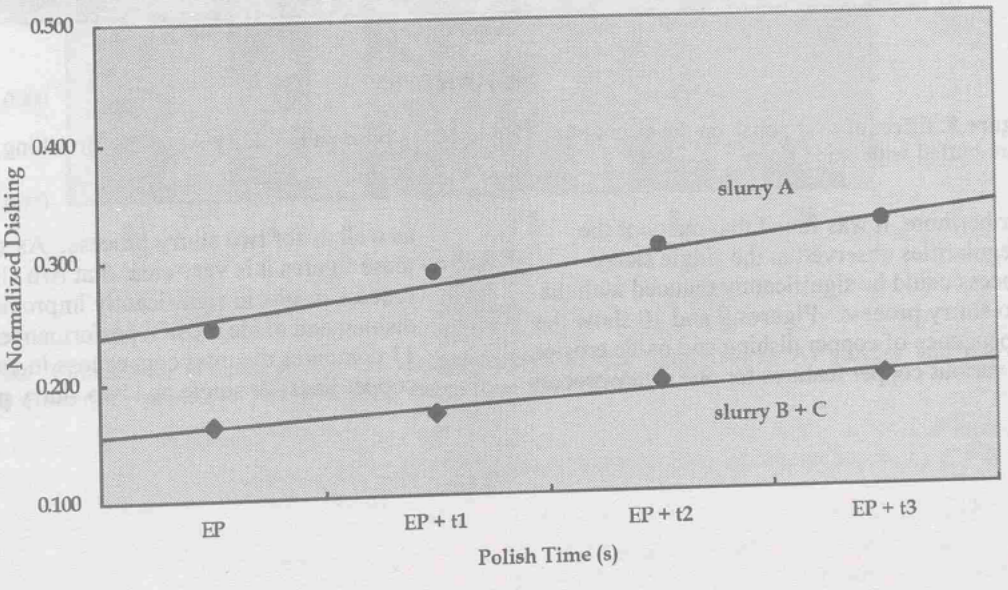

Figure 7. Comparison of copper dishing of 100 mm bond pad for one slurry (slurry A) process and two slurry (slurry B and slurry C) processes. In the case of one slurry process, EP is the time to reach end-point and t1, t2, t3 are the over polish times. In the case of the two slurry process, t1, t2, and t3 are the over polish times with slurry C.

In the two slurry polish process, copper was polished to the barrier layer with slurry B followed by removal of the barrier layer with slurry C. It is very important to remove all the copper with slurry B before using slurry C since slurry C has a very low copper removal rate. Figure 7 compares the copper dishing observed in a 100µm copper line with one slurry process as well as the two slurry process. Slurry A was used only in the one slurry process to clear the film stack all the way down to the oxide layer. In the case of the two slurry process approach, slurry B was used to polish copper. With the use of ISRM, polishing was stopped when copper was cleared to the Ta layer. Slurry C was used to polish the Ta layer and for evaluation of overpolish effects after reaching oxide. As shown in Figure 7, although the extent of dishing increases as a function of the amount of over polish for both processes, the two slurry process considerably reduces the amount of copper dishing. In the case of the single slurry process, the extent of dishing significantly increases with the amount of over-polish.

Because of the significant uniformity variation of the incoming wafers, in some copper wafers, copper dishing was observed even at a 20% under-polish (Figure 8). As shown in Figure 8 the amount of copper dishing linearly increases with the extent of over polish. Therefore, unnecessary over-polishing should be avoided and could be greatly reduced by using a reliable end-point detection system.

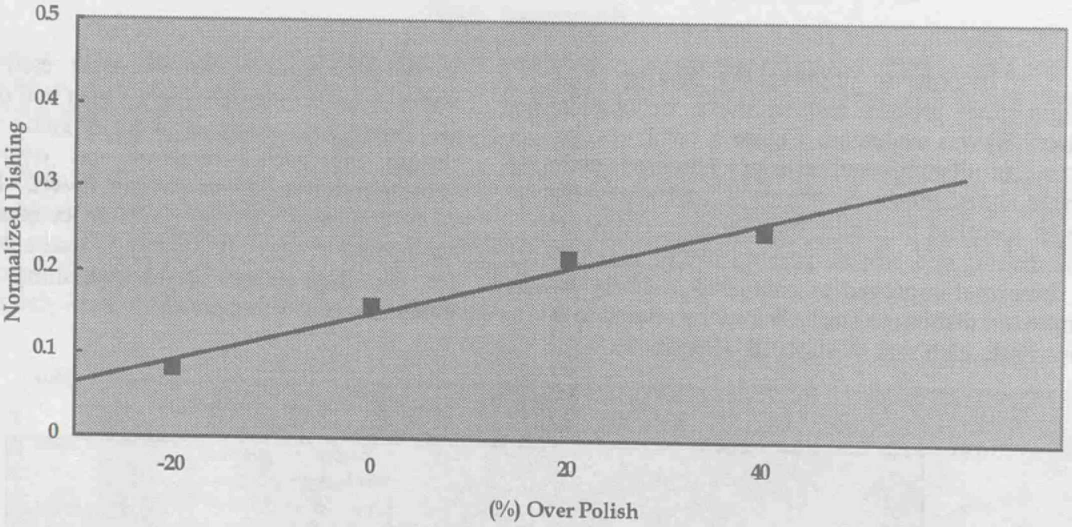

Figure 8. Effect of over polish on the extent of dishing in 100 m bond pads (slurry A). After polishing the wafers were buffed with oxide slurry.

Furthermore, it was found that many of the irregularities observed in the single slurry process could be significantly reduced with the two slurry process. Figures 9 and 10 show the dependence of copper dishing and oxide erosion on various copper features for one slurry process as well as for two slurry process. As shown in these figures it is very clear that two slurry process results in significantly improved copper dishing and oxide erosion performances. Figure 11 compares the total copper loss in various copper lines for single and two slurry processes.

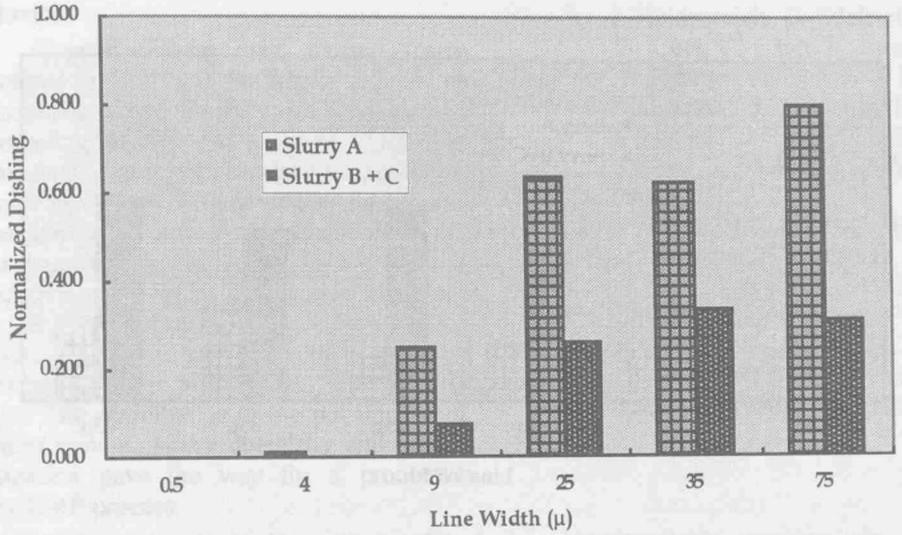

Figure 9. Comparison of copper dishing of various copper features for one slurry (slurry A) process and two slurry (slurry B + slurry C) processes.

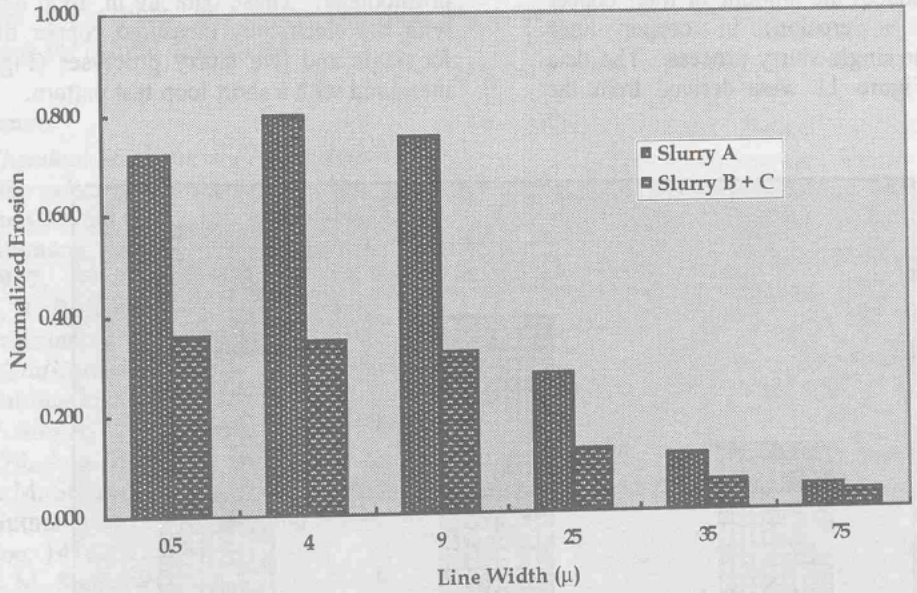

Figure 10. Comparison of oxide erosion on various features for one slurry (slurry A) process and two slurry (slurry B + slurry C) processes. Pattern density varies from 55% to 80%.

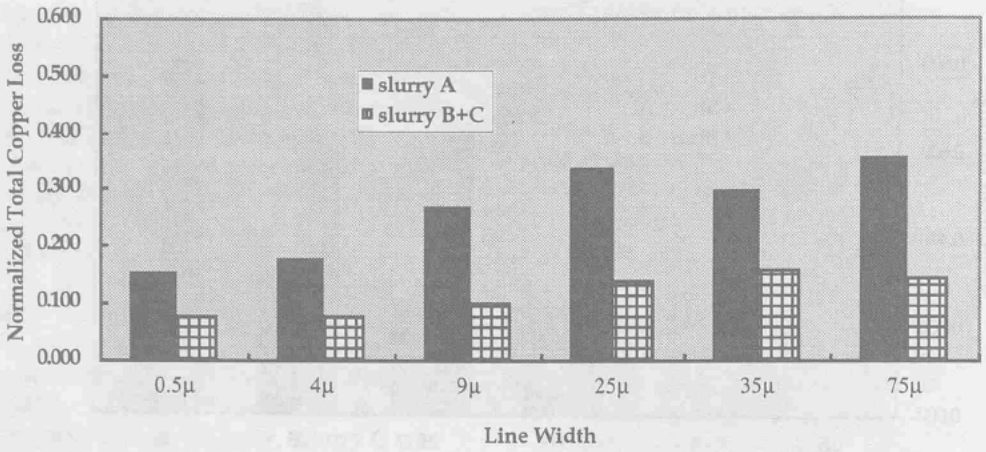

Figure 11. Comparison of total copper loss (dishing + erosion) for one slurry (slurry A) and two slurry (slurry B + slurry C) processes in a variety of copper line sizes.

As seen in Figure 11, the two slurry process significantly reduces the amount of total copper loss (dishing + erosion) in copper lines compared to the single slurry process. The data presented in Figure 11 were derived from the measurements made with a high resolution profilometer. These data are in good agreement with the electrically measured copper thickness for single and two slurry processes (Figure 12) measured with a short loop test pattern.

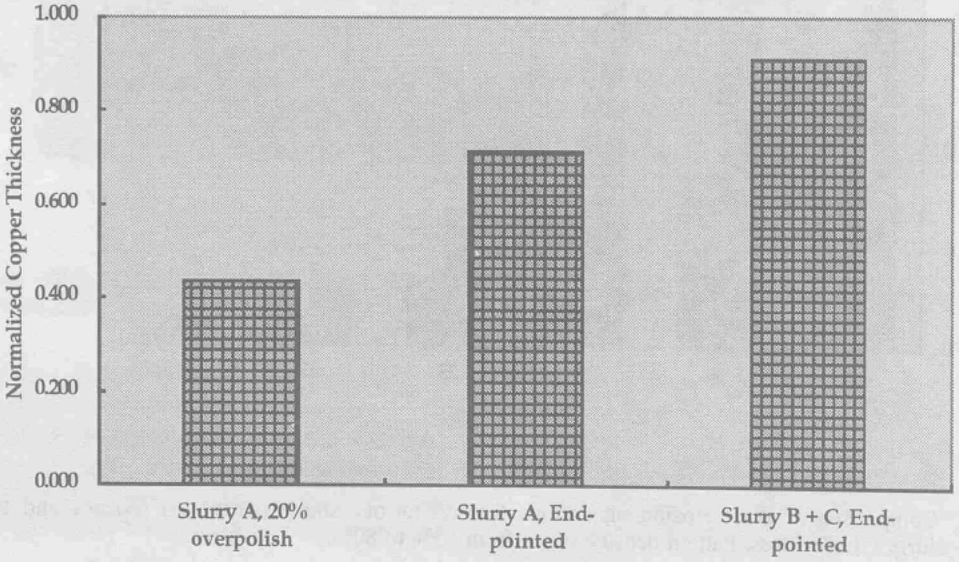

Figure 12. Comparison of electrically measured copper thickness for one slurry (slurry A) and two slurry (slurry B + slurry C) processes. Measurements were performed on a 10 m x10m Van der Pauw structure.

The data displayed in Figure 12 were measured on 10µx10µ Van der Pauw structures. As expected, the wafers processed with slurry A show heavy copper loss in the line structures. It can be seen that about 40% of additional copper is lost by performing 20% over-polish after end-point detection. However, in the case of two slurry process, only 10% copper is lost when polishing was stopped at end-point.

Conclusion

Copper dishing and oxide erosion encountered in CMP can be largely reduced by implementing a two slurry process as well as implementing multiple process steps. Use of an accurate end-point system can lead to substantial reduction in copper dishing and oxide erosion. Further improvements to slurry chemistry and copper deposition techniques are highly desirable for improving the extent of copper dishing and oxide erosion observed in current CMP processes. Also, the use of multiple polishing platens greatly simplifies two slurry CMP process. The combination of the polishing tool, end-point system, slurry chemistry and process optimization pave the way for a production worthy CMP process.

Acknowledgments

Authors would like to acknowledge Gino Addiego for his management support and very valuable suggestions and Gary Schwartz of Sematech for helpful discussions.

References

1. *Chemical Mechanical Planarrization of Microelectronic Materials*, J. M. Steigerwald, S. M. Murarka and R. J. Gutmann, John Wiley & Sons, New York, **1997.**
2. S. R. Wilson, C. J. Tracy and J. L. Freeman, *Handbook of Multilevel Metalization for Integrated Circuits*, Noyes Publications, **1993.**
3. P. Singer, *Semiconductor International*, p79, Aug. **1997.**
4. J. M. Steigerwald, S. M. Murarka and R. J. Gutmann and D. J. Duquette, *J. Electochem. Soc.* 141, 3512, **1994.**
5. J. M. Steigerwald, R. Zirpoli, S. M. Murarka, D. Price and R. J. Gutmann, *Electochem. Soc.* 141, 2842, **1994.**
6. D. Zeidler, Z. Stavreva, M. Plotner, K. Drescher, *Microelectronic Engineering*, 33, 259, **1997.**
7. S. V. Babu, Yuzhuo Li, M. Hariharaputhrian, S. Ramarajan, Jie Zhang, Yie-Shein Her and John E. Prendergast, *Proceedings of Fifteenth International VLSI Multilevel Interconnection Conference*, p443, **1998.**
8. T. Park, T. Tugbawa, J. Yoon, D. Boning, J. Chung, R. Muralidhar, S. Hymes, Y. Gotkis, S. Alamgir, R. Walesa, L. Shumway, G. Wu, F. Zhang, R. Kistler, J. Hawkins, *Proceedings of Fifteenth International VLSI Multilevel Interconnection Conference*, p437, **1998.**
9. J. Heidenreich, D. Edelstein, R. Goldblatt, W. Cote, C. Uzoh, L. Lustig, T. McDevitt, A. Stamper, A. Simon, J. Dukovic, P. Andricacos, R. Wachnik, H. Rathore, T. Katsetos, P. McLaughlin, S. Luce and J. Slattery, *Proceedings of the IITC*, p151, **1998.**
10. V. Brusic, M. A. Frisch, B. N. Eldridge, F. P. Novak, F. B. Kaufman, B. M. Rush and G. S. Frankel, *J. Electrochem. Soc.* 13, 2253, **1991.**
11. E. Zhao, L. Zhang, H. Li, D. Hymes, J. Larios and W. Krusell, *Proceedings of CMP-MIC conference*, p359, **1998.**