

UNITED STATES PATENT AND TRADEMARK OFFICE

**BEFORE THE PATENT TRIAL AND APPEAL BOARD**

Taiwan Semiconductor Manufacturing Company Limited

Petitioner

v.

Godo Kaisha IP Bridge 1

Patent Owner

**DECLARATION OF DR. SANJAY K. BANERJEE  
IN SUPPORT OF PETITION FOR *INTER PARTES* REVIEW OF UNITED  
STATES PATENT NO. 6,538,324**

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I, Sanjay Kumar Banerjee, declare as follows:

## **I. INTRODUCTION**

1. My name is Dr. Sanjay Kumar Banerjee. I have been asked to submit this declaration on behalf of Taiwan Semiconductor Manufacturing Company Limited (“TSMC” or “Petitioner”) for a petition for *inter partes* review of U.S. Patent No. 6,538,324 (“the ’324 patent”), which I understand is being submitted to the Patent Trial and Appeal Board of the United States Patent and Trademark Office by TSMC. I have been told that the ’324 patent is owned by Godo Kaisha IP Bridge 1.

2. I have been retained as a technical expert by TSMC to study and provide my opinions on the technology claimed in, and the patentability or non-patentability of, claims 1-3, 5-7, and 9 in the ’324 patent (“Challenged Claims”). I have also been asked to provide my opinions regarding the level of ordinary skill in the art at the time the Japanese priority application of the U.S. application leading to the ’324 patent was filed, which I have been told was June 24, 1999.

## **II. SUMMARY OF OPINIONS**

3. Based on my experience, knowledge of the art at the relevant time, analysis of prior art references, and the understanding a person of ordinary skill in the art would give to the claim terms in light of the specification, it is my opinion

that all of the Challenged Claims of the '324 patent are unpatentable as being obvious over the prior art references I discuss below.

### **III. BACKGROUND AND QUALIFICATIONS**

#### **A. Background**

4. I am currently the Cockrell Family Chair Professor of Electrical and Computer Engineering at the University of Texas at Austin. At UT Austin, I am also the director of the Microelectronics Research Center. I have been a faculty member at UT Austin since 1987.

5. I have also been active in industries related to the relevant field of semiconductor processing for integrated circuits. As a Member of the Technical Staff, Corporate Research, Development and Engineering of Texas Instruments Incorporated from 1983–1987, I worked on polysilicon transistors and dynamic random access trench memory cells used by Texas Instruments in the world's first 4-Megabit DRAM, for which I was co-recipient of the Best Paper Award, IEEE International Solid State Circuits Conference, 1986.

6. I received a B.Tech from the Indian Institute of Technology, Kharagpur, an M.S. and Ph.D. from the University of Illinois at Urbana-Champaign, all in Electrical Engineering.

7. I am a leading researcher and educator in various areas of transistor device fabrication technology, including the fabrication, characterization and

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