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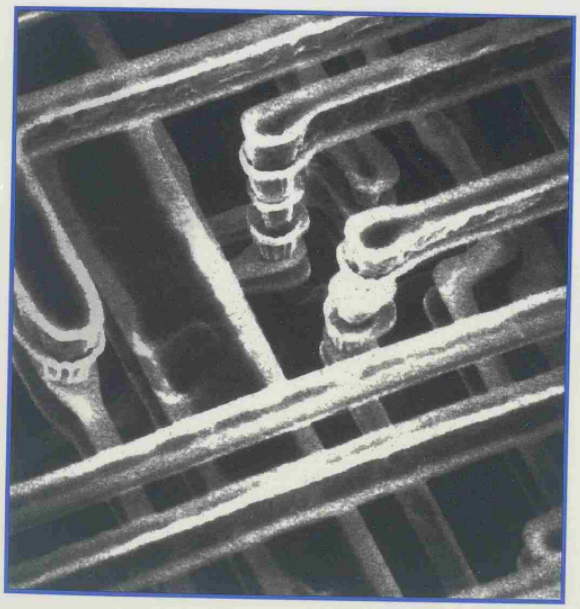

June 1-3, 1998

Hyatt Regency Airport Hotel, San Francisco, California

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TECHNICAL SESSIONS

Monday, June 1

PLENARY SESSION

SESSION 2: INTERCONNECT TECHNOLOGY TRENDS

Co-Chairs: James Meindl and Hans-Joachim Barth

SESSION 3: INTERCONNECT RELIABILITY I

Co-chair: Konrad Hieber

SESSION 4: INORGANIC LOW K DIELECTRIC INTEGRATION

Co-chairs: Michael Thomas and Nobuo Hayasaka

Tuesday, June 2

SESSION 5: IMPACT ON CIRCUIT PERFORMANCE

Co-chairs: Krishna Saraswat and Genda Hu

SESSION 6: CHEMICAL MECHANICAL POLISHING

Co-chairs: Gary Ray and Michel Brillouet

SESSION 7: ADVANCED INTERCONNECT PROCESSES

Co-chair: Robin Cheung

SESSION 8: SILICIDES AND DIFFUSION BARRIERS

Co-chairs: George Cumming and Robert Wolters

SESSION 11: ALUMINUM DUAL DAMASCENE

Co-chairs: Mehdi Moussavi and Nobuyoshi Kobayashi

SESSION 12: COPPER INTERCONNECT

Co-chairs: Betsy Weitzman and Yuji Furumura

POSTER SESSION I

POSTER SESSION II

Comparison of Barrier Materials and Deposition Processes for Copper Integration

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Abstract

This paper reports the investigation of MOCVD (Metal Organic Chemical Vapor Deposition) TiN, and IMP (Ionized Metal Plasma) Ta and TaN thin films as barrier layers for copper metallization. Evaluation of both deposition techniques including step coverage, Cu adhesion, Cu diffusion and selectivity regarding Cu-CMP process have been performed. Successful implementation with copper metallization in high aspect ratio line and via patterns is reported.

Introduction

As circuit integration density continuously increases, interconnection size is predicted to decrease both in vertical and lateral dimensions. Unfortunately, intrinsic properties of the materials currently used for interconnection such as resistivity and electromigration performance do not allow an optimal scaling. This explains the growing interest in copper for overcoming limitations of the conventional aluminium based alloys (1,2). The two most critical aspects for integration of copper metallization are the optimal choice of diffusion barrier material - the Cu diffusion in the active areas resulting into degradation of the devices- and diffusion barrier material and copper deposition techniques. The barrier layer should meet stringent requirements : the thickness has to be small enough to not impact interconnect resistance while still acting as a good barrier against Cu diffusion. Several barrier materials have been reported as good candidates. TiN barrier, currently used with Al-based metallization, has shown convenient results (3). However other papers suggest that Tantalum and Tantalum nitride could be the best choice. In this work a comprehensive comparison of the TiN, Ta and TaN performance was carried out with regards to Cu integration. A variety of solutions have been developed to deposit copper : Ionized Metal Plasma, CVD, combination of these techniques and the new electroplating method.

Experimental

A. Barrier Materials

An Applied Materials Endura system using IMP (Ionized Metal Plasma) was used to deposit Ta and TaN barriers. Prior to film deposition, wafers were degassed at 350°C and sputter cleaned using a standard AMAT PCII reactor. CVD TiN was performed in P5000 reactor using TDMAT precursor with successive steps of deposition and plasma treatments.

B. Copper Deposition Equipment

IMP copper used as a seed layer was deposited on an Endura system. The Chemical Vapor Deposition of copper was performed in a Precision 5000 AMAT cluster tool. Two CVD chambers are available, one for copper deposition and the second for TiN-CVD. Copper was therefore deposited on TiN barrier, without vacuum break between TiN. The cluster equipment allows a clean and reproducible TiN/Cu interface. Copper Electroplating on various seed layers was performed on a Semitool Equinox system using pulsed current in order to achieve uniform films with high deposition rates up to 400 nm/min.

C. Chemical Mechanical Polishing

Polishing experiments were carried out on a PRESI MECAPOL 550 polisher, using a RODEL IC1000 pad stacked on a SUBA IV pad. The slurry is alumina-based and has to be mixed with hydrogen peroxide oxidizer prior to use (5).
Copper and barrier removal rates (RR) were determined by polishing respectively Cu, TiN, Ta and TaN blanket wafers. Barrier layer selectivities were calculated by the following formula: Selectivity = Copper RR / Barrier RR.
Planarization performance was investigated on topological wafers with copper line widths and oxide spaces varying from 0.3µm to 100µm.

Results

A. Barrier Materials

Materials properties and barriers performance of IMP Ta, IMP TaN, CVD TiN films were extensively characterized The main results are summarized in Table 1. Stress was measured on 500nm thick film for IMP Ta and TaN and on 60nm thick film for CVD TiN. Tensile stress are measured on IMP films while the stress is compressive in CVD TiN film.

To evaluate barrier efficiency against Cu diffusion, 500nm of CVD copper was deposited on barriers (10nm IMPTa or TaN and 40nm TiN); Cu contamination in silicon was determined by SIMS after annealing at 450°C. On account of the different barrier thicknesses, the efficiency are similar for the three materials. For CMP application, selectivity between barrier and copper was evaluated on blanket wafers.

Properties	IMPTa	IMPTaN	CVDTiN
Resistivity	170μΩ.cm	250μΩ.cm	130 μΩ.cm
Stress	+350MPa	+1500MPa	-750MPa
Barrier performance	$6E^{16}$at/cm³	$6E^{17}$at/cm³	$1E^{17}$at/cm³
Conformity (0.3μ line) side wall / bottom	20% / 40%	40% / 40%	100%/1 00%
CMP selectivity vs Cu	23	20	1

Table 1: Barrier characteristics

Step coverage was determined by SEM observations on patterned wafers with lines of 0.3 to 100μm widths.

Step coverage of CVD TiN is 100% whatever the pattern size. Figure 1 presents the variations of bottom and side-wall coverage of IMP Ta and IMP TaN. When increasing line width, bottom coverage increases up to 100% while side wall coverage remains around 20%.

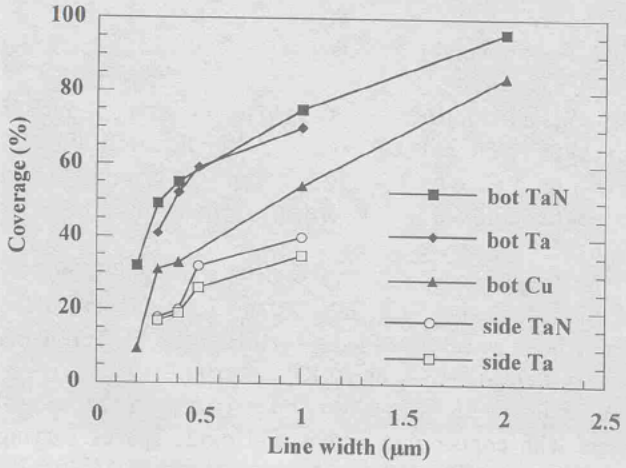

Figure 1: Coverage for IMP Ta, IMP TaN and IMP Cu vs line width

Figure 2 represents a SEM cross-section of 0.3μm line with 40nm thick IMP TaN layer. The IMP technique is efficient to achieve a continuous coverage of the barrier layer, even at the corners.

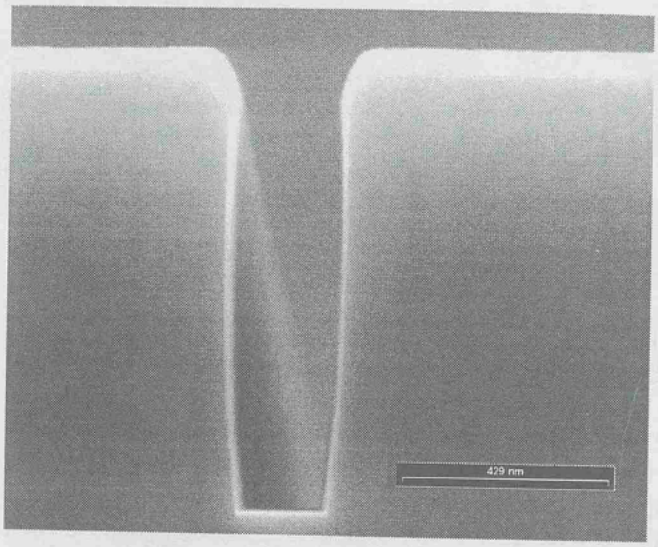

Figure 2: Coverage of IMP Ta film in 0.3μm line

B. Copper Deposition Processes

Copper deposition in high aspect ratio (3:1) trenches and vias was performed either by using Cu CVD alone or by combining a thin Cu liner with Cu electroplating for pattern filling.

In this work, pure Cu(hfac)(TMVS) was chosen as precursor for the CVD deposition. The detail of the process have been reported previously (4). Very conformal process was therefore available to achieve a void-free filling of the interconnect patterns. The nucleation step was also optimized in order to obtain very thin continuous seed layers. Good adhesion of Cu CVD with the underlying barrier material was obtained by using an in-situ treatment performed in the deposition equipment.

The electroplated copper films showed a void-free gap filling with a good resistivity of 1.9 μΩ.cm, and an adhesion compatible with CMP requirements. Figure (3) shows such film as deposited, and after CMP.

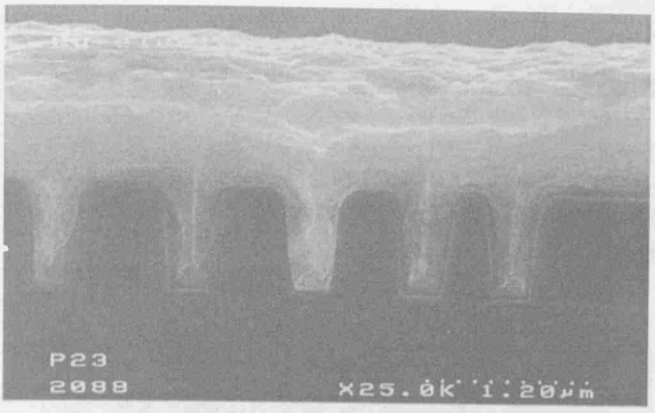

Figure 3a. As deposited Electroplated copper

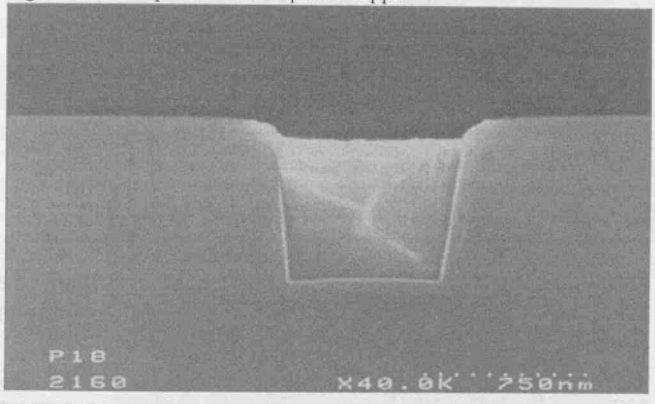

Figure3b. Electroplated Copper Film after CMP

C. Chemical Mechanical Polishing

Barrier versus copper selectivity determined on full sheet wafers are reported on table 1. Unlike TiN, Ta and TaN removal rates are much lower than copper removal rate.
The elimination of these barrier layers was investigated on topological wafers. The 40nm TiN layer was entirely removed while keeping acceptable copper dishing and oxide erosion effects. The high selectivity of Ta and TaN barrier layers was confirmed on topological wafers. To quantitatively determine this effect, a thick Ta barrier layer (100nm) was used. After polishing using the same conditions than for the TiN barrier layer, the remaining Ta barrier thickness was measured by SEM. As shown on figure 4, less than 5nm of the barrier layer were removed, demonstrating the excellent CMP stop layer capability of Ta material.

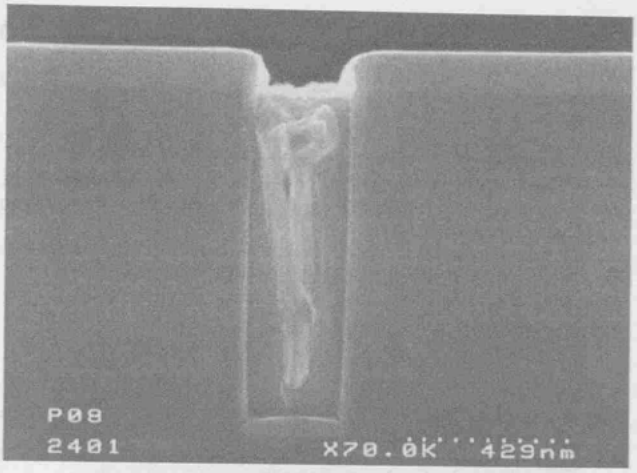

Figure 4. Copper CMP with Ta barrier
(0.3 µm line width / 0.3 µm oxide space)

Conclusion

A variety of solutions for 0.25µm copper interconnect technology have been developed. Complete via filling was achieved by combination of CVD and IMP techniques, and by electroplating deposition. A comprehensive comparison of TiN, Ta and TaN materials as barrier layers for copper metallization has been carried out, as these three materials proved to block copper diffusion. TiN was suitable for usual CMP process, involving removal of the entire metal stack during polishing. Ta and TaN barriers showed excellent CMP stop layer capabilities. Therefore, these new materials can lead to a novel CMP approach, in which the barrier layer is used to prevent from oxide erosion.

Acknowledgment

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