FUNDAMENTALS OF SEMICONDUCTOR PROCESSING TECHNOLOGY

by

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Preface

The drive toward new semiconductor technologies is intricately related to market demands for cheaper, smaller, faster, and more reliable circuits with lower power consumption. The development of new processing tools and technologies is aimed at optimizing one or more of these requirements. This goal can, however, only be achieved by a concerted effort between scientists, engineers, technicians, and operators in research, development, and manufacturing. It is therefore important that experts in specific disciplines, such as device and circuit design, understand the principle, capabilities, and limitations of tools and processing technologies. It is also important that those working on specific unit processes, such as lithography or hot processes, be familiar with other unit processes used to manufacture the product.

Several excellent books have been published on the subject of process technologies. These texts, however, cover subjects in too much detail, or do not cover topics important to modern technologies. This book is written with the need for a "bridge" between different disciplines in mind. It is intended to present to engineers and scientists those parts of modern processing technologies that are of greatest importance to the design and manufacture of semiconductor circuits. The material is presented with sufficient detail to understand and analyze interactions between processing and other semiconductor disciplines, such as design of devices and circuits, their electrical parameters, reliability, and yield.

The book was developed from notes prepared for courses taught at IBM and the University of Vermont. It serves as a base on which to build an understanding of the manufacture of semiconductor products. It is written in a form to satisfy the needs of engineers and scientists in semiconductor research, development and manufacturing, and to be conveniently used for a one-semester graduate-level course in a semiconductor engineering or material science curriculum. The book consists of eight chapters on unit processes that are arranged in a conventional sequence that reflects typical integrated process technologies. It begins with the preparation of semiconductor crystals and continues with thermal oxidation, thin-film deposition, lithography, etching, ion implanta-

tion, diffusion, and contact and interconnect technology. The last chapter is co-authored by J. G. Ryan, manager of Thin Film and Chemical-Mechanical Polishing Development at IBM.

One of the challenges faced when writing a book on semiconductor technologies is finding satisfactory explanations to observations reported in the literature. Semiconductor processes are based more heavily on empirical data than on prediction by simulation of physical or chemical phenomena. This by itself, requires a thorough review and comparison of published data and observations. It is easier to predict electrical parameters from given horizontal and vertical device geometries than to define processing conditions that result in such geometries. The reader should therefore not be surprised to find sections describing "how" a process is performed without the accompanying "why".

The author is indebted to all those who helped shaping the book in its present form. He is very grateful to his friends and colleagues, Albert Puttlitz and Ashwin Ghatalia, for relentlessly checking for flaws in the manuscript and making valuable suggestions. He also thanks Robert Simonton (Eaton Corporation) and Larry Larson (SEMATECH) for spending a great deal of time with him on ion implantation equipment. The author gratefully acknowledges all his IBM colleagues for their invaluable inputs and discussions; Don Chesebro, Burn Lin, Tim Brunning, Mike Hibbs for their inputs on advanced lithography, Geoff Akiki for providing information on advanced mask preparation, Hans Pfeiffer on electron-beam lithography, Randy Mann and Robert Geffken on silicides and metallization.

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FUNDAMENTALS OF SEMICONDUCTOR PROCESSING TECHNOLOGY

Chapter 1

Semiconductor Crystals

1.0 Introduction

The first step in the manufacture of modern integrated circuits is the preparation of a single crystal of semiconductor material. In crystalline solids, the elements are stacked in a periodic pattern as illustrated in Fig. 1.1. When the periodicity extends throughout the solid, one speaks of a **single crystal,** or monocrystal, as opposed to a **polycrystal** which consists of small crystals, called **grains,** arranged in random directions and adhering together at their boundaries (Fig. 1.2).

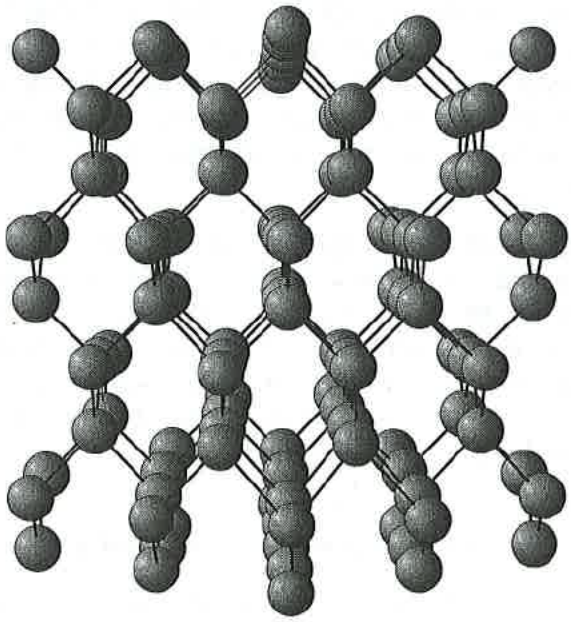


Fig. 1.1 Model of silicon crystal, seen along the <110> direction [1]. (Crystallographic directions are discussed in the following section).

Fig. 1.2 Micrograph of polycrystalline silicon. The crystallites are called grains and the regions between the grains are called grain boundaries. (Courtesy: W. Tice, IBM).

Noncrystalline solids are called **amorphous.** Normally, solids assume the crystalline form because it is the atomic arrangement of minimum energy. In most solids at room temperature atoms occupy, on the average, fixed positions relative to each other. The atoms, however, are in constant vibration about their equilibrium position.

Semiconductor properties are not exclusive to single crystals. Many non-crystalline materials exhibit semiconductor properties similar to those of crystalline semiconductors. In this chapter, however, we restrict ourselves to the discussion of the preparation and properties of single crystal semiconductors, in particular silicon since this is the best understood and most widely used materials in integrated circuits (IC).

1.1 Crystals and Crystallographic Orientations

A crystal can be described in terms of a periodic **lattice.** We can attach to each lattice point an atom or a group of atoms called the **basis.** The basis is repeated in space to form the crystal (Fig. 1.3).

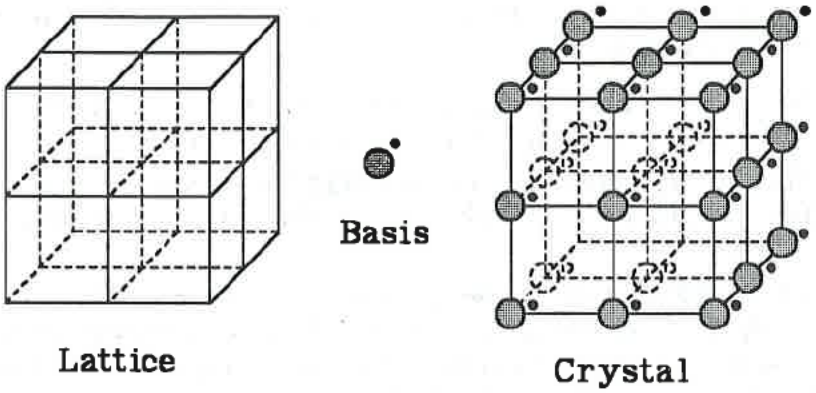


Fig. 1.3 Lattice + basis = crystal structure.

One can think of three intersecting families of parallel crystal planes passing through the lattice and dividing the crystal space in small, identical parallelepipeds. The crystal can then be visualized as a repetition in space of one parallelepiped, called the **unit cell** (Fig. 1.4). The edges of the unit cell define the chosen directions of crystal axes. The lengths OA, OB and OC are called the **lattice constants** a, b and c. In a cubic crystal, a = b = c and the axes are perpendicular.

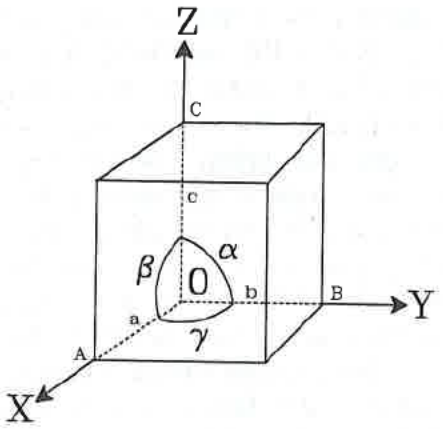


Fig. 1.4 Unit cell of the most general crystal type, showing crystal axes OX, OY and OZ, and the lattice constants a, b and c. Angles $\angle BOC$, $\angle AOC$ and $\angle AOB$ are α, β and γ. In a cubic crystal a = b = c and $\alpha = \beta = \gamma = 90°$.

Crystal planes are best represented by **Miller indices** which are specified as follows:

1. Let the plane intercept the crystal axes at the lattice points $\mathbf{n}_1$a, $\mathbf{n}_2$b and $\mathbf{n}_3$c, relative to a chosen origin O (Fig. 1.4).
2. The intercepts are expressed as integral multiples of the lattice constants a, b and c. The planes are defined by a set of integers n_1, n_2 and n_3.
3. The reciprocals of the numbers n_1, n_2 and n_3 are usually fractions. Reduce the fractions to the smallest three integers having the same ratio as the fractions. The three integers obtained are called the Miller indices h, k, and l.

The group of integers (hkl) defines a set of equally spaced parallel planes, as illustrated in Fig. 1.5. If a plane crosses the axis on the negative side of the chosen origin, then the corresponding index is negative and is written with a bar over it such as $(h\bar{k}l)$. For cubic crystals of a single element the (100), (010), (001), $(\bar{1}00)$, $(0\bar{1}0)$ and $(00\bar{1})$ planes are indistinguishable, as are the planes (110), (101) and (011).

A family of equivalent planes is described with the indices enclosed in braces: $\{hkl\}$. These braces define planes which may have different Miller indices but are equivalent by symmetry. For example, in the silicon crystal {100} describes the equivalent planes (100), (010), (001), $(\bar{1}00)$, $(0\bar{1}0)$, and $(00\bar{1})$. A particular direction in the crystal is denoted by a vector which is specified by a group of indices in brackets [*uvw*]. The indices are integers and have no common factor larger than unity. The direction [*uvw*] is obtained by moving from the chosen origin over a distance **u**a along the a-axis, **v**b along the b-axis and **w**c along the c-axis. The vector that connects the chosen origin to the point thus obtained is then the direction specified by the indices [*uvw*]. In a cubic crystal the [100] direction is the x-axis while the (100) plane is perpendicular to the x-axis. In cubic crystals the [*uvw*] direction is always perpendicular to a plane (hkl) having the same indices. A set of equivalent directions in a crystal is represented as < uvw > .

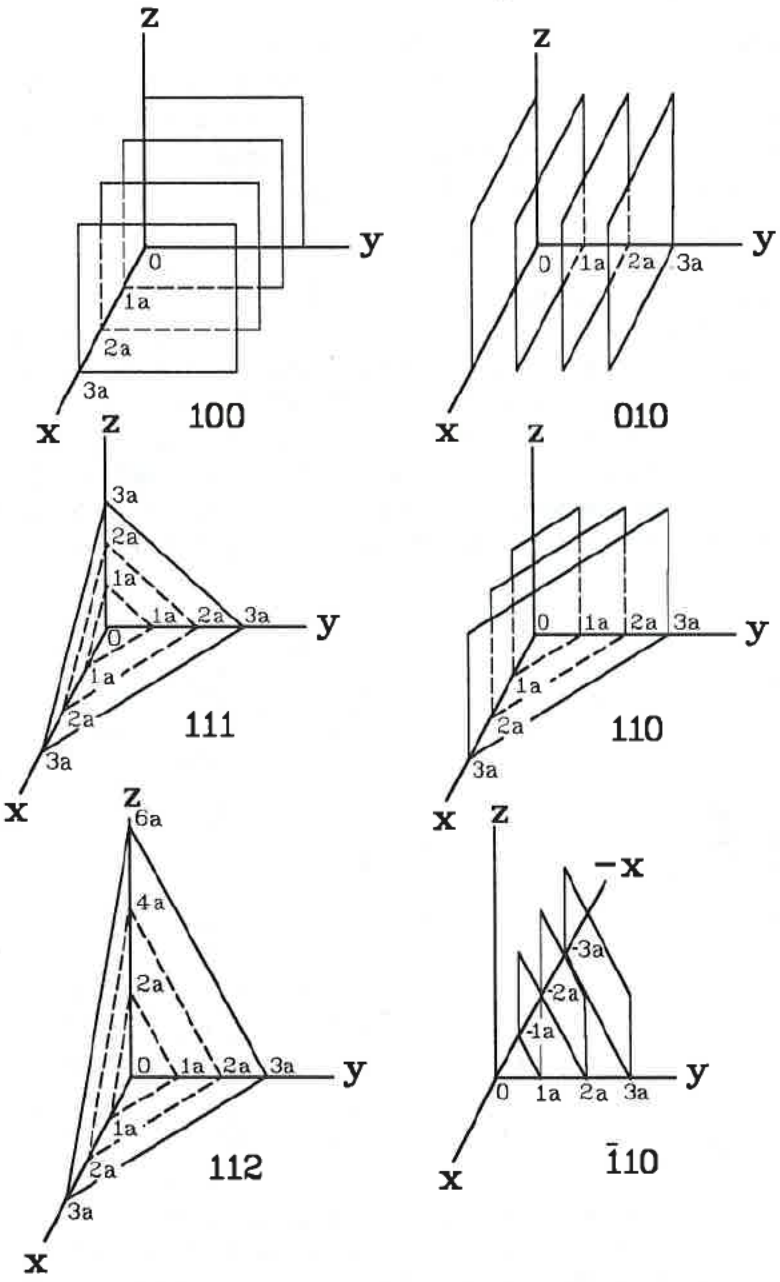


Fig. 1.5 Miller indices of some important planes in a cubic crystal.

1.2 The Silicon Crystal

The silicon crystal has a diamond structure and belongs to the cubic crystal system. In diamond crystals, pairs of valence electrons with opposite spins are shared between four neighboring atoms and form **covalent bonds.** The 3s and 3p orbitals of the parent atoms are mixed to form a new set of equivalent four bonding orbitals, called *hybridized orbitals,* that are directed toward the four nearest neighbors (Fig. 1.6). In the diamond structure each atom is symmetrically surrounded by four equally spaced atoms; it forms tetrahedral bonds with its four nearest neighbors. This type of bonding is very strong, highly localized, and directional because the distribution of valence electrons around the atom becomes shifted toward the nearest neighbor. The silicon crystal is therefore very hard, and has a high melting point. Because of the directionality, the crystal does not assume the closest packing configuration, but allows a large volume per atom.

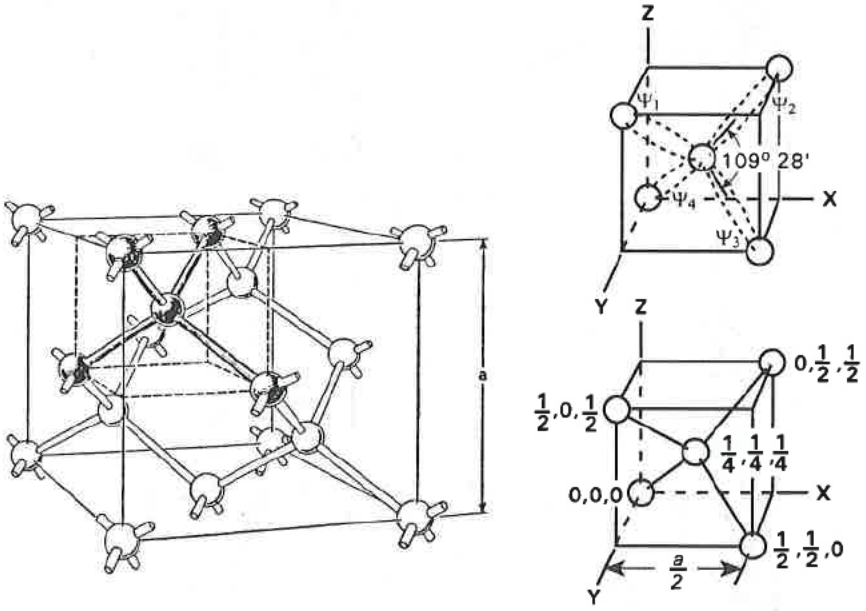


Fig. 1.6 Diamond structure and subcell illustrating the tetrahedral bonds. Each atom has four nearest neighbors. The hybridized orbitals are ψ_1, ψ_2, ψ_3, and ψ_4.

The unit cell configuration in a diamond crystal is best described by projecting the cube onto a two-dimensional plane as shown in Fig. 1.7. The plane of the paper is chosen as one of the cube's planes. The numbers then define the location of the atom centers relative to the plane of the paper in fractions of the cube's edge *a*. For example, atoms located at the centers of cube faces normal to the page are labeled 1/2.

For most discussions, it is convenient to use a simplified two-dimensional picture of the silicon crystal as illustrated in Fig. 1.8. The arrangement shows that when all bonds are in place, each silicon atom has four nearest neighbors. Each bond is represented by two links representing two electrons per bond.

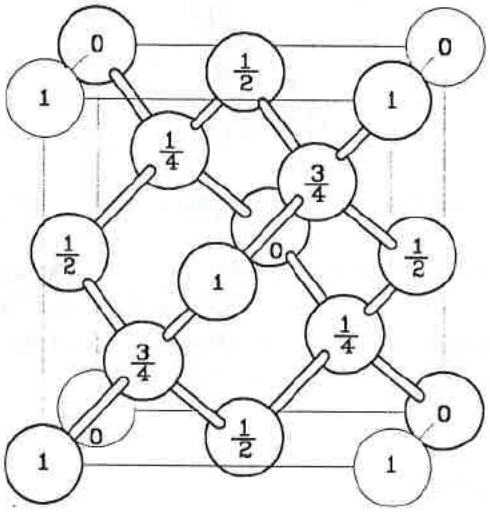


Fig. 1.7 Three-dimensional representation of the unit cell in a diamond crystal. Numbers show displacement of atoms normal to the plane of the paper in fraction of the cube edge *a* [2].

When using this simplified scheme, it should be remembered that the structure is three-dimensional, and that the tetrahedral bonds form one continuous three-dimensional chain throughout the solid. The electrons are not constrained to one particular bond. Instead, they can move throughout the crystal, exchanging places with other valence electrons (no net current is

involved). One must consider the entire system, where the bonding electrons belong to the entire crystal, not to a particular atom. This picture will be of great help when discussing energy-band diagrams and related semiconductor properties.

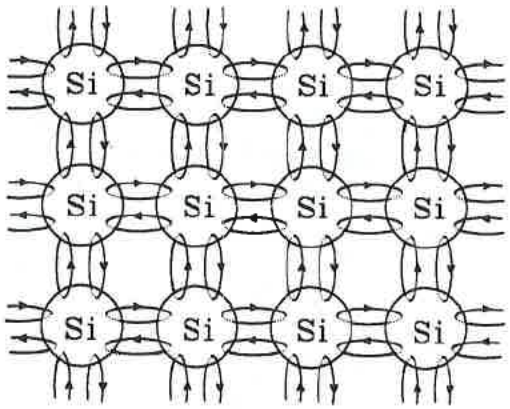


Fig. 1.8 Two-dimensional representation of a silicon crystal.

Important properties of the silicon crystal are given in Table 1.1. The table also contains silicon parameters such as energy gap, electron affinity, effective mass, carrier concentration and dielectric constant. These parameters are discussed in the following chapters.

1.2.1 Crystal Growth

The most common technique for growing silicon crystals of commercial dimensions is the Czochralski (CZ) crystal pull method. In this method, polycrystalline silicon **(polysilicon)*** is melted in a crucible usually made of graphite with fused silica lining (Fig. 1.9). Power is provided by resistance heating or radio-frequency. A seed crystal of known orientation is immersed into the surface of the melt and then slowly withdrawn while rotated.

*Polysilicon is prepared by depositing silicon from gaseous mixtures of trichlorosilene ($SiHCl_3$) or silicon tetrachloride ($SiCl_4$) and hydrogen, (Chap. 3).

Table 1.1 Some Important Properties of Silicon at 25 °C [3, 4].

Symbol	Si
Color	Blue-grey
Atomic number	14
Atomic weight	28.09 g/Mole
Crystal structure	Diamond
Lattice constant	5.4307 Å
Silicon radius	1.18 Å
Atomic density	$5.02x10^{22}$ atoms/cm^3
Density	2.328 g/cm^3
Melting point	1412 °C
Specific heat	0.7 J/g.K
Thermal conductivity	1.5 W/cm.K
Vapor pressure	10^{-7} Torr (1050 °C)
Thermal expansion coefficient	$2.6x10^{-6}K^{-1}$
Relative dielectric constant	11.7
Index of refraction	3.42
Energy gap	1.12 eV
Intrinsic carrier concentration	$1.25x10^{10}$cm^{-3}
Electron affinity	4.05 eV
Conduction band density of states	$2.80x10^{19}$cm^{-3}
Valence band density of states	$1.04x10^{19}$cm^{-3}
Lattice electron mobility	1450 cm^2/V.s
Lattice hole mobility	500 cm^2/V.s
Average optical phonon energy	0.063 eV
Optical phonon mean-free path	7.6 nm (e); 5.5 nm (h)
Intrinsic Debye length	24 μm
Intrinsic resistivity	$2.3x10^5$ Ohm-cm
Donors	P, As, Sb
Acceptors	B
Hardness	7 Mohs
Poisson's ratio	0.42
Tensile Strength in <111>	$3.5x10^8$N/m^2
Modulus of Elasticity in <111>	$1.9x10^{11}$N/m^2
Modulus of Elasticity in <110>	$1.7x10^{11}$N/m^2
Modulus of Elasticity in <100>	$1.3x10^{11}$N/m^2

Both the crucible and the growing crystal are rotated to average variations in temperature and impurity concentration within the melt. The ambient gas is typically argon. The crystal diameter is computer controlled during growth. The crystal is grown oversize, ground to the desired dimension, and then sliced into thin wafers which are used for device fabrication.

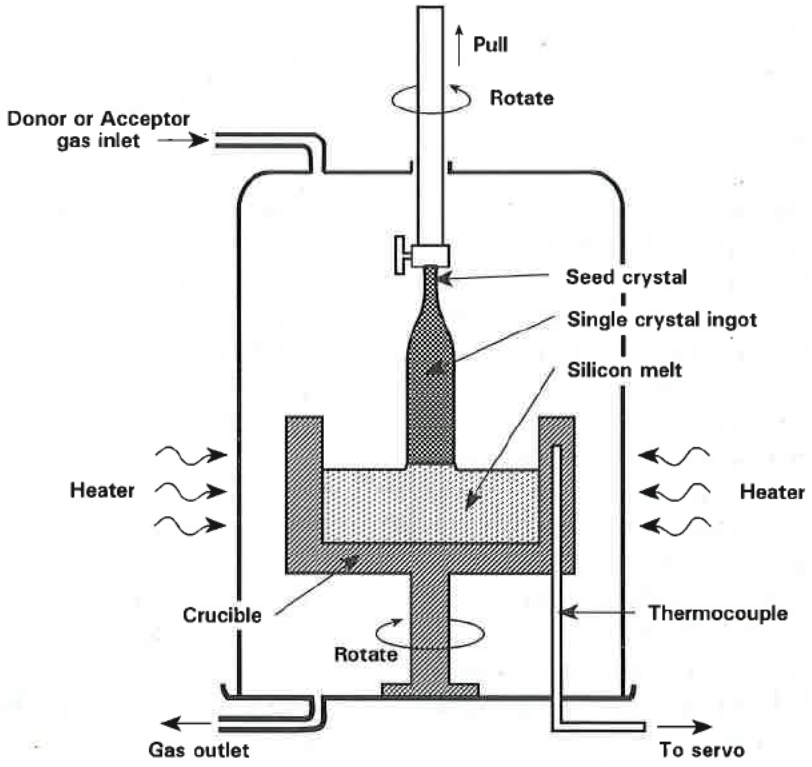


Fig. 1.9 The Czochralski crystal pull method

One of the problems with Czochralski grown crystals is their high impurity content (especially oxygen and carbon). These impurities are introduced unintentionally during crystal growth and originate primarily at the quartz crucible lining. Typical oxygen concentrations range between $5x10^{17}\,cm^{-3}$ and $10^{18}\,cm^{-3}$ [5]. Carbon is found in concentrations between $10^{16}\,cm^{-3}$ and $10^{17}\,cm^{-3}$ [6]. The presence of *controlled* amounts of oxygen, however, can be advantageous: it can help remove harmful impurities and defects from the surface of the wafer, as discussed in section 1.2.3.

Silicon crystals of high purity can be grown by the floating zone (FZ) method (Fig. 1.10). A polycrystalline rod is clamped in a vertical position in a chuck at the top, and a seed crystal with the desired orientation is clamped at the bottom. The formation of the single crystal begins by melting a small "floating" zone (typically 1.5 cm wide) in contact with the seed. The floating zone is generated by moving a polycrystalline rod relative to a water-cooled induction coil supplied with radio frequency power in the megacycle range. Either the rod is moved downward or the coil is moved upward. In both cases the floating zone starts at the seed and propagates up the rod. The ends of the rod are rotated in opposite directions, resulting in straight, round crystals. As the zone travels from the seed to the top of the polycrystalline rod, the silicon melts and resolidifies into a single crystal which has the same orientation as the seed. The molten zone is held in place by a combination of RF levitation and surface tension and does not come in contact with any crucible. The concentration of impurities is therefore considerably lower in FZ than in CZ crystals. Also, most remaining impurities can be swept to the top of the crystal by making successive passes of the floating zone from seed to top. High purity crystals obtained from the floating-zone technique are used in specific applications, such as high voltage devices, as discussed in the chapters to follow.

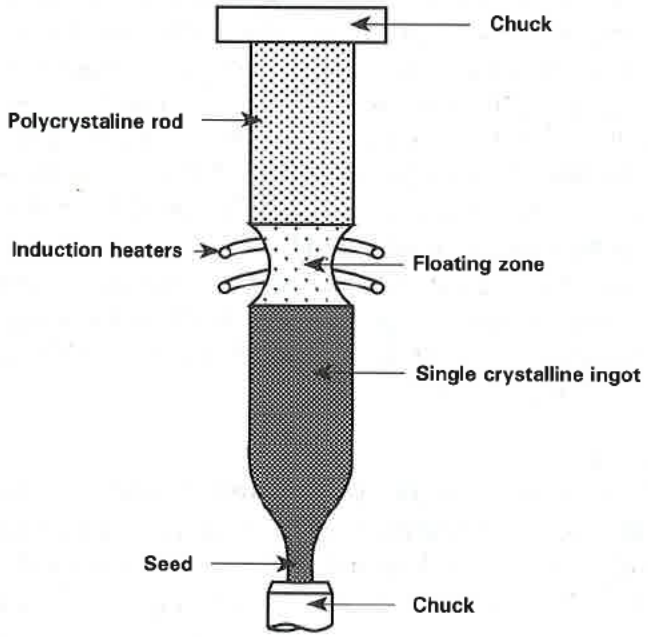


Fig. 1.10 The floating-zone crystal growth technique

Since the molten zone is held together only by surface tension and RF levitation, stability problems limit the grown crystal diameter to $\simeq$10 cm [7]. Also, the very low oxygen concentration in FZ crystals can become a disadvantage in some applications where intrinsic gettering plays a dominant role in reducing the surface defect density (Sec. 1.2.3).

1.2.2 Crystal Doping

The introduction of controlled amounts of selected impurities in lattice sites otherwise occupied by silicon is called **doping.** Lattice sites occupied by impurities are referred to as **substitutional sites.**

In the Czochralski method the crystal is doped by dissolving the desired impurity in the melt (boron for p-type crystals; arsenic, phosphorus, or antimony for n-type crystals). The dopant is added to the melt in the form of a gas, powder, or heavily doped polysilicon. In the floating-zone method the silicon is doped by introducing a controlled amount of the dopant in the argon atmosphere surrounding the crystal during growth. Other techniques for doping the crystal are discussed in chapters 6 and 7.

Segregation Coefficient

In the floating-zone technique we found that impurities are swept by the traveling zone to the top of the rod. This is because at a given temperature the concentration of most impurities is higher in the melt than in the solid. At the interface between melt and solid in CZ and FZ grown crystals, the excess dopant in the solid is "thrown-off" into the melt. The difference in impurity concentration between melt and solid is described by a factor called the **segregation coefficient k.** This is the ratio of the impurity concentration (by weight) in the solid to that in the melt, at the interface between the two phases. Equilibrium segregation coefficients of typical impurities in silicon are given in table 1.2. As can be seen, k is less than unity.

Misfit Factor

Each silicon atom is situated within a tetrahedron, equidistant from four neighbors (Fig. 1.6). In a hard sphere model it can be assigned a tetrahedral radius r_o. Substitutional impurities can also be assigned a "hard sphere" radius $r_i = r_o(1 \pm \Delta)$, where

the ratio Δ/r_o describes the mismatch in size between the impurity and "host" atom, and is called the **misfit factor.** It is indicative of the strain in the lattice caused by introducing impurities into the crystal. Misfit factors of typical dopants in silicon are given in table 1.3. Note that arsenic is the only impurity that has a perfect fit with silicon.

Table 1.2 Segregation coefficients of typical impurities in silicon

Element	Segregation Coefficient
B	0.72
Al	0.0018
Ga	0.0072
P	0.32
As	0.27
Sb	0.02

Table 1.3 Misfit factors of typical impurities in Silicon

Impurity	Radius (Å)	Misfit Factor
B	0.88	0.254
Al	1.26	0.068
Ga	1.26	0.068
In	1.44	0.220
P	1.10	0.068
As	1.18	0.000
Sb	1.36	0.153

Solid Solubility

There is a limit to the concentration of substitutional impurities that can be incorporated in silicon without seriously disrupting the lattice. This is referred to as the **solid solubility limit** of the impurity. Note that the solubility of typical impurities in silicon is very small and depends on temperature (Fig. 1.11). The highest concentration of boron in silicon for example, is less than 1%. The solubility initially increases with temperature and then

begins to decrease as the crystal melting temperature is approached. When the maximum solubility is achieved at a certain temperature, the crystal is said to be saturated with the impurity at that temperature. If the crystal is cooled to a lower temperature without removing the excess impurity, a supersaturated condition is created. The crystal may return to the saturated condition by precipitating impurities present above the solubility limit.

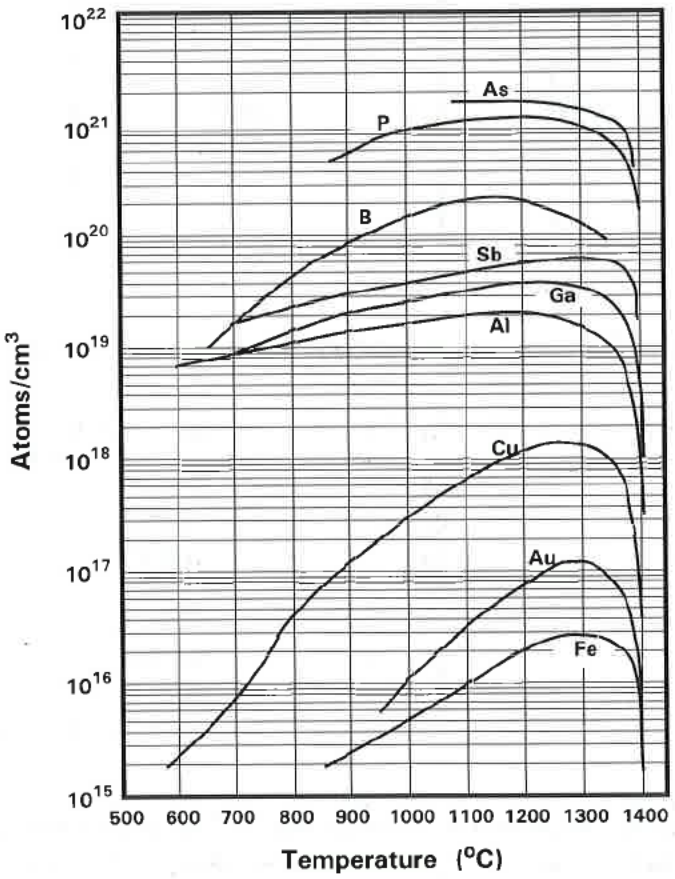


Fig. 1.11 Solid solubility of impurities in silicon [8, 9].

1.2.3 Defects in Silicon Crystals

A model silicon crystal contains only silicon atoms perfectly arranged in a periodic pattern assumed to be infinite in three dimensions (Fig. 1.1). Real crystals, however, terminate at boundaries called **surfaces,** and contain imperfections in the bulk and at surfaces. These imperfections, referred to as **defects,** are inherent to the crystal or created during crystal growth or subsequent processing. Even the best grown crystals contain at least one defect per billion crystal atoms. This is approximately 10^{13} defects per cm^3. Defects can drastically alter the electrical and physical properties of the crystal. They play an important role in the transport of impurities and carriers in the crystal.

Four types of crystal defects can be distinguished: **point defects, line defects, plane defects** and **volume defects.**

Substitutional impurities, **interstitial** atoms, **vacancies** and **vacancy pairs** are examples of point defects. As mentioned, a substitutional impurity is one that occupies a position otherwise occupied by the original crystal atom. An interstitial impurity occupies a position between regular crystal atom sites. A vacancy is a regular site that is not occupied by any atom.

Typical line defects are crystal **dislocations.** For example, a dislocation is formed when ten atoms occupy the space which would be normally occupied by nine atoms.

The most important plane defects are **stacking faults.** These are created when the stack sequence of the crystal atoms is disrupted, as discussed later in this section.

One example of volume imperfections is the oxygen-precipitation-induced defects that can act as "sinks" for heavy metals in large volumes of the crystal.

Point Defects

Four types of point defects are shown in Fig. 1.12. A lattice vacancy is shown in Fig. 1.12a. It is created when the four valence bonds of a tetrahedral silicon atom are broken. When the atom which is set free migrates to the crystal surface, the vacancy is called a **Schottky defect** (Fig. 1.12b). When a silicon atom is set free from its lattice site and "eases itself" into an interstitial position, the vacancy-interstitial pair is called a **Frenkel defect** (Fig. 1.12c). Schottky and Frenkel type defects are created by thermal energy: vibrations of lattice atoms interact and may add at a lattice site to displace an atom from its position.

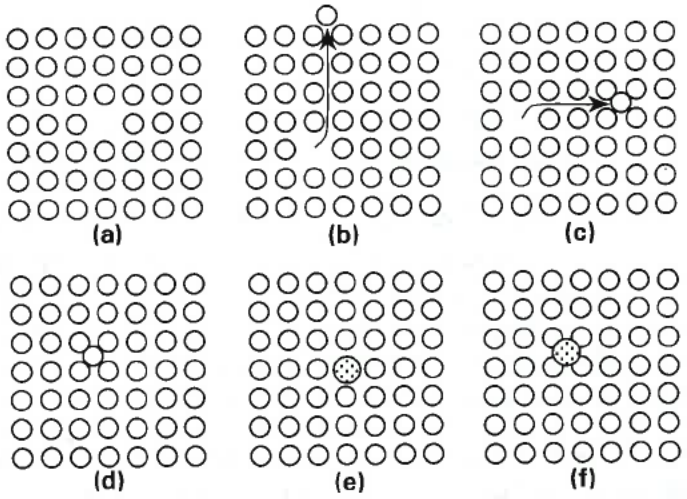


Fig. 1.12 Point defects. (a) Lattice vacancy. (b) Schottky-type defect. (c) Frenkel-type defect. (d) Interstitial "host" atom. (e) Substitutional impurity. (f) Interstitial impurity.

The density of defects can be determined by the laws of statistical mechanics. The equilibrium density of Schottky defects is found as:

$$n_s = Ne^{-E_s/kT} \qquad 1.1$$

where

n_s = density of Schottky defects (cm^{-3})
N = atomic density of silicon (cm^{-3})

E_s = energy of formation of a Schottky defect ($\simeq$ 2.3 eV)
k = Boltzmann constant ($8.62x10^{-5}eV/K$)
T = absolute temperature (K)

The equilibrium density of Frenkel type defects is given as:

$$n_f = \sqrt{NN'}\ e^{-E_f/2kT} \qquad 1.2$$

where

n_f = density of Frenkel defects (cm^{-3})
N' = density of available interstitial sites (cm^{-3})
E_f = energy of formation of a Frenkel defect ($\simeq$ 1.1 eV)

Point defects can enhance or retard the motion of impurities in the crystal, as discussed in Chap. 7.

An interstitial "host" atom is a silicon atom which occupies a **void,** that is the space between lattice sites (Fig. 1.12d). A substitutional impurity is shown in Fig. 1.12e, and an interstitial impurity in Fig. 1.12f.

Line Defects

Line defects appear in form of dislocations in regions where permanent deformation of the crystal has occurred [10]. The stress producing the dislocation can be mechanical (shear stress), thermal (crystal growth), chemical (misfit of impurity atoms) or radiative (ion bombardment).

Figure 1.13 illustrates one type of dislocation called **edge dislocation.** Here, the dislocation occurs at the termination of an extra plane inserted in the lower half of the crystal. A two-dimensional bubble model of an edge dislocation is shown in Fig. 1.14. When viewed along the indicated arrow, the pattern exhibits an extra line of bubbles on the lower half of the plane [11].

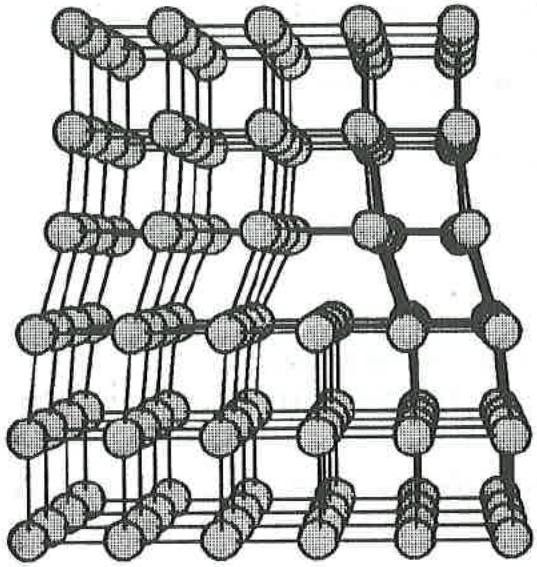


Fig. 1.13 Edge dislocation. Dislocation occurs at the termination of the extra plane of atoms.

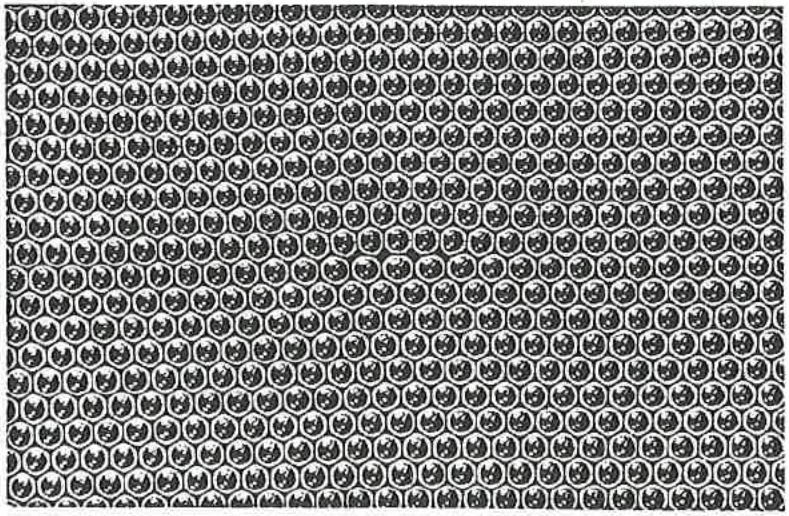


Fig. 1.14 Two-dimensional bubble model of an edge dislocation. The dislocation can be viewed by turning the page by 30 ° and sighting at a low angle.

The following thought experiment describes the formation of an edge dislocation [12].

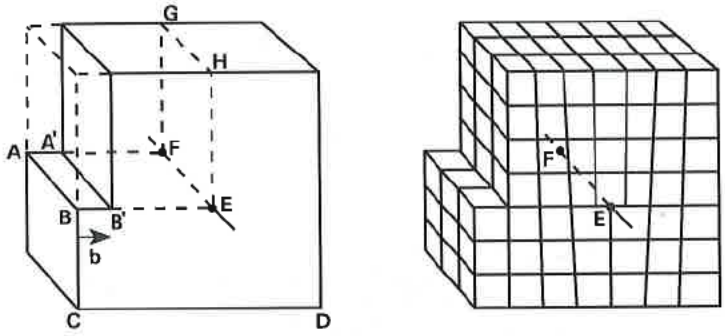


Fig. 1.15 Thought experiment to illustrate the formation of an edge dislocation. EF represents an edge dislocation line.

Suppose that the crystal in Fig. 1.15 is cut across a plane ABEF, and the upper half displaced so that line A'B' which was initially coincident with line AB is slipped by a distance b, as indicated. If now the two halves are stuck together, an edge dislocation is formed. The crystal plane along which the slip has occurred is known as the slip plane. In this example, the upper half of the crystal is under compression and the lower half is under tension. The termination of the extra plane is an edge dislocation. As in Fig. 1.13, the dislocation line extends out of the paper and is perpendicular to the slip direction.

If the extra plane is above the slip plane, the edge dislocation is positive, below the slip plane it is negative. The slip process resulting from a moving edge dislocation is illustrated in Fig. 1.16.

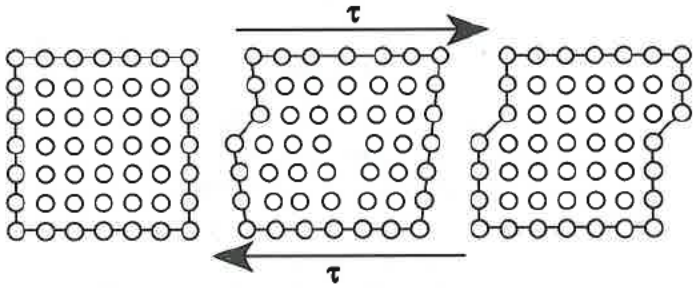


Fig. 1.16 Movement of dislocation under shearing stress τ, positive edge dislocation moving to the right.

Another type of dislocation is the **screw dislocation** that is shown for a simple cubic lattice in Fig. 1.17.

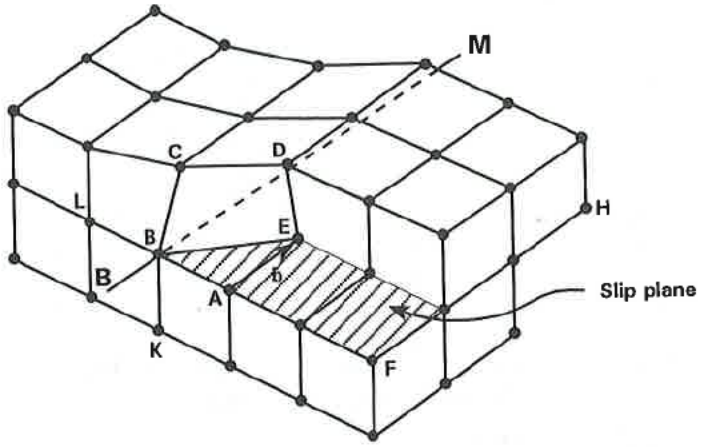


Fig. 1.17 Schematic representation of a screw dislocation in a simple cubic lattice.

It can be visualized in a thought experiment as follows: Suppose the crystal is cut across the plane BFHM and the upper part displaced in the direction of the vector b. The dislocation line is parallel to b. As one moves around the dislocation line along a path such as AKLCDE, one advances along BM by an amount equal to b for every turn; hence the term "screw dislocation" [1.12].

Plane Defects

As mentioned earlier, the most important type of plane defects is the stacking fault [10]. To illustrate a stacking fault, consider the normal stack of silicon atoms in the <111> direction (Fig. 1.18).

The sequence of atoms in the stack can be defined by choosing a reference layer and labelling the atoms in this layer as A-atoms. All atoms in other layers having identical crystallographic positions to those in the reference layer are also named A-atoms and the layers are called A-layers. Layers of atoms in other positions are named B-layers, C layers, and so on. In Fig. 1.18 the sequence of atoms in a stack is ABCABC... When this regular sequence of atoms in the stack is interrupted, a stacking fault is created. A stacking fault appears at the surface of the crystal.

Figure 1.19 shows a disrupted stack sequence. In Fig. 1.19a part of the C layer is missing. This results in a break in the stack sequence and is referred to as an **intrinsic stacking fault.** In Fig. 1.19b an extra A layer is present between a B and a C-layer. The fault created by the extra layer is called an **extrinsic stacking fault.** Figure 1.19c illustrates how a stacking fault propagates to the surface of the crystal.

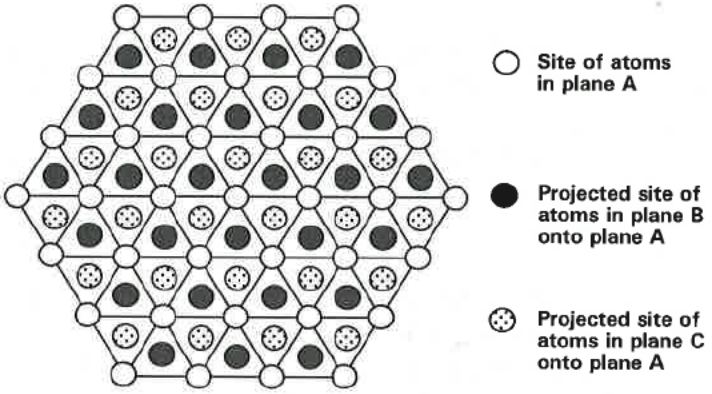


Fig. 1.18 Normal stack of atoms in silicon, viewed in the < 111 > direction.

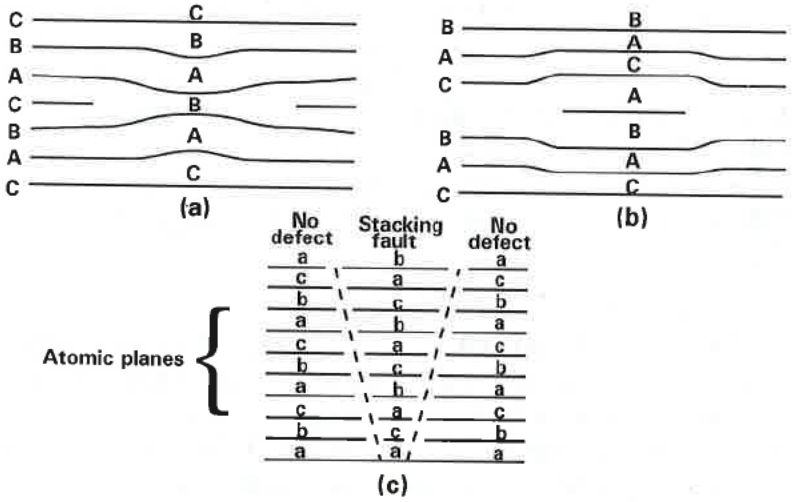


Fig. 1.19 Stacking fault in silicon. (a) Intrinsic stacking fault. (b) Extrinsic stacking fault. (c) Propagation of stacking fault.

When observed in an optical microscope, stacking faults appear as straight bands at the surface. They lie on (111) planes and intercept the surface along the <110> direction. They appear as equilateral triangles on the surface of (111) oriented silicon, or as squares on the surface of (100) silicon.

In most cases, stacking faults alone do not affect device properties. They can, however, act as nucleation centers for the precipitation of impurities which deteriorate device properties.

Volume Defects

Oxygen is one of the main impurities that is unintentionally introduced in silicon during crystal growth in silica crucibles. Its typical concentration in silicon varies from 10^{17} - $10^{18}\,cm^{-3}$. Oxygen becomes a major device yield detractor when present at high concentrations in silicon, creating dislocations and sites for heavy-metal precipitation. At concentrations above $10^{17}\,cm^{-3}$, it causes precipitates of silicon-oxygen complexes when the crystal is subjected to high temperatures. This is accompanied by the generation of mobile dislocations around the precipitates [13]. In an interstitial position, oxygen forms a silicon-oxygen bond which exhibits a strong infrared (IR) absorption band at 9.1 μm. This allows routine measurements of the oxygen content in silicon by infrared spectroscopy.

Along with oxygen, carbon is a major unintentionally introduced impurity in CZ or FZ crystals. It is found in concentrations between 10^{16} and $10^{17}cm^{-3}$. At high concentrations carbon can create precipitates and stacking faults during high temperature processing [14]. The effects of carbon are, however, not well understood. As with oxygen, IR spectroscopy is used to measure the concentration of carbon, which exhibits strong absorption at $\simeq 16.6\,\mu m$.

Process-Induced Defects

Defects can be introduced into the crystal intentionally and unintentionally. Dopants such as arsenic, phosphorus, antimony, and boron are intentionally introduced to locally change the conductivity of the crystal. Unintentional defects are introduced during crystal growth or during processing. The fabrication of silicon devices requires a certain number of high temperature processing steps. These steps can create unintentional defects, some in conjunction with existing defects in the starting material. Examples

of defects introduced during processing are dislocations and stacking faults caused by the misfit of impurities at high concentration; displacement of atoms by ion bombardment (Chap. 6); stress-induced deformations due to different thermal expansion coefficients of superimposed layers; and oxidation-induced stacking faults (Chap. 2).

Gettering

There is a favorable mechanism observed in the presence of oxygen at concentrations near $10^{17}\ cm^{-3}$. As discussed in the following section, the crystal is cut into thin slices, called **wafers,** used for device fabrication. When, prior to device processing, a silicon wafer is heated to $\simeq$ 1000 °C in N_2 or HCl atmosphere, most of the oxygen near the surface of the wafer is removed by the atmosphere. Deep in the "bulk" of the crystal, however, oxygen remains at high concentration and precipitates as complexes. The surface of the wafer - where most active devices are fabricated - becomes depleted of oxygen, while a region in the wafer several microns away from the surface becomes rich in defects. The defective region acts as a "sink" that attracts impurities such as heavy metals. As the wafer is heated, the defects are attracted to this sink and thus removed from the surface. This segregation mechanism is called **intrinsic gettering** [15]. The region which is depleted of oxygen is sometimes referred to as the **denuded zone.**

In addition to intrinsic gettering there are treatments which can be applied before or during device fabrication to remove defects and metallic impurities from the regions where devices are fabricated. Gettering can be achieved by intentionally damaging the back of the silicon wafer and then subjecting it to high temperature. The damaged region acts as a sink for impurities, such as heavy metals, which then diffuse from the surface to the back side and deposit there. A common method to create strain in the back side of the wafer is to mechanically damage it, or dope it heavily with impurities such as argon (Chap. 7) [16, 17].

1.3 Wafer Preparation

Typical wafers are prepared by grinding the silicon ingot to the desired diameter and then cutting it into single slices of thickness 0.5-1 mm, depending on the wafer diameter. For coarse wafer

alignment and future identification, a notch and one or more flats are ground along the length of the crystal before it is sliced. The notch and primary flat are used to position the wafer in the tool and to orient the design with respect to a specified crystallographic direction. The primary flat is typically located on a $(01\bar{1})$ surface and is used (with a secondary flat, when present) to quickly identify the type and crystal orientation of the wafer (Fig. 1.20).

The wafers are then lapped, polished, and cleaned to remove the damage caused by slicing. Wafer cleaning and processing is performed in a "clean-room" environment. A clean room is classified according to the number of particles per unit volume of air that are larger than or equal to a specified diameter. For example, a class 10 room has less than 350 particles per cubic meter that are larger than or equal to 0.3 μm in diameter. Clean rooms are discussed in more detail in Chap. 5.

The specifications for crystal diameter, type, resistivity, and orientation depend on the anticipated process sequence, the available manufacturing tools, and the required device characteristics. Typical crystal diameters range from 50 mm to 300 mm. For most applications, the wafer is oriented in the <100> or <111> direction.

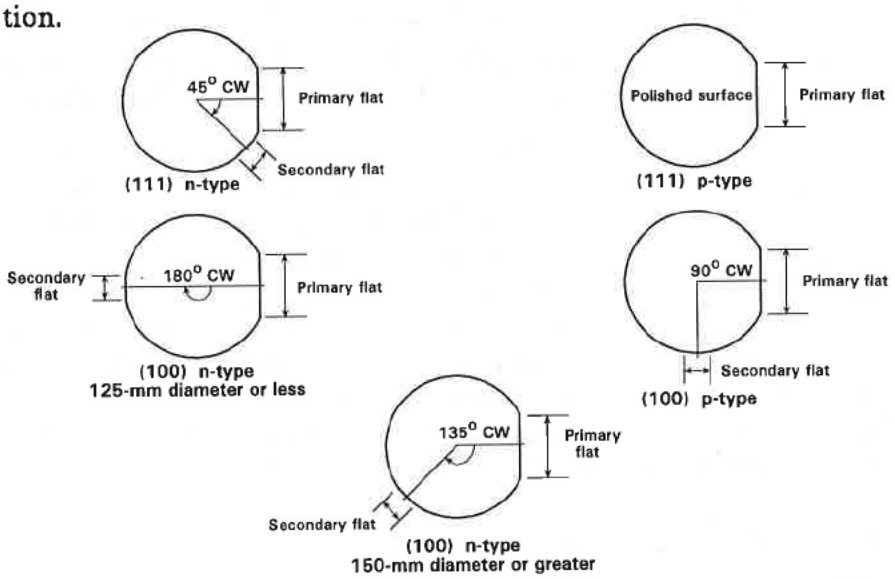


Fig. 1.20 Convention for silicon wafer identification. Source: Semiconductor Equipment and Materials Institute (SEMI) sta[illegible]

1.3.1 Wafer Type and Orientation

The crystal is usually doped p- or n-type while grown, depending on wafer specifications. Only a thin layer of the wafer, approximately 1-μm to 15-μm deep, is used to define the device structure. In most cases, the remainder of the wafer acts as a mechanical support.

Several process parameters and device characteristics are sensitive to wafer orientation. For example, the rate of epitaxial growth of silicon depends on its crystallographic orientation. Since the {111} planes have the smallest separation, silicon grows faster along a <111> direction than along a <110> or <100> direction. Also, since (111) planes have the highest density of atoms, the dissolution of silicon in an etching solution is slowest in the <111> direction. The rate of thermal oxidation and the diffusivity of impurities are also dependent on the crystal orientation. For example, the oxidation rate of silicon is largest in the <111> direction and smallest in the <100> direction.

Electronic traps created at the silicon surface increase the surface charge and alter device parameters. The density of these **interface traps** depends on the crystallographic orientation. It is highest in <111> oriented wafers and lowest in <100> oriented wafers [18]. This is one reason for choosing <100> oriented wafers for most device fabrication.

An important step in the manufacture of integrated circuits is dicing the wafer into rectangles called **chips** or **dies.** Typical dicing is performed with a saw that cuts through the wafer along lines that define identical chips (Fig. 1.21). In some cases, however, the chips are separated by initially scribing the wafer along lines and then cleaving the crystal. It is easier to cleave the wafer along (111) planes than in other crystallographic directions, because the tensile strength and modulus of elasticity are largest in the <111> direction (Table 1.1). In <100> oriented wafers, (111) planes intersect the surface at an angle of 54.74° and in <110> directions which are perpendicular to each other. Therefore, for best results, the wafer is cleaved in <110> directions (see problems 1.3 and 1.4 at the end of the chapter).

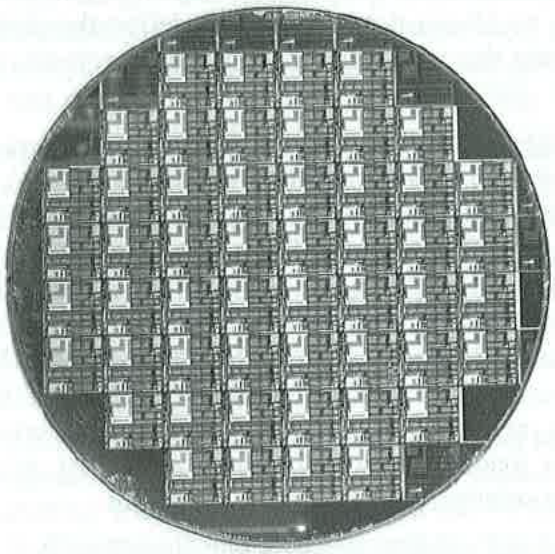


Fig. 1.21 Processed wafer with identical chips.

1.3.2 Axial and Radial Variations

Variations in the wafer properties (such as dopant concentration, defect density, scratches) cause variations in device and circuit properties within a chip and from chip to chip. These variations can be induced during crystal growth or wafer preparation. The properties of grown crystals vary axially (along the crystal) and radially from the center to the periphery of the crystal. Axial variations limit the number of wafers that fall within certain specifications. Therefore, wafers are grouped according to the section of the crystal from which they are sliced and those that fall outside the specifications are not used. Of greater importance is the radial variation in the wafer properties. Since processing cost is affected by the number of chips per wafer that pass final test specifications, it is cost effective to eliminate, before processing, those wafers that exhibit large variations in their properties.

1.4 Compound Semiconductors

Many important applications, particularly in optoelectronics, are not possible with silicon crystals. Typical examples are light emitting diodes (LEDs), semiconductor lasers, and ultra-high-speed devices. These devices operate best with certain compound semiconductors [19]. Differences in light emission and carrier transport between elemental and compound semiconductors are explained when discussing energy band diagrams of the different types of semiconductors.

The most technologically advanced and widely used compound semiconductor is gallium-arsenide (GaAs). This is a binary compound because it consists of only two different elements - gallium from column III and arsenic from column V of the periodic table. Other binary III-V compound semiconductors of interest are GaP, InP and InSb. Examples of tertiary compounds are AlGaAs and GaAsP. For special applications II-VI compound semiconductors such as CdTe and ZnS can also be used. In this section, however, we only discuss the properties of GaAs crystals.

Gallium has the electronic structure $4s^2 4p^1$, while arsenic has the structure $4s^2 4p^3$. Two silicon-like atoms can be produced from Ga and As by transferring one of the p-electrons from As to an empty p-level in Ga, so that each atom then has the $4s^2 4p^2$ configuration, similar to that of a group IV atom. The bond between nearest neighbors is thus partially polar, since gallium is left negative and arsenic positive. It is essentially a covalent bond, however, leading to a tetrahedral bond configuration similar to that of silicon. This is because when the bond is formed, the reduction of energy more than compensates for the energy necessary to transfer the electron from As to Ga. Both gallium-arsenide and silicon crystals belong to the cubic lattice family. Compound semiconductor crystals are sometimes said to belong to the **zincblende** structure, which is similar to the diamond structure with one important difference (Fig. 1.22): comparing silicon to gallium-arsenide, for example, we find identical atoms in the silicon crystal (diamond), while in gallium-arsenide (zincblende) each gallium atom is surrounded by four arsenic atoms and vice versa.

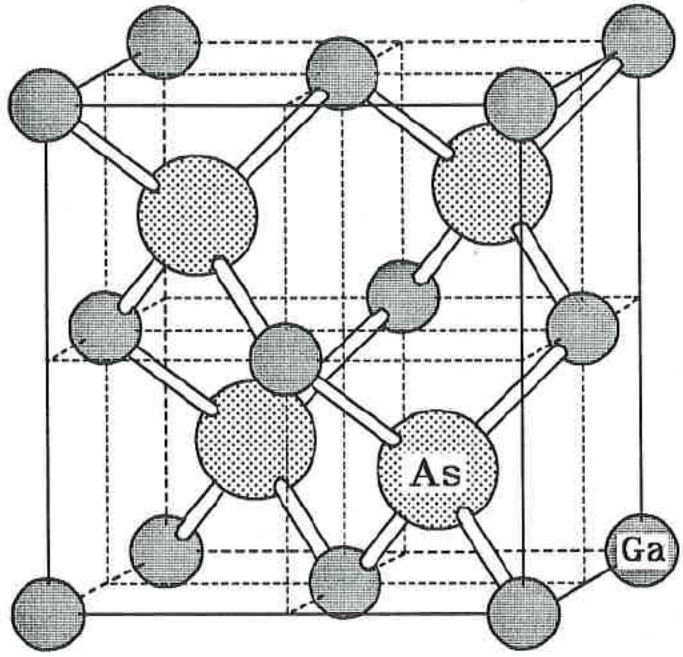


Fig. 1.22 Zincblende structure, illustrated for gallium-arsenide.

The GaAs structure consists of two interpenetrating face-centered-cubic (fcc) sublattices, each containing atoms of only one type. One atom of the second sublattice is located at one fourth of the distance along a major diagonal of the first sublattice (Fig. 1.23). Gallium-arsenide (100) surfaces contain either only gallium or only arsenic atoms (Fig. 1.24). In either case, each atom has two bonds to atoms in the lower plane. This leaves two dangling bonds per atom at the surface. The preferred cleavage in GaAs is along (110) planes. These intercept $<100>$ surfaces at right angles and are orthogonal. When cleaved in these directions the crystal forms parallel plates, which is essential for the preparation of resonant cavities for lasers.

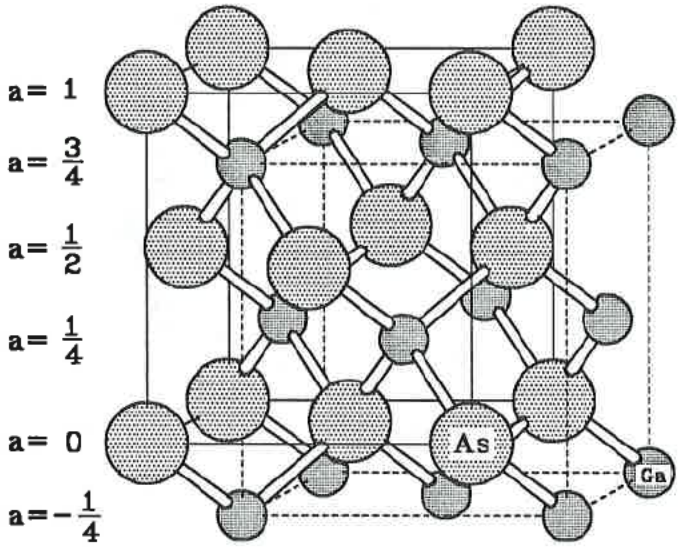


Fig. 1.23 Representation of the gallium-arsenide structure as two interpenetrating face-centered-cubic sublattices.

While all (111) planes are identical in silicon, there are two types of (111) planes in GaAs, the (111)Ga and the (111)As plane (Fig. 1.25). All three valence electrons of gallium atoms in the (111)Ga planes are bonded, but only three of the five valence electrons of arsenic atoms in the (111)As planes are bonded. Therefore, As(111) faces exhibit the highest electronic activity since two of five electrons of each arsenic atom are "free". The properties of the two surfaces are thus very different. For example, etching proceeds more rapidly and results in a smoother surface on (111)As than on (111)Ga surfaces. Some important properties of gallium-arsenide are given in Table 1.4.

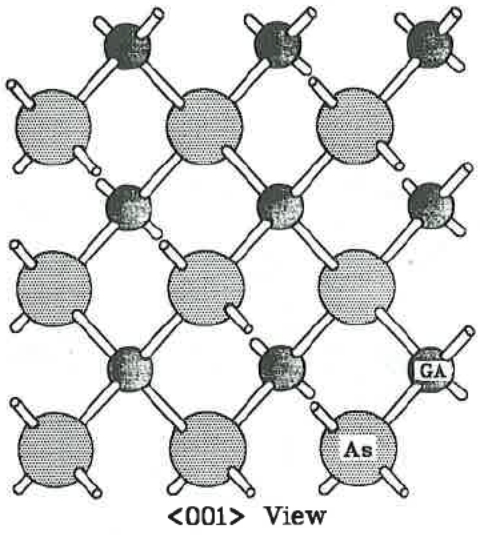


Fig. 1.24 Gallium-arsenide crystal viewed in the < 001 > direction.

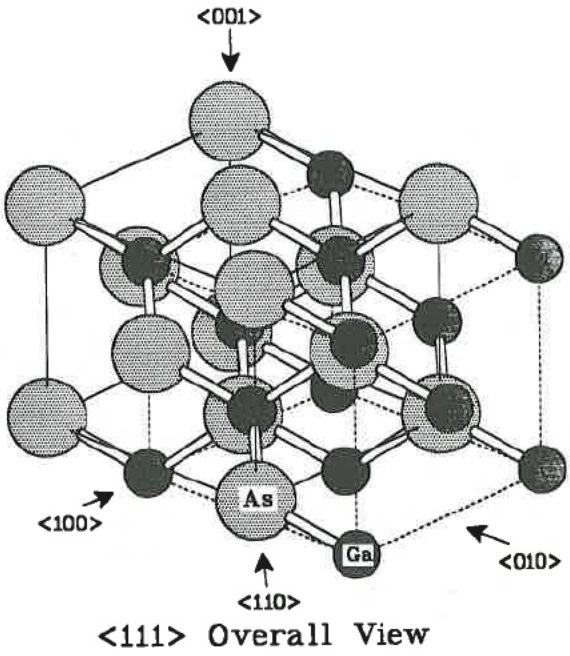


Fig. 1.25 Gallium-arsenide crystal viewed in the < 111 > direction

Table 1.4 Some important properties of gallium-arsenide at 25 °C

Symbol	GaAs
Molecular weight	144.63 g/Mole
Crystal	Zincblende
Lattice constant	5.6533 Å
Arsenic radius	1.18 Å
Gallium radius	1.26 Å
Atomic density	$4.42x10^{22}$ atoms/cm^3
Density	5.3176 g/cm^3
Melting point	1238 °C
Specific heat	0.35 J/g.K
Linear thermal expansion coefficient	$6.86x10^{-6}$ K^{-1}
Thermal conductivity	0.46 W/cm.K
Relative dielectric constant	13.1
Index of refraction	3.3
Energy gap	1.424
Intrinsic carrier concentration	$1.70x10^{6}$cm^{-3}
Electron affinity	4.07 eV
Conduction band density of states	$4.7x10^{17}$cm^{-3}
Valence band density of states	$7.0x10^{18}$cm^{-3}
Electron mobility	8500 $cm^2/V.s$
Hole mobility	360 $cm^2/V.s$
Optical phonon energy	0.035 eV
Donors (As-site)	S, Se, Sn, Te
Acceptors (Ga-site)	Zn, Be, Mg, Cd

1.4.1 Crystal Growth

The most common method for preparing GaAs wafers for IC applications is the **Liquid Encapsulated Czochralski (LEC)** technique. Another method of crystal growing, called the **horizontal Bridgman** method, is used primarily to prepare GaAs material for optoelectronic applications. As with silicon, the starting material in the LEC technique is polycrystalline GaAs. It is molten in either a quartz, or boron nitride crucible [20, 21]. In some cases, arsenic and gallium are added separately to form the melt [22]. A cap layer of inert liquid, about 2-cm thick, covers the melt to avoid evaporation of As and the decomposition of GaAs because of the high volatility of arsenic (Fig. 1.26). Boron trioxide (B_2O_3) is the

most commonly used material for the cap. It floats on the GaAs molten surface, is inert, and is impervious to arsenic diffusion, (provided that the argon or nitrogen ambient pressure is maintained at $\simeq$ 2 atm).

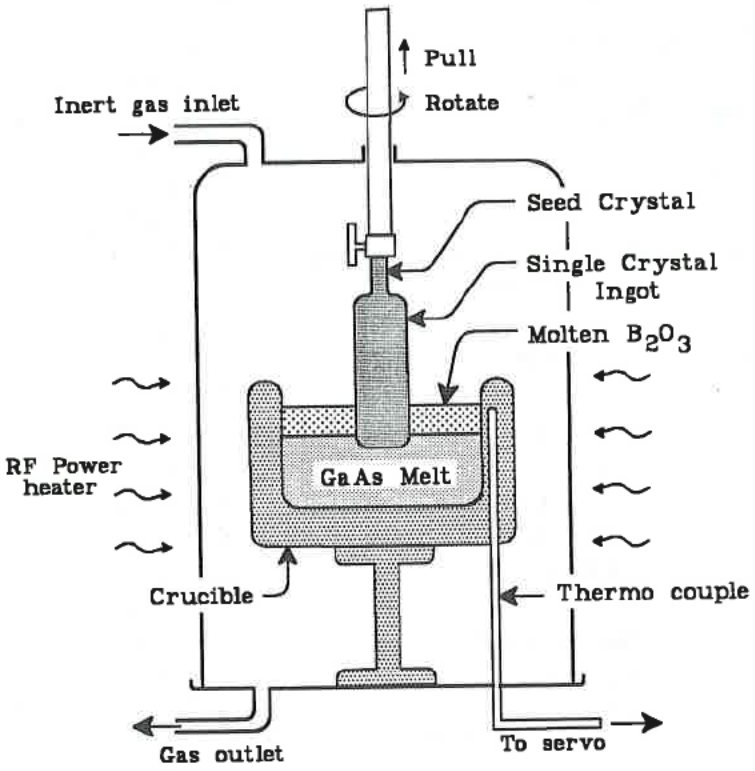


Fig. 1.26 Principle of the Liquid Encapsulated Czochralski crystal growth method.

A seed having the desired crystallographic orientation is lowered into the GaAs melt through the transparent B_2O_3 layer. The seed is cut to allow growth in the <111> or <100> direction. The seed and crucible are rotated in opposite directions to improve crystal uniformity.

The growth rate in the <111> direction is only 0.25-1.50 cm/h. It is limited mainly because of the small thermal conductivity of GaAs (Table 1.4). Growth in the <100> is slower.

The dislocation density in semi-insulating GaAs substrates is higher than in silicon and is of great concern. While large diameter (10-20 cm) silicon crystals can be grown essentially dislocation-free, only very small diameter (less than 1.5 cm) GaAs crystals have been reported with comparable structural perfection [23].

The major cause for dislocation formation in semiconductors is stress induced by temperature gradients during growth and cooling. Under the same growth conditions, gallium-arsenide is more susceptible to dislocation formation for two reasons. First, the bonds in GaAs are not as strong as in Si, so dislocations form more easily. Second, the thermal conductivity of silicon is about three-fold that of GaAs (Tables 1.1, 1.4). Therefore, it is more difficult to reduce thermal gradients in GaAs crystals.

The horizontal Bridgman method consists of loading the material into a long and narrow container, typically made of fused silica of circular cross-section. The container is moved horizontally from a zone of temperature slightly above the material's melting point to a zone of temperature slightly below the melting point. For single-crystal growth, a seed of the desired orientation is placed at one end of the container and partially kept in the zone below the melting point. As the container is slowly moved, the melt freezes onto the seed as a single crystal.

1.4.2 Impurities and Crystal Doping

Oxygen and carbon are unavoidable contaminants in GaAs crystals. As a substitutional impurity, oxygen forms a deep donor level which contributes to trapping charge in the bulk of the substrate and reduces its conductivity. Oxygen has a solubility limit of $\simeq 10^{17}\,cm^{-3}$ in GaAs. Carbon in GaAs creates a shallow acceptor level. It is found in LEC crystals in concentrations of $\simeq 2x10^{15} - 10^{16} cm^{-3}$, depending on the crucible used. The effects of shallow and deep trap levels on conductivity are discussed in the chapters to follow.

Very high resistivity GaAs substrates (termed **semi-insulating,** or SI) are of great importance for the isolation of high speed devices in integrated circuits. Using oxygen as a dopant for making semi-insulating substrates is not practical, since oxygen is

highly mobile at device processing temperatures. In some special cases, after all high temperature cycles have been completed, oxygen is introduced locally for device isolation. The electrical properties of undoped LEC GaAs crystals depend strongly on the melt stoichiometry. It is found that the crystal is p-type below a critical arsenic concentration and semi-insulating above it. The semi-insulating property is associated with compensating effects of a deep donor level (referred to as **EL2**) and shallow carbon acceptors. EL2 levels are created when arsenic atoms occupy gallium positions [24]. Carbon is one of the principal impurities in LEC crystals. It is found at concentrations $2x10^{15}\,cm^{-3}$ - $10^{16}\,cm^{-3}$. In some cases, chromium (Cr) is intentionally added to the substrate to create a deep acceptor level and reduce conductivity, leading to SI GaAs. The nature and placement of the Cr level in the GaAs bandgap are, however, not well understood.

Table 1.5 Dopants in gallium-arsenide.

Dopant	Segregation coefficient	Dopant type
Sulfur	0.3	n
Tellurium	0.06	n
Tin	0.08	n
Selenium	0.3	n
Carbon	0.8	n/p
Germanium	0.01	n/p
Silicon	0.14	n/p
Beryllium	--	p
Magnesium	0.1	p
Zinc	0.4	p
Chromium	0.0006	SI

Typical dopants are introduced into GaAs wafers by ion implantation (Chap. 6). Their type and segregation coefficients are given in Table 1.5. Sulfur, selenium, tellurium and tin are shallow donors when they occupy arsenic sites. Beryllium, magnesium and zinc are acceptors when they occupy gallium sites. Carbon, germanium and silicon can be donors or acceptors, depending on whether they occupy arsenic or gallium sites. This can be influenced by the doping conditions which are not detailed here.

PROBLEMS

1.1 Assume a hard sphere model and find the ratio of volume occupied to volume available in the following crystals:

a) Simple cubic

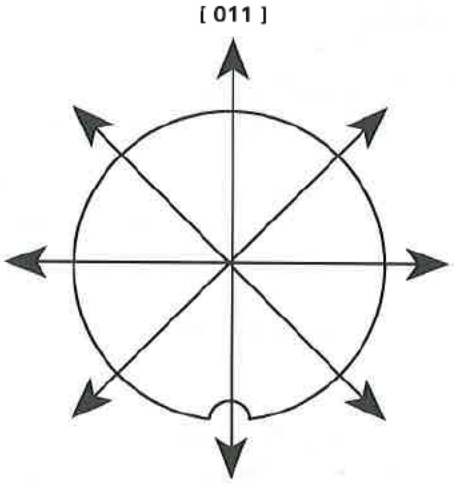
b) Body-centered cubic

c) Face-centered cubic

d) Diamond

1.2 Show that the angle between the tetrahedral bonds of silicon is 109 ° 28′.

1.3 The plane of the paper is the (100) plane of a silicon wafer. Define the seven remaining directions on the sketch below.



1.4 In problem 1.3 what is the angle between a (111) plane and the plane of the paper?

1.5 In silicon, the cube edge a = 5.43 Å. Assume a hard sphere model and:

a) Calculate the radius of a silicon atom.

b) Define the coordinates of voids in the cube.

c) Calculate the radius of the largest atom which can fit in a void.

d) Calculate the shortest distance between silicon atoms.

e) Determine the density of silicon atoms in atoms/cm^3.

f) Use Avogadro's number to find the density of silicon.

1.6 Find the number of atoms per square centimeter in a silicon crystal in:

a) (100) plane

b) (111) plane

1.7 A Czochralski grown crystal is doped with boron. Why is the boron concentration larger at the tail-end of the crystal than at the seed-end?

Do you expect this axial variation to be larger or smaller for arsenic? Why?

Suggest a method to improve the axial uniformity of boron in the floating-zone technique.

1.8 Assume the energy of formation of a Frenkel-type defect to be 1.1 eV and estimate the defect density at 25 °C and 1000 °C.

1.9 How many dies of area 2 cm^2 can be placed on a 200-mm diameter wafer? Explain your assumptions on die-shape and unused wafer perimeter.

1.10 Why is the impurity concentration larger in the center of the wafer than at its perimeter?

1.11 A 1 mm thick silicon wafer having a diameter of 20 cm contains 6.77 mg boron ($_{11}B^5$) uniformly distributed in substitutional sites. Find:

(a) The boron concentration in atoms/cm^3.

(b) The average distance between boron atoms.

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