Ian Crayford

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Professional Experience

Summary

20+ years' experience in broadband wired and wireless communications.
Recognized industry expert in all aspects of Ethernet LANs, including system hardware/software definition, architecture and implementation issues and tradeoffs for NIC, repeater, bridge, switch and router devices.
Intimately familiar with 802.3 standards issues for 10Mb/s, 100Mb/s, 1Gb/s and 10 Gb/s.
Familiarity with wireless networks including 802.11 and BLE, network protocols (TCP/IP, SNMP), L2-L4 switching, deep packet/statefull inspection, management agents, MIBs, and VLAN tagging/administration.
Understanding of software issues including embedded RTOS, drivers and upper layer protocols.
Familiar with mainstream microprocessors, PC buses, and high speed I/O.
Proven expertise in specifying, architecting, and delivering complex communication SoCs including running multidisciplinary teams.
Expertise in semiconductor development, fabrication and manufacturing processes.
Proven track record in identifying new markets and products, establishing key customer and co-development relationships, and executing complex engineering and marketing launch plans.
Over 40 US Patents granted in the area of LAN communications and related technology.

Sep '12 – Present

Smartbotics, Inc. – CTO and Co-Founder of start-up company focused on wireless and smart phone app technology that can be applied to home and commercial automation products.

Nov '02 – Present

Network Generation LLC – Founder of consultancy focused on communications system and semiconductor businesses, primarily assisting start-up companies and VCs. Services include engineering/strategic marketing development/evaluation, architectural design/review, due-diligence, customer validation, engineering analysis, patent protection, etc..
Past customers include AMD, Azanda Networks (acquired by Cortina), Broadcom, Broadway Networks (acquired by Finisar), Enphase Energy, Falchion Enteprises, Fulcrum Microsystems (acquired by Intel), FireEar, Halo Electronics, Intel, Sandburst (acquired by Broadcom), Terari (acquired by LSI), Teranetics (acquired by PLX Technology), Wilson Sonsini, etc. Currently assisting several start-ups in areas such as electric vehicles, green technologies, and commercial and residential lighting, automation, monitoring and control.

Apr '98 – Nov '02:

Broadcom Corp., San Jose, CA. Director Business Development. Responsible for identification of new and emerging markets in broadband communications, focused on LAN, WAN and wireless opportunities. Led technical due-diligence teams on a number of prospective and completed acquisitions and investments including Maverick Networks (L2/L3 Stackable Switches), BlueSteel Networks (Security Processors), SiByte (MIPS Processors), Newport Communications (SONet PHYs and Framers), TiMetra Networks (Switch Fabric). Used as corporate resource to help drive converging broadband semiconductor opportunities.

Director – LAN Switching Technology. Responsible for SOHO/ROBO-switch initial feature set, architecture definition, and delivery of early family of devices and support collateral. By year end '02, multiple devices in family shipped over 200 million ports of 10/100/1G Ethernet and accounted for a revenue base in excess of $50M annually.

Apr '97 – Apr –'98:

Bay Networks Inc., Santa Clara, CA. Director, Switch Architecture and Strategy, Multi-LAN Switching Business Unit. Responsible for definition and execution of next generation modular switch products, for heterogeneous enterprise LANs (ATM, Ethernet and Token Ring). Primary business unit engineering interface to customers, sales force, other Bay business units, and Bay Architecture Labs (BAL).

Mar '88 - Apr '97:

Advanced Micro Devices Inc., Sunnyvale, CA. AMD Fellow (March '93), Architecture and Advanced Development group. Responsible for identification and evaluation of new technologies for future high volume connectivity market place. Develop architectural definition and feasibility analysis for silicon and system implementations. Identify and champion product and technology concepts and promote adoption by appropriate business units. Technical focal point for 802.3 Standards and related developments such as 100BASE-T (Chaired Link Signaling Sub-Group), Full Duplex/Flow Control, Switched Ethernet, and Gigabit Ethernet.

Manager - System Engineering & Network Development. Identification and definition of new products, primarily for the Ethernet market place. Planned and executed a variety of projects for chip and system level products. Responsibilities included identifying key technology and market trends, assessing business opportunity, and defining cost effective products. Manager of a team of 10-15 engineers, responsible for support of existing and development of new chip and system level products. Significant customer interaction, including detailed negotiations for joint development projects with key strategic customers. Represented AMD at IEEE 802.3 throughout multiple standards developments. Program Manager for initial 10BASE-T/Ethernet products in the Repeater, NIC and Switch markets.

Oct. '82 - Mar. '88: G.P.Elliott Electronic Systems Ltd., Merton, London, U.K.. Development Engineer/Project Manager. Design and development of fault tolerant computer and communications equipment for high reliability control and shutdown systems deployed in hazardous environments. Developed 802.4 based Token Bus network. 2 year secondment to G.E. (Charlottesville, VA), to develop fault tolerant "intelligent I/O" industrial control network.

Sep. '81 - Oct. '82: Babcock-Bristol Ltd., Croydon, Surrey, U.K.. Systems Engineer. Hardware and software design for real time process control and data acquisition systems for power station, boiler control and water treatment plant.

Sep. '75 - Aug. '81: Foxboro Yoxall Ltd., Redhill, Surrey, U.K.. Student Engineer/Service Engineer. Design of process control instrumentation equipment. Basic electrical, electronic, pneumatic and mechanical engineering design. 4 year sponsored degree program.

Education: 1977-1981: Kingston Polytechnic, Kingston, Surrey, UK.
BSc (Hons) Degree in Electrical and Electronic Engineering.

Miscellaneous: Executive and/or Advisory Board affiliations: Dhaani Systems, Formative Ventures, Falchion Enterprises, Fulcrum Microsystems, Pond Ventures, Smartbotics, WANdisco.

Publications & Papers:

Fault Tolerant Control Systems, 16th Annual International Programmable Controllers Conference & Exposition, April 7-9, 1987, Detroit, Michigan.

10BASE-T in the Office, Wescon, November 19-21, 1991, San Francisco, California.

Integrating Managed Hub and File Server Technologies, Silicon Valley Networking Conference, April 27-29 1992, Santa Clara, California.

Lo Standard 10BASE-T nei PC - ELECTRONICA OGGI (Italy), July 1992 (translated from "10BASE-T in the Office").

802.3/Ethernet - The Handbook of International Connectivity Standards (Chapter 11), Edited by Gary R. McClain, Published by Van Nostrand Reinhold (1992), ISBN 0-442-30851-5.

The Standards Jigsaw - How the IEEE Pieces fit the Puzzle, LANFair, October 21, 1993, Denver, Colorado.

Accelerating Ethernet: Options and Implications, WinHEC 94, February 23, 1994, San Francisco, California; WinHEC 94 Asia, June 30, 1994, Taipei, Taiwan.

The IEEE 802.3 and Ethernet Standards - Encyclopedia of Telecommunications (Volume 9), Editor-in-Chief Fritz E. Froehlich, Co-Editor Allen Kent, Published by Marcel Dekker (1995), ISBN 0-8247-2902.

Ethernet Upgrade Options, WinHEC '95, March 20, 1995, San Francisco, California; WinHEC 95 Asia, May 23, 1995, Taipei, Taiwan.

Accelerating Ethernet: Options and Implications, Northcon/95, October 11, 1995, Portland, Oregon.

Fast Ethernet Gets Plug-and-Play, Wescon/95, November 7, 1995, San Francisco, California.

Fast Ethernet Alternatives for Client-Server Computing, Wescon/95, November 7, 1995, San Francisco, California.

Gigabit Ethernet – Migrating to High Bandwidth LANs, Jayant Kadambi, Ian Crayford, Mohan Kalkunte, Published by Prentice Hall (1998), ISBN 0-13-913286.

Patents:

47 US Patents granted (and foreign equivalents), several applications in prosecution.

US Patent: 5,164,960	Issued: Feb 15, 1990	Medium Attachment Unit for Use With Twisted Pair Local Area Network
US Patent: 5,257,287	Issued: Oct 26, 1993	Automatic Polarity Detection and Correction Method and Apparatus

US Patent: 5,305,321	Issued: Apr 19, 1994	Ethernet Media Access Controller With External Address Detection Interface and Associated Method
US Patent: 5,327,465	Issued: Jul 5, 1994	Method and Apparatus for Squelch Circuit In Network Communication
US Patent: 5,404,544	Issued: Apr 4, 1995	System for Periodically Transmitting Signals To/From Sleeping Node Identifying Its Existence to a Network and Awakening the Sleeping Node Responding to a Received Instruction
US Patent: 5,414,694	Issued: May 9, 1995	Address Tracking Over Repeater Based Networks
US Patent: 5,432,775	Issued: Jul 11, 1995	Auto-Negotiation System for a Communications Network
US Patent: 5,467,369	Issued: Nov 14, 1995	AUI to Twisted Pair Loopback
US Patent: 5,539,737	Issued: Jul 23, 1996	Programmable Disrupt of Multicast Packets for Secure Networks
US Patent: 5,550,803	Issued: Aug 27, 1996	Method and System for Increasing Network Information Carried in a Data Packet Via Packet Tagging
US Patent: 5,581,559	Issued: Dec 3, 1996	Inverse Packet Disrupt for Secure Networks
US Patent: 5,592,486	Issued: Jan 7, 1997	A System and Method for Efficiently Monitoring Information in a Network Having a Plurality of Repeaters
US Patent: 5,610,903	Issued: Mar 11, 1997	Auto-Negotiation System for a Communications Network
US Patent: 5,640,393	Issued: Jun 17, 1997	Multiple Address Security Architecture
US Patent: 5,654,985	Issued: Aug 5, 1997	Address Tracking Over Repeater Based Networks
US Patent: 5,673,254	Issued: Sep 30, 1997	Enhancements to 802.3 Media Access Control and Associated Signaling Schemes for Ethernet Switching
US Patent: 5,754,525	Issued: May 19, 1998	Programmable Delay of Disrupt for Secure Networks
US Patent: 5,850,515	Issued: Dec 15, 1998	Intrusion Control in Repeater Based Networks
US Patent: 5,859,837	Issued: Jan 12, 1999	Flow Control Method and Apparatus for Ethernet Packet Switched Hub
US Patent: 5,890,100	Issued: Mar 30, 1999	Chip Temperature Monitor Using Delay Lines
US Patent: 5,940,392	Issued: Aug 17, 1999	Programmable Address Mapping Matrix for Secure Networks
US Patent: 5,943,206	Issued: Aug 24, 1999	Chip Temperature Protection Using Delay Lines
US Patent: 5,978,853	Issued: Nov 2, 1999	Address Administration for 100BASE-T PHY Devices
US Patent: 6,016,308	Issued: Jan 18, 2000	Method and System for Increasing Network Information Carried in a Data Packet via Packet Tagging
US Patent: 6,078,627	Issued: Jun 20, 2000	Circuit and Method for Multilevel Signal Decoding, Descrambling, and Error Detection
US Patent: 6,084,878	Issued: Jul 4, 2000	External Rules Checker Interface
US Patent: 6,091,348	Issued: Jul 18, 2000	Circuit and Method for on-the-fly Bit Detection and Substitution
US Patent: 6,122,669	Issued: Sep 19, 2000	Method and Apparatus for Auto-incrementing Through Table and Updating Single Register in Memory
US Patent: 6,128,654	Issued: Oct 3, 2000	Method and Apparatus for Transmitting Multiple Copies by Replicating Data Identifiers
US Patent: 6,151,316	Issued: Nov 21, 2000	Apparatus and Method for Synthesizing Management Packets for Transmission Between a Network Switch and a Host Controller
US Patent: 6,167,054	Issued: Dec 26, 2000	Method and Apparatus Providing Programmable Thresholds for Full-Duplex Flow Control in a Network Switch
US Patent: 6,192,028	Issued: Feb 20, 2001	Method and Apparatus Providing Programmable Thresholds for Half-Duplex Flow Control in a Network Switch
US Patent: 6,255,969	Issued: Jul 3, 2001	Circuit and Method for High Speed Bit Stream Capture Using a Digital Delay Line
US Patent: 6,269,098	Issued: Jul 31, 2001	Method and Apparatus for Scaling Number of Virtual LANs in a Switch Using an Indexing Scheme

US Patent 6,487,212	Issued: Nov 26, 2002	Queuing Structure and Method for Prioritization of Frames in a Network Switch
US Patent 6, 556.589	Issued: Apr 29, 2003	Network Transceiver for Steering Network Data to Selected Paths Based on Determined Link Speed
US Patent 6,704,296	Issued: Mar 9, 2004	Optimized MII for 802.3u (100BASE-T) Fast Ethernet PHYs
US Patent 6,885,657	Issued: Apr 26, 2005	Network Telephony System
US Patent 6,970,419	Issued: Nov 29, 2005	Method and Apparatus for Preserving Frame Ordering Across Aggregated Links Between Source and Destination Nodes
US Patent 6,970,420	Issued: Nov 29, 2005	Method and Apparatus for Preserving Frame Ordering Across Aggregated Links Supporting a Plurality of Quality of Service Levels
US Patent 6,973,031	Issued: Dec 6, 2005	Method and Apparatus for Preserving Frame Ordering Across Aggregated Links Supporting a Plurality of Quality of Transmission Rates
US Patent 6,977,892	Issued: Dec 20, 2005	Method and Apparatus for Preserving Flow Order Across Links of a Multi Link Trunk
US Patent 7,457,857	Issued: Nov 25, 2008	Method and Apparatus for a Network Hub to Diagnose Network Operation and Broadcast Information to a Remote Host or Monitoring Device
US Patent 7,936,744	Issued: May 3, 2011	Network Telephony System
US Patent 8,051,160	Issued: Nov 1, 2011	Method and Apparatus for a Network Hub to Diagnose Network Operation and Broadcast Information to a Remote Host or Monitoring Device
US Patent 8,619,758	Issued: Dec 31, 2013	Network Telephony System
US Patent 9,019,957	Issued: Apr 28, 2015	Network Telephony System