Recognized as an
American National Standard (ANSI)

IEEE Std 802.3u-1995
(Supplement to ISO/IEC 8802-3: 1993
[ANSI/IEEE Std 802.3, 1993 Edition])

IEEE Standards for Local and Metropolitan Area Networks:

Supplement to Carrier Sense Multiple Access with Collision Detection (CSMA/CD) Access Method and Physical Layer Specifications

Media Access Control (MAC) Parameters, Physical Layer, Medium Attachment Units, and Repeater for 100 Mb/s Operation, Type 100BASE-T (Clauses 21–30)

Sponsor

LAN MAN Standards Committee
of the
IEEE Computer Society

Approved 14 June 1995
IEEE Standards Board

Approved 4 April 1996
American National Standards Institute

2nd Printing, Corrected Edition

Abstract: The ISO/IEC CSMA/CD Media Access Control (MAC) is given an additional set of parameters for 100 Mb/s operation. A repeater and added Physical Layers, known collectively as 100BASE-T, as well as significant additional supporting material for a Media Independent Interface (MII), management, and automatic configuration, are specified. This includes 100BASE-T4, which uses four pairs of Category 3, 4, or 5 generic twisted, balanced cable; 100BASE-TX, which uses two pairs of Category 5 balanced cable or 150 Ω shielded balanced cable; and 100BASE-FX, which uses two multi-mode fibers. Fibre Distributed Data Interface (FDDI) media interface specifications are referenced to provide the 100BASE-TX and 100BASE-FX physical signaling channels, defined under the subcategory 100BASE-X.
Keywords: 100BASE-FX, 100BASE-T, 100BASE-T4, 100BASE-TX, 100BASE-X, Auto-Negotiation, Fast Ethernet, management, Media Independent Interface (MII), repeater

---

The Institute of Electrical and Electronics Engineers, Inc.
345 East 47th Street, New York, NY 10017-2394, USA

ISBN 1-55937-542-6

IEEE Standards documents are developed within the Technical Committees of the IEEE Societies and the Standards Coordinating Committees of the IEEE Standards Board. Members of the committees serve voluntarily and without compensation. They are not necessarily members of the Institute. The standards developed within IEEE represent a consensus of the broad expertise on the subject within the Institute as well as those activities outside of IEEE that have expressed an interest in participating in the development of the standard.

Use of an IEEE Standard is wholly voluntary. The existence of an IEEE Standard does not imply that there are no other ways to produce, test, measure, purchase, market, or provide other goods and services related to the scope of the IEEE Standard. Furthermore, the viewpoint expressed at the time a standard is approved and issued is subject to change brought about through developments in the state of the art and comments received from users of the standard. Every IEEE Standard is subjected to review at least every five years for revision or reaffirmation. When a document is more than five years old and has not been reaffirmed, it is reasonable to conclude that its contents, although still of some value, do not wholly reflect the present state of the art. Users are cautioned to check to determine that they have the latest edition of any IEEE Standard.

Comments for revision of IEEE Standards are welcome from any interested party, regardless of membership affiliation with IEEE. Suggestions for changes in documents should be in the form of a proposed change of text, together with appropriate supporting comments.

Interpretations: Occasionally questions may arise regarding the meaning of portions of standards as they relate to specific applications. When the need for interpretations is brought to the attention of IEEE, the Institute will initiate action to prepare appropriate responses. Since IEEE Standards represent a consensus of all concerned interests, it is important to ensure that any interpretation has also received the concurrence of a balance of interests. For this reason IEEE and the members of its technical committees are not able to provide an instant response to interpretation requests except in those cases where the matter has previously received formal consideration.

Comments on standards and requests for interpretations should be addressed to:

Secretary, IEEE Standards Board
445 Hoes Lane
P.O. Box 1331
Piscataway, NJ 08855-1331
USA

Note: Attention is called to the possibility that implementation of this standard may require use of subject matter covered by patent rights. By publication of this standard, no position is taken with respect to the existence or validity of any patent rights in connection therewith. The IEEE shall not be responsible for identifying all patents for which a license may be required by an IEEE standard or for conducting inquiries into the legal validity or scope of those patents that are brought to its attention.

Corrected Edition, June 1996

The following corrections have been made to this edition:

Page 23: The designation of reference [A5] has been corrected to ANSI/EIA/TIA 526-14-1990. *[Note that further updates to annex A can be found in ISO/IEC 8802-3: 1996.]*

Page 32: In the last line of text on the page, the word "fourth" has been corrected to "sixth."

Page 174: In figure 24-11, the "BAD SSD" box text has been corrected. "RXD<3.0> ⇐ 1110" now reads "RXD<3:0> ⇐ 1110".

Page 234: The page, containing subclauses 27.7.4.11 and 27.7.4.12, was inadvertently omitted from the first printing. It is now included.

Page 286: Under list item a), notes 2 and 3 were misnumbered and have been corrected. Also, references in notes 2 and 3 to table 29-2 have been corrected to table 29-3.

Page 301: In table 30-1d, "aAutoNegAdvertisedTechnologyAbilit" has been corrected to "aAutoNegAdvertisedTechnologyAbility".

Page 312: In subclause 30.4.1.1.2, the reference to 20.2.2.3 for "other" has been corrected to 30.2.5.

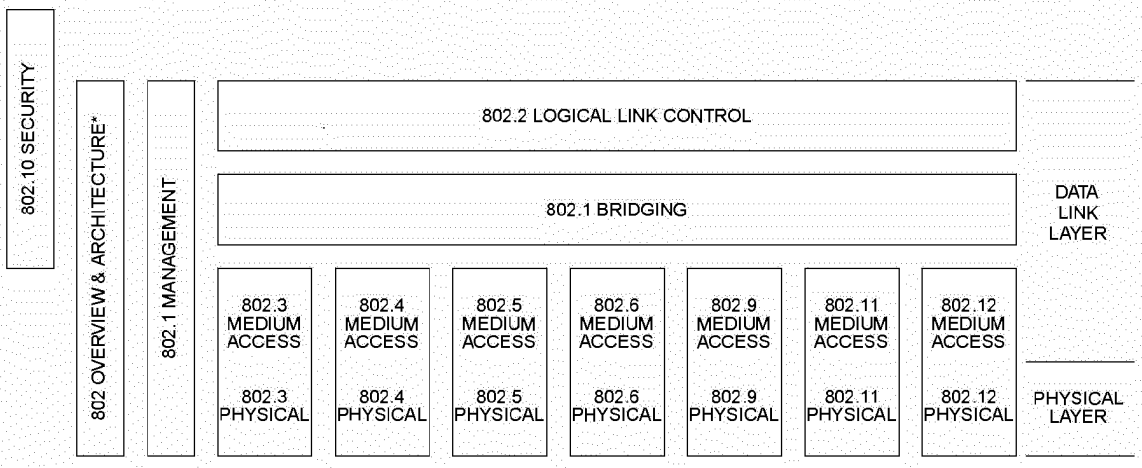
Page 323: In subclause 30.5.1.1.2, the reference to 20.2.2.3 for "other" has been corrected to 30.2.5.

Note that additional corrections are under consideration, and that some reference documents have been updated. These will be included in future maintenance documents.

Introduction

(This introduction is not part of IEEE Std 802.3u-1995.)

This standard is part of a family of standards for local and metropolitan area networks. The relationship between the standard and other members of the family is shown below. (The numbers in the figure refer to IEEE standard numbers.)



* Formerly IEEE Std 802.1A.

This family of standards deals with the Physical and Data Link layers as defined by the International Organization for Standardization (ISO) Open Systems Interconnection Basic Reference Model (ISO 7498 : 1984). The access standards define several types of medium access technologies and associated physical media, each appropriate for particular applications or system objectives. Other types are under investigation.

The standards defining the technologies noted above are as follows:

- IEEE Std 802[1]: Overview and Architecture. This standard provides an overview to the family of IEEE 802 Standards. This document forms part of the 802.1 scope of work.
- ANSI/IEEE Std 802.1B [ISO/IEC 15802-2]: LAN/MAN Management. Defines an Open Systems Interconnection (OSI) management-compatible architecture, and services and protocol elements for use in a LAN/MAN environment for performing remote management.
- ANSI/IEEE Std 802.1D [ISO/IEC 10038]: MAC Bridging. Specifies an architecture and protocol for the interconnection of IEEE 802 LANs below the MAC service boundary.
- ANSI/IEEE Std 802.1E [ISO/IEC 15802-4]: System Load Protocol. Specifies a set of services and protocol for those aspects of management concerned with the loading of systems on IEEE 802 LANs.

[1]The 802 Architecture and Overview standard, originally known as IEEE Std 802.1A, has been renumbered as IEEE Std 802. This has been done to accommodate recognition of the base standard in a family of standards. References to IEEE Std 802.1A should be considered as references to IEEE Std 802.

- ANSI/IEEE Std 802.2 [ISO/IEC 8802-2]: Logical Link Control
- ANSI/IEEE Std 802.3 [ISO/IEC 8802-3]: CSMA/CD Access Method and Physical Layer Specifications
- ANSI/IEEE Std 802.4 [ISO/IEC 8802-4]: Token Bus Access Method and Physical Layer Specifications
- ANSI/IEEE Std 802.5 [ISO/IEC 8802-5]: Token Ring Access Method and Physical Layer Specifications
- ANSI/IEEE Std 802.6 [ISO/IEC 8802-6]: Distributed Queue Dual Bus Access Method and Physical Layer Specifications
- IEEE Std 802.9: Integrated Services (IS) LAN Interface at the Medium Access Control (MAC) and Physical (PHY) Layers
- IEEE Std 802.10: Interoperable LAN/MAN Security, *Currently approved:* Secure Data Exchange (SDE)
- IEEE 802.12: Demand Priority Access Method/Physical Layer Specifications

In addition to the family of standards, the following is a recommended practice for a common Physical Layer technology:

- IEEE Std 802.7: IEEE Recommended Practice for Broadband Local Area Networks

The following additional working groups have authorized standards projects under development:

- IEEE 802.11: Wireless LAN Medium Access Control (MAC) Sublayer and Physical Layer Specifications
- IEEE 802.14: Standard Protocol for Cable-TV Based Broadband Communication Network

The reader of this standard is urged to become familiar with the complete family of standards.

Conformance test methodology

An additional standards series, identified by the number 1802, has been established to identify the conformance test methodology documents for the 802 family of standards. Thus the conformance test documents for 802.3 are numbered 1802.3, the conformance test documents for 802.5 will be 1802.5, and so on. Similarly, ISO will use 18802 to number conformance test standards for 8802 standards.

IEEE Std 802.3u-1995

At the time this standard (IEEE Std 802.3u-1995) was published, the IEEE 802.3 standard consisted of the following published documents:

- ISO/IEC 8802-3: 1993 [ANSI/IEEE Std 802.3, 1993 Edition]
- IEEE Std 802.3j-1993, Fiber Optic Active and Passive Star-Based Segments, Type 10BASE-F (Clauses 15–18)
- IEEE Std 802.3k-1992, Layer Management for 10 Mb/s Baseband Repeaters (Clause 19)
- IEEE Std 802.3l-1992, Type 10BASE-T Protocol Implementation Conformance Statement (PICS) Proforma (Subclause 14.10)
- IEEE Std 802.3p-1993 *and* IEEE Std 802.3q-1993, Guidelines for the Development of Managed Objects (GDMO) (ISO/IEC 10165-4) Format for Layer-Managed Objects (Clause 5) *and* Layer Management for 10 Mb/s Baseband Medium Attachment Units (MAUs) (Clause 20)
- IEEE Std 1802.3d-1993, Type 10BASE-T Medium Attachment Unit (MAU) (Conformance Test Methodology (Clause 6)

At the time this standard was published, there was revision and supplementary material that had been approved and scheduled for publication. Also, a new edition of ISO/IEC 8802-3 was in preparation to consolidate a significant amount of the above material. Information on the current state of this and other IEEE 802 standards may be obtained from

Secretary, IEEE Standards Board
445 Hoes Lane
P.O. Box 1331
Piscataway, NJ 08855-1331
USA

IEEE 802 committee working documents are available from

IEEE Document Distribution Service
AlphaGraphics #35 Attn: P. Thrush
10201 N. 35th Avenue
Phoenix, AZ 85051
USA

Patent information

The IEEE Standards Board calls attention to the fact that it is claimed that portions of IEEE Std 802.3u-1995 are the subject of patents owned by a number of companies. The IEEE takes no position with respect to patent validity. Each of these companies has assured IEEE that it is willing to grant a license on these patents on reasonable and nondiscriminatory terms to anyone wishing to obtain such a license. The undertakings of these companies in this respect are on file with the IEEE Standards Department, and the license details may be obtained by contacting the Standards Department.

Participants

When the IEEE 802.3 Working Group approved IEEE Std 802.3u-1995, it had the following membership:

Geoffrey O. Thompson, *Chair*
Peter Tarrant, *Type 100BASE-T Task Force Chair, Phase 1*
Howard Frazier, *Type 100BASE-T Task Force Chair, Phase 2*
Paul Sherer, *Editor-in-Chief, Phase 1*
Howard Johnson, *Editor-in-Chief, Phase 2*
Colin Mick, *Comment Editor*

Martin Adams
Don Aelmore
Paul Ahrens
Vish Akella
Abe Ali
Nitish Amin
Mike Armstrong
Denis Beaudoin
Larry Birenbaum*
Mark Bohrer
Paul Booth*
Samuel Bourche
David Bourque
Sidney Bouzaglo
Richard Bowers
Richard Brand
Charles E. Brill
Bill Bunch†
Peter Campbell
Kiwon Chang
Samuel Chang
Howard Charney
Hon Wah Chin
Jacques Christ
Ronald J. Cooper
Ron Crane
Ian Crayford*
Robert Curtis
Bernard Daines
Sean Dingman
Thuyen Dinh
Dan Dove
James Doyle
Peter Ecclesine
Dean Edwards
George Eisler
Nick Esser
Jim Everitt
David Fischer
Alan Flatman
Christian G. Folting
Atsuhisa Fukuoka
Wolfgang Heidasch
Walter Hurwitz†
Ernie Jensen
Clarence Joh
Anthony Jordan
Dieter Junkers
Omer Kal
Ron Kao
Yongbum Kim
Srinivas Kola
Josef Kozilek
George Kubovcik
Hans Lackner
Erik Lander
David Law*
Chun-Tsung Lee
Jack Lee
Vincent Lefebvre
Richard Lewis
Sam Liang
Chan-De Lin
Chang-Chi Liu
Terry Lockyer
Ken Lu
Andy J. Luque
Brian MacLeod
Kenneth MacLeod
Joseph Mazor
Mike McConnell
John McCool
Tim McShane
Mart L. Molle
Shimon Muller
Samba Murthy
Larry Nicholson
Paul Nikolich
Ahmad Nouri
J. Michael O'Connor
Lloyd Oliver
Pat Overs
Sandeep Patel
John Payne
Tony Peatfield
William Quackenbush
Thomas J. Quigley
Mohammad Rajabzadeh
Shlomo Rakib
Brian Ramelson
Peter Rautenberg
Dennis Rehm
Victor Renteria
Sean Riley
Gary Robinson
Khosrow Sadeghi
David Schwartz
Stephen Sedio
Rich Seifert
Koichiro Seto
Chen-Chung Shih
Som Sikdar
Charan J. Singh*
Paramjeet (P. J.) Singh
Dinah Sloan
Tom Slykhouse
Michael Smith
Dror Sofer
Gregory Somer
Walter Sotelo
Peter Staub
Ron Sulyma
Daniel Sze
Martin Takessian
Wen-Tsung Tang
Tim Teckman
Douglas Thomson
Nader Vijeh
Moshe Voloshin
Ikuo Wakayama
Chang Jung Wang
Yun-Che Wang
Ken Ward
Bob Watson
David Wong
Paul Woodruff*
Nariman Yousefi
Jamie Zartman

* served as sub-task force chair or clause editor
† served as clause editor but was not a working group member at the time of ballot

The following persons were on the balloting committee:

Don Aelmore
Bernhard Albert
Alan Albrecht
Abe Ali
Hasan S. Alkhatib
Corey Anderson
Kit Athul
William E. Ayen
Kendall F. Barney
Larry Birenbaum
Simon Black
Kwame Boakye
Kathleen L. Briggs
Peter K. Campbell
James T. Carlo
Alan J. Chwick
Alistair Coles
Ian Crayford
Robert S. Crowder
Joe Curcio
Ibibia K. Dabipi
Robert Donnan
Daniel Dove
Edward A. Dunlop
John E. Emrich
Alvin W. Eng
Philip H. Enslow, Jr.
Changxin Fan
John W. Fendrich
David Fifield
Michael Fischer
Christian G. Folting
Howard M. Frazier
Harvey A. Freeman
Robert J. Gagliano
D. G. Gan
Harry Gold
Patrick Gonia
Andrew Gruskay
Jacob J. Hsu
Howard Johnson
Gary C. Kessler
Mladen Kezunovic
Yongbum Kim
Mikio Kiyono
Kenneth C. Kung
David Law
Lanse M. Leach
Sam Liang
Randolph S. Little
Donald C. Loughry
Robert D. Love
William C. Lynch
Peter Martini
William C. McDonald
Tim J. McShane
Bennett Meyer
Colin K. Mick
Ann Miller
Bruce D. Miller
Richard H. Miller
David S. Millman
Warren Monroe
John E. Montague
Kinji Mori
David J. Morris
James R. Moulton
Wayne D. Moyers
Shimon Muller
Paul Nikolich
Ellis S. Nolley
Robert O'Hara
Donal O'Mahony
Young Oh
Joerg Ottensmeyer
Roger Pandanda
Lalit Mohan Patnaik
Lucy W. Person
Thomas L. Phinney
Kirk Preiss
Alberto Profumo
Vikram Punj
Andris Putnins
Brian Ramelson
Fernando Ramos
Eugene J. Reilly
Everett O. Rigsbee
Gary S. Robinson
Philip T. Robinson
James W. Romlein
Floyd E. Ross
S. I. Samoylenko
Frederick E. Sauer
Frederick Scholl
David Schwartz
Mick Seaman
John Selep
Koichiro Seto
Donald A. Sheppard
Leo Sintonen
William R. Smith
Harry P. Solomon
Robert K. Southard
Efstathios D. Sykas
Steven R. Taylor
Patricia Thaler
Geoffrey O. Thompson
Kaichi Tsuno
Mark-Rene Uchida
Barry M. Vornbrock
Yun-Che Wang
Alan J. Weissberger
Frank J. Weisser
Raymond P. Wenig
Earl J. Whitaker
Jerry A. Wyatt
Oren Yuen

When the IEEE Standards Board approved this standard on June 14, 1995, it had the following membership:

E. G. "Al" Kiener, *Chair* **Donald C. Loughry,** *Vice Chair*

Andrew G. Salem, *Secretary*

Gilles A. Baril
Clyde R. Camp
Joseph A. Cannatelli
Stephen L. Diamond
Harold E. Epstein
Donald C. Fleckenstein
Jay Forster*
Donald N. Heirman
Richard J. Holleman
Jim Isaak
Ben C. Johnson
Sonny Kasturi
Lorraine C. Kevra
Ivor N. Knight
Joseph L. Koepfinger*
D. N. "Jim" Logothetis
L. Bruce McClung
Marco W. Migliaro
Mary Lou Padgett
John W. Pope
Arthur K. Reilly
Gary S. Robinson
Ingo Rusch
Chee Kiow Tan
Leonard L. Tripp

*Member Emeritus

Also included are the following nonvoting IEEE Standards Board liaisons:

Satish K. Aggarwal
Richard B. Engelman
Robert E. Hebner
Chester C. Taylor

Kristin M. Dittmann
IEEE Standards Project Editor

Contents

IEEE Standards for Local and Metropolitan Area Networks:

Supplement to Carrier Sense Multiple Access with Collision Detection (CSMA/CD) Access Method and Physical Layer Specifications

Revisions to ISO/IEC 8802-3 : 1993 [ANSI/IEEE Std 802.3, 1993 Edition]

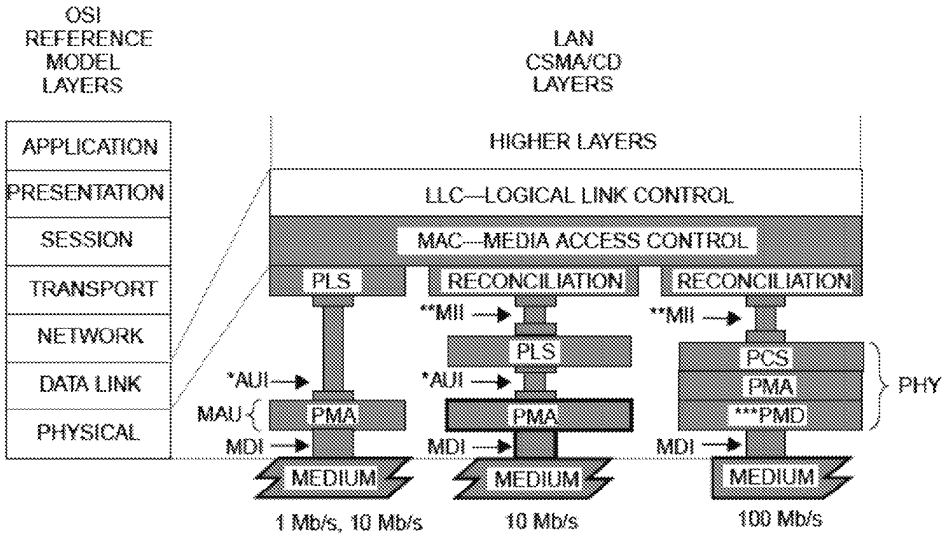
EDITORIAL NOTES

1—The following changes to ISO/IEC 8802-3 : 1993 [ANSI/IEEE Std 802.3, 1993 Edition] (and supplements 802.3j-1993, 802.3k-1992, 802.3l-1992, and 802.3p&q-1993) affect clauses 1, 2, 4, 5, 14, 19, 20, Annex A, and Annex D. These changes must also be applied to the 1995 edition of ISO/IEC 8802-3, which will incorporate all the supplements.

2—The text as shown includes editorial changes that accommodate recent changes to the IEEE style.

3—Editing instructions are shown in ***bold italic*** type. Where modifications are made to paragraphs of existing text, deletions are shown in ~~strikethrough type~~ and additions are underscored. Editorial notes will not be carried over into future editions.

Replace figure 1-1 with the following:



AUI = ATTACHMENT UNIT INTERFACE
MDI = MEDIUM DEPENDENT INTERFACE
MII = MEDIA INDEPENDENT INTERFACE
MAU = MEDIUM ATTACHMENT UNIT

PLS = PHYSICAL LAYER SIGNALING
PCS = PHYSICAL CODING SUBLAYER
PMA = PHYSICAL MEDIUM ATTACHMENT
PHY = PHYSICAL LAYER DEVICE
PMD = PHYSICAL MEDIUM DEPENDENT

NOTE—The three types of layers below the MAC sublayer are mutually independent.
* AUI is optional for 10 Mb/s systems and is not specified for 1 Mb/s and 100 Mb/s systems.
** MII is optional for 10 Mb/s DTEs and for 100 Mb/s systems and is not specified for 1 Mb/s systems.
*** PMD is specified for 100BASE-X only; 100BASE-T4 does not use this layer.
For an exposed AUI residing below an MII, see 22.5.

Figure 1-1—LAN standard relationship to the ISO Opens Systems Interconnection (OSI) reference model

Change 1.1.1 to read as follows:

The Carrier Sense Multiple Access with Collision Detection (CSMA/CD) media access method is the means by which two or more stations share a common transmission medium. To transmit, a station waits (defers) for a quiet period on the medium (that is, no other station is transmitting) and then sends the intended message in bit-serial form. If, after initiating a transmission, the message collides with that of another station, then each transmitting station intentionally ~~sends a few additional bytes~~ transmits for an additional predefined period to ensure propagation of the collision throughout the system. The station remains silent for a random amount of time (backoff) before attempting to transmit again. Each aspect of this access method process is specified in detail in subsequent sections of this standard.

This is a comprehensive standard for Local Area Networks employing CSMA/CD as the access method. This standard is intended to encompass several media types and techniques for signal rates of from 1 Mb/s to ~~20 Mb/s~~ 100 Mb/s. This edition of the standard provides the necessary specifications for ~~10 Mb/s baseband and broadband systems, a 1 Mb/s baseband system, and a Repeater Unit.~~ three families of systems: a 1 Mb/s baseband system, 10 Mb/s baseband and broadband systems, and a 100 Mb/s baseband system.

Change 1.1.2.2 to read as follows:

~~Two~~ Three important compatibility interfaces are defined within what is architecturally the Physical Layer.

a) *Medium Dependent Interfaces (MDI).* To communicate in a compatible manner, all stations shall adhere rigidly to the exact specification of physical media signals defined in ~~Section~~ clause 8 (and beyond) in this standard, and to the procedures that define correct behavior of a station. The medium-independent aspects of the LLC sublayer and the MAC sublayer should not be taken as detracting from this point; communication by way of the ISO/IEC 8802-3 [ANSI/IEEE Std 802.3] Local Area Network requires complete compatibility at the Physical Medium interface (that is, the ~~coaxial~~ physical cable interface).

b) *Attachment Unit Interface (AUI).* It is anticipated that most DTEs will be located some distance from their connection to the ~~coaxial~~ physical cable. A small amount of circuitry will exist in the Medium Attachment Unit (MAU) directly adjacent to the ~~coaxial~~ physical cable, while the majority of the hardware and all of the software will be placed within the DTE. The AUI is defined as a second compatibility interface. While conformance with this interface is not strictly necessary to ensure communication, it is highly recommended, since it allows maximum flexibility in intermixing MAUs and DTEs. The AUI may be optional or not specified for some implementations of this standard that are expected to be connected directly to the medium and so do not use a separate MAU or its interconnecting AUI cable. The PLS and PMA are then part of a single unit, and no explicit AUI implementation is required.

c) *Media Independent Interface (MII).* It is anticipated that some DTEs will be connected to a remote PHY, and/or to different medium dependent PHYs. The MII is defined as a third compatibility interface. While conformance with implementation of this interface is not strictly necessary to ensure communication, it is highly recommended, since it allows maximum flexibility in intermixing PHYs and DTEs. The MII is optional.

1.3 References

Replace 1.3 with the following:

The following standards contain provisions which, through references in this text, constitute provisions of this International Standard. At the time of publication, the editions indicated were valid. All standards are subject to revision, and parties to agreements based on this International Standard are encouraged to investigate the possibility of applying the most recent editions of the standards listed below. Members of IEC and ISO maintain registers of currently valid International Standards.

EDITORIAL NOTE—In the following references, changes are not indicated by strikethroughs and underscores.

ANSI X3.237-1995, Rev 2.1 (1 January 1995), FDDI Low-Cost Fibre Physical Layer—Medium Dependent (LCF-PMD) (ISO/IEC CD 9314-9).

ANSI X3.263: 1995, Revision 2.2 (1 March 1995), FDDI Twisted Pair—Physical Medium Dependent (TP-PMD) (ISO/IEC CD 9314-10).

CISPR 22: 1993, Limits and Methods of Measurement of Radio Interference Characteristics of Information Technology Equipment.[1]

IEC 60, High-voltage test techniques.[2]

IEC 68, Basic environmental testing procedures.

IEC 96-1: 1986, Radio-frequency cables, Part 1: General requirements and measurement methods, and Amendment 2: 1993.

IEC 169-8: 1978 and -16: 1982, Radio-frequency connectors, Part 8: Radio-frequency coaxial connectors with inner diameter of outer conductor 6.5 mm (0.256 in) with bayonet lock—Characteristic impedence 50 ohms (Type BNC) and Part 16: Radio-frequency coaxial connectors with inner diameter of outer conductor 7 mm (0.276 in) with screw coupling—Characteristic impedence 50 ohms (75 ohms) (Type N).

IEC 380: 1985, Safety of electrically energized office machines.[3]

IEC 435: 1983, Safety of data processing equipment.[4]

IEC 603-7: 1990, Connectors for frequencies below 3 MHz for use with printed boards, Part 7: Detail specification for connectors, 8-way, including fixed and free connectors with common mating features.

IEC 793-1: 1992, Optical fibres, Part 1: Generic specification.

IEC 793-2: 1989, Optical fibres, Part 2: Product specifications.[5]

IEC 794-1: 1993, Optical fibre cables, Part 1: Generic specification.

IEC 794-2: 1989, Optical fibre cables, Part 2: Product specifications.

IEC 807-2: 1992, Rectangular connectors for frequencies below 3 MHz, Part 2: Detail specification for a range of connectors with assessed quality, with trapezoidal shaped metal shells and round contacts—Fixed solder contact types.

IEC 825-1: 1993, Safety of laser products, Part 1: Equipment classification, requirements and user's guide.

---

[1]CISPR documents are available from the International Electrotechnical Commission, 3 rue de Varembé, Case Postale 131, CH 1211, Genève 20, Switzerland/Suisse. CISPR documents are also available in the United States from the Sales Department, American National Standards Institute, 11 West 42nd Street, 13th Floor, New York, NY 10036, USA.

[2]IEC publications are available from International Electrotechnical Commission. IEC publications are also available in the United States from the American National Standards Institute.

[3]IEC 380: 1985 was withdrawn in 1991. It has been replaced by IEC 950: 1991.

[4]IEC 435: 1983 was withdrawn in 1991. It has been replaced by IEC 950: 1991.

[5]Subclause 9.9 is to be read with the understanding that the following changes to IEC 793-2: 1989 have been requested: a) Correction of the numerical aperture tolerance in table III to ±0.015; and b) Addition of another bandwidth category of 150 MHz referred to 1 km, for the type A1b fibre in table III.

IEC 874-1: 1993, Connectors for optical fibres and cables, Part 1: Generic specification.

IEC 874-2: 1993, Connectors for optical fibres and cables, Part 2: Sectional specification for fibre optic connector—Type F-SMA.

IEC 950: 1991, Safety of information technology equipment, including electrical business equipment.[6]

IEC 1076-3-101: 1995 [48B Secretariat 276], Detail specification for a range of shielded connectors with trapezoidal shaped shells and nonremovable rectangular contacts on a 1.27 × 2.54 millimeter centerline.[7]

IEEE Std 802-1990, IEEE Standards for Local and Metropolitan Area Networks: Overview and Architecture (ANSI).[8]

IEEE Std 802.1F-1993, IEEE Standards for Local and Metropolitan Area Networks: Common Definitions and Procedures for IEEE 802 Management Information (ANSI).

ISO 2382-9: 1984, Data processing—Vocabulary—Part 9: Data communications.[9]

ISO 7498: 1984, Information processing systems—Open Systems Interconnection—Basic Reference Model.

ISO/IEC 8824: 1990, Information technology—Open Systems Interconnection—Specification of Abstract Syntax Notation One (ASN.1).

ISO/IEC 8825: 1990, Information technology—Open Systems Interconnection—Specification of Basic Encoding Rules for Abstract Syntax Notation One (ASN.1).

ISO 9314-1: 1989, Information processing systems—Fibre Distributed Data Interface (FDDI)—Part 1: Token Ring Physical Layer Protocol (PHY).

ISO 9314-2: 1989, Information processing systems—Fibre Distributed Data Interface (FDDI)—Part 2: Token Ring Media Access Control (MAC).

ISO 9314-3: 1990, Information processing systems—Fibre Distributed Data Interface (FDDI)—Part 3: Physical Layer Medium Dependent (PMD).

ISO/IEC 10040: 1992, Information technology—Open Systems Interconnection—Systems management overview.

ISO/IEC 10164-1: 1993, Information technology—Open Systems Interconnection—Systems management—Object Management Function.

ISO/IEC 10165-1: 1993, Information technology—Open Systems Interconnection—Management information services—Structure of management information—Management Information Model.

ISO/IEC 10165-2: 1992, Information technology—Open Systems Interconnection—Management information services—Structure of management information—Definition of management information.

---

[6]IEC 950: 1991 replaces IEC 380: 1985 and 435: 1983.

[7]Presently this is a committee draft.

[8]IEEE publications are available from the Institute of Electrical and Electronics Engineers, Service Center, 445 Hoes Lane, P.O. Box 1331, Piscataway, NJ 08855-1331, USA.

[9]ISO and ISO/IEC publications are available from the International Organization for Standardization, Case Postale 56, 1 rue de Varembé, CH-1211, Genève 20, Switzerland/Suisse. They are also available in the United States from the American National Standards Institute.

ISO/IEC 10165-4: 1992, Information technology—Open Systems Interconnection—Management information services—Structure of management information—Part 4: Guidelines for the definition of managed objects.

ISO/IEC 7498-4: 1989, Information processing systems—Open Systems Interconnection—Basic Reference Model—Part 4: Management framework.

ISO/IEC 8877: 1992, Information technology—Telecommunications and information exchange between systems—Interface connector and contact assignments for ISDN Basic Access Interface located at reference points S and T.

ISO/IEC 9646-1: 1994, Information technology—Open Systems Interconnection—Conformance testing methodology and framework—Part 1: General concepts.

ISO/IEC 9646-2: 1994, Information technology—Open Systems Interconnection—Conformance testing methodology and framework—Part 2: Abstract Test Suite specification.

ISO/IEC 10165-4: 1992, Information technology—Open Systems Interconnection—Structure of management information—Part 4: Guidelines for the definition of managed objects.

ISO/IEC 11801: 1995, Information technology—Generic cabling for customer premises.

NOTE—Local and national standards such as those supported by ANSI, EIA, IEEE, MIL, NPFA, and UL are not a formal part of the ISO/IEC 8802-3 standard except where no international standard equivalent exists. Reference to such local or national standards may be useful resource material and are located in annex A.

1.4 Definitions

EDITORIAL NOTE—The definitions subclauses within several clauses of ISO/IEC 8802-3 are consolidated in this revised clause. In the following definitions, changes are not indicated by strikethroughs and underscores. See the end of this subclause for further editing instructions.

Replace 1.4 with the following text:

1.4.1 100BASE-FX: IEEE 802.3 Physical Layer specification for a 100 Mb/s CSMA/CD LAN over two optical fibers. (See IEEE 802.3 clauses 24 and 26.)

1.4.2 100BASE-T: IEEE 802.3 Physical Layer specification for a 100 Mb/s CSMA/CD LAN. (See IEEE 802.3 clauses 22 and 28.)

1.4.3 100BASE-T4: IEEE 802.3 Physical Layer specification for a 100 Mb/s CSMA/CD LAN over four pairs of Category 3, 4, and 5 unshielded twisted-pair (UTP) wire. (See IEEE 802.3 clause 23.)

1.4.4 100BASE-TX: IEEE 802.3 Physical Layer specification for a 100 Mb/s CSMA/CD LAN over two pairs of Category 5 UTP or shielded twisted-pair (STP) wire. (See IEEE 802.3 clauses 24 and 25.)

1.4.5 100BASE-X: IEEE 802.3 Physical Layer specification for a 100 Mb/s CSMA/CD LAN that uses the PMD sublayer and MDI of the ISO 9314 group of standards developed by ASC X3T12 (FDDI). (See IEEE 802.3 clause 24.)

1.4.6 10BASE2: IEEE 802.3 Physical Layer specification for a 10 Mb/s CSMA/CD LAN over RG 58 coaxial cable. (See IEEE 802.3 clause 10.)

1.4.7 10BASE5: IEEE 802.3 Physical Layer specification for a 10 Mb/s CSMA/CD LAN over coaxial cable (i.e., thicknet). (See IEEE 802.3 clause 8.)

1.4.8 10BASE-F: IEEE 802.3 Physical Layer specification for a 10 Mb/s CSMA/CD LAN over fiber optic cable. (See IEEE 802.3 clause 15.)

1.4.9 10BASE-FB port: A port on a repeater that contains an internal 10BASE-FB Medium Attachment Unit (MAU) that can connect to a similar port on another repeater. (See IEEE 802.3 clause 9, figure 15-1(b) and 17.3.)

1.4.10 10BASE-FB segment: A fiber optic link segment providing a point-to-point connection between two 10BASE-FB ports on repeaters. (See link segment IEEE 802.3 figure 15-1(b) and figure 15-2.)

1.4.11 10BASE-FL segment: A fiber optic link segment providing point-to-point connection between two 10BASE-FL MAUs. (See link segment IEEE 802.3 figure 15.1 (c) and figure 15-2.)

1.4.12 10BASE-FP segment: A fiber optic mixing segment, including one 10BASE-FP Star and all of the attached fiber pairs. (See IEEE 802.3 figure 15-1(a), figure 15-2, and mixing segment.)

1.4.13 10BASE-FP Star: A passive device that is used to couple fiber pairs together to form a 10BASE-FP segment. Optical signals received at any input port of the 10BASE-FP Star are distributed to all of its output ports (including the output port of the optical interface from which it was received). A 10BASE-FP Star is typically comprised of a passive-star coupler, fiber optic connectors, and a suitable mechanical housing. (See IEEE 802.3, 16.5.)

1.4.14 10BASE-T: IEEE 802.3 Physical Layer specification for a 10 Mb/s CSMA/CD LAN over two pairs of twisted-pair telephone wire. (See IEEE 802.3 clause 14.)

1.4.15 10BROAD36: IEEE 802.3 Physical Layer specification for 10 Mb/s CSMA/CD LAN over single broadband cable. (See IEEE 802.3 clause 11.)

1.4.16 1BASE5: IEEE 802.3 Physical Layer specification for 1 Mb/s CSMA/CD LAN over two pairs of twisted-pair telephone wire. (See IEEE 802.3 clause 12.)

1.4.17 ability: A mode that a device can advertise using Auto-Negotiation. For modes that represent a type of data service, a device shall be able to operate that data service before it may advertise this ability. A device may support multiple abilities. (See IEEE 802.3, 28.2.1.2.2.)

1.4.18 Acknowledge Bit: A bit used by IEEE 802.3 Auto-Negotiation to indicate that a station has successfully received multiple identical copies of the Link Code Word. This bit is only set after an identical Link Code Word has been received three times in succession. (See IEEE 802.3, 28.2.1.2.4.)

1.4.19 advertised ability: An operational mode that is advertised using Auto-Negotiation. (See IEEE 802.3, 28.2.1.2.2.)

1.4.20 agent code: A term used to refer to network management entity software residing in a node that can be used to remotely configure the host system based on commands received from the network control host, collect information documenting the operation of the host, and communicate with the network control host. (See IEEE 802.3 clause 30.)

1.4.21 agent: A term used to refer to the managed nodes in a network. Managed nodes are those nodes that contain a network management entity (NME), which can be used to configure the node and/or collect data describing operation of that node. The agent is controlled by a network control host or manager that contains both an NME and network management application (NMA) software to control the operations of agents. Agents include systems that support user applications as well as nodes that provide communications services such as front-end processors, bridges, and routers. (See IEEE 802.3 clause 30.)

1.4.22 agile device: A device that supports automatic switching between multiple Physical Layer technologies. (See IEEE 802.3 clause 28.)

1.4.23 Attachment Unit Interface (AUI): In 10 Mb/s CSMA/CD, the interface between the MAU and the data terminal equipment (DTE) within a data station. Note that the AUI carries encoded signals and provides for duplex data transmission. (See IEEE 802.3 clauses 7 and 8.)

1.4.24 Auto-Negotiation: The algorithm that allows two devices at either end of a link segment to negotiate common data service functions. (See IEEE 802.3 clause 28.)

1.4.25 balanced cable: A cable consisting of one or more metallic symmetrical cable elements (twisted pairs or quads). (From ISO/IEC 11801: 1995.)

1.4.26 Base Link Code Word: The first 16-bit message exchanged during IEEE 802.3 Auto-Negotiation. (See IEEE 802.3, 28.2.1.2.)

1.4.27 Base Page: *See:* **Base Link Code Word**.

1.4.28 baseband coaxial system: A system whereby information is directly encoded and impressed upon the transmission medium. At any point on the medium only one information signal at a time can be present without disruption.

1.4.29 baud: A unit of signaling speed, expressed as the number of times per second the signal can change the electrical state of the transmission line or other medium. *Note*—Depending on the encoding strategies, a signal event may represent a single bit, more, or less that one bit. *Contrast with:* **bit rate**; **bits per second**. (From IEEE Std 610.7-1995 [A16].[10])

1.4.30 Binary Phase Shift Keying (Binary PSK or BPSK): A form of modulation in which binary data are transmitted by changing the carrier phase by 180 degrees. (See IEEE 802.3 clause 11.)

1.4.31 bit cell: The time interval used for the transmission of a single data (CD0 or CD1) or control (CVH or CVL) symbol.

1.4.32 bit rate (BR): The total number of bits per second transferred to or from the Medium Access Control (MAC). For example, 100BASE-T has a bit rate of one hundred million bits per second (10^8 b/s).

1.4.33 bit time (BT): The duration of one bit as transferred to and from the MAC. The bit time is the reciprocal of the bit rate. For example, for 100BASE-T the bit rate is 10^{-8} s or 10 ns.

1.4.34 BR/2: One half of the BR in Hertz.

1.4.35 branch cable: In 10BROAD36, the AUI cable interconnecting the DTE and MAU system components.

1.4.36 bridge: A layer 2 interconnection device that does not form part of a CSMA/CD collision domain but rather, appears as a MAC to the collision domain. (See also IEEE Std 610.7-1995 [A16].)

1.4.37 Broadband LAN: A local area network in which information is transmitted on modulated carriers, allowing coexistence of multiple simultaneous services on a single physical medium by frequency division multiplexing. (See IEEE 802.3 clause 11.)

[10]Numbers in brackets correspond to those of the additional reference material in annex A.

1.4.38 bundle: A group of signals that have a common set of characteristics and differ only in their information content.

1.4.39 carrier sense: In a local area network, an ongoing activity of a data station to detect whether another station is transmitting. *Note*—The carrier sense signal indicates that one or more DTEs are currently transmitting.

1.4.40 Category 3 balanced cabling: Balanced 100 Ω and 120 Ω cabling (cable and associated connecting hardware) whose transmission characteristics are specified up to 16 MHz (i.e., performance meets the requirements of a Class C link in accordance with ISO/IEC 11801: 1995). Commonly used by IEEE 802.3 10BASE-T installations. In addition to the requirements outlined in ISO/IEC 11801: 1995, IEEE 802.3 clause 23 specifies additional requirements for these cables when used with 100BASE-T4.

1.4.41 Category 4 balanced cabling: Balanced 100 Ω and 120 Ω cabling (cable and associated connecting hardware) whose transmission characteristics are specified up to 20 MHz in accordance with ISO/IEC 11801: 1995. In addition to the requirements outlined in ISO/IEC 11801: 1995, IEEE 802.3 clause 23 specifies additional requirements for these cables when used with 100BASE-T4.

1.4.42 Category 5 balanced cabling: Balanced 100 Ω and 120 Ω cabling (cable and associated connecting hardware) whose transmission characteristics are specified up to 100 MHz (i.e., performance meets the requirements of a Class D link as per ISO/IEC 11801: 1995). In addition to the requirements outlined in ISO/IEC 11801: 1995, IEEE 802.3 clauses 23 and 25 specify additional requirements for these cables when used with 100BASE-T.

1.4.43 CATV-Type broadband medium: A broadband system comprising coaxial cables, taps, splitters, amplifiers, and connectors the same as those used in Community Antenna Television (CATV) or cable television installations. (See IEEE 802.3 clause 11.)

1.4.44 center wavelength: The average of two optical wavelengths at which the spectral radiant intensity is 50% of the maximum value. (See IEEE 802.3 clause 11.)

1.4.45 channel: A band of frequencies dedicated to a certain service transmitted on the broadband medium. (See IEEE 802.3 clause 11.)

1.4.46 circuit: The physical medium on which signals are carried across the AUI for 10BASE-T or MII (for 100BASE-T). For 10BASE-T, the data and control circuits consist of an A circuit and a B circuit forming a balanced transmission system so that the signal carrier on the B circuit is the inverse of the signal carried on the A circuit.

1.4.47 Class I repeater: A type of 100BASE-T repeater set with internal delay such that only one repeater set may exist between any two DTEs within a single collision domain when two maximum length copper cable segments are used. (See IEEE 802.3 clause 27.)

1.4.48 Class II repeater: A type of IEEE 802.3 100BASE-T repeater set with internal delay such that only two or fewer such repeater sets may exist between any two DTEs within a single collision domain when two maximum length copper cable segments are used. (See IEEE 802.3 clause 27.)

1.4.49 Clocked Data One (CD1): A Manchester-encoded data 1. A CD1 is encoded as a LO for the first half of the bit-cell and a HI for the second half of the bit-cell. (See IEEE 802.3 clause 12.)

1.4.50 Clocked Data Zero (CD0): A Manchester-encoded data 0. A CDO is encoded as a HI for the first half of the bit-cell and a LO for the second half of the bit-cell. (See IEEE 802.3 clause 12.)

1.4.51 Clocked Violation HI (CVH): A symbol that deliberately violates Manchester-encoding rules, used as a part of the Collision Presence signal. A CVH is encoded as a transition from LO to HI at the beginning of the bit cell, HI for the entire bit cell, and a transition from HI to LO at the end of the bit cell. (See IEEE 802.3 clause 12.)

1.4.52 Clocked Violation LO (CVL): A symbol that deliberately violates Manchester-encoding rules, used as a part of the Collision Presence signal. A CVL is encoded as a transition from HI to LO at the beginning of the bit cell, LO for the entire bit cell, and a transition from LO to HI at the end of the bit cell. (See IEEE 802.3 clause 12.)

1.4.53 coaxial cable interface: The electrical and mechanical interface to the shared coaxial cable medium either contained within or connected to the MAU. Also known as the Medium Dependent Interface (MDI).

1.4.54 coaxial cable section: A single length of coaxial cable, terminated at each end with a male BNC connector. Cable sections are joined to other cable sections via BNC plug/receptacle barrel or Type T adapters.

1.4.55 coaxial cable segment: A length of coaxial cable made up from one or more coaxial cable sections and coaxial connectors, and terminated at each end in its characteristic impedance.

1.4.56 coaxial cable: A two-conductor (center conductor, shield system), concentric, constant impedance transmission line used as the trunk medium in the baseband system.

1.4.57 Code Rule Violation (CRV): An analog waveform that is not the result of the valid Manchester-encoded output of a single optical transmitter. The collision of two or more 10BASE-FB optical transmissions will cause multiple CRVs. The preamble encoding of a single 10BASE-FP optical transmission contains a single CRV. (See IEEE 802.3, 16.3.1.1.)

1.4.58 code-bit: In 100BASE-X, the unit of data passed across the PMA service interface, and the smallest signaling element used for transmission on the medium. A group of five code-bits constitutes a code-group in the 100BASE-X PCS. (See IEEE 802.3 clause 24.)

1.4.59 code-group: For IEEE 802.3, a set of encoded symbols representing encoded data or control information. For 100BASE-T4, a set of six ternary symbols that, when representing data, conveys an octet. (See IEEE 802.3 clause 23.) For 100BASE-TX and 100BASE-FX, a set of five code-bits that, when representing data, conveys a nibble. (See IEEE 802.3 clause 24.)

1.4.60 collision domain: A single CSMA/CD network. If two or more MAC sublayers are within the same collision domain and both transmit at the same time, a collision will occur. MAC sublayers separated by a repeater are in the same collision domain. MAC sublayers separated by a bridge are within different collision domains.

1.4.61 collision presence: A signal generated within the Physical Layer by an end station or hub to indicate that multiple stations are contending for access to the transmission medium. (See IEEE 802.3 clauses 8 and 12.)

1.4.62 collision: A condition that results from concurrent transmissions from multiple DTE sources within a single collision domain.

1.4.63 common-mode voltage: The instantaneous algebraic average of two signals applied to a balanced circuit, with both signals referenced to a common reference. Also called *longitudinal voltage* in the telephone industry.

1.4.64 compatibility interfaces: The MDI cable, the AUI branch cable, and the MII; the three points at which hardware compatibility is defined to allow connection of independently designed and manufactured components to a baseband transmission medium. (See IEEE 802.3 clause 8.)

1.4.65 continuous wave (CW): A carrier that is not modulated or switched.

1.4.66 Control Signal One (CS1): An encoded control signal used on the Control In and Control Out circuits. A CS1 is encoded as a signal at half the bit rate (BR/2). (See IEEE 802.3 clause 12.)

1.4.67 Control Signal Zero (CS0): An encoded control signal used on the Control In and Control Out circuits. A CS0 is encoded as a signal at the bit rate (BR). (See IEEE 802.3 clause 12.)

1.4.68 cross connect: A group of connection points, often wall- or rack-mounted in a wiring closet, used to mechanically terminate and interconnect twisted-pair building wiring.

1.4.69 data frame: Consists of the Destination Address, Source Address, Length Field, logical link control (LLC) Data, PAD, and Frame Check Sequence.

1.4.70 Data Terminal Equipment (DTE): Any source or destination of data connected to the LAN.

1.4.71 dBmV: Decibels referenced to 1.0 mV measured at the same impedence. Used to define signal levels in CATV-type broadband systems. (See IEEE 802.3 clause 11.)

1.4.72 dedicated service: A CSMA/CD network in which the collision domain consists of two and only two DTEs so that the total network bandwidth is dedicated to supporting the flow of information between them.

1.4.73 differential-mode voltage: The instantaneous algebraic difference between the potential of two signals applied to the two sides of a balanced circuit. Also called *metallic voltage* in the telephone industry.

1.4.74 drop cable: In 10BROAD36, the small diameter flexible coaxial cable of the broadband medium that connects to a MAU. (*See:* **trunk cable**.)

1.4.75 eight-pin modular: An eight-wire connector. (From ISO/IEC 8877: 1992.)

1.4.76 End-of-Stream Delimiter (ESD): A code-group pattern used to terminate a normal data transmission. For 100BASE-T4, the ESD is indicated by the transmission of five predefined ternary code-groups named eop1-5. (See IEEE 802.3 clause 23.) For 100BASE-X, the ESD is indicated by the transmission of the code-group /T/R. (See IEEE 802.3 clause 24.)

1.4.77 Extinction Ratio: The ratio of the low optical power level to the high optical power level on an optical segment. (See IEEE 802.3 clause 15.)

1.4.78 Fast Link Pulse (FLP) Burst: A group of no more than 33 and not less than 17 10BASE-T compatible link integrity test pulses. Each FLP Burst encodes 16 bits of data using an alternating clock and data pulse sequence. (See figure 14-12, IEEE 802.3 clause 14 and figure 28-4, IEEE 802.3 clause 28.)

1.4.79 Fibre Distributed Data Interface (FDDI): A 100 Mb/s, fiber optic-based, token-ring LAN standard (ANSI X3T12, formerly X3.237-199X.

1.4.80 fiber optic cable: A cable containing one or more optical fibers as specified in IEEE 802.3, 15.3.1.

1.4.81 Fiber Optic Inter-Repeater Link (FOIRL): A Fiber Optic Inter-Repeater Link segment and its two attached MAUs. (See IEEE 802.3 clause 15.)

1.4.82 Fiber Optic Inter-Repeater Link Segment (FOIRL Segment): A fiber optic link segment providing a point-to-point connection between two FOIRL MAUs or between one FOIRL MAU and one 10BASE-FL MAU. *See:* **link segment**.

1.4.83 Fiber Optic Medium Attachment Unit (FOMAU): A MAU for fiber applications. (See IEEE 802.3 clause 9.)

1.4.84 Fiber Optic Medium-Dependent Interface (FOMDI): For 10BASE-F, the mechanical and optical interface between the optical fiber cable link segment and the FOMAU. (See IEEE 802.3 clause 9.)

1.4.85 Fiber Optic Physical Medium Attachment (FOPMA): For 10BASE-F, the portion of the FOMAU that contains the functional circuitry. (See IEEE 802.3 clause 9.)

1.4.86 fiber pair: Optical fibers interconnected to provide two continuous light paths terminated at each end in an optical connector. Any intermediate optical connections must have insertion and return loss characteristics that meet or exceed IEEE 802.3, 15.3.2.1 and 15.3.2.2, respectively. (See IEEE 802.3, 15.3.1.)

1.4.87 FOIRL BER: For 10BASE-F, the mean bit error rate of the FOIRL. (See IEEE 802.3 clause 9.)

1.4.88 FLP Burst Sequence: The sequence of FLP Bursts transmitted by the Local Station. This term is intended to differentiate the spacing between FLP Bursts from the individual pulse spacings within an FLP Burst. (See IEEE 802.3 clause 28.)

1.4.89 FOIRL collision: For 10BASE-F, the simultaneous transmission and reception of data in a FOMAU. (See IEEE 802.3 clause 9.)

1.4.90 FOIRL Compatibility Interface: For 10BASE-F, the FOMDI and AUI (optional); the two points at which hardware compatibility is defined to allow connection of independently designed and manufactured components to the baseband optical fiber cable link segment. (See IEEE 802.3 clause 9.)

1.4.91 FOMAU's Receive Optical Fiber: For 10BASE-F, the optical fiber from which the local FOMAU receives signals. (See IEEE 802.3 clause 9.)

1.4.92 FOMAU's Transmit Optical Fiber: For 10BASE-F, the optical fiber into which the local FOMAU transmits signals. (See IEEE 802.3 clause 9.)

1.4.93 full duplex: A type of networking that supports duplex transmission as defined in IEEE Std 610.7-1995 [A16]. Although some types of full-duplex networking are popularly referred to as Ethernet because they use the IEEE 802.3 defined frame, full duplex does not employ CSMA/CD and is not covered by this standard.

1.4.94 group: A repeater port or a collection of repeater ports that can be related to the logical arrangement of ports within a repeater.

1.4.95 group delay: In 10BROAD36, the rate of change of total phase shift, with respect to frequency, through a component or system. Group delay variation is the maximum difference in delay as a function of frequency over a band of frequencies. (See IEEE 802.3 clause 11.)

1.4.96 headend: In 10BROAD36, the location in a broadband system that serves as the root for the branching tree comprising the physical medium; the point to which all inbound signals converge and the point from which all outbound signals emanate. (See IEEE 802.3 clause 11.)

1.4.97 header hub (HH): The highest-level hub in a hierarchy of hubs. The HH broadcasts signals transmitted to it by lower level hubs or DTEs such that they can be received by all DTEs that may be connected to it either directly or through intermediate hubs. (See IEEE 802.3, 12.2.1 for details.)

1.4.98 hub: A device used to provide connectivity between DTEs. Hubs perform the basic functions of restoring signal amplitude and timing, collision detection, and notification and signal broadcast to lower level hubs and DTEs. (See IEEE 802.3 clause 12.)

1.4.99 idle (IDL): A signal condition where no transition occurs on the transmission line, that is used to define the end of a frame and ceases to exist after the next LO or HI transition on the AUI or MII circuits. An IDL always begins with a HI signal level. A driver is required to send the IDL signal for at least 2 bit times and a receiver is required to detect IDL within 1.6 bit times. (See IEEE 802.3, 7.3 and 12.3.2.4.4 for additional details.)

1.4.100 in-band signaling: The transmission of a signal using a frequency that is within the bandwidth of the information channel. *Contrast with:* **out-of-band signaling**. *Syn:* **in-channel signaling**. (From IEEE Std 610.7-1995 [A16].)

1.4.101 Inter-Repeater Link (IRL): A mechanism for connecting two and only two repeater sets.

1.4.102 Inter-Packet Gap (IPG): A delay or time gap between CSMA/CD packets intended to provide interframe recovery time for other CSMA/CD sublayers and for the Physical Medium. (See IEEE 802.3, 4.2.3.2.1 and 4.2.3.2.2.) For example, for 10BASE-T, the IPG is 9.6 ∝s (96 bit times); for 100BASE-T, the IPG is 0.96 ∝s (96 bit times.)

1.4.103 intermediate hub (IH): A hub that occupies any level below the header hub in a hierarchy of hubs. (See IEEE 802.3, 12.2.1 for details.)

1.4.104 Jabber function: A mechanism for controlling abnormally long transmissions (i.e., jabber.)

1.4.105 jabber: A condition wherein a station transmits for a period of time longer than the maximum permissible packet length, usually due to a fault condition.

1.4.106 link: The transmission path between any two interfaces of generic cabling. (From ISO/IEC 11801: 1995.)

1.4.107 Link Code Word: The 16 bits of data encoded into a Fast Link Pulse Burst. (See IEEE 802.3 clause 28.)

1.4.108 link partner: The device at the opposite end of a link segment from the local station. The link partner device may be either a DTE or a repeater. (See IEEE 802.3 clause 28.)

1.4.109 link pulse: Communication mechanism used in 10BASE-T and 100BASE-T networks to indicate link status and (in Auto-Negotiation-equipped devices) to communicate information about abilities and negotiate communication methods. 10BASE-T uses Normal Link Pulses (NLPs), which indicate link status only. 10BASE-T and 100BASE-T nodes equipped with Auto-Negotiation exchange information using a Fast Link Pulse (FLP) mechanism that is compatible with NLP. (See IEEE 802.3 clauses 14 and 28.)

1.4.110 link segment: The point-to-point full-duplex medium connection between two and only two MDIs.

1.4.111 Link Segment Delay Value (LSDV): A number associated with a given segment that represents the delay on that segment used to assess path delays for 100 Mb/s CSMA/CD networks. LSDV is similar to SDV; however, LSDV values do not include the delays associated with attached end stations and/or repeaters. (See IEEE 802.3, 29.3.)

1.4.112 local ability: *See:* **ability**.

1.4.113 local device: The local device that may attempt to Auto-Negotiate with a link partner. The local device may be either a DTE or repeater. (See IEEE 802.3 clause 28.)

1.4.114 Media Access Control (MAC): The data link sublayer that is responsible for transferring data to and from the Physical Layer.

1.4.115 Media Independent Interface (MII): A transparent signal interface at the bottom of the Reconciliation sublayer. (See IEEE 802.3 clause 22.)

1.4.116 Medium Attachment Unit (MAU): A device containing an AUI, PMA, and MDI that is used to connect a repeater or DTE to a transmission medium.

1.4.117 Medium Dependent Interface (MDI): The mechanical and electrical interface between the transmission medium and the MAU (10BASE-T) or PHY (100BASE-T).

1.4.118 Message Code (MC): The predefined 12-bit code contained in an Auto-Negotiation Message Page. (See IEEE 802.3 clause 28.)

1.4.119 Message Page (MP): An Auto-Negotiation Next Page encoding that contains a predefined 12-bit message code. (See IEEE 802.3 clause 28.)

1.4.120 Management Information Base (MIB): A repository of information to describe the operation of a specific network device.

1.4.121 mixing segment: A medium that may be connected to more than two MDIs.

1.4.122 network control host: A network management central control center that is used to configure agents, communicate with agents, and display information collected from agents.

1.4.123 Next Page Algorithm (NPA): The algorithm that governs Next Page communication. (See IEEE 802.3 clause 28.)

1.4.124 Next Page Bit: A bit in the Auto-Negotiation base Link Code Word or Next Page encoding(s) that indicates that further Link Code Word transfer is required. (See IEEE 802.3 clause 28.)

1.4.125 Next Page: General class of pages optionally transmitted by Auto-Negotiation-able devices following the base Link Code Word negotiation. (See IEEE 802.3 clause 28.)

1.4.126 nibble: A group of four data bits. The unit of data exchange on the MII. (See IEEE 802.3 clause 22.)

1.4.127 NLP Receive Link Integrity Test Function: Auto-Negotiation's Link Integrity Test function that allows backward compatibility with the 10BASE-T Link Integrity Test function of IEEE 802.3 figure 14-6. (See IEEE 802.3 clause 28.)

1.4.128 NLP sequence: A Normal Link Pulse sequence, defined in IEEE 802.3, 14.2.1.1 as TP_IDL.

1.4.129 Normal Link Pulse (NLP): An out-of-band communications mechanism used in 10BASE-T to indicate link status. (See IEEE 802.3 figure 14-12.)

1.4.130 NRZI-bit: A code-bit transferred in NRZI format. The unit of data passed across the PMD service interface in 100BASE-X.

1.4.131 NRZI: Non-Return-to-Zero, Invert on Ones. An encoding technique used in FDDI (ISO 9314-1: 1989, ISO 9314-2: 1989, ISO 9314-3: 1989) where a polarity transition represents a logical ONE. The absence of a polarity transition denotes a logical ZERO.

1.4.132 octet: A byte composed of eight bits. (From IEEE Std 610.7-1995 [A16].)

1.4.133 Optical Fiber Cable Interface: *See:* **FOMDI**.

1.4.134 Optical Fiber Cable Link Segment: A length of optical fiber cable that contains two optical fibers and is comprised of one or more optical fiber cable sections and their means of interconnection, with each optical fiber terminated at each end in the optical connector plug. (See IEEE 802.3, 9.9.5.1 and 9.9.5.2.)

1.4.135 optical fiber: A filament-shaped optical waveguide made of dielectric materials.

1.4.136 Optical Idle Signal: The signal transmitted by the FOMAU into its transmit optical fiber during the idle state of the DO circuit. (See IEEE 802.3 clause 9.)

1.4.137 Optical Interface: The optical input and output connection interface to a 10BASE-FP Star. (See IEEE 802.3 clause 15.)

1.4.138 out-of-band signaling: The transmission of a signal using a frequency that is within the pass band of the transmission facility but outside a frequency range normally used for data transmission. *Contrast with:* **in-band signaling**. (From IEEE Std. 610.7-1995 [A16].)

1.4.139 packet: Consists of a data frame as defined previously, preceded by the Preamble and the Start Frame Delimiter, encoded, as appropriate, for the PHY type.

1.4.140 page: In Auto-Negotiation, the encoding for a Link Code Word. Auto-Negotiation can support an arbitrary number of Link Code Word encodings. The base page has a constant encoding as defined in 28.2.1.2. Additional pages may have a predefined encoding *(see:* **Message Page**) or may be custom encoded *(see:* **Unformatted Page**).

1.4.141 parallel detection: In Auto-Negotiation, the ability to detect 100BASE-TX and 100BASE-T4 technology specific link signaling while also detecting the NLP sequence or FLP Burst sequence. (See IEEE 802.3 clause 28.)

1.4.142 Passive-Star Coupler: A component of a 10BASE-FP fiber optic mixing segment that divides optical power received at any of N input ports among all N output ports. The division of optical power is approximately uniform. (See IEEE 802.3 clause 15.)

1.4.143 patch cord: Flexible cable unit or element with connectors(s) used to establish connections on a patch panel. (From ISO/IEC 11801: 1995.)

1.4.144 patch panel: A cross-connect designed to accommodate the use of patch cords. It facilitates administration for moves and changes. (From ISO/IEC 11801: 1995.)

1.4.145 Path Delay Value (PDV): The sum of all Segment Delay Values for all segments along a given path. (See IEEE 802.3 clauses 13 and 29.)

1.4.146 Path Variability Value (PVV): The sum of all Segment Variability Values for all the segments along a given path. (See IEEE 802.3 clause 13.)

1.4.147 path: The sequence of segments and repeaters providing the connectivity between two DTEs in a single collision domain. In CSMA/CD networks there is one and only one path between any two DTEs.

1.4.148 Physical Coding Sublayer (PCS): A sublayer used in 100BASE-T to couple the MII and the PMA. The PCS contains the functions to encode data bits into code-groups that can be transmitted over the physical medium. Two PCS structures are defined for 100BASE-T—one for 100BASE-X and one for 100BASE-T4. (See IEEE 802.3 clauses 23 and 24.)

1.4.149 Physical Layer entity (PHY): The portion of the Physical Layer between the MDI and MII consisting of the PCS, PMA, and, if present, PMD sublayers. The PHY contains the functions that transmit, receive, and manage the encoded signals that are impressed on and recovered from the physical medium. (See IEEE 802.3 clauses 23–26.)

1.4.150 Physical Medium Attachment (PMA) sublayer: That portion of the Physical Layer that contains the functions for transmission, collision detection, reception, and (in the case of 100BASE-T4) clock recovery and skew alignment. (See IEEE 802.3 clauses 23 and 24.)

1.4.151 Physical Medium Dependent (PMD) sublayer: In 100BASE-X, that portion of the Physical Layer responsible for interfacing to the transmission medium. The PMD is located just above the MDI. (See IEEE 802.3 clause 24.)

1.4.152 Physical Signaling Sublayer (PLS): In 10BASE-T, that portion of the Physical Layer contained within the DTE that provides the logical and functional coupling between the MAU and the Data Link Layer.

1.4.153 port: A segment or IRL interface of a repeater unit.

1.4.154 postamble: In 10BROAD36, the bit pattern appended after the last bit of the Frame Check Sequence by the MAU. The Broadband End-of-Frame Delimiter (BEOFD). (See IEEE 802.3 clause 11.)

1.4.155 Priority Resolution Table: The look-up table used by Auto-Negotiation to select the network connection type where more than one common network ability exists (100BASE-TX, 100BASE-T4, 10BASE-T, etc.) The priority resolution table defines the relative hierarchy of connection types from the highest common denominator to the lowest common denominator. (See IEEE 802.3 clause 28.)

1.4.156 quad: *See:* **star quad**.

1.4.157 Reconciliation Sublayer (RS): A 100BASE-T mapping function that reconciles the signals at the MII to the MAC-PLS service definitions. (See IEEE 802.3 clause 22.)

1.4.158 remote fault: The generic ability of a link partner to signal its status even in the event that it may not have an operational receive link. (See IEEE 802.3 clause 28.)

1.4.159 renegotiation: Restart of the Auto-Negotiation algorithm caused by management or user interaction. (See IEEE 802.3 clause 28.)

1.4.160 repeater port: *See:* **port**.

1.4.161 repeater set: A repeater unit plus its associated Physical Layer interfaces (MAUs or PHYs) and, if present, AU or MI Interfaces (i.e., AUIs, MIIs).

1.4.162 repeater unit: The portion of a repeater that is inboard of its PMA/PLS or PMA/PCS interfaces.

1.4.163 repeater: A device used to extend the length, topology or interconnectivity of the physical medium beyond that imposed by a single segment, up to the maximum allowable end-to-end trunk transmission line length. Repeaters perform the basic actions of restoring signal amplitude, waveform, and timing applied to the normal data and collision signals. For wired star topologies, repeaters provide a data distribution function. In 100BASE-T, a device that allows the interconnection of 100BASE-T Physical Layer network

segments using similar or dissimilar PHY implementations (e.g., 100BASE-X to 100BASE-X, 100BASE-X to 100BASE-T4, etc.). (See IEEE 802.3 clauses 9 and 27.)

1.4.164 Return Loss: In 10BROAD36, the ratio in decibels of the power reflected from a port to the power incident to the port. An indicator of impedance matching in a broadband system. (See IEEE 802.3 clause 11.)

1.4.165 router: A layer 3 interconnection device that appears as a MAC to a CSMA/CD collision domain. (See IEEE Std 610.7-1995 [A16].)

1.4.166 Seed: In 10BROAD36, the 23 bits residing in the scrambler shift register prior to the transmission of a packet. (See IEEE 802.3 clause 11.)

1.4.167 Segment Delay Value (SDV): A number associated with a given segment that represents the delay on that segment including repeaters and end stations, if present, used to assess path delays for 10 Mb/s CSMA/CD networks. (See IEEE 802.3, 13.4.)

1.4.168 Segment Variability Value (SVV): A number associated with a given segment that represents the delay variability on that segment (including a repeater) for 10 Mb/s CSMA/CD networks. The SVVs for different segment types are specified in IEEE 802.3 table 13-3. (See IEEE 802.3, 13.4.)

1.4.169 segment: The medium connection, including connectors, between MDIs in a CSMA/CD LAN.

1.4.170 Selector field: A five-bit field in the Base Link Code Word encoding that is used to encode up to 32 types of messages that define basic abilities. For example, selector field 00001 indicates that the base technology is IEEE 802.3. (See IEEE 802.3 clause 28.)

1.4.171 shared service: A CSMA/CD network in which the collision domain consists of more than two DTEs so that the total network bandwidth is shared among them.

1.4.172 shielded twisted-pair (STP) cable: An electrically conducting cable, comprising one or more elements, each of which is individually shielded. There may be an overall shield, in which case the cable is referred to as shielded twisted pair cable with an overall shield. (From ISO/IEC 11801: 1995.) Specifically for IEEE 802.3 100BASE-TX, 150 | balanced inside cable with performance characteristics specified to 100 MHz (i.e., performance to Class D link standards as per ISO/IEC 11801: 1995). In addition to the requirements specified in ISO/IEC 11801: 1995, IEEE 802.3 clauses 23 and 25 provide additional performance requirements for 100BASE-T operation over STP.

1.4.173 Simplex Fiber Optic Link Segment: A single fiber path between two MAUs or PHYs, including the terminating connectors, consisting of one or more fibers joined serially with appropriate connection devices, for example, patch cables and wall plates. (See IEEE 802.3 clause 15.)

1.4.174 simplex link segment: A path between two MDIs, including the terminating connectors, consisting of one or more segments of twisted pair cable joined serially with appropriate connection devices, for example, patch cords and wall plates. (See IEEE 802.3 figure 14-2.)

1.4.175 skew between pairs: The difference in arrival times of two initially coincident signals propagated over two different pairs, as measured at the receiving end of the cable. Total skew includes contributions from transmitter circuits as well as the cable.

1.4.176 special link (SL): A transmission system that replaces the normal medium. (See IEEE 802.3, 12.8.)

1.4.177 Spectral Width, Full-Width Half Maximum (FWHM): The absolute difference between the wavelengths at which the spectral radiant intensity is 50% of the maximum. (See IEEE 802.3 clause 15.)

1.4.178 spectrum mask: A graphic representation of the required power distribution as a function of frequency for a modulated transmission.

1.4.179 star quad: A cable element that comprises four insulated connectors twisted together. Two diametrically facing conductors form a transmission pair. *Note*—Cables containing star quads can be used interchangeably with cables consisting of pairs, provided the electrical characteristics meet the same specifications. (From ISO/IEC 11801: 1995.)

1.4.180 Start-of-Stream Delimiter (SSD): A pattern of defined code words used to delineate the boundary of a data transmission sequence on the Physical Layer stream. The SSD is unique in that it may be recognized independent of previously defined code-group boundaries and it defines subsequent code-group boundaries for the stream it delimits. For 100BASE-T4, SSD is a pattern of three predefined sosb code-groups (one per wire pair) indicating the positions of the first data code-group on each wire pair. For 100BASE-X, SSD consists of the code-group sequence /J/K/.

1.4.181 stream: The Physical Layer encapsulation of a MAC frame. Depending on the particular PHY, the MAC frame may be modified or have information appended or prepended to it to facilitate transfer through the PMA. Any conversion from a MAC frame to a PHY stream and back to a MAC frame is transparent to the MAC. (See IEEE 802.3 clauses 23 and 24.)

1.4.182 symbol: The smallest unit of data transmission on the medium. Symbols are unique to the coding system employed. 100BASE-T4 uses ternary symbols; 10BASE-T and 100BASE-X use binary symbols or code bits.

1.4.183 symbol rate (SR): The total number of symbols per second transferred to or from the Media Dependent Interface (MDI) on a single wire pair. For 100BASE-T4, the symbol rate is 25 megabaud; for 100BASE-X, the symbol rate is 125 megabaud.

1.4.184 symbol time (ST): The duration of one symbol as transferred to and from the MDI via a single wire pair. The symbol time is the reciprocal of the symbol rate.

1.4.185 Technology Ability Field: An eight-bit field in the Auto-Negotiation base page that is used to indicate the abilities of a local station, such as support for 10BASE-T, 100BASE-TX, 100BASE-T4, as well as full-duplex capabilities.

1.4.186 ternary symbol: In 100BASE-T4, a ternary data element. A ternary symbol can have one of three values: –1, 0, or +1. (See IEEE 802.3 clause 23.)

1.4.187 translation: In a single-cable 10BROAD36 system, the process by which incoming transmissions at one frequency are converted into another frequency for outgoing transmission. The translation takes place at the headend. (See IEEE 802.3 clause 11.)

1.4.188 truncation loss: In a modulated data waveform, the power difference before and after implementation filtering necessary to constrain its spectrum to a specified frequency band.

1.4.189 trunk cable: The main (often large diameter) cable of a coaxial cable system. (*See:* **drop cable**.)

1.4.190 twisted-pair cable binder group: A group of twisted pairs within a cable that are bound together. Large telephone cables have multiple binder groups with high interbinder group near-end crosstalk loss.

1.4.191 twisted-pair cable: A bundle of multiple twisted pairs within a single protective sheath. (From ISO/IEC 11801: 1995.)

1.4.192 twisted-pair link: A twisted-pair cable plus connecting hardware. (From ISO/IEC 11801: 1995.)

1.4.193 twisted-pair link segment: In 100BASE-T, a twisted-pair link for connecting two PHYs.

1.4.194 twisted pair: A cable element that consists of two insulated conductors twisted together in a regular fashion to form a balanced transmission line. (From ISO/IEC 11801: 1995.)

1.4.195 Unformatted Page (UP): A Next Page encoding that contains an unformatted 12-bit message field. Use of this field is defined through Message Codes and information contained in the UP. (See IEEE 802.3, 28.2.1.2.)

1.4.196 unshielded twisted-pair cable (UTP): An electrically conducting cable, comprising one or more pairs, none of which is shielded. There may be an overall shield, in which case the cable is referred to as unshielded twisted pair with overall shield. (From ISO/IEC 11801: 1995.)

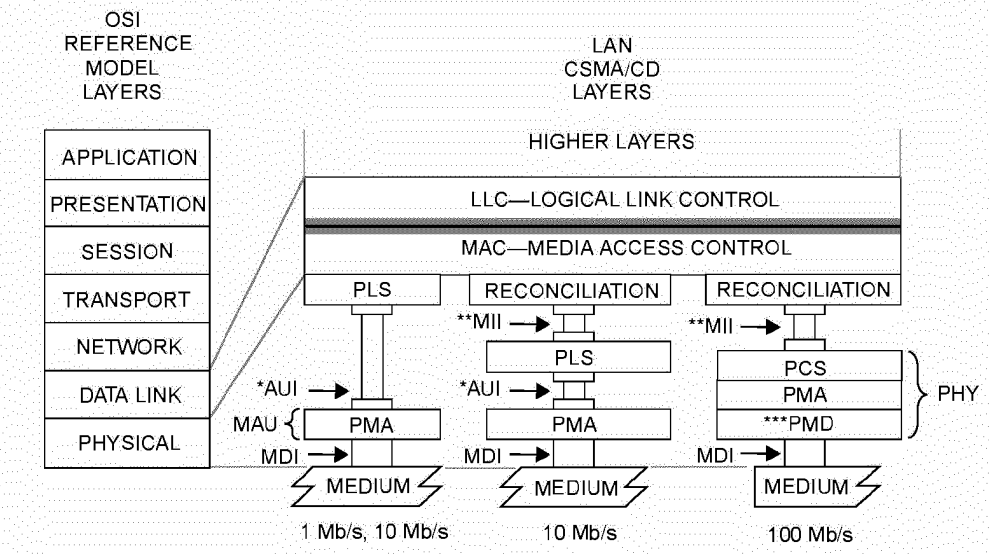
1.4.197 weight of 6T code group: The algebraic sum of the logical ternary symbol values listed in the 100BASE-T4 8B6T code table. (See IEEE 802.3 clause 23.)

Remove the definitions from 7.1.1, 8.1.2, 9.2, 10.1.2, 11.1.2, 12.1.3, 13.2, 14.1.2, 15.1.2, and 19.1.3 and insert the following text under each of these subclauses:

See 1.4.

2. MAC service specification

Replace figure 2-1 with the following:



AUI = ATTACHMENT UNIT INTERFACE
MDI = MEDIUM DEPENDENT INTERFACE
MII = MEDIA INDEPENDENT INTERFACE
MAU = MEDIUM ATTACHMENT UNIT

PLS = PHYSICAL LAYER SIGNALING
PCS = PHYSICAL CODING SUBLAYER
PMA = PHYSICAL MEDIUM ATTACHMENT
PHY = PHYSICAL LAYER DEVICE
PMD = PHYSICAL MEDIUM DEPENDENT

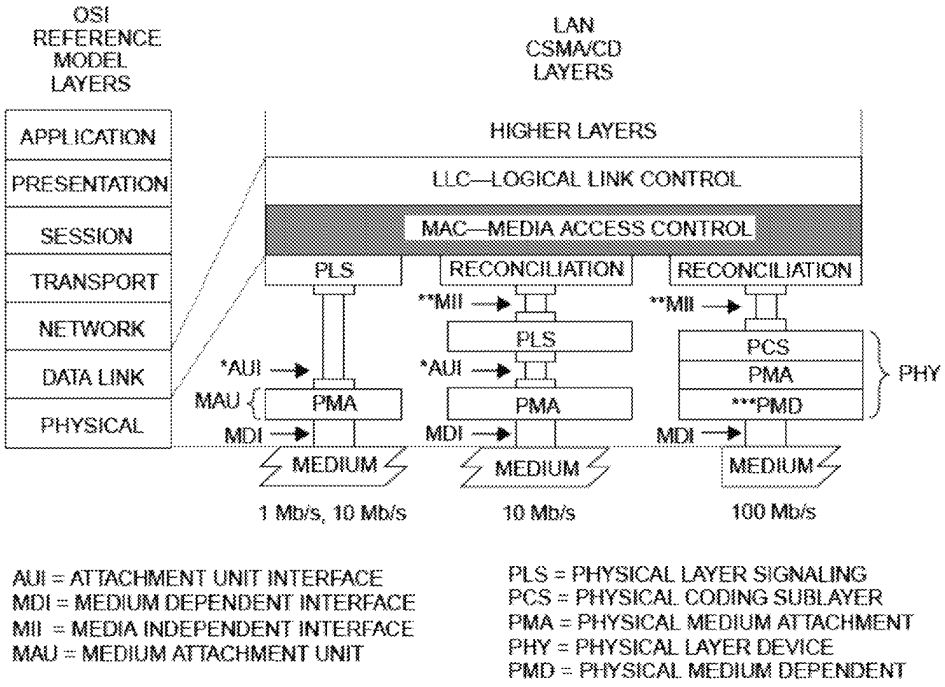
NOTE—The three types of layers below the MAC sublayer are mutually independent.

* AUI is optional for 10 Mb/s systems and is not specified for 1 Mb/s and 100 Mb/s systems.
** MII is optional for 10 Mb/s DTEs and for 100 Mb/s systems and is not specified for 1 Mb/s systems.
*** PMD is specified for 100BASE-X only; 100BASE-T4 does not use this layer.
For an exposed AUI residing below an MII, see 22.5.

Figure 2-1—Service specification relation to the LAN model

4. Media Access Control

Replace figure 4-1 with the following:



NOTE—The three types of layers below the MAC sublayer are mutually independent.

* AUI is optional for 10 Mb/s systems and is not specified for 1 Mb/s and 100 Mb/s systems.
** MII is optional for 10 Mb/s DTEs and for 100 Mb/s systems and is not specified for 1 Mb/s systems.
*** PMD is specified for 100BASE-X only; 100BASE-T4 does not use this layer.
For an exposed AUI residing below an MII, see 22.5.

Figure 4-1—MAC sublayer partitioning, relationship to the ISO Open Systems Interconnection (OSI) reference model

Add to 4.4.2 the following subclause:

4.4.2.3 Parameterized values

The following parameter values shall be used for 100 Mb/s implementations:

Parameters	Values
slotTime	512 bit times
interFrameGap	0.96 µs
attemptLimit	16
backoffLimit	10
jamSize	32 bits
maxFrameSize	1518 octets
minFrameSize	512 bits (64 octets)
addressSize	48 bits

WARNING—Any deviation from the above specified values may affect proper operation of the network.

5. Layer management

Insert before 5.1:

Clause 5 is deprecated by clause 30.

14. Twisted-pair Medium Attachment Unit (MAU) and baseband medium, Type 10BASE-T

EDITORIAL NOTE—The following changes add references to Auto-Negotiation and specifications for Auto-Negotiation to the appropriate places in clause 14 of ISO/IEC 8802-3: 1993 [ANSI/IEEE Std 802.3-1993 Edition] and IEEE Std 802.3l-1992. (These changes will also identically affect the 1995 edition of ISO/IEC 8802-3.) The changes do not alter the specifications for existing systems.

In 14.2, renumber the list items (1) through (7) as a) through g) and add the following paragraph as the eighth functional capability:

h) Auto-Negotiation. Optionally provides the capability for a device at one end of a link segment to advertise its abilities to the device at the other end (its link partner), to detect information defining the abilities of the link partner, and to determine if the two devices are compatable.

Add to 14.2.1 the following sentence to the end of the paragraph:

The MAU may optionally provide the Auto-Negotiation algorithm. When provided, the Auto-Negotiation algorithm shall be implemented in accordance with clause 28.

Add to 14.2.1.1 the following paragraph after the fourth paragraph:

For a MAU that implements the Auto-Negotiation algorithm defined in clause 28, clause 28 shall define the allowable transmitted link pulse sequence.

Add to 14.2.1.7 the following sentence at the end of the fourth paragraph:

For a MAU that implements the Auto-Negotiation algorithm defined in clause 28, the MAU shall enter the LINK TEST FAIL RESET state at power-on as specified in clause 28. For a MAU that does not implement the Auto-Negotiation algorithm defined in clause 28, it is highly recommended that it also power-on in the LINK TEST FAIL RESET state, although implementations may power-on in the LINK TEST PASS state. For a MAU that implements the Auto-Negotiation function defined in clause 28, the Auto-Negotiation Technology Dependent Interface shall be supported. Supporting the Technology Dependent Interface requires that in the Link Integrity Test function state diagram 'link_status=OK' is added to the LINK TEST PASS state and 'link_status=FAIL' is added to the LINK TEST FAIL RESET state. Note these ISO message variables follow the conventions of clause 21.

Add to 14.3.1.2.1 the following paragraph after the sixth paragraph:

For a MAU that implements the Auto-Negotiation algorithm defined in clause 28, the FLP Burst Sequence will consist of multiple link test pulses. All link test pulses in the FLP Burst sequence shall meet the template requirements of figure 14-12 when measured across each of the test loads defined in figure 14-11; both with the load connected directly to the TD circuit and with the load connected through the twisted-pair model as defined in figures 14-7 and 14-8.

Add to 14.10.4.5.1 the following entry as the eighth parameter:

	Parameter	Section	Req	Imp	Value/Comment
8	Auto-Negotiation		C		Function provided by MAUs implementing the Auto-Negotiation algorithm, as defined in clause 28

Add this new subclause after 14.10.4.7:

14.10.4.8 PICS proforma tables for Auto-Negotiation-able MAUs

The following are conditional on whether the Auto-Negotiation algorithm is provided (clause 28).

	Parameter	Section	Req	Imp	Value/Comment
1	TP_IDL	14.2.1.1	C		Defined in clause 28.2.1
2	Link Integrity Test Function State Diagram power-on default	14.2.1.7	C		Power-on in Link Test Fail Reset state
3	Link Test Fail state exit conditions	14.2.1.7	C		autoneg_wait_timer expired and either RD = active or consecutive link test pulses = 3 min., 10 max
4	Technology Dependent Interface support	14.2.1.7	C		In the Link Integrity Test state diagram function 'link_status=OK' is added to the LINK TEST PASS state and 'link_status=FAIL' is added to the LINK TEST FAIL RESET state
5	Link test pulse waveform for FLP Burst with and without twisted-pair model	14.3.1.2.1	C		Within figure 14-10 template for, all pulses in FLP Burst, overshoot " +50 mV after excursion below –50 mV

19. Layer management for 10 Mb/s baseband repeaters

EDITORIAL NOTE—This clause can be found in IEEE Std 802.3k-1992.

Insert the following phrase in front of 19.1:

Clause 19 is deprecated by clause 30.

20. Layer management for 10 Mb/s baseband Medium Attachment Units (MAUs)

EDITORIAL NOTE—This clause can be found in IEEE Stds 802.3p&q-1993.

Insert the following phrase in front of 20.1:

Clause 20 is deprecated by clause 30.

Annex A

(informative)[11]

Additional reference material

EDITORIAL NOTES

1—This clause was changed from Annex to Annex A by IEEE Std 802.3j-1993.

2—In the following references, changes are not indicated by strikethroughs and underscores.

3—The reference numbers in this annex do not correspond to those of ISO/IEC 8802-3: 1993 or the 1995 edition of ISO/IEC 8802-3.

Replace annex A with the following:

[A1] ANSI/EIA 364A: 1987, Standard Test Procedures for Low-Frequency (Below 3 MHz) Electrical Connector Test Procedure.

[A2] ANSI/EIA 455-34: 1985, Fiber Optics—Interconnection Device Insertion Loss Test.

[A3] ANSI/EIA/TIA 455-59-1989, Measurement of Fiber Point Defects Using an Optical Time Domain Reflectometer (ODTR).

[A4] ANSI/EIA/TIA 455-180-1990, FOTP-180, Measurement of the Optical Transfer Coefficients of a Passive Branching Device (Coupler).

[A5] ANSI/EIA/TIA 526-14-1990, Optical Power Loss Measurements of Installed Multimode Fiber Cable Plant.

[A6] ANSI/EIA/TIA 568-1991, Commercial Building Telecommunications Wiring Standard.

[A7] ANSI/IEEE Std 770X3.97-1983, IEEE Standard Pascal Computer Programming Language.[12]

[A8] ANSI/NFPA 70-1993, National Electrical Code.

[A9] ANSI/UL 94-1990, Tests for Flammability of Plastic Materials for Parts in Devices and Appliances.

[A10] ANSI/UL 114-1982, Safety Standard for Office Appliances and Business Equipment.[13]

[11]This annex is informative for the International Standard but normative for IEEE Std 802.3.

[12]ANSI/IEEE Std 770X3.97-1983 has been withdrawn; however, copies can be obtained from Global Engineering, 15 Inverness Way East, Englewood, CO 80112-5704, USA, tel. (303) 792-2181.

[13]ANSI/UL 114-1982 was withdrawn and replaced by ANSI/UL 1950-1994.

[A11] ANSI/UL 478-1979, Safety Standard for Electronic Data-Processing Units and Systems.[14]

[A12] ANSI/UL 1950-1994, Safety Standard for Information Technology Equipment Including Electrical Business Equipment.

[A13] ECMA-97 (1985), Local Area Networks Safety Requirements.

[A14] EIA CB8-1981, Components Bulletin (Cat 4) List of Approved Agencies, US and Other Countries, Impacting Electronic Components and Equipment.

[A15] FCC Docket 20780-1980 (Part 15), Technical Standards for Computing Equipment. Amendment of Part 15 to redefine and clarify the rules governing restricted radiation devices and low-power communication devices. Reconsidered First Report and Order, April 1980.

[A16] IEEE Std 610.7-1995, IEEE Standard Glossary of Computer Networking Terminology.

[A17] IEEE Std 802.9a-1995, IEEE Standards for Local and Metropolitan Area Networks: Integrated Services (IS) LAN: IEEE 802.9 Isochronous Services with Carrier Sense Multiple Access with Collision Detection (CSMA/CD) Media Access Control (MAC) Service.[15]

[A18] IEEE P1394/D8.0v3, Draft Standard for a High-Performance Serial Bus (July 7, 1995).

[A19] MIL-C-17F-1983, General Specification for Cables, Radio Frequency, Flexible and Semirigid.

[A20] MIL-C-24308B-1983, General Specifications for Connector, Electric, Rectangular, Miniature Polarized Shell, Rack and Panel.

[A21] AMP, Inc., Departmental Publication 5525, Design Guide to Coaxial Taps. Harrisburg, PA 17105, USA.

[A22] AMP, Inc., Instruction Sheet 6814, Active Tap Installation. Harrisburg, PA 17105, USA.

[A23] Brinch Hansen, P. *The Architecture of Concurrent Programs.* Englewood Cliffs, NJ: Prentice Hall, 1977.

[A24] Digital Equipment Corporation, Intel, Xerox, The Ethernet, Version 2.0, November 1982.

[A25] Hammond, J. L., Brown, J. E., and Liu, S. S. Development of a Transmission Error Model and Error Control Model. Technical Report RADC-TR-75-138. Rome: Air Development Center (1975).

[A26] Shoch, J. F., Dalal, Y. K., Redell, D. D., and Crane, R. C., "The Evolution of Ethernet," *Computer Magazine*, August 1982.

[A27] UL Subject No 758: UL VW-1, Description of Appliance Wiring Material.

[14]ANSI/UL 478-1979 was withdrawn and replaced by ANSI/UL 1950-1994.

[15]As this standard goes to press, IEEE Std 802.9a-1995 is approved but not yet published. The approved draft standard is, however, available from the IEEE. Anticipated publication date is early 1996. Contact the IEEE Standards Department at 1 (908) 562-3800 for status information.

Annex D

(normative)

GDMO specifications for CSMA/CD managed objects

EDITORIAL NOTE—This annex can be found in IEEE Stds 802.3p&q-1993.

Insert the following note at three places immediately following the headings D1, D2, and D3:

NOTE—The arcs (that is, object identifier values) defined in annex 30A deprecate the arcs previously defined in D1 (Layer Management), D2 (Repeater Management), and D3 (MAU Management). See IEEE Std 802.1F-1993, annex C4.

IEEE Standards for Local and Metropolitan Area Networks:

Supplement to Carrier Sense Multiple Access with Collision Detection (CSMA/CD) Access Method and Physical Layer Specifications

Media Access Control (MAC) Parameters, Physical Layer, Medium Attachment Units, and Repeater for 100 Mb/s Operation, Type 100BASE-T (Clauses 21–30)

21. Introduction to 100 Mb/s baseband networks, type 100BASE-T

21.1 Overview

100BASE-T couples the ISO/IEC 8802-3 CSMA/CD MAC with a family of 100 Mb/s Physical Layers. While the MAC can be readily scaled to higher performance levels, new Physical Layer standards are required for 100 Mb/s operation.

The relationships between 100BASE-T, the existing ISO/IEC 8802-3 (CSMA/CD MAC), and the ISO Open System Interconnection (OSI) reference model is shown in figure 21-1.

100BASE-T uses the existing ISO/IEC 8802-3 MAC layer interface, connected through a Media-Independent Interface layer to a Physical Layer entity (PHY) sublayer such as 100BASE-T4, 100BASE-TX, or 100BASE-FX.

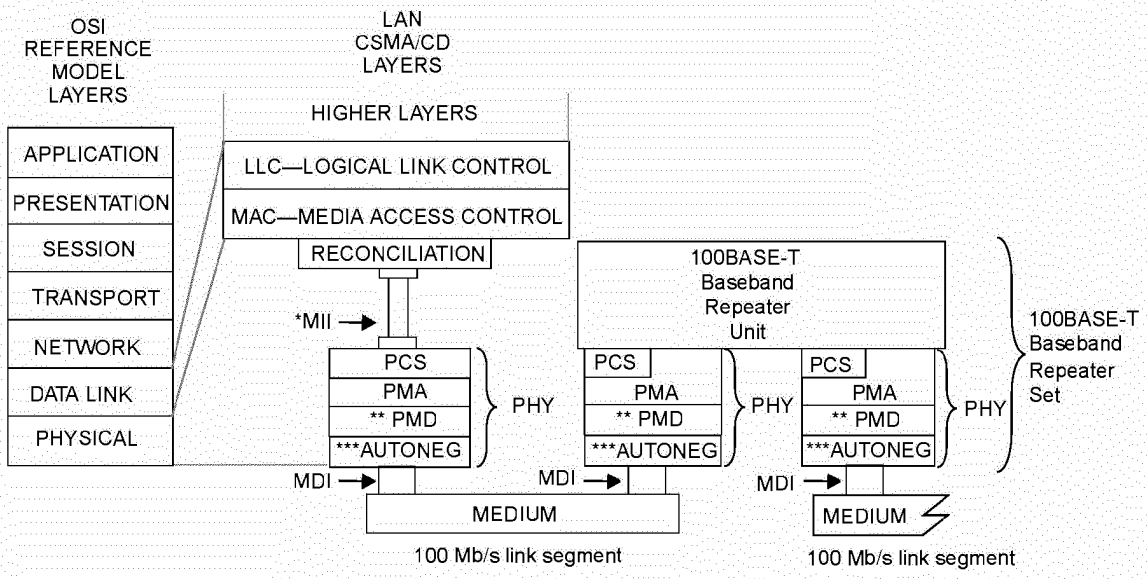
100BASE-T extends the ISO/IEC 8802-3 MAC to 100 Mb/s. The bit rate is faster, bit times are shorter, packet transmission times are reduced, and cable delay budgets are smaller—all in proportion to the change in bandwidth. This means that the ratio of packet duration to network propagation delay for 100BASE-T is the same as for 10BASE-T.

21.1.1 Reconciliation Sublayer (RS) and Media Independent Interface (MII)

The Media Independent Interface (clause 22) provides an interconnection between the Media Access Control (MAC) sublayer and Physical Layer entities (PHY) and between PHY Layer and Station Management (STA) entities. This MII is capable of supporting both 10 Mb/s and 100 Mb/s data rates through four bit wide (nibble wide) transmit and receive paths. The Reconciliation sublayer provides a mapping between the signals provided at the MII and the MAC/PLS service definition.

21.1.2 Physical Layer signaling systems

This standard specifies a family of Physical Layer implementations. 100BASE-T4 (clause 23) uses four pairs of ISO/IEC 11801: 1995 Category 3, 4, or 5 balanced cable. 100BASE-TX (clauses 24 and 25) uses two pairs of Category 5 balanced cable or 150 Ω shielded balanced cable as defined by ISO/IEC 11801: 1995. 100BASE-FX (clauses 24 and 26) uses two multi-mode fibers. FDDI (ISO 9314 and ANSI X3T12) Physical Layers are used to provide 100BASE-TX and 100BASE-FX physical signaling channels, which are defined in 100BASE-X (clause 24).



MDI = MEDIUM DEPENDENT INTERFACE
MII = MEDIA INDEPENDENT INTERFACE
PCS = PHYSICAL CODING SUBLAYER
PMA = PHYSICAL MEDIUM ATTACHMENT
PHY = PHYSICAL LAYER DEVICE
PMD = PHYSICAL MEDIUM DEPENDENT

* MII is optional for 10 Mb/s DTEs and for 100 Mb/s systems and is not specified for 1 Mb/s systems.
** PMD is specified for 100BASE-X only; 100BASE-T4 does not use this layer.
Use of MII between PCS and Baseband Repeater Unit is optional.
*** AUTONEG is optional.

Figure 21-1—Architectural positioning of 100BASE-T

21.1.3 Repeater

Repeater sets (clause 27) are an integral part of any 100BASE-T network with more than two DTEs in a collision domain. They extend the physical system topology by coupling two or more segments. Multiple repeaters are permitted within a single collision domain to provide the maximum path length.

21.1.4 Auto-Negotiation

Auto-Negotiation (clause 28) provides a linked device with the capability to detect the abilities (modes of operation) supported by the device at the other end of the link, determine common abilities, and configure for joint operation. Auto-Negotiation is performed out-of-band using a pulse code sequence that is compatible with the 10BASE-T link integrity test sequence.

21.1.5 Management

Managed objects, attributes, and actions are defined for all 100BASE-T components (clause 30). This clause consolidates all IEEE 802.3 management specifications so that 10 Mb/s, 100 Mb/s or 10/100 Mb/s agents can be managed by existing 10 Mb/s-only network management stations with little or no modification to the agent code.

21.2 Abbreviations

This document contains the following abbreviations:

8802-3	ISO/IEC 8802-3 (IEEE Std 802.3)
8802-5	ISO/IEC 8802-5 (IEEE Std 802.5)
ASIC	application-specific integrated circuit
ASN.1	abstract syntax notation one as defined in ISO/IEC 8824: 1990
AUI	attachment unit interface
BPSK	binary phase shift keying
BR	bit rate
BT	bit time
CAT3	Category 3 balanced cable
CAT4	Category 4 balanced cable
CAT5	Category 5 balanced cable
CD0	clocked data zero
CD1	clocked data one
CMIP	common management information protocol as defined in ISO/IEC 9596-1: 1991
CMIS	common management information service as defined in ISO/IEC 9595: 1991
CMOS	complimentary metal oxide semiconductor
CRC	cyclic redundancy check
CVH	clocked violation high
CVL	clocked violation low
CRV	code rule violation
CS0	control signal zero
CS1	control signal one
CW	continuous wave
DTE	data terminal equipment
ELFEXT	equal-level far-end crosstalk
ESD	end of stream delimiter
FCS	frame check sequence
FDDI	fibre distributed data interface
FEXT	far-end crosstalk
FIFO	first in, first out
FLP	fast link pulse
FOIRL	fiber optic inter-repeater link
FOMAU	fiber optic medium attachment unit
FOMDI	fiber optic medium dependent interface
FOPMA	fiber optic physical medium attachment
HH	header hub
IH	intermediate hub
IPG	inter-packet gap
IRL	inter-repeater link
LAN	local area network
LLC	logical link control
LSDV	link segment delay value
MAC	medium access control
MAU	medium attachment unit
MC	message code
MDELFEXT	multiple-disturber equal-level far-end crosstalk
MDFEXT	multiple-disturber far-end crosstalk
MDI	medium dependent interface
MDNEXT	multiple-disturber near-end crosstalk
MIB	management information base

MII	media independent interface
MP	message page
NEXT	near-end crosstalk
NLP	normal link pulse
NPA	next page algorithm
NRZI	non return to zero and invert on ones
PCS	physical coding sublayer
PDV	path delay value
PHY	Physical Layer entity sublayer
PICS	protocol implementation conformance statement
PLS	physical signaling sublayer
PMA	physical medium attachment
PMD	physical medium dependent
PMI	physical medium independent
PVV	path variability value
RS	reconciliation sublayer
SSD	start-of-stream delimiter
SDV	segment delay value
SFD	start-of-frame delimiter
SR	symbol rate
ST	symbol time
STA	station management entity
STP	shielded twisted pair (copper)
SVV	segment variability value
UCT	unconditional transition
UP	unformatted page
UTP	unshielded twisted pair

21.3 References

References are shown beginning on pages 2 and 23 of this document (as updates to 1.3 and annex A).

21.4 Definitions

Definitions are shown beginning on page 5 of this document (as an update to 1.4).

21.5 State diagrams

State machine diagrams take precedence over text.

The conventions of 1.2 are adopted, with the following extensions.

21.5.1 Actions inside state blocks

The actions inside a state block execute instantaneously. Actions inside state blocks are atomic (i.e., uninterruptible).

After performing all the actions listed in a state block one time, the state block then continuously evaluates its exit conditions until one is satisfied, at which point control passes through a transition arrow to the next block. While the state awaits fulfillment of one of its exit conditions, the actions inside do not implicitly repeat.

The characters • and [bracket] are *not* used to denote any special meaning.

Valid state actions may include .indicate and request messages.

No actions are taken outside of any state block.

21.5.2 State diagram variables

Once set, variables retain their values as long as succeeding blocks contain no references to them.

Setting the parameter of a formal interface message assures that, on the next transmission of that message, the last parameter value set will be transmitted.

Testing the parameter of a formal interface messages tests the value of that message parameter that was received on the last transmission of said message. Message parameters may be assigned default values that persist until the first reception of the relevant message.

21.5.3 State transitions

The following terms are valid transition qualifiers:

a) Boolean expressions
b) An event such as the expiration of a timer: timer_done
c) An event such as the reception of a message: PMA_UNITDATA.indicate
d) An unconditional transition: UCT
e) A branch taken when other exit conditions are not satisfied: ELSE

Any open arrow (an arrow with no source block) represents a global transition. Global transitions are evaluated continuously whenever any state is evaluating its exit conditions. When a global transition becomes true, it supersedes all other transitions, including UCT, returning control to the block pointed to by the open arrow.

21.5.4 Operators

The state machine operators are shown in table 21-1.

Table 21-1—State machine operators

Character	Meaning
*	Boolean AND
+	Boolean OR
⊕	Boolean XOR
!	Boolean NOT
<	Less than
″	Less than or equal to
=	Equals (a test of equality)
↑	Not equals
≥	Greater than or equal to
>	Greater than
( )	Indicates precedence
⇐	Assignment operator
∈	Indicates membership
∉	Indicates nonmembership
ELSE	No other state condition is satisfied

21.6 Protocol Implementation Conformance Statement (PICS) proforma

21.6.1 Introduction

The supplier of a protocol implementation that is claimed to conform to any part of the IEEE 802.3u 100BASE-T clauses 21 through 30 shall complete a Protocol Implementation Conformance Statement (PICS) proforma.

A completed PICS proforma is the PICS for the implementation in question. The PICS is a statement of which capabilities and options of the protocol have been implemented. A PICS is included at the end of each clause as appropriate. The PICS can be used for a variety of purposes by various parties, including the following:

a) As a checklist by the protocol implementor, to reduce the risk of failure to conform to the standard through oversight;
b) As a detailed indication of the capabilities of the implementation, stated relative to the common basis for understanding provided by the standard PICS proforma, by the supplier and acquirer, or potential acquirer, of the implementation;
c) As a basis for initially checking the possibility of interworking with another implementation by the user, or potential user, of the implementation (note that, while interworking can never be guaranteed, failure to interwork can often be predicted from incompatible PICS);
d) As the basis for selecting appropriate tests against which to assess the claim for conformance of the implementation, by a protocol tester.

21.6.2 Abbreviations and special symbols

The following symbols are used in the PICS proforma:

M	mandatory field/function
O	optional field/function
O.<n>	optional field/function, but at least one of the group of options labeled by the same numeral <n> is required
O/<n>	optional field/function, but one and only one of the group of options labeled by the same numeral <n> is required
X	prohibited field/function
<item>:	simple-predicate condition, dependent on the support marked for <item>
<item1>*<item2>:	AND-predicate condition, the requirement must be met if both optional items are implemented

21.6.3 Instructions for completing the PICS proforma

The first part of the PICS proforma, Implementation Identification and Protocol Summary, is to be completed as indicated with the information necessary to identify fully both the supplier and the implementation.

The main part of the PICS proforma is a fixed-format questionnaire divided into subclauses, each containing a group of items. Answers to the questionnaire items are to be provided in the right-most column, either by simply marking an answer to indicate a restricted choice (usually Yes, No, or Not Applicable), or by entering a value or a set or range of values. (Note that there are some items where two or more choices from a set of possible answers can apply; all relevant choices are to be marked.)

Each item is identified by an item reference in the first column; the second column contains the question to be answered; the third column contains the reference or references to the material that specifies the item in the main body of the standard; the sixth column contains values and/or comments pertaining to the question

to be answered. The remaining columns record the status of the items—whether the support is mandatory, optional or conditional—and provide the space for the answers.

The supplier may also provide, or be required to provide, further information, categorized as either Additional Information or Exception Information. When present, each kind of further information is to be provided in a further subclause of items labeled A<i> or X<i>, respectively, for cross-referencing purposes, where <i> is any unambiguous identification for the item (e.g., simply a numeral); there are no other restrictions on its format or presentation.

A completed PICS proforma, including any Additional Information and Exception Information, is the Protocol Implementation Conformance Statement for the implementation in question.

Note that where an implementation is capable of being configured in more than one way, according to the items listed under Major Capabilities/Options, a single PICS may be able to describe all such configurations. However, the supplier has the choice of providing more than one PICS, each covering some subset of the implementation's configuration capabilities, if that would make presentation of the information easier and clearer.

21.6.4 Additional information

Items of Additional Information allow a supplier to provide further information intended to assist the interpretation of the PICS. It is not intended or expected that a large quantity will be supplied, and the PICS can be considered complete without any such information. Examples might be an outline of the ways in which a (single) implementation can be set up to operate in a variety of environments and configurations; or a brief rationale, based perhaps upon specific application needs, for the exclusion of features that, although optional, are nonetheless commonly present in implementations.

References to items of Additional Information may be entered next to any answer in the questionnaire, and may be included in items of Exception Information.

21.6.5 Exceptional information

It may occasionally happen that a supplier will wish to answer an item with mandatory or prohibited status (after any conditions have been applied) in a way that conflicts with the indicated requirement. No preprinted answer will be found in the Support column for this; instead, the supplier is required to write into the Support column an X<i> reference to an item of Exception Information, and to provide the appropriate rationale in the Exception item itself.

An implementation for which an Exception item is required in this way does not conform to this standard.

Note that a possible reason for the situation described above is that a defect in the standard has been reported, a correction for which is expected to change the requirement not met by the implementation.

21.6.6 Conditional items

The PICS proforma contains a number of conditional items. These are items for which both the applicability of the item itself, and its status if it does apply—mandatory, optional, or prohibited—are dependent upon whether or not certain other items are supported.

Individual conditional items are indicated by a conditional symbol of the form "<item>:<s>" in the Status column, where "<item>" is an item reference that appears in the first column of the table for some other item, and "<s>" is a status symbol, M (Mandatory), O (Optional), or X (Not Applicable).

If the item referred to by the conditional symbol is marked as supported, then 1) the conditional item is applicable, 2) its status is given by "<s>", and 3) the support column is to be completed in the usual way. Otherwise, the conditional item is not relevant and the Not Applicable (N/A) answer is to be marked.

Each item whose reference is used in a conditional symbol is indicated by an asterisk in the Item column.

21.7 Relation of 100BASE-T to other standards

Suitable entries for table G1 of ISO/IEC 11801: 1995, annex G, would be as follows:

a) Within the section Balanced Cable Link Class C (specified up to 16 MHz):
CSMA/CD 100BASE-T4 ISO/IEC 8802-3/DAD 1995 4
b) Within the section Optical Link:
CSMA/CD 100BASE-FX ISO/IEC 8802-3/DAD 1995 2
c) Within the section Balanced Cable Link Class D (Defined up to 100 MHz):
CSMA/CD 100BASE-TX ISO/IEC 8802-3/DAD 1995 2

NOTE—To support 100BASE-T4 applications, class C links shall have a NEXT value of at least 3 dB in excess of the values specified in 6.2.4.

Suitable entries for table G2 of ISO/IEC 11801: 1995, annex G, would be as follows:

	Balanced cabling per clauses 5, 7, and 8							**Performance based cabling per clause 6**												
								Class A			**Class B**			**Class C**			**Class D**		
	Cat 3 100 Ω	**Cat 4 100 Ω**	**Cat 5 100 Ω**	**Cat 3 120 Ω**	**Cat 4 120 Ω**	**Cat 5 120 Ω**	**150 Ω**	**100 Ω**	**120 Ω**	**150 Ω**	**100 Ω**	**120 Ω**	**150 Ω**	**100 Ω**	**120 Ω**	**150 Ω**	**100 Ω**	**120 Ω**	**150 Ω**
8802-3: 100BASE-T4	I*	I*	I*		I	I								I			I*	I	
8802-3: 100BASE-TX			I*				I*										I*		I*

*8802-3 imposes additional requirements on propagation delay.

A suitable entry for table G3 of ISO/IEC 11801: 1995, annex G, would be as follows:

	Fibre per 5, 7, and 8			Optical link per clause 8								
				Horizontal			Building backbone			Campus backbone		
	62.5/125 μm MMF	50/125 μm MMF	10/125 μm MMF	62.5/125 μm MMF	50/125 μm MMF	10/125 μm MMF	62.5/125 μm MMF	50/125 μm MMF	10/125 μm MMF	62.5/125 μm MMF	50/125 μm MMF	10/125 μm MMF
8802-3: 100BASE-FX	N	I		N	I		N	I		N	I	

21.8 MAC delay constraints (exposed MII)

100BASE-T makes the following assumptions about MAC performance. These assumptions apply to any MAC with an exposed MII used with a 100BASE-T PHY.

Table 21-2—MAC delay assumptions (exposed MII)

Sublayer measurement points	Event	Min (bits)	Max (bits)	Input timing reference	Output timing reference
MAC ⇔ MII	MAC transmit start to TX_EN sampled		4		TX_CLK rising
	CRS assert to MAC detect	0	8		
	CRS de-assert to MAC detect	0	8		
	CRS assert to TX_EN sampled (worst case nondeferred transmit)		16		TX_CLK rising
	COL assert to MAC detect	0	8		
	COL de-assert to MAC detect	0	8		
	COL assert to TXD = Jam sampled (worst-case collision response)		16		TX_CLK rising; first nibble of jam

22. Reconciliation Sublayer (RS) and Media Independent Interface (MII)

22.1 Overview

This clause defines the logical, electrical, and mechanical characteristics for the Reconciliation Sublayer (RS) and Media Independent Interface (MII) between CSMA/CD media access controllers and various PHYs. Figure 22-1 shows the relationship of the Reconciliation sublayer and MII to the ISO (IEEE) OSI reference model.

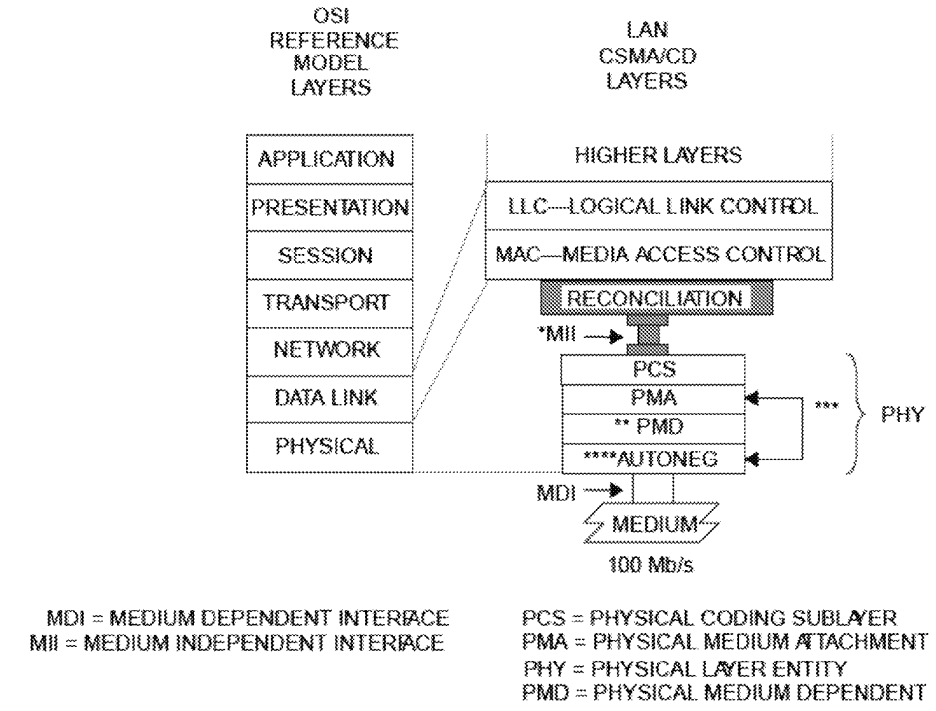


Figure 22-1—MII location in the protocol stack

The purpose of this interface is to provide a simple, inexpensive, and easy-to-implement interconnection between Media Access Control (MAC) sublayer and PHYs, and between PHYs and Station Management (STA) entities.

This interface has the following characteristics:

a) It is capable of supporting both 10 Mb/s and 100 Mb/s data rates.
b) Data and delimiters are synchronous to clock references.
c) It provides independent four bit wide transmit and receive data paths.
d) It uses TTL signal levels, compatible with common digital CMOS ASIC processes.
e) It provides a simple management interface.
f) It is capable of driving a limited length of shielded cable.

22.1.1 Summary of major concepts

a) Each direction of data transfer is serviced with seven (making a total of 14) signals: Data (a four-bit bundle), Delimiter, Error, and Clock.

b) Two media status signals are provided. One indicates the presence of carrier, and the other indicates the occurrence of a collision.

c) A management interface comprised of two signals provides access to management parameters and services.

d) The Reconciliation sublayer maps the signal set provided at the MII to the PLS service definition specified in clause 6.

22.1.2 Application

This clause applies to the interface between MAC sublayer and PHYs, and between PHYs and Station Management entities. The implementation of the interface may assume any of the following three forms:

a) A chip-to-chip (integrated circuit to integrated circuit) interface implemented with traces on a printed circuit board.

b) A motherboard to daughterboard interface between two or more printed circuit boards.

c) An interface between two printed circuit assemblies that are attached with a length of cable and an appropriate connector.

Figure 22-2 provides an example of the third application environment listed above. All MII conformance tests are performed at the mating surfaces of the MII connector, identified by the line A-A.

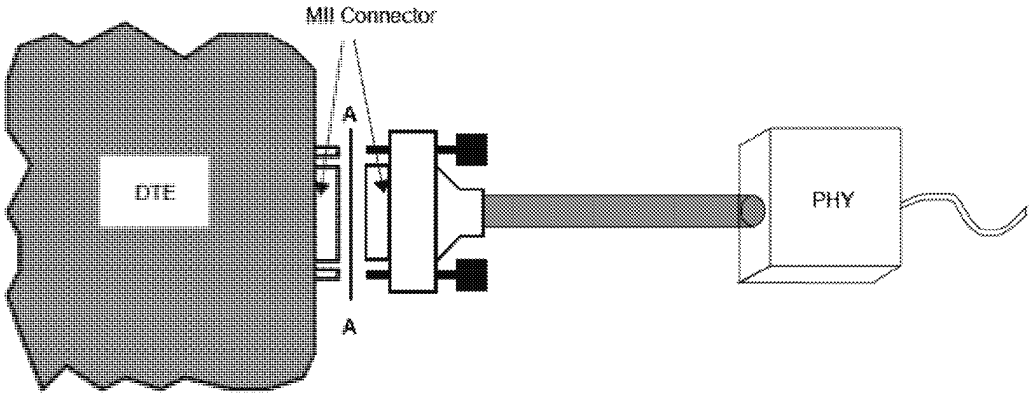


Figure 22-2—Example application showing location of conformance test

This interface is used to provide media independence for various forms of unshielded twisted-pair wiring, shielded twisted-pair wiring, fiber optic cabling, and potentially other media, so that identical media access controllers may be used with any of these media.

To allow for the possibility that multiple PHYs may be controlled by a single Station Management entity, the MII management interface has provisions to accommodate up to 32 PHYs, with the restriction that a maximum of one PHY may be attached to a management interface via the mechanical interface defined in 22.6.

22.1.3 Rates of operation

The MII can support two specific data rates, 10 Mb/s and 100 Mb/s. The functionality is identical at both data rates, as are the signal timing relationships. The only difference between 10 Mb/s and 100 Mb/s operation is the nominal clock frequency.

PHYs that provide an MII are not required to support both data rates, and may support either one or both. PHYs must report the rates they are capable of operating at via the management interface, as described in 22.2.4.

22.1.4 Allocation of functions

The allocation of functions at the MII is such that it readily lends itself to implementation in both PHYs and MAC sublayer entities. The division of functions balances the need for media independence with the need for a simple and cost-effective interface.

While the Attachment Unit Interface (AUI) was defined to exist between the Physical Signaling (PLS) and Physical Media Attachment (PMA) sublayers for 10 Mb/s DTEs, the MII maximizes media independence by cleanly separating the Data Link and Physical Layers of the ISO (IEEE) seven-layer reference model. This allocation also recognizes that implementations can benefit from a close coupling of the PLS or PCS sublayer and the PMA sublayer.

22.2 Functional specifications

The MII is designed to make the differences among the various media absolutely transparent to the MAC sublayer. The selection of logical control signals and the functional procedures are all designed to this end. Additionally, the MII is designed to be easily implemented at minimal cost using conventional design techniques and manufacturing processes.

22.2.1 Mapping of MII signals to PLS service primitives and Station Management

The Reconciliation sublayer maps the signals provided at the MII to the PLS service primitives defined in clause 6. The PLS service primitives provided by the Reconciliation sublayer behave in exactly the same manner as defined in clause 6. The MII signals are defined in detail in 22.2.2 below.

Figure 22-3 depicts a schematic view of the Reconciliation sublayer inputs and outputs, and demonstrates that the MII management interface is controlled by the Station Management entity (STA).

22.2.1.1 Mapping of PLS_DATA.request

22.2.1.1.1 Function

Map the primitive PLS_DATA request to the MII signals TXD<3:0>, TX_EN and TX_CLK.

22.2.1.1.2 Semantics of the service primitive

PLS_DATA request (OUTPUT_UNIT)

The OUTPUT_UNIT parameter can take one of three values: ONE, ZERO, or DATA_COMPLETE. It represents a single data bit. The values ONE and ZERO are conveyed by the signals TXD<3>, TXD<2>, TXD<1> and TXD<0>, each of which conveys one bit of data while TX_EN is asserted. The value DATA_COMPLETE is conveyed by the de-assertion of TX_EN. Synchronization between the Reconciliation sublayer and the PHY is achieved by way of the TX_CLK signal.

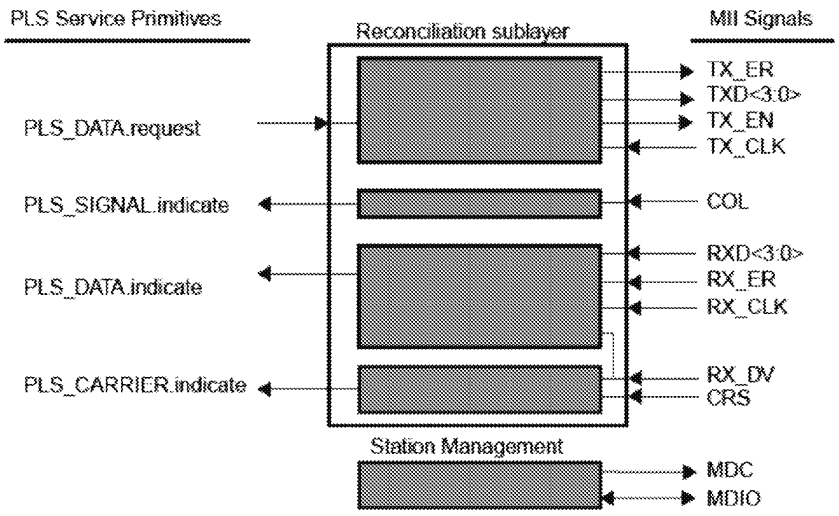


Figure 22-3—Reconciliation Sublayer (RS) inputs and outputs and STA connections to MII

22.2.1.1.3 When generated

The TX_CLK signal is generated by the PHY. The TXD<3:0> and TX_EN signals are generated by the Reconciliation sublayer after every group of four PLS_DATA request transactions from the MAC sublayer to request the transmission of four data bits on the physical medium or to stop transmission.

22.2.1.2 Mapping of PLS_DATA.indicate

22.2.1.2.1 Function

Map the primitive PLS_DATA.indicate to the MII signals RXD<3:0>, RX_DV, RX_ER, and RX_CLK.

22.2.1.2.2 Semantics of the service primitive

PLS_DATA.indicate (INPUT_UNIT)

The INPUT_UNIT parameter can take one of two values: ONE or ZERO. It represents a single data bit. The values ONE and ZERO are derived from the signals RXD<3>, RXD<2>, RXD<1>, and RXD<0>, each of which represents one bit of data while RX_DV is asserted.

The value of the data transferred to the MAC is controlled by the RX_ER signal, see 22.2.1.5, Response to RX_ER indication from MII.

Synchronization between the PHY and the Reconciliation sublayer is achieved by way of the RX_CLK signal.

22.2.1.2.3 When generated

This primitive is generated to all MAC sublayer entities in the network after a PLS_DATA.request is issued. Each nibble of data transferred on RXD<3:0> will result in the generation of four PLS_DATA.indicate transactions.

22.2.1.3 Mapping of PLS_CARRIER.indicate

22.2.1.3.1 Function

Map the primitive PLS_CARRIER.indicate to the MII signals CRS and RX_DV.

22.2.1.3.2 Semantics of the service primitive

PLS_CARRIER.indicate (CARRIER_STATUS)

The CARRIER_STATUS parameter can take one of two values: CARRIER_ON or CARRIER_OFF. The values CARRIER_ON and CARRIER_OFF are derived from the MII signals CRS and RX_DV.

22.2.1.3.3 When generated

The PLS_CARRIER.indicate service primitive is generated by the Reconciliation sublayer whenever the CARRIER_STATUS parameter changes from CARRIER_ON to CARRIER_OFF or vice versa.

While the RX_DV signal is de-asserted, any transition of the CRS signal from de-asserted to asserted must cause a transition of CARRIER_STATUS from the CARRIER_OFF to the CARRIER_ON value, and any transition of the CRS signal from asserted to de-asserted must cause a transition of CARRIER_STATUS from the CARRIER_ON to the CARRIER_OFF value. At any time after CRS and RX_DV are both asserted, de-assertion of RX_DV must cause CARRIER_STATUS to transition to the CARRIER_OFF value. This transition of CARRIER_STATUS from the CARRIER_ON to the CARRIER_OFF value must be recognized by the MAC sublayer, even if the CRS signal is still asserted at the time.

NOTE—The behavior of the CRS signal is specified within this clause so that it can be mapped directly (with the appropriate implementation-specific synchronization) to the carrierSense variable in the MAC process Deference, which is described in 4.2.8. The behavior of the RX_DV signal is specified within this clause so that it can be mapped directly to the carrierSense variable in the MAC process BitReceiver, which is described in 4.2.9, provided that the MAC process BitReceiver is implemented to receive a nibble of data on each cycle through the inner loop.

22.2.1.4 Mapping of PLS_SIGNAL.indicate

22.2.1.4.1 Function

Map the primitive PLS_SIGNAL.indicate to the MII signal COL.

22.2.1.4.2 Semantics of the service primitive

PLS_SIGNAL.indicate (SIGNAL_STATUS)

The SIGNAL_STATUS parameter can take one of two values: SIGNAL_ERROR or NO_SIGNAL_ERROR. SIGNAL_STATUS assumes the value SIGNAL_ERROR when the MII signal COL is asserted, and assumes the value NO_SIGNAL_ERROR when COL is de-asserted.

22.2.1.4.3 When generated

The PLS_SIGNAL.indicate service primitive is generated whenever SIGNAL_STATUS makes a transition from SIGNAL_ERROR to NO_SIGNAL_ERROR or vice versa.

22.2.1.5 Response to RX_ER indication from MII

If, during frame reception, both RX_DV and RX_ER are asserted, the Reconciliation sublayer shall ensure that the MAC will detect a FrameCheckError in that frame.

This requirement may be met by incorporating a function in the Reconciliation sublayer that produces a result that is guaranteed to be not equal to the CRC result, as specified by the algorithm in 3.2.8, of the sequence of nibbles comprising the received frame as delivered to the MAC sublayer. The Reconciliation sublayer must then ensure that the result of this function is delivered to the MAC sublayer at the end of the received frame in place of the last nibble(s) received from the MII.

Other techniques may be employed to respond to RX_ER, provided that the result is that the MAC sublayer behaves as though a FrameCheckError occurred in the received frame.

22.2.1.6 Conditions for generation of TX_ER

If, during the process of transmitting a frame, it is necessary to request that the PHY deliberately corrupt the contents of the frame in such a manner that a receiver will detect the corruption with the highest degree of probability, then the signal TX_ER may be generated.

For example, a repeater that detects an RX_ER during frame reception on an input port may propagate that error indication to its output ports by asserting TX_ER during the process of transmitting that frame.

Since there is no mechanism in the definition of the MAC sublayer by which the transmit data stream can be deliberately corrupted, the Reconciliation sublayer is not required to generate TX_ER.

22.2.2 MII signal functional specifications

22.2.2.1 TX_CLK (transmit clock)

TX_CLK (Transmit Clock) is a continuous clock that provides the timing reference for the transfer of the TX_EN, TXD, and TX_ER signals from the Reconciliation sublayer to the PHY. TX_CLK is sourced by the PHY.

The TX_CLK frequency shall be 25% of the nominal transmit data rate ± 100 ppm. For example, a PHY operating at 100 Mb/s must provide a TX_CLK frequency of 25 MHz, and a PHY operating at 10 Mb/s must provide a TX_CLK frequency of 2.5 MHz. The duty cycle of the TX_CLK signal shall be between 35% and 65% inclusive.

NOTE—See additional information in 22.2.4.1.5.

22.2.2.2 RX_CLK (receive clock)

RX_CLK is a continuous clock that provides the timing reference for the transfer of the RX_DV, RXD, and RX_ER signals from the PHY to the Reconciliation sublayer. RX_CLK is sourced by the PHY. The PHY may recover the RX_CLK reference from the received data or it may derive the RX_CLK reference from a nominal clock (e.g., the TX_CLK reference).

The minimum high and low times of RX_CLK shall be 35% of the nominal period under all conditions.

While RX_DV is asserted, RX_CLK shall be synchronous with recovered data, shall have a frequency equal to 25% of the data rate of the received signal, and shall have a duty cycle of between 35% and 65% inclusive.

When the signal received from the medium is continuous and the PHY can recover the RX_CLK reference and supply the RX_CLK on a continuous basis, there is no need to transition between the recovered clock reference and a nominal clock reference on a frame-by-frame basis. If loss of received signal from the medium causes a PHY to lose the recovered RX_CLK reference, the PHY shall source the RX_CLK from a nominal clock reference.

Transitions from nominal clock to recovered clock or from recovered clock to nominal clock shall be made only while RX_DV is de-asserted. During the interval between the assertion of CRS and the assertion of RX_DV at the beginning of a frame, the PHY may extend a cycle of RX_CLK by holding it in either the high or low condition until the PHY has successfully locked onto the recovered clock. Following the de-assertion of RX_DV at the end of a frame, the PHY may extend a cycle of RX_CLK by holding it in either the high or low condition for an interval that shall not exceed twice the nominal clock period.

NOTE—This standard neither requires nor assumes a guaranteed phase relationship between the RX_CLK and TX_CLK signals. See additional information in 22.2.4.1.5.

22.2.2.3 TX_EN (transmit enable)

TX_EN indicates that the Reconciliation sublayer is presenting nibbles on the MII for transmission. It shall be asserted by the Reconciliation sublayer synchronously with the first nibble of the preamble and shall remain asserted while all nibbles to be transmitted are presented to the MII. TX_EN shall be negated prior to the first TX_CLK following the final nibble of a frame. TX_EN is driven by the Reconciliation sublayer and shall transition synchronously with respect to the TX_CLK.

Figure 22-4 depicts TX_EN behavior during a frame transmission with no collisions.

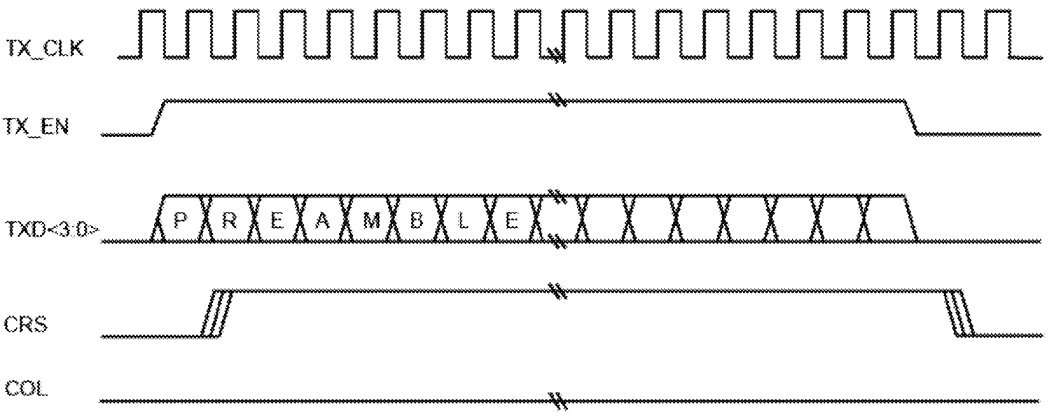


Figure 22-4—Transmission with no collision

22.2.2.4 TXD (transmit data)

TXD is a bundle of 4 data signals (TXD<3:0>) that are driven by the Reconciliation sublayer. TXD<3:0> shall transition synchronously with respect to the TX_CLK. For each TX_CLK period in which TX_EN is asserted, TXD<3:0> are accepted for transmission by the PHY. TXD<0 >is the least significant bit. While TX_EN is de-asserted, TXD<3:0> shall have no effect upon the PHY.

Figure 22-4 depicts TXD<3:0> behavior during the transmission of a frame.

Table 22-1 summarizes the permissible encodings of TXD<3:0>, TX_EN, and TX_ER.

22.2.2.5 TX_ER (transmit coding error)

TX_ER shall transition synchronously with respect to the TX_CLK. When TX_ER is asserted for one or more TX_CLK periods while TX_EN is also asserted, the PHY shall emit one or more symbols that are not

Table 22-1—Permissible encodings of TXD<3:0>, TX_EN, and TX_ER

TX_EN	TX_ER	TXD<3:0>	Indication
0	0	0000 through 1111	Normal inter-frame
0	1	0000 through 1111	Reserved
1	0	0000 through 1111	Normal data transmission
1	1	0000 through 1111	Transmit error propagation

part of the valid data or delimiter set somewhere in the frame being transmitted. The relative position of the error within the frame need not be preserved.

Assertion of the TX_ER signal shall not affect the transmission of data when a PHY is operating at 10 Mb/s, or when TX_EN is de-asserted.

Figure 22-5 shows the behavior of TX_ER during the transmission of a frame propagating an error.

Table 22-1 summarizes the permissible encodings of TXD<3:0>, TX_EN, and TX_ER.

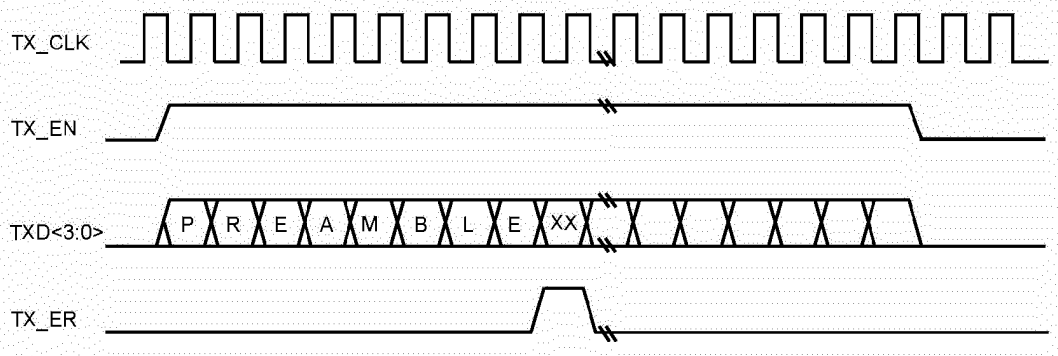


Figure 22-5—Propagating an error

The TX_ER signal shall be implemented at the MII of a PHY, may be implemented at the MII of a repeater that provides an MII port, and may be implemented in MAC sublayer devices. If a Reconciliation sublayer or a repeater with an MII port does not actively drive the TX_ER signal, it shall ensure that the TX_ER signal is pulled down to an inactive state at all times.

22.2.2.6 RX_DV (Receive Data Valid)

RX_DV (Receive Data Valid) is driven by the PHY to indicate that the PHY is presenting recovered and decoded nibbles on the RXD<3:0> bundle and that the data on RXD<3:0> is synchronous to RX_CLK. RX_DV shall transition synchronously with respect to the RX_CLK. RX_DV shall remain asserted continuously from the first recovered nibble of the frame through the final recovered nibble and shall be negated prior to the first RX_CLK that follows the final nibble. In order for a received frame to be correctly interpreted by the Reconciliation sublayer and the MAC sublayer, RX_DV must encompass the frame, starting no later than the Start Frame Delimiter (SFD) and excluding any End-of-Frame delimiter.

Figure 22-6 shows the behavior of RX_DV during frame reception.

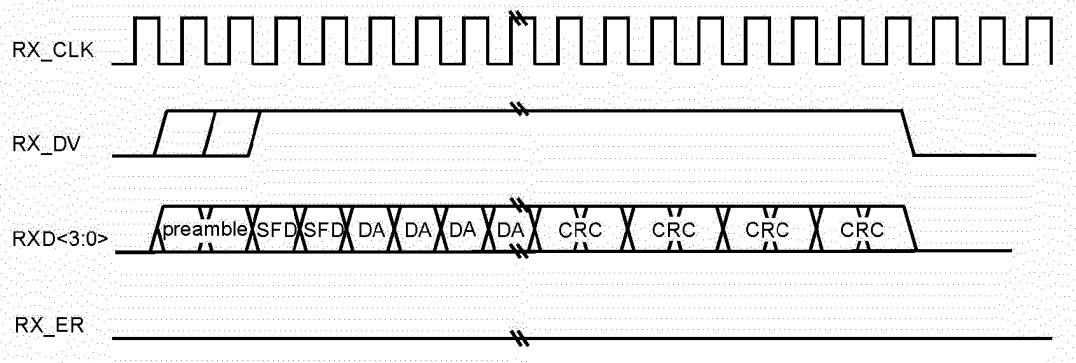


Figure 22-6—Reception with no errors

22.2.2.7 RXD (receive data)

RXD is a bundle of four data signals (RXD<3:0>) that transition synchronously with respect to the RX_CLK. RXD<3:0> are driven by the PHY. For each RX_CLK period in which RX_DV is asserted, RXD<3:0> transfer four bits of recovered data from the PHY to the Reconciliation sublayer. RXD<0> is the least significant bit. While RX_DV is de-asserted, RXD<3:0> shall have no effect on the Reconciliation sublayer.

While RX_DV is de-asserted, the PHY may provide a False Carrier indication by asserting the RX_ER signal while driving the value <1110> onto RXD<3:0>. See 24.2.4.4.2 for a description of the conditions under which a PHY will provide a False Carrier indication.

In order for a frame to be correctly interpreted by the MAC sublayer, a completely formed SFD must be passed across the MII. A PHY is not required to loop data transmitted on TXD<3:0> back to RXD<3:0> unless the loopback mode of operation is selected as defined in 22.2.4.1.2.

Figure 22-6 shows the behavior of RXD<3:0> during frame reception.

Table 22-2 summarizes the permissible encoding of RXD<3:0>, RX_ER, and RX_DV, along with the specific indication provided by each code.

Table 2—Permissible encoding of RXD<3:0>, RX_ER, and RX_DV

RX_DV	RX_ER	RXD<3:0>	Indication
0	0	0000 through 1111	Normal inter-frame
0	1	0000	Normal inter-frame
0	1	0001 through 1101	Reserved
0	1	1110	False Carrier indication
0	1	1111	Reserved
1	0	0000 through 1111	Normal data reception
1	1	0000 through 1111	Data reception with errors

22.2.2.8 RX_ER (receive error)

RX_ER (Receive Error) is driven by the PHY. RX_ER shall be asserted for one or more RX_CLK periods to indicate to the Reconciliation sublayer that an error (e.g., a coding error, or any error that the PHY is capable of detecting, and that may otherwise be undetectable at the MAC sublayer) was detected somewhere in the frame presently being transferred from the PHY to the Reconciliation sublayer. RX_ER shall transition synchronously with respect to RX_CLK. While RX_DV is de-asserted, RX_ER shall have no effect on the Reconciliation sublayer.

While RX_DV is de-asserted, the PHY may provide a False Carrier indication by asserting the RX_ER signal for at least one cycle of the RX_CLK while driving the appropriate value onto RXD<3:0>, as defined in 22.2.2.7. See 24.2.4.4.2 for a description of the conditions under which a PHY will provide a False Carrier indication.

The effect of RX_ER on the Reconciliation sublayer is defined in 22.2.1.5, Response to RX_ER indication from MII.

Figure 22-7 shows the behavior of RX_ER during the reception of a frame with errors.

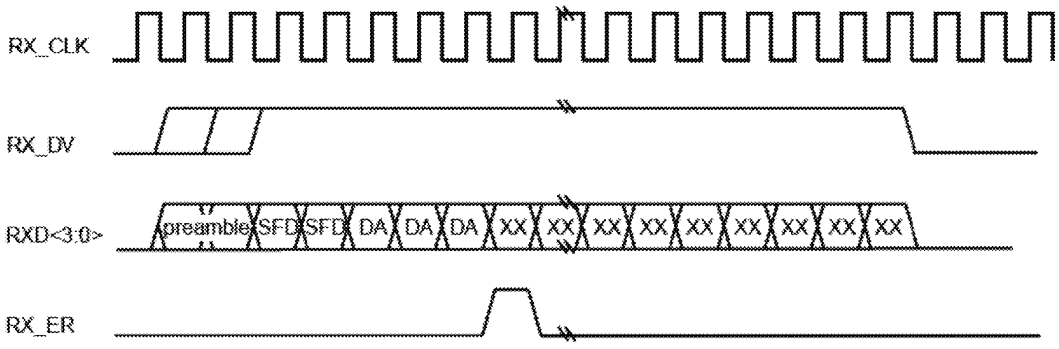


Figure 22-7—Reception with errors

Figure 22-8 shows the behavior of RX_ER, RX_DV and RXD<3:0> during a False Carrier indication.

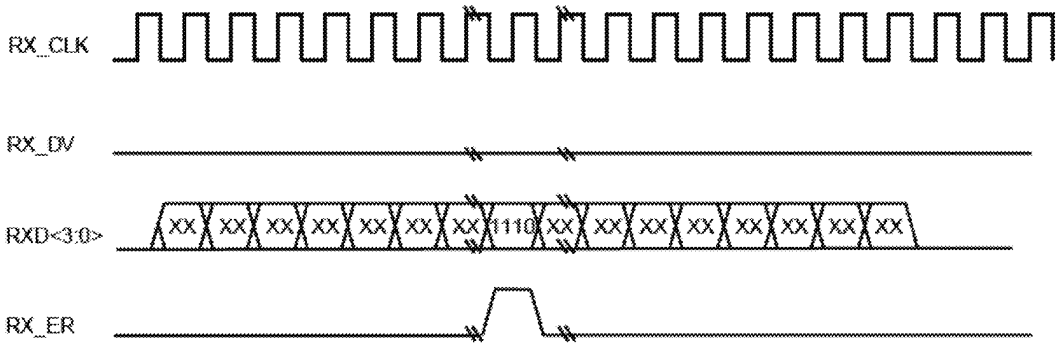


Figure 22-8—False Carrier indication

22.2.2.9 CRS (carrier sense)

CRS shall be asserted by the PHY when either the transmit or receive medium is nonidle. CRS shall be de-asserted by the PHY when both the transmit and receive media are idle. The PHY shall ensure that CRS remains asserted throughout the duration of a collision condition.

CRS is not required to transition synchronously with respect to either the TX_CLK or the RX_CLK.

The behavior of the CRS signal is unspecified when the duplex mode bit 0.8 in the control register is set to a logic one, as described in 22.2.4.1.8, or when the Auto-Negotiation process selects a full duplex mode of operation.

Figure 22-4 shows the behavior of CRS during a frame transmission without a collision, while Figure 22-9 shows the behavior of CRS during a frame transmission with a collision.

22.2.2.10 COL (collision detected)

COL shall be asserted by the PHY upon detection of a collision on the medium, and shall remain asserted while the collision condition persists.

COL shall be asserted by a PHY that is operating at 10 Mb/s in response to a *signal_quality_error* message from the PMA.

COL is not required to transition synchronously with respect to either the TX_CLK or the RX_CLK.

The behavior of the COL signal is unspecified when the duplex mode bit 0.8 in the control register is set to a logic one, as described in 22.2.4.1.8, or when the Auto-Negotiation process selects a full-duplex mode of operation.

Figure 22-9 shows the behavior of COL during a frame transmission with a collision.

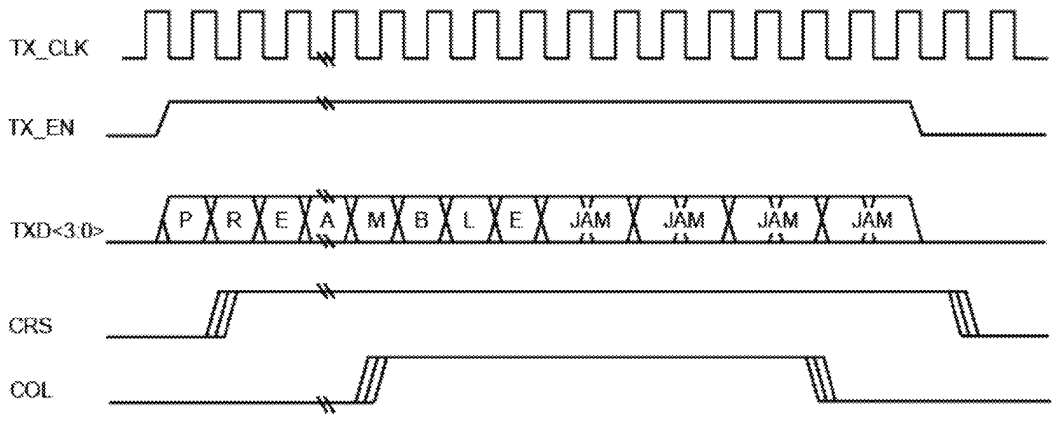


Figure 22-9—Transmission with collision

NOTE—The circuit assembly that contains the Reconciliation sublayer may incorporate a weak pull-up on the COL signal as a means of detecting an open circuit condition on the COL signal at the MII. The limit on the value of this pull-up is defined in 22.4.4.2.

22.2.2.11 MDC (management data clock)

MDC is sourced by the Station Management entity to the PHY as the timing reference for transfer of information on the MDIO signal. MDC is an aperiodic signal that has no maximum high or low times. The minimum high and low times for MDC shall be 160 ns each, and the minimum period for MDC shall be 400 ns, regardless of the nominal period of TX_CLK and RX_CLK.

22.2.2.12 MDIO (management data input/output)

MDIO is a bidirectional signal between the PHY and the STA. It is used to transfer control information and status between the PHY and the STA. Control information is driven by the STA synchronously with respect to MDC and is sampled synchronously by the PHY. Status information is driven by the PHY synchronously with respect to MDC and is sampled synchronously by the STA.

MDIO shall be driven through three-state circuits that enable either the STA or the PHY to drive the signal. A PHY that is attached to the MII via the mechanical interface specified in 22.6 shall provide a resistive pull-up to maintain the signal in a high state. The STA shall incorporate a resistive pull-down on the MDIO signal and thus may use the quiescent state of MDIO to determine if a PHY is connected to the MII via the mechanical interface defined in 22.6. The limits on the values of these pull-ups and pull-downs are defined in 22.4.4.2.

22.2.3 Frame structure

Data frames transmitted through the MII shall have the frame format shown in figure 22-10.

<inter-frame><preamble><sfd><data><efd>

Figure 22-10—MII frame format

For the MII, transmission and reception of each octet of data shall be done a nibble at a time with the order of nibble transmission and reception as shown in figure 22-11.

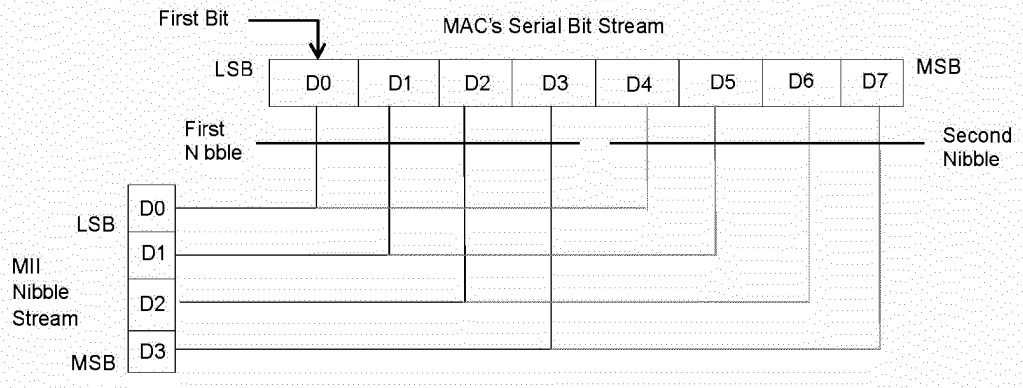


Figure 22-11—Octet/nibble transmit and receive order

The bits of each octet are transmitted and received as two nibbles, bits 0 through 3 of the octet corresponding to bits 0 through 3 of the first nibble transmitted or received, and bits 4 through 7 of the octet corresponding to bits 0 through 3 of the second nibble transmitted or received.

22.2.3.1 Inter-frame

The inter-frame period provides an observation window for an unspecified amount of time during which no data activity occurs on the MII. The absence of data activity is indicated by the de-assertion of the RX_DV signal on the receive path, and the de-assertion of the TX_EN signal on the transmit path. The MAC inter-FrameSpacing parameter defined in clause 4 is measured from the de-assertion of the CRS signal to the assertion of the CRS signal.

22.2.3.2 Preamble and start of frame delimiter

22.2.3.2.1 Transmit case

The preamble <preamble> begins a frame transmission. The bit value of the preamble field at the MII is unchanged from that specified in 7.2.3.2 and shall consist of 7 octets with the following bit values:

10101010 10101010 10101010 10101010 10101010 10101010 10101010

In the preceding example, the preamble is displayed using the bit order it would have if transmitted serially. This means that for each octet the leftmost 1 value represents the LSB of the octet, and the rightmost 0 value the octet MSB.

The SFD (Start Frame Delimiter) <sfd> indicates the start of a frame and follows the preamble. The bit value of the SFD at the MII is unchanged from that specified in 7.2.3.3 and is the bit sequence:

10101011

The preamble and SFD shall be transmitted through the MII as nibbles starting from the assertion of TX_EN as shown in table 22-3.

Table 3—Transmitted preamble and SFD

Signal	Bit values of nibbles transmitted through MII																		
TXD0	X	1*	1	1	1	1	1	1	1	1	1	1	1	1	1	1†	1	D0‡	D4§
TXD1	X	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	D1	D5
TXD2	X	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	D2	D6
TXD3	X	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	D3	D7
TX_EN	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

*1st preamble nibble transmitted.
†1st SFD nibble transmitted.
‡1st data nibble transmitted.
§D0 through D7 are the first eight bits of the data field from the Protocol Data Unit (PDU).

22.2.3.2.2 Receive case

The conditions for assertion of RX_DV are defined in 22.2.2.6.

The alignment of the received SFD and data at the MII shall be as shown in table 22-4 and table 22-5. Table 22-4 depicts the case where no preamble nibbles are conveyed across the MII, and table 22-5 depicts the case where the entire preamble is conveyed across the MII.

Table 4—Start of receive with no preamble preceding SFD

Signal	Bit values of nibbles received through MII										
RXD0	X	X	X	X	X	X	X	1*	1	D0†	D4‡
RXD1	X	X	X	X	X	X	X	0	0	D1	D5
RXD2	X	X	X	X	X	X	X	1	1	D2	D6
RXD3	X	X	X	X	X	X	X	0	1	D3	D7
RX_DV	0	0	0	0	0	0	0	1	1	1	1

*1st SFD nibble received.
†1st data nibble received.
‡D0 through D7 are the first eight bits of the data field from the PDU.

Table 5—Start of receive with entire preamble preceding SFD

Signal	Bit values of nibbles received through MII																		
RXD0	X	1*	1	1	1	1	1	1	1	1	1	1	1	1	1	1†	1	D0‡	D4§
RXD1	X	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	D1	D5
RXD2	X	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	D2	D6
RXD3	X	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	D3	D7
RX_DV	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

*1st preamble nibble received.
†1st SFD nibble received.
‡1st data nibble received.
§D0 through D7 are the first eight bits of the data field from the PDU.

22.2.3.3 Data

The data in a well formed frame shall consist of N octets of data transmitted as 2N nibbles. For each octet of data the transmit order of each nibble is as specified in figure 22-11. Data in a collision fragment may consist of an odd number of nibbles.

22.2.3.4 End-of-Frame delimiter (EFD)

De-assertion of the TX_EN signal constitutes an End-of-Frame delimiter for data conveyed on TXD<3:0>, and de-assertion of RX_DV constitutes an End-of-Frame delimiter for data conveyed on RXD<3:0>.

22.2.3.5 Handling of excess nibbles

An excess nibble condition occurs when an odd number of nibbles is conveyed across the MII beginning with the SFD and including all nibbles conveyed until the End-of-Frame delimiter. Reception of a frame containing a non-integer number of octets shall be indicated by the PHY as an excess nibble condition.

Transmission of an excess nibble may be handled by the PHY in an implementation-specific manner. No assumption should be made with regard to truncation, octet padding, or exact nibble transmission by the PHY.

22.2.4 Management functions

The management interface specified here provides a simple, two-wire, serial interface to connect a management entity and a managed PHY for the purposes of controlling the PHY and gathering status from the PHY. This interface is referred to as the MII Management Interface.

The management interface consists of a pair of signals that physically transport the management information across the MII, a frame format and a protocol specification for exchanging management frames, and a register set that can be read and written using these frames. The register definition specifies a basic register set with an extension mechanism.

The basic register set consists of two registers referred to as the Control Register (register 0) and the Status Register (register 1). The status and control functions defined here are considered basic and fundamental to 100 Mb/s PHYs. All PHYs that provide an MII shall incorporate the basic register set. Registers 2 through 7 are part of the extended register set.

The full set of management registers is listed in table 22-6.

Table 6—MII management register set

Register address	Register name	Basic/Extended
0	Control	B
1	Status	B
2,3	PHY Identifier	E
4	Auto-Negotiation Advertisement	E
5	Auto-Negotiation Link Partner Ability	E
6	Auto-Negotiation Expansion	E
7	Auto-Negotiation Next Page Transmit	E
8 through 15	Reserved	E
16 through 31	Vendor Specific	E

22.2.4.1 Control register (register 0)

The assignment of bits in the Control Register is shown in table 22-7 below. The default value for each bit of the Control Register should be chosen so that the initial state of the PHY upon power up or reset is a normal operational state without management intervention.

Table 7—Control register bit definitions

Bit(s)	Name	Description	R/W*
0.15	Reset	1 = PHY reset 0 = normal operation	R/W SC
0.14	Loopback	1 = enable loopback mode 0 = disable loopback mode	R/W
0.13	Speed Selection	1 = 100 Mb/s 0 = 10 Mb/s	R/W
0.12	Auto-Negotiation Enable	1 = Enable Auto-Negotiation Process 0 = Disable Auto-Negotiation Process	R/W
0.11	Power Down	1 = power down 0 = normal operation†	R/W
0.10	Isolate	1 = electrically Isolate PHY from MII 0 = normal operation[b]	R/W
0.9	Restart Auto-Negotiation	1 = Restart Auto-Negotiation Process 0 = normal operation	R/W SC
0.8	Duplex Mode	1 = Full Duplex‡ 0 = Half Duplex	R/W
0.7	Collision Test	1 = enable COL signal test 0 = disable COL signal test	R/W
0.6:0	Reserved	Write as 0, ignore on Read	R/W

*R/W = Read/Write, SC = Self-Clearing.
†For normal operation, both 0.10 and 0.11 must be cleared to zero, see 22.2.4.1.5.
‡Specifications for full-duplex mode operation are planned for future work.

22.2.4.1.1 Reset

Resetting a PHY is accomplished by setting bit 0.15 to a logic one. This action shall set the status and control registers to their default states. As a consequence this action may change the internal state of the PHY and the state of the physical link associated with the PHY. This bit is self-clearing, and a PHY shall return a value of one in bit 0.15 until the reset process is completed. A PHY is not required to accept a write transaction to the control register until the reset process is completed, and writes to bits of the control register other than 0.15 may have no effect until the reset process is completed. The reset process shall be completed within 0.5 s from the setting of bit 0.15.

The default value of bit 0.15 is zero.

NOTE—This operation may interrupt data communication.

22.2.4.1.2 Loopback

The PHY shall be placed in a loopback mode of operation when bit 0.14 is set to a logic one. When bit 0.14 is set, the PHY receive circuitry shall be isolated from the network medium, and the assertion of TX_EN at the MII shall not result in the transmission of data on the network medium. When bit 0.14 is set, the PHY shall accept data from the MII transmit data path and return it to the MII receive data path in response to the assertion of TX_EN. When bit 0.14 is set, the delay from the assertion of TX_EN to the assertion of RX_DV shall be less than 512 BT. When bit 0.14 is set, the COL signal shall remain de-asserted at all times, unless bit 0.7 is set, in which case the COL signal shall behave as described in 22.2.4.1.9. Clearing bit 0.14 to zero allows normal operation.

The default value of bit 0.14 is zero.

NOTE—The signal path through the PHY that is exercised in the loopback mode of operation is implementation specific, but it is recommended that the signal path encompass as much of the PHY circuitry as is practical. The intention of providing this loopback mode of operation is to permit a diagnostic or self-test function to perform the transmission and reception of a PDU, thus testing the transmit and receive data paths. Other loopback signal paths through a PHY may be enabled via the extended register set, in an implementation-specific fashion.

22.2.4.1.3 Speed selection

Link speed can be selected via either the Auto-Negotiation process, or manual speed selection. Manual speed selection is allowed when Auto-Negotiation is disabled by clearing bit 0.12 to zero. When Auto-Negotiation is disabled, setting bit 0.13 to a logic one configures the PHY for 100 Mb/s operation, and clearing bit 0.13 to a logic zero configures the PHY for 10 Mb/s operation. When Auto-Negotiation is enabled, bit 0.13 can be read or written, but the state of bit 0.13 has no effect on the link configuration, and it is not necessary for bit 0.13 to reflect the operating speed of the link when it is read. If a PHY reports via bits 1.15:11 that it is able to operate at only one speed, the value of bit 0.13 shall correspond to the speed at which the PHY can operate, and any attempt to change the setting of the bit shall be ignored.

The default value of bit 0.13 is one, unless the PHY reports via bits 1.15:11 that it is able to operate only at 10 Mb/s, in which case the default value of bit 0.13 is zero.

22.2.4.1.4 Auto-Negotiation enable

The Auto-Negotiation process shall be enabled by setting bit 0.12 to a logic one. If bit 0.12 is set to a logic one, then bits 0.13 and 0.8 shall have no effect on the link configuration, and the Auto-Negotiation process will determine the link configuration. If bit 0.12 is cleared to a logic zero, then bits 0.13 and 0.8 will determine the link configuration, regardless of the prior state of the link configuration and the Auto-Negotiation process.

If a PHY reports via bit 1.3 that it lacks the ability to perform Auto-Negotiation, the PHY shall return a value of zero in bit 0.12. If a PHY reports via bit 1.3 that it lacks the ability to perform Auto-Negotiation, bit 0.12 should always be written as zero, and any attempt to write a one to bit 0.12 shall be ignored.

The default value of bit 0.12 is one, unless the PHY reports via bit 1.3 that it lacks the ability to perform Auto-Negotiation, in which case the default value of bit 0.12 is zero.

22.2.4.1.5 Power down

The PHY may be placed in a low-power consumption state by setting bit 0.11 to a logic one. Clearing bit 0.11 to zero allows normal operation. The specific behavior of a PHY in the power-down state is implementation specific. While in the power-down state, the PHY shall respond to management transactions. During the transition to the power-down state and while in the power-down state, the PHY shall not generate spurious signals on the MII.

A PHY is not required to meet the RX_CLK and TX_CLK signal functional requirements when either bit 0.11 or bit 0.10 is set to a logic one. A PHY shall meet the RX_CLK and TX_CLK signal functional requirements defined in 22.2.2 within 0.5 s after both bit 0.11 and 0.10 are cleared to zero.

The default value of bit 0.11 is zero.

22.2.4.1.6 Isolate

The PHY may be forced to electrically isolate its data paths from the MII by setting bit 0.10 to a logic one. Clearing bit 0.10 allows normal operation. When the PHY is isolated from the MII it shall not respond to the TXD<3:0>, TX_EN, and TX_ER inputs, and it shall present a high impedance on its TX_CLK, RX_CLK, RX_DV, RX_ER, RXD<3:0>, COL, and CRS outputs. When the PHY is isolated from the MII it shall respond to management transactions.

A PHY that is connected to the MII via the mechanical interface defined in 22.6 shall have a default value of one for bit 0.10 so as to avoid the possibility of having multiple MII output drivers actively driving the same signal path simultaneously.

NOTE—This clause neither requires nor assumes any specific behavior at the MDI resulting from setting bit 0.10 to a logic one.

22.2.4.1.7 Restart Auto-Negotiation

If a PHY reports via bit 1.3 that it lacks the ability to perform Auto-Negotiation, or if Auto-Negotiation is disabled, the PHY shall return a value of zero in bit 0.9. If a PHY reports via bit 1.3 that it lacks the ability to perform Auto-Negotiation, or if Auto-Negotiation is disabled, bit 0.9 should always be written as zero, and any attempt to write a one to bit 0.9 shall be ignored.

Otherwise, the Auto-Negotiation process shall be restarted by setting bit 0.9 to a logic one. This bit is self-clearing, and a PHY shall return a value of one in bit 0.9 until the Auto-Negotiation process has been initiated. The Auto-Negotiation process shall not be affected by writing a zero to bit 0.9.

The default value of bit 0.9 is zero.

22.2.4.1.8 Duplex mode

The duplex mode can be selected via either the Auto-Negotiation process, or manual duplex selection. Manual duplex selection is allowed when Auto-Negotiation is disabled by clearing bit 0.12 to zero. When Auto-Negotiation is disabled, setting bit 0.8 to a logic one configures the PHY for full-duplex operation, and clearing bit 0.8 to a logic zero configures the PHY for half-duplex operation. When Auto-Negotiation is enabled, bit 0.8 can be read or written, but the state of bit 0.8 has no effect on the link configuration. If a PHY reports via bits 1.15:11 that it is able to operate in only one duplex mode, the value of bit 0.8 shall correspond to the mode in which the PHY can operate, and any attempt to change the setting of bit 0.8 shall be ignored.

When a PHY is placed in the loopback mode of operation via bit 0.14, the behavior of the PHY shall not be affected by the state of bit 0.8.

The default value of bit 0.8 is zero, unless a PHY reports via bits 1.15:11 that it is able to operate only in full-duplex mode, in which case the default value of bit 0.8 is one.

22.2.4.1.9 Collision test

The COL signal at the MII may be tested by setting bit 0.7 to a logic one. When bit 0.7 is set to one, the PHY shall assert the COL signal within 512 BT in response to the assertion of TX_EN. While bit 0.7 is set to one,

the PHY shall de-assert the COL signal within 4 BT in response to the de-assertion of TX_EN. Clearing bit 0.7 to zero allows normal operation.

The default value of bit 0.7 is zero.

NOTE—It is recommended that the Collision Test function be used only in conjunction with the loopback mode of operation defined in 22.2.4.1.2.

22.2.4.1.10 Reserved bits

Bits 0.6:0 are reserved for future standardization. They shall be written as zero and shall be ignored when read; however, a PHY shall return the value zero in these bits.

22.2.4.2 Status register (register 1)

The assignment of bits in the Status register is shown in table 22-8 below. All of the bits in the Status register are read only, a write to the Status register shall have no effect.

Table 8—Status register bit definitions

Bit(s)	Name	Description	R/W*
1.15	100BASE-T4	1 = PHY able to perform 100BASE-T4 0 = PHY not able to perform 100BASE-T4	RO
1.14	100BASE-X Full Duplex†	1 = PHY able to perform full-duplex 100BASE-X 0 = PHY not able to perform full-duplex 100BASE-X	RO
1.13	100BASE-X Half Duplex	1 = PHY able to perform half-duplex 100BASE-X 0 = PHY not able to perform half-duplex 100BASE-X	RO
1.12	10 Mb/s Full Duplex[b]	1 = PHY able to operate at 10 Mb/s in full-duplex mode 0 = PHY not able to operate at 10 Mb/s in full-duplex mode	RO
1.11	10 Mb/s Half Duplex	1 = PHY able to operate at 10 Mb/s in half-duplex mode 0 = PHY not able to operate at 10 Mb/s in half-duplex mode	RO
1.10:7	Reserved	ignore when read	RO
1.6	MF Preamble Suppression	1 = PHY will accept management frames with preamble suppressed. 0 = PHY will not accept management frames with preamble suppressed.	RO
1.5	Auto-Negotiation Complete	1 = Auto-Negotiation process completed 0 = Auto-Negotiation process not completed	RO
1.4	Remote Fault	1 = remote fault condition detected 0 = no remote fault condition detected	RO/ LH
1.3	Auto-Negotiation Ability	1 = PHY is able to perform Auto-Negotiation 0 = PHY is not able to perform Auto-Negotiation	RO
1.2	Link Status	1 = link is up 0 = link is down	RO/ LL
1.1	Jabber Detect	1 = jabber condition detected 0 = no jabber condition detected	RO/ LH
1.0	Extended Capability	1 = extended register capabilities 0 = basic register set capabilities only	RO

*RO = Read Only, LL = Latching Low, LH = Latching High
†Specifications for full-duplex mode operation are planned for future work.

22.2.4.2.1 100BASE-T4 ability

When read as a logic one, bit 1.15 indicates that the PHY has the ability to perform link transmission and reception using the 100BASE-T4 signaling specification. When read as a logic zero, bit 1.15 indicates that the PHY lacks the ability to perform link transmission and reception using the 100BASE-T4 signaling specification.

22.2.4.2.2 100BASE-X full-duplex ability

When read as a logic one, bit 1.14 indicates that the PHY has the ability to perform full-duplex link transmission and reception using the 100BASE-X signaling specification. When read as a logic zero, bit 1.14 indicates that the PHY lacks the ability to perform full-duplex link transmission and reception using the 100BASE-X signaling specification.

NOTE—Specifications for full-duplex mode operation are planned for future work.

22.2.4.2.3 100BASE-X half-duplex ability

When read as a logic one, bit 1.13 indicates that the PHY has the ability to perform half-duplex link transmission and reception using the 100BASE-X signaling specification. When read as a logic zero, bit 1.13 indicates that the PHY lacks the ability to perform half-duplex link transmission and reception using the 100BASE-X signaling specification.

22.2.4.2.4 10 Mb/s full-duplex ability

When read as a logic one, bit 1.12 indicates that the PHY has the ability to perform full duplex link transmission and reception while operating at 10 Mb/s. When read as a logic zero, bit 1.12 indicates that the PHY lacks the ability to perform full duplex link transmission and reception while operating at 10 Mb/s.

NOTE—Specifications for full-duplex mode operation are planned for future work.

22.2.4.2.5 10 Mb/s half-duplex ability

When read as a logic one, bit 1.11 indicates that the PHY has the ability to perform half-duplex link transmission and reception while operating at 10 Mb/s. When read as a logic zero, bit 1.11 indicates that the PHY lacks the ability to perform half-duplex link transmission and reception while operating at 10 Mb/s.

22.2.4.2.6 Reserved bits

Bits 1.10:7 are reserved for future standardization and shall be ignored when read; however, a PHY shall return the value zero in these bits. Bits 1.10:8 are specifically reserved for future PHY capabilities that will be reflected in the Auto-Negotiation base link code word Technology Ability field, as defined in 28.2.1.2.

22.2.4.2.7 MF preamble suppression ability

When read as a logic one, bit 1.6 indicates that the PHY is able to accept management frames regardless of whether they are or are not preceded by the preamble pattern described in 22.2.4.4.2. When read as a logic zero, bit 1.6 indicates that the PHY is not able to accept management frames unless they are preceded by the preamble pattern described in 22.2.4.4.2.

22.2.4.2.8 Auto-Negotiation complete

When read as a logic one, bit 1.5 indicates that the Auto-Negotiation process has been completed, and that the contents of registers 4, 5, 6, and 7 are valid. When read as a logic zero, bit 1.5 indicates that the Auto-

Negotiation process has not been completed, and that the contents of registers 4, 5, 6, and 7 are meaningless. A PHY shall return a value of zero in bit 1.5 if Auto-Negotiation is disabled by clearing bit 0.12. A PHY shall also return a value of zero in bit 1.5 if it lacks the ability to perform Auto-Negotiation.

22.2.4.2.9 Remote fault

When read as a logic one, bit 1.4 indicates that a remote fault condition has been detected. The type of fault as well as the criteria and method of fault detection is PHY specific. The Remote Fault bit shall be implemented with a latching function, such that the occurrence of a remote fault will cause the Remote Fault bit to become set and remain set until it is cleared. The Remote Fault bit shall be cleared each time register 1 is read via the management interface, and shall also be cleared by a PHY reset.

If a PHY has no provision for remote fault detection, it shall maintain bit 1.4 in a cleared state. Further information regarding the remote fault indication can be found in 28.2.1.2, and in 24.3.2.1.

22.2.4.2.10 Auto-Negotiation ability

When read as a logic one, bit 1.3 indicates that the PHY has the ability to perform Auto-Negotiation. When read as a logic zero, bit 1.3 indicates that the PHY lacks the ability to perform Auto-Negotiation.

22.2.4.2.11 Link Status

When read as a logic one, bit 1.2 indicates that the PHY has determined that a valid link has been established. When read as a logic zero, bit 1.2 indicates that the link is not valid. The criteria for determining link validity is PHY specific. The Link Status bit shall be implemented with a latching function, such that the occurrence of a link failure condition will cause the Link Status bit to become cleared and remain cleared until it is read via the management interface. This status indication is intended to support the management attribute defined in 30.5.1.1.4, aMediaAvailable.

22.2.4.2.12 Jabber detect

When read as a logic one, bit 1.1 indicates that a jabber condition has been detected. This status indication is intended to support the management attribute defined in 30.5.1.1.6, aJabber, and the MAU notification defined in 30.5.1.3.1, nJabber. The criteria for the detection of a jabber condition is PHY specific. The Jabber Detect bit shall be implemented with a latching function, such that the occurrence of a jabber condition will cause the Jabber Detect bit to become set and remain set until it is cleared. The Jabber Detect bit shall be cleared each time register 1 is read via the management interface, and shall also be cleared by a PHY reset.

PHYs specified for 100 Mb/s operation (100BASE-X and 100BASE-T4) do not incorporate a Jabber Detect function, as this function is defined to be performed in the repeater unit in 100 Mb/s systems. Therefore, 100BASE-X and 100BASE-T4 PHYs shall always return a value of zero in bit 1.1.

22.2.4.2.13 Extended capability

When read as a logic one, bit 1.0 indicates that the PHY provides an extended set of capabilities which may be accessed through the extended register set. When read as a logic zero, bit 1.0 indicates that the PHY provides only the basic register set.

22.2.4.3 Extended capability registers

In addition to the basic register set defined in 22.2.4.1 and 22.2.4.2, PHYs may provide an extended set of capabilities that may be accessed and controlled via the MII management interface. Six registers have been defined within the extended address space for the purpose of providing a PHY-specific identifier to layer management, and to provide control and monitoring for the Auto-Negotiation process.

If an attempt is made to perform a read transaction to a register in the extended register set, and the PHY being read does not implement the addressed register, the PHY shall not drive the MDIO line in response to the read transaction. If an attempt is made to perform a write transaction to a register in the extended register set, and the PHY being written does not implement the addressed register, the write transaction shall be ignored by the PHY.

22.2.4.3.1 PHY Identifier (registers 2 and 3)

Registers 2 and 3 provide a 32-bit value, which shall constitute a unique identifier for a particular type of PHY. A PHY may return a value of zero in each of the 32 bits of the PHY Identifier.

Bit 2.15 shall be the MSB of the PHY Identifier, and bit 3.0 shall be the LSB of the PHY Identifier.

The PHY Identifier shall be composed of the third through 24th bits of the Organizationally Unique Identifier (OUI) assigned to the PHY manufacturer by the IEEE,[28] plus a six-bit manufacturer's model number, plus a four-bit manufacturer's revision number. The PHY Identifier is intended to provide sufficient information to support the oResourceTypeID object as required in 30.1.2.

The third bit of the OUI is assigned to bit 2.15, the fourth bit of the OUI is assigned to bit 2.14, and so on. Bit 2.0 contains the eighteenth bit of the OUI. Bit 3.15 contains the nineteenth bit of the OUI, and bit 3.10 contains the twenty-fourth bit of the OUI. Bit 3.9 contains the MSB of the manufacturer's model number. Bit 3.4 contains the LSB of the manufacturer's model number. Bit 3.3 contains the MSB of the manufacturer's revision number, and bit 3.0 contains the LSB of the manufacturer's revision number.

Figure 22-12 depicts the mapping of this information to the bits of Registers 2 and 3. Additional detail describing the format of OUIs can be found in IEEE Std 802-1990.

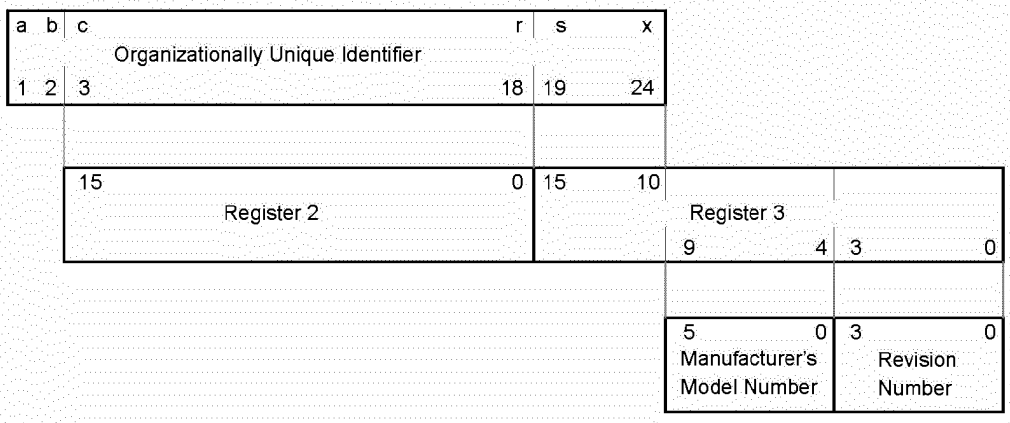


Figure 22-12—Format of PHY Identifier

22.2.4.3.2 Auto-Negotiation advertisement (register 4)

Register 4 provides 16 bits that are used by the Auto-Negotiation process. See 28.2.4.1.

[28]Interested applicants should contact the IEEE Standards Department, Institute of Electrical and Electronics Engineers, 445 Hoes Lane, P.O. Box 1331, Piscataway, NJ 08855-1331, USA.

22.2.4.3.3 Auto-Negotiation link partner ability (register 5)

Register 5 provides 16 bits that are used by the Auto-Negotiation process. See 28.2.4.1.

22.2.4.3.4 Auto-Negotiation expansion (register 6)

Register 6 provides 16 bits that are used by the Auto-Negotiation process. See 28.2.4.1.

22.2.4.3.5 Auto-Negotiation next page (register 7)

Register 7 provides 16 bits that are used by the Auto-Negotiation process. See 28.2.4.1.

22.2.4.3.6 PHY specific registers

A particular PHY may provide additional registers beyond those defined above. Register addresses 16 through 31 (decimal) may be used to provide vendor-specific functions or abilities. Register addresses 8 through 15 (decimal) are reserved for assignment within future editions of this standard.

22.2.4.4 Management frame structure

Frames transmitted on the MII Management Interface shall have the frame structure shown in table 22-9. The order of bit transmission shall be from left to right.

Table 9—Management frame format

	Management frame fields							
	PRE	ST	OP	PHYAD	REGAD	TA	DATA	IDLE
READ	1...1	01	10	AAAAA	RRRRR	Z0	DDDDDDDDDDDDDDDD	Z
WRITE	1...1	01	01	AAAAA	RRRRR	10	DDDDDDDDDDDDDDDD	Z

22.2.4.4.1 IDLE (IDLE condition)

The IDLE condition on MDIO is a high-impedance state. All three state drivers shall be disabled and the PHY's pull-up resistor will pull the MDIO line to a logic one.

22.2.4.4.2 PRE (preamble)

At the beginning of each transaction, the station management entity shall send a sequence of 32 contiguous logic one bits on MDIO with 32 corresponding cycles on MDC to provide the PHY with a pattern that it can use to establish synchronization. A PHY shall observe a sequence of 32 contiguous one bits on MDIO with 32 corresponding cycles on MDC before it responds to any transaction.

If the STA determines that every PHY that is connected to the MDIO signal is able to accept management frames that are not preceded by the preamble pattern, then the STA may suppress the generation of the preamble pattern, and may initiate management frames with the ST (Start of Frame) pattern.

22.2.4.4.3 ST (start of frame)

The start of frame is indicated by a <01> pattern. This pattern assures transitions from the default logic one line state to zero and back to one.

22.2.4.4.4 OP (operation code)

The operation code for a read transaction is <10>, while the operation code for a write transaction is <01>.

22.2.4.4.5 PHYAD (PHY Address)

The PHY Address is five bits, allowing 32 unique PHY addresses. The first PHY address bit transmitted and received is the MSB of the address. A PHY that is connected to the station management entity via the mechanical interface defined in 22.6 shall always respond to transactions addressed to PHY Address zero <00000>. A station management entity that is attached to multiple PHYs must have a priori knowledge of the appropriate PHY Address for each PHY.

22.2.4.4.6 REGAD (Register Address)

The Register Address is five bits, allowing 32 individual registers to be addressed within each PHY. The first Register Address bit transmitted and received is the MSB of the address. The register accessed at Register Address zero <00000> shall be the control register defined in 22.2.4.1, and the register accessed at Register Address one <00001> shall be the status register defined in 22.2.4.2.

22.2.4.4.7 TA (turnaround)

The turnaround time is a 2 bit time spacing between the Register Address field and the Data field of a management frame to avoid contention during a read transaction. For a read transaction, both the STA and the PHY shall remain in a high-impedance state for the first bit time of the turnaround. The PHY shall drive a zero bit during the second bit time of the turnaround of a read transaction. During a write transaction, the STA shall drive a one bit for the first bit time of the turnaround and a zero bit for the second bit time of the turnaround. Figure 22-13 shows the behavior of the MDIO signal during the turnaround field of a read transaction.

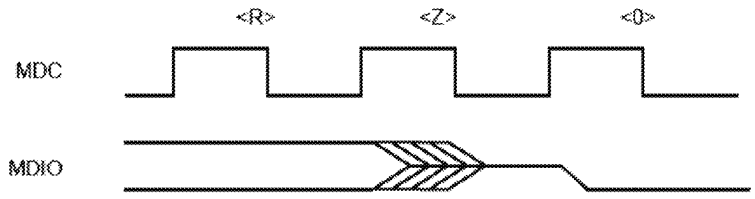


Figure 22-13—Behavior of MDIO during TA field of a read transaction

22.2.4.4.8 DATA (data)

The data field is 16 bits. The first data bit transmitted and received shall be bit 15 of the register being addressed.

22.3 Signal timing characteristics

All signal timing characteristics shall be measured using the techniques specified in annex 22C. The signal threshold potentials $V_{ih(min)}$ and $V_{il(max)}$ are defined in 22.4.4.1.

The HIGH time of an MII signal is defined as the length of time that the potential of the signal is greater than or equal to $V_{ih(min)}$. The LOW time of an MII signal is defined as the length of time that the potential of the signal is less than or equal to $V_{il(max)}$.

The setup time of an MII signal relative to an MII clock edge is defined as the length of time between when the signal exits and remains out of the switching region and when the clock enters the switching region. The hold time of an MII signal relative to an MII clock edge is defined as the length of time between when the clock exits the switching region and when the signal enters the switching region.

The propagation delay from an MII clock edge to a valid MII signal is defined as the length of time between when the clock exits the switching region and when the signal exits and remains out of the switching region.

22.3.1 Signals that are synchronous to TX_CLK

Figure 22-14 shows the timing relationship for the signals associated with the transmit data path at the MII connector. The clock to output delay shall be a minimum of 0 ns and a maximum of 25 ns.

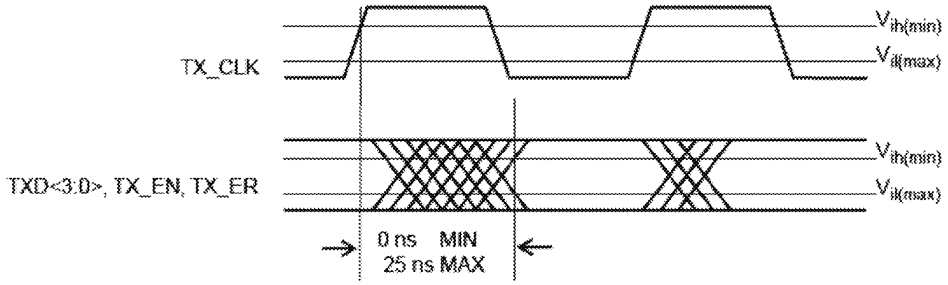


Figure 22-14—Transmit signal timing relationships at the MII

22.3.1.1 TX_EN

TX_EN is transitioned by the Reconciliation sublayer synchronously with respect to the TX_CLK rising edge with the timing as shown in figure 22-14.

22.3.1.2 TXD<3:0>

TXD<3:0> is transitioned by the Reconciliation sublayer synchronously with respect to the TX_CLK rising edge with the timing as depicted in figure 22-14.

22.3.1.3 TX_ER

TX_ER is transitioned synchronously with respect to the rising edge of TX_CLK as shown in figure 22-14.

22.3.2 Signals that are synchronous to RX_CLK

Figure 22-15 shows the timing relationship for the signals associated with the receive data path at the MII connector. The timing is referenced to the rising edge of the RX_CLK. The input setup time shall be a minimum of 10 ns and the input hold time shall be a minimum of 10 ns.

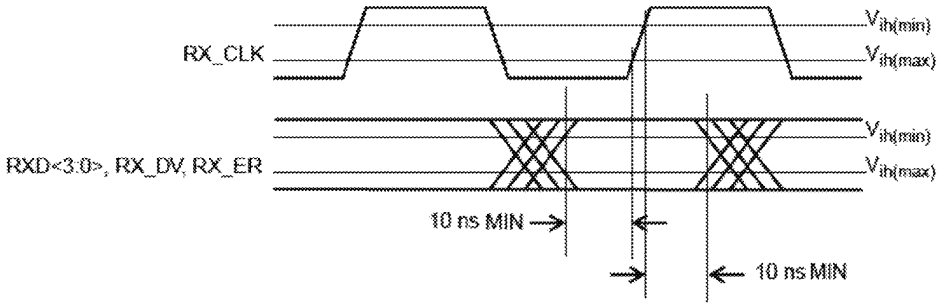


Figure 22-15—Receive signal timing relationships at the MII

22.3.2.1 RX_DV

RX_DV is sampled by the Reconciliation sublayer synchronously with respect to the rising edge of RX_CLK with the timing shown in figure 22-15.

22.3.2.2 RXD<3:0>

RXD<3:0> is sampled by the Reconciliation sublayer synchronously with respect to the rising edge of RX_CLK as shown in figure 22-15. The RXD<3:0> timing requirements must be met at all rising edges of RX_CLK.

22.3.2.3 RX_ER

RX_ER is sampled by the Reconciliation sublayer synchronously with respect to the rising edge of RX_CLK as shown in figure 22-15. The RX_ER timing requirements must be met at all rising edges of RX_CLK.

22.3.3 Signals that have no required clock relationship

22.3.3.1 CRS

CRS is driven by the PHY. Transitions on CRS have no required relationship to either of the clock signals provided at the MII.

22.3.3.2 COL

COL is driven by the PHY. Transitions on COL have no required relationship to either of the clock signals provided at the MII.

22.3.4 MDIO timing relationship to MDC

MDIO (Management Data Input/Output) is a bidirectional signal that can be sourced by the Station Management Entity (STA) or the PHY. When the STA sources the MDIO signal, the STA shall provide a minimum of 10 ns of setup time and a minimum of 10 ns of hold time referenced to the rising edge of MDC, as shown in figure 22-16, measured at the MII connector.

When the MDIO signal is sourced by the PHY, it is sampled by the STA synchronously with respect to the rising edge of MDC. The clock to output delay from the PHY, as measured at the MII connector, shall be a minimum of 0 ns, and a maximum of 300 ns, as shown in figure 22-17.

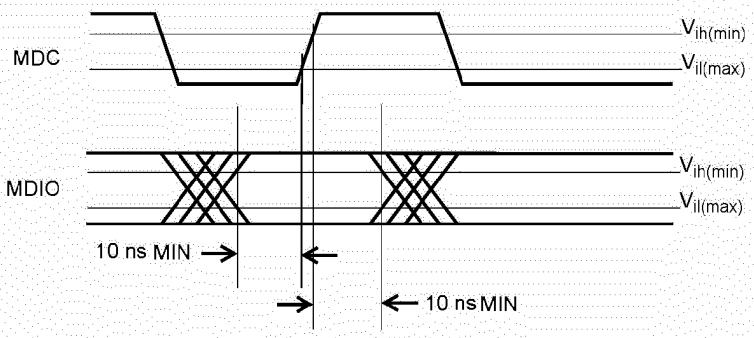


Figure 22-16—MDIO sourced by STA

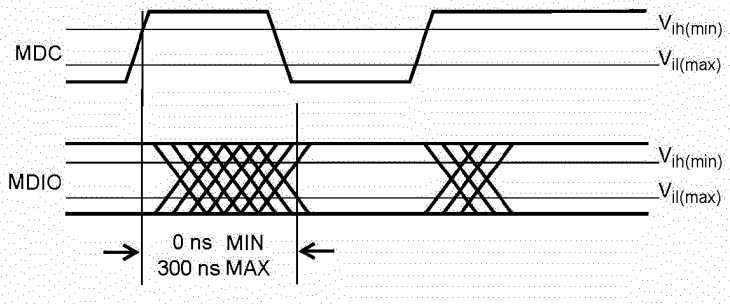


Figure 22-17—MDIO sourced by PHY

22.4 Electrical characteristics

The electrical characteristics of the MII are specified such that the three application environments described in 22.1 are accommodated. The electrical specifications are optimized for the integrated circuit to integrated circuit application environment, but integrated circuit drivers and receivers that are implemented in compliance with the specification will also support the mother board to daughter board and short cable application environments, provided those environments are constrained to the limits specified in this clause.

NOTE—The specifications for the driver and receiver characteristics can be met with TTL compatible input and output buffers implemented in a digital CMOS ASIC process.

22.4.1 Signal levels

The MII uses TTL signal levels, which are compatible with devices operating at a nominal supply voltage of either 5.0 or 3.3 V.

NOTE—Care should be taken to ensure that all MII receivers can tolerate dc input potentials from 0.00 V to 5.50 V, referenced to the COMMON signal, and transient input potentials as high as 7.3 V, or as low as –1.8 V, referenced to the COMMON signal, which can occur when MII signals change state. The transient duration will not exceed 15 ns. The dc source impedance will be no less than $R_{oh(min)}$. The transient source impedance will be no less than (68 × 0.85 =) 57.8 Ω.

22.4.2 Signal paths

MII signals can be divided into two groups: signals that go between the STA and the PHY, and signals that go between the Reconciliation sublayer and the PHY.

Signals between the STA and the PHY may connect to one or more PHYs. When a signal goes between the STA and a single PHY, the signal's path is a point-to-point transmission path. When a signal goes between the STA and multiple PHYs, the signal's transmission path has drivers and receivers attached in any order along the length of the path and is not considered a point-to-point transmission path.

Signals between the Reconciliation sublayer and the PHY may also connect to one or more PHYs. However, the transmission path of each of these signals shall be either a point-to-point transmission path or a sequence of point-to-point transmission paths connected in series.

All connections to a point-to-point transmission path are at the path ends. The simplest point-to-point transmission path has a driver at one end and a receiver at the other. Point-to-point transmission paths can also have more than one driver and more than one receiver if the drivers and receivers are lumped at the ends of the path, and if the maximum propagation delay between the drivers and receivers at a given end of the path is a very small fraction of the 10%–90% rise/fall time for signals driven onto the path.

The MII shall use unbalanced signal transmission paths. The characteristic impedance Z_o of transmission paths is not specified for electrically short paths where transmission line reflections can be safely ignored.

The characteristic impedance Z_o of electrically long transmission paths or path segments shall be 68 | ± 15%.

The output impedance of the driver shall be used to control transmission line reflections on all electrically long point-to-point signal paths.

NOTE—In the context of this clause, a transmission path whose round-trip propagation delay is less than half of the 10%–90% rise/fall time of signals driven onto the path is considered an electrically short transmission path.

22.4.3 Driver characteristics

The driver characteristics defined in this clause apply to all MII signal drivers. The driver characteristics are specified in terms of both their ac and dc characteristics.

NOTE—Rail-to-rail drivers that comply with the driver output V-I diagrams in annex 22B will meet the following ac and dc characteristics.

22.4.3.1 DC characteristics

The high (one) logic level output potential V_{oh} shall be no less than 2.40 V at an output current I_{oh} of –4.0 mA. The low (zero) logic level output potential V_{ol} shall not be greater than 0.40 V at an output current I_{ol} of 4.0 mA.

22.4.3.2 AC characteristics

Drivers must also meet certain ac specifications in order to ensure adequate signal quality for electrically long point-to-point transmission paths. The ac specifications shall guarantee the following performance requirements.

The initial incident potential change arriving at the receiving end of a point-to-point MII signal path plus its reflection from the receiving end of the path must switch the receiver input potential monotonically from a valid high (one) level to V_{il} ″ $V_{il(max)} - 200$ mV, or from a valid low (zero) level to $V_{ih} \geq V_{ih(min)} + 200$ mV.

Subsequent incident potential changes arriving at the receiving end of a point-to-point MII signal path plus their reflections from the receiving end of the path must not cause the receiver input potential to reenter the range $V_{il(max)} - 200\ mV < V_i < V_{ih(min)} + 200\ mV$ except when switching from one valid logic level to the other. Such subsequent incident potential changes result from a mismatch between the characteristic impedance of the signal path and the driver output impedance.

22.4.4 Receiver characteristics

The receiver characteristics are specified in terms of the threshold levels for the logical high (one) and logical low (zero) states. In addition, receivers must meet the input current and capacitance limits.

22.4.4.1 Voltage thresholds

An input potential V_i of 2.00 V or greater shall be interpreted by the receiver as a logical high (one). Thus, $V_{ih(min)} = 2.00$ V. An input potential V_i of 0.80 V or less shall be interpreted by the receiver as a logical low (zero). Thus, $V_{il(max)} = 0.80$ V. The switching region is defined as signal potentials greater than $V_{il(max)}$ and less than $V_{ih(min)}$. When the input signal potential is in the switching region, the receiver output is undefined.

22.4.4.2 Input current

The input current requirements shall be measured at the MII connector and shall be referenced to the +5 V supply and COMMON pins of the connector. The input current requirements shall be met across the full range of supply voltage specified in 22.5.1.

The bidirectional signal MDIO has two sets of input current requirements. The MDIO drivers must be disabled when the input current measurement is made.

The input current characteristics for all MII signals shall fall within the limits specified in table 22-10.

Table 10—Input current limits

Symbol	Parameter	Condition	Signal(s)	Min (μA)	Max (μA)
I_{ih}	Input High Current	V_i=5.25 V	All except COL, MDC, MDIO*	—	200
			COL†	—	20
			MDC‡	—	20
			MDIO§	—	3000
			MDIO**	—	20
I_{il}	Input Low Current	V_i=0.00 V	All except COL, MDC, MDIO[a]	–20	—
			COL[b]	–200	—
			MDC[c]	–20	—
			MDIO[d]	–180	—
			MDIO[e]	–3800	—

Table 10—Input current limits *(Continued)*

Symbol	Parameter	Condition	Signal(s)	Min (μA)	Max (μA)
I_{iq}	Input Quiescent Current	V_i=2.4 V	MDIO[d]	—	1450
			MDIO[e]	–1450	—

*Measured at input of Reconciliation sublayer for CRS, RXD<3:0>, RX_CLK, RX_DV, RX_ER, and TX_CLK. Measured at inputs of PHY for TXD<3:0>, TX_EN, and TX_ER.
†Measured at input of Reconciliation sublayer.
‡Measured at input of PHY.
§Measured at input of STA.
**Measured at input of PHY, which can be attached via the mechanical interface specified in 22.6.

NOTE—These limits for dc input current allow the use of weak resistive pull-ups or pull-downs on the input of each MII signal. They allow the use of weak resistive pull-downs on the signals other than COL, MDC, and MDIO. They allow the use of a weak resistive pull-up on the signal COL. They allow the use of a resistive pull-down of 2 k | ± 5% on the MDIO signal in the STA. They require a resistive pull-up of 1.5 k | ± 5% on the MDIO signal in a PHY that is attached to the MII via the mechanical interface specified in 22.6. The limits on MDC and MDIO allow the signals to be "bused" to several PHYs that are contained on the same printed circuit assembly, with a single PHY attached via the MII connector.

22.4.4.3 Input capacitance

For all signals other than MDIO, the receiver input capacitance C_i shall not exceed 8 pF.

For the MDIO signal, the transceiver input capacitance shall not exceed 10 pF.

22.4.5 Cable characteristics

The MII cable consists of a bundle of individual twisted pairs of conductors with an overall shield covering this bundle. Each twisted pair shall be composed of a conductor for an individual signal and a return path dedicated to that signal.

NOTE—It is recommended that the signals RX_CLK and TX_CLK be connected to pairs that are located in the center of the cable bundle.

22.4.5.1 Conductor size

The specifications for dc resistance in 22.4.5.6 and characteristic impedance in 22.4.5.2 assume a conductor size of 0.32 mm (28 AWG).

22.4.5.2 Characteristic impedance

The single-ended characteristic impedance of each twisted pair shall be 68 | ± 10%. The characteristic impedance measurement shall be performed with the return conductor connected to the cable's overall shield at both ends of the cable.

22.4.5.3 Delay

The propagation delay for each twisted pair, measured from the MII connector to the PHY, shall not exceed 2.5 ns. The measurement shall be made with the return conductor of the pair connected to the cable's overall shield at both ends of the cable. The propagation delay shall be measured at a frequency of 25 MHz.

22.4.5.4 Delay variation

The variation in the propagation delay of the twisted pairs in a given cable bundle, measured from the MII connector to the PHY, shall not exceed 0.1 ns. The measurement shall be made with the return conductor of the pair connected to the cable's overall shield at both ends of the cable.

22.4.5.5 Shielding

The overall shield must provide sufficient shielding to meet the requirements of protection against electromagnetic interference.

The overall shield shall be terminated to the connector shell as defined in 22.6.2. A double shield, consisting of both braid and foil shielding, is strongly recommended.

22.4.5.6 DC resistance

The dc resistance of each conductor in the cable, including the contact resistance of the connector, shall not exceed 150 m| measured from the MII connector to the remote PHY.

22.4.6 Hot insertion and removal

The insertion or removal of a PHY from the MII with power applied (hot insertion or removal) shall not damage the devices on either side of the MII. In order to prevent contention between multiple output buffers driving the PHY output signals, a PHY that is attached to the MII via the mechanical interface defined in 22.6 shall ensure that its output buffers present a high impedance to the MII during the insertion process, and shall ensure that this condition persists until the output buffers are enabled via the Isolate control bit in the management interface basic register.

NOTE—The act of inserting or removing a PHY from an operational system may cause the loss of one or more packets or management frames that may be in transit across the MII or MDI.

22.5 Power supply

When the mechanical interface defined in 22.6 is used to interconnect printed circuit subassemblies, the Reconciliation sublayer shall provide a regulated power supply for use by the PHY.

The power supply shall use the following MII lines:

+5 V: The plus voltage output to the PHY.

COMMON: The return to the power supply.

22.5.1 Supply voltage

The regulated supply voltage to the PHY shall be 5 Vdc ± 5% at the MII connector with respect to the COMMON circuit at the MII over the range of load current from 0 to 750 mA. The method of over/under voltage protection is not specified; however, under no conditions of operation shall the source apply a voltage to the +5 V circuit of less than 0 V or greater than +5.25 Vdc.

Implementations that provide a conversion from the MII to the Attachment Unit Interface (AUI) to support connection to 10 Mb/s Medium Attachment Units (MAUs) will require a supplemental power source in order to meet the AUI power supply requirements specified in 7.5.2.5.

22.5.2 Load current

The sum of the currents carried on the +5 V lines shall not exceed 750 mA, measured at the MII connector. The surge current drawn by the PHY shall not exceed 5 A peak for a period of 10 ms. The PHY shall be capable of powering up from 750 mA current limited sources.

22.5.3 Short-circuit protection

Adequate provisions shall be made to ensure protection of the power supply from overload conditions, including a short circuit between the +5 V lines and the COMMON lines.

22.6 Mechanical characteristics

When the MII is used to interconnect two printed circuit assemblies via a short length of cable, the cable shall be connected to the circuit assembly that implements the Reconciliation sublayer by means of the mechanical interface defined in this clause.

22.6.1 Definition of mechanical interface

A 40-pole connector having the mechanical mateability dimensions as specified in IEC 1076-3-101: 1995 shall be used for the MII connector. The circuit assembly that contains the MAC sublayer and Reconciliation sublayer shall have a female connector with screw locks, and the mating cable shall have a male connector with jack screws.

No requirements are imposed on the mechanical interface used to connect the MII cable to the PHY circuit assembly when the MII cable is permanently attached to the PHY circuit assembly, as shown in figure 22-2. If the cable is not permanently attached to the PHY circuit assembly, then a male connector with jack screws shall be used for the MII connector at the PHY circuit assembly.

NOTE—All MII conformance tests are performed at the mating surfaces of the MII connector at the Reconciliation sublayer end of the cable. If a PHY circuit assembly does not have a permanently attached cable, the vendor must ensure that all of the requirements of this clause are also met when a cable that meets the requirements of 22.4.5 is used to attach the PHY circuit assembly to the circuit assembly that contains the Reconciliation sublayer.

22.6.2 Shielding effectiveness and transfer impedance

The shells of these connectors shall be plated with conductive material to ensure the integrity of the current path from the cable shield to the chassis. The transfer impedance of this path shall not exceed the values listed in table 22-11, after a minimum of 500 cycles of mating and unmating. The shield transfer impedance values listed in the table are measured in accordance with the procedure defined in annex L of IEEE P1394 [A18].

Table 11—Transfer impedance performance requirements

Frequency	Value
30 MHz	–26 dB
159 MHz	–13 dB
500 MHz	–5 dB

All additions to provide for female shell to male shell conductivity shall be on the shell of the connector with male contacts. There should be multiple contact points around the sides of this shell to provide for shield continuity.

22.6.3 Connector pin numbering

Figure 22-18 depicts the MII connector pin numbering, as seen looking into the contacts of a female connector from the mating side.

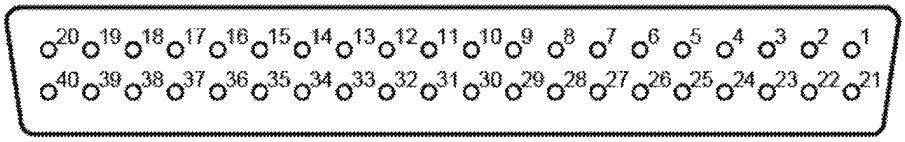


Figure 22-18—MII connector pin numbering

22.6.4 Clearance dimensions

The circuit assembly that contains the MAC sublayer and Reconciliation sublayer shall provide sufficient clearance around the MII connector to allow the attachment of cables that use die cast metal backshells and overmold assemblies. This requirement may be met by providing the clearance dimensions shown in figure 22-19.

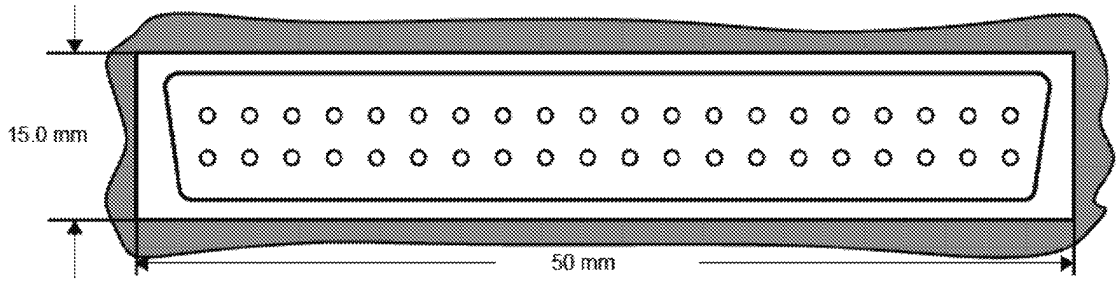


Figure 22-19—MII connector clearance dimensions

22.6.5 Contact assignments

Table 22-12 shows the assignment of circuits to connector contacts.

Table 12—MII connector contact assignments

Contact	Signal name	Contact	Signal name
1	+5 V	21	+5 V
2	MDIO	22	COMMON
3	MDC	23	COMMON
4	RXD<3>	24	COMMON
5	RXD<2>	25	COMMON
6	RXD<1>	26	COMMON
7	RXD<0>	27	COMMON
8	RX_DV	28	COMMON
9	RX_CLK	29	COMMON
10	RX_ER	30	COMMON
11	TX_ER	31	COMMON
12	TX_CLK	32	COMMON
13	TX_EN	33	COMMON
14	TXD<0>	34	COMMON
15	TXD<1>	35	COMMON
16	TXD<2>	36	COMMON
17	TXD<3>	37	COMMON
18	COL	38	COMMON
19	CRS	39	COMMON
20	+5 V	40	+5 V

22.7 Protocol Implementation Conformance Statement (PICS) proforma for clause 22, Reconciliation Sublayer (RS) and Media Independent Interface (MII)[29]

22.7.1 Introduction

The supplier of a protocol implementation that is claimed to conform to IEEE Std 802.3u-1995, Reconciliation Sublayer (RS) and Media Independent Interface (MII), shall complete the following Protocol Implementation Conformance Statement (PICS) proforma.

A detailed description of the symbols used in the PICS proforma, along with instructions for completing the PICS proforma, can be found in clause 21.

22.7.2 Identification

22.7.2.1 Implementation identification

Supplier	
Contact point for enquiries about the PICS	
Implementation Name(s) and Version(s)	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Names(s)	
NOTES 1—Only the first three items are required for all implementations; other information may be completed as appropriate in meeting the requirements for the identification. 2—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

22.7.2.2 Protocol summary

Identification of protocol standard	IEEE Std 802.3u-1995, Reconciliation Sublayer (RS) and Media Independent Interface (MII)
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required? No [ ] Yes [ ] (See clause 21; the answer Yes means that the implementation does not conform to the standard.)	
Date of Statement	

[29] *Copyright release for PICS proformas* Users of this standard may freely reproduce the PICS proforma in this annex so that it can be used for its intended purpose and may further publish the completed PICS.

22.7.3 PICS proforma tables for reconciliation sublayer and media independent interface

22.7.3.1 Mapping of PLS service primitives

Item	Feature	Subclause	Status	Support	Value/Comment
PL1	Response to RX_ER	22.2.1.5	M		Must produce FrameCheckError at MAC

22.7.3.2 MII signal functional specifications

Item	Feature	Subclause	Status	Support	Value/Comment
SF1	TX_CLK frequency	22.2.2.1	M		25% of transmitted data rate (25 MHz or 2.5 MHz)
SF2	TX_CLK duty cycle	22.2.2.1	M		35% to 65%
SF3	RX_CLK min high/low time	22.2.2.2	M		35% of nominal period
SF4	RX_CLK synchronous to recovered data	22.2.2.2	M		
SF5	RX_CLK frequency	22.2.2.2	M		25% of received data rate (25 MHz or 2.5 MHz)
SF6	RX_CLK duty cycle	22.2.2.2	M		35% to 65%
SF7	RX_CLK source due to loss of signal	22.2.2.2	M		Nominal clock reference (e.g., TX_CLK reference)
SF8	RX_CLK transitions only while RX_DV de-asserted	22.2.2.2	M		
SF9	RX_CLK max high/low time following de-assertion of RX_DV	22.2.2.2	M		max 2 times the nominal period
SF10	TX_EN assertion	22.2.2.3	M		On first nibble of preamble
SF11	TX_EN remains asserted	22.2.2.3	M		Stay asserted while all nibbles are transmitted over MII
SF12	TX_EN transitions	22.2.2.3	M		Synchronous with TX_CLK
SF13	TX_EN negation	22.2.2.3	M		Before first TX_CLK after final nibble of frame
SF14	TXD<3:0> transitions	22.2.2.4	M		Synchronous with TX_CLK
SF15	TXD<3:0> effect on PHY while TX_EN is de-asserted	22.2.2.4	M		No effect
SF16	TX_ER transitions	22.2.2.5	M		Synchronous with TX_CLK
SF17	TX_ER effect on PHY while TX_EN is asserted	22.2.2.5	M		Cause PHY to emit invalid symbol
SF18	TX_ER effect on PHY while operating at 10 Mb/s, or when TX_EN is de-asserted	22.2.2.5	M		No effect on PHY

Item	Feature	Subclause	Status	Support	Value/Comment
SF19	TX_ER implementation	22.2.2.5	M		At MII of a PHY
SF20	TX_ER pulled down if not actively driven	22.2.2.5	M		At MII of a repeater or MAC/RS only
SF21	RX_DV transitions	22.2.2.6	M		Synchronous with RX_CLK
SF22	RX_DV assertion	22.2.2.6	M		From first recovered nibble to final nibble of a frame per figure 22-6
SF23	RX_DV negation	22.2.2.6	M		Before the first RX_CLK follows the final nibble per figure 22-6
SF24	RXD<3:0> effect on Reconciliation sublayer while RX_DV is de-asserted	22.2.2.7	M		No effect
SF25	RX_ER assertion	22.2.2.8	M		By PHY to indicate error
SF26	RX_ER transitions	22.2.2.8	M		Synchronous with RX_CLK
SF27	RX_ER effect on Reconciliation sublayer while RX_DV is de-asserted	22.2.2.8	M		No effect
SF28	CRS assertion	22.2.2.9	M		By PHY when either transmit or receive is NON-IDLE
SF29	CRS de-assertion	22.2.2.9	M		By PHY when both transmit and receive are IDLE
SF30	CRS assertion during collision	22.2.2.9	M		Remain asserted throughout
SF31	COL assertion	22.2.2.10	M		By PHY upon detection of collision on medium
SF32	COL remains asserted while collision persists	22.2.2.10	M		
SF33	COL response to SQE	22.2.2.10	M		Assertion by PHY
SF34	MDC min high/low time	22.2.2.11	M		160 ns
SF35	MDC min period	22.2.2.11	M		400 ns
SF36	MDIO uses three-state drivers	22.2.2.12	M		
SF37	PHY pullup on MDIO	22.2.2.12	M		1.5 k⏐ ± 5% (to +5 V)
SF38	STA pulldown on MDIO	22.2.2.12	M		2 k⏐ ± 5% (to 0 V)

22.7.3.3 Frame structure

Item	Feature	Subclause	Status	Support	Value/Comment
FS1	Format of transmitted frames	22.2.3	M		Per figure 22-10
FS2	Nibble transmission order	22.2.3	M		Per figure 22-11
FS3	Preamble 7 octets long	22.2.3.2.1	M		10101010 10101010 10101010 10101010 10101010 10101010 10101010
FS4	Preamble and SFD transmission	22.2.3.2.1	M		Per table 22-3
FS5	Preamble and SFD reception	22.2.3.2.2	M		Per table 22-4, table 22-5
FS6	N octets transmitted as 2N nibbles	22.2.3.3	M		Per figure 22-11
FS7	Indication of excess nibbles	22.2.3.5	M		Frame contains non-integer number of octets is received

22.7.3.4 Management functions

Item	Feature	Subclause	Status	Support	Value/Comment
MF1	Incorporate of basic register set	22.2.4	M		Two 16-bit registers as Control register (register 0) and Status register (register 1)
MF2	Action on reset	22.2.4.1.1	M		Reset the entire PHY including Control and Status to default value and 0.15 ″ 1
MF3	Return 1 until reset completed	22.2.4.1.1	M		Yes (when reset is done, 0.15 is self clearing)
MF4	Reset completes within 0.5 s	22.2.4.1.1	M		
MF5	Loopback mode	22.2.4.1.2	M		Whenever 0.14 is 1
MF6	Receive circuitry isolated from network in loopback mode	22.2.4.1.2	M		
MF7	Effect of assertion of TX_EN in loopback mode	22.2.4.1.2	M		No transmission
MF8	Propagation of data in loopback mode	22.2.4.1.2	M		PHY accepts transmit data and return it as receive data
MF9	Delay from TX_EN to RX_DV in loopback mode	22.2.4.1.2	M		Less than 512 BT
MF10	Behavior of COL in loopback mode	22.2.4.1.2	M		De-asserted (for 0.7 = 0)
MF11	Behavior of COL in loopback mode	22.2.4.1.2	M		If 0.7 = 1, see MF33 and MF34

Item	Feature	Subclause	Status	Support	Value/Comment
MF12	Value of speed selection bit for single speed PHY	22.2.4.1.3	M		Set to match the correct PHY speed
MF13	Single speed PHY ignores writes to speed selection bit	22.2.4.1.3	M		
MF14	Auto-Negotiation enable	22.2.4.1.4	M		By setting 0.12 = 1
MF15	Duplex mode, speed selection have no effect when Auto-Negotiation is enabled	22.2.4.1.4	M		If 0.12=1, bits 0.13 and 0.8 have no effect on link configuration
MF16	PHY without Auto-Negotiation returns value of zero	22.2.4.1.4	M		Yes (if 1.3=0, then 0.12=0)
MF17	PHY without Auto-Negotiation ignores writes to enable bit	22.2.4.1.4	M		Yes (if 1.3=0, 0.12 always = 0 and cannot be changed)
MF18	Response to management transactions in power down	22.2.4.1.5	M		Remains active
MF19	Spurious signals in power down	22.2.4.1.5	M		None (not allowed)
MF20	TX_CLK and RX_CLK stabilize within 0.5 s	22.2.4.1.5	M		Yes (after both bits 0.11 and 0.10 are cleared to zero)
MF21	PHY Response to input signals while isolated	22.2.4.1.6	M		NONE
MF22	High impedance on PHY output signals while isolated	22.2.4.1.6	M		Yes (TX_CLK, RX_CLK, RX_DV, RX_ER, RXD<3:0>, COL, and CRS)
MF23	Response to management transactions while isolated	22.2.4.1.6	M		Remains active
MF24	Default value of isolate	22.2.4.1.6	M		0.10 =1
MF25	PHY without Auto-Negotiation returns value of zero	22.2.4.1.7	M		0.9 = 0 if 1.3 = 0 or 0.12 = 0
MF26	PHY without Auto-Negotiation ignores writes to restart bit	22.2.4.1.7	M		0.9 = 0, cannot be changed if 1.3 = 0 or 0.12 = 0
MF27	Restart Auto-Negotiation	22.2.4.1.7	M		When 0.9 = 1 if 0.12 = 1 and 1.3 = 1
MF28	Return 1 until Auto-Negotiation initiated	22.2.4.1.7	M		0.9 is self clearing to 0
MF29	Auto-Negotiation not effected by clearing bit	22.2.4.1.7	M		
MF30	Value of duplex mode bit for PHYs with one duplex mode	22.2.4.1.8	M		Set 0.8 to match the correct PHY duplex mode
MF31	PHY with one duplex mode ignores writes to duplex bit	22.2.4.1.8	M		Yes (0.8 remains unchanged)
MF32	Loopback not affected by duplex mode	22.2.4.1.8	M		Yes (0.8 has no effect on PHY when 0.14 = 1)
MF33	Assertion of COL in collision test mode	22.2.4.1.9	M		Within 512 BT after TX_EN is asserted

Item	Feature	Subclause	Status	Support	Value/Comment
MF34	De-assertion of COL in collision test mode	22.2.4.1.9	M		Within 4 BT after TX_EN is de-asserted
MF35	Reserved bits written as zero	22.2.4.1.10	M		
MF36	Reserved bits ignored when read	22.2.4.1.10	M		
MF37	PHY returns 0 in reserved bits	22.2.4.1.10	M		
MF38	Effect of write on status register	22.2.4.2	M		No effect
MF39	Reserved bits ignored when read	22.2.4.2.6	M		
MF40	PHY returns 0 in reserved bits	22.2.4.2.6	M		
MF41	PHY returns 0 if Auto-Negotiation disabled	22.2.4.2.8	M		Yes (1.5 = 0 when 0.12 = 0)
MF42	PHY returns 0 if it lacks ability to perform Auto-Negotiation	22.2.4.2.8	M		Yes (1.5 = 0 when 1.3 = 0)
MF43	Remote fault has latching function	22.2.4.2.9	M		Yes (once set will remain set until cleared)
MF44	Remote fault cleared on read	22.2.4.2.9	M		Yes
MF45	Remote fault cleared on reset	22.2.4.2.9	M		Yes (when 0.15 = 1)
MF46	PHY without remote fault returns value of zero	22.2.4.2.9	M		Yes (1.4 always 0)
MF47	Link status has latching function	22.2.4.2.11	M		Yes (once cleared by link failure will remain cleared until read by MII)
MF48	Jabber detect has latching function	22.2.4.2.12	M		Yes (once set will remain set until cleared)
MF49	Jabber detect cleared on read	22.2.4.2.12	M		
MF50	Jabber detect cleared on reset	22.2.4.2.12	M		
MF51	100BASE-T4 and 100BASE-X PHYs return 0 for jabber detect	22.2.4.2.12	M		Yes (1.1 always = 0 for 100BASE-T4 and 100BASE-TX)
MF52	MDIO not driven if register read is unimplemented	22.2.4.3	M		Yes (MDIO remain high impedance)
MF53	Write has no effect if register written is unimplemented	22.2.4.3	M		
MF54	Registers 2 and 3 constitute unique identifier for PHY type	22.2.4.3.1	M		
MF55	MSB of PHY identifier is 2.15	22.2.4.3.1	M		
MF56	LSB of PHY identifier is 3.0	22.2.4.3.1	M		
MF57	Composition of PHY identifier	22.2.4.3.1	M		22-bit OUI, 6-bit model, 4-bit version per figure 22-12
MF58	Format of management frames	22.2.4.4	M		Per table 22-9

Item	Feature	Subclause	Status	Support	Value/Comment
MF59	Idle condition on MDIO	22.2.4.4.1	M		High impedance state
MF60	MDIO preamble sent by STA	22.2.4.4.2	M		32 contiguous logic one bits
MF61	MDIO preamble observed by PHY	22.2.4.4.2	M		32 contiguous logic one bits
MF62	Assignment of PHYAD 0	22.2.4.4.5	M		Address of PHY attached via Mechanical Interface
MF63	Assignment of REGAD 0	22.2.4.4.6	M		MII control register address
MF64	Assignment of REGAD 1	22.2.4.4.6	M		MII status register address
MF65	High impedance during first bit time of turnaround in read transaction	22.2.4.4.7	M		
MF66	PHY drives zero during second bit time of turnaround in read transaction	22.2.4.4.7	M		
MF67	STA drives MDIO during turn-around in write transaction	22.2.4.4.7	M		
MF68	First data bit transmitted	22.2.4.4.8	M		Bit 15 of the register being addressed

22.7.3.5 Signal timing characteristics

Item	Feature	Subclause	Status	Support	Value/Comment
ST1	Timing characteristics measured in accordance with annex 22C	22.3	M		
ST2	Transmit signal clock to output delay	22.3.1	M		Min = 0 ns; Max = 25 ns per figure 22-14
ST3	Receive signal setup time	22.3.2	M		Min = 10 ns per figure 22-15
ST4	Receive signal hold time	22.3.2	M		Min = 10 ns per figure 22-15
ST5	MDIO setup and hold time	22.3.4	M		Setup min = 10 ns; Hold min = 10 ns per figure 22-16
ST6	MDIO clock to output delay	22.3.4	M		Min = 0 ns; Max = 300 ns per figure 22-17

22.7.3.6 Electrical characteristics

Item	Feature	Subclause	Status	Support	Value/Comment
EC1	Signal paths are either point to point, or a sequence of point-to-point transmission paths	22.4.2	M		
EC2	MII uses unbalanced signal transmission paths	22.4.2	M		
EC3	Characteristic impedance of electrically long paths	22.4.2	M		68 Ω ± 15%
EC4	Output impedance of driver used to control reflections	22.4.2	M		On all electrically long point to point signal paths
EC5	V_{oh}	22.4.3.1	M		≥ 2.4 V (I_{oh} = –4 mA)
EC6	V_{ol}	22.4.3.1	M		″ 0.4 V (I_{ol} = 4 mA)
EC7	Performance requirements to be guaranteed by ac specifications	22.4.3.2	M		Min switching potential change (including its reflection) ≥ 1.8 V
EC8	$V_{ih(min)}$	22.4.4.1	M		2 V
EC9	$V_{il(max)}$	22.4.4.1	M		0.8 V
EC10	Input current measurement point	22.4.4.2	M		At MII connector
EC11	Input current reference potentials	22.4.4.2	M		Reference to MII connector +5 V and COMMON pins
EC12	Input current reference potential range	22.4.4.2	M		0 V to 5.25 V
EC13	Input current limits	22.4.4.2	M		Per table 22-10

Item	Feature	Subclause	Status	Support	Value/Comment
EC14	Input capacitance for signals other than MDIO	22.4.4.3	M		″ 8 pF
EC15	Input capacitance for MDIO	22.4.4.3	M		″ 10 pF
EC16	Twisted-pair composition	22.4.5	M		Conductor for each signal with dedicated return path
EC17	Single-ended characteristic impedance	22.4.5.2	M		68 | ± 10%
EC18	Characteristic impedance measurement method	22.4.5.2	M		With return conductor connected to cable shield
EC19	Twisted-pair propagation delay	22.4.5.3	M		″ 2.5 ns
EC20	Twisted-pair propagation delay measurement method	22.4.5.3	M		With return conductor connected to cable shield
EC21	Twisted-pair propagation delay measurement frequency	22.4.5.3	M		25 MHz
EC22	Twisted-pair propagation delay variation	22.4.5.4	M		″ 0.1 ns
EC23	Twisted-pair propagation delay variation measurement method	22.4.5.4	M		With return conductor connected to cable shield
EC24	Cable shield termination	22.4.5.5	M		To the connector shell
EC25	Cable conductor DC resistance	22.4.5.6	M		″ 150 m |
EC26	Effect of hot insertion/removal	22.4.6	M		Causes no damage
EC27	State of PHY output buffers during hot insertion	22.4.6	M		High impedance
EC28	State of PHY output buffers after hot insertion	22.4.6	M		High impedance until enabled via Isolate bit

22.7.3.7 Power supply

Item	Feature	Subclause	Status	Support	Value/Comment
PS1	Regulated power supply provided	22.5	M		To PHY by Reconciliation sublayer
PS2	Power supply lines	22.5	M		+5 V and COMMON (return of +5 V)
PS3	Regulated supply voltage limits	22.5.1	M		5 Vdc ± 5%
PS4	Over/under voltage limits	22.5.1	M		Over limit = 5.25 Vdc Under limit = 0 V
PS5	Load current limit	22.5.2	M		750 mA
PS6	Surge current limit	22.5.2	M		" 5 A peak for 10 ms
PS7	PHY can power up from current limited source	22.5.2	M		From 750 mA current limited source
PS8	Short-circuit protection	22.5.3	M		When +5 V and COMMON are shorted

22.7.3.8 Mechanical characteristics

Item	Feature	Subclause	Status	Support	Value/Comment
*MC1	Use of Mechanical Interface	22.6	O		Optional
MC2	Connector reference standard	22.6.1	MC1:M		IEC 1076-3-101: 1995
MC3	Use of female connector	22.6.1	MC1:M		At MAC/RS side
MC4	Use of male connector	22.6.1	MC1:M		At PHY mating cable side
MC5	Connector shell plating	22.6.2	MC1:M		Use conductive material
MC6	Shield transfer impedance	22.6.2	MC1:M		After 500 cycles of mating/unmating, per table 22-11
MC7	Additions to provide for female shell to male shell conductivity	22.6.2	MC1:M		On shell of conductor with male contacts
MC8	Clearance dimensions	22.6.4	MC1:M		15 mm × 50 mm, per figure 22-19

23. Physical Coding Sublayer (PCS), Physical Medium Attachment (PMA) sublayer and baseband medium, type 100BASE-T4

23.1 Overview

The 100BASE-T4 PCS, PMA, and baseband medium specifications are aimed at users who want 100 Mb/s performance, but would like to retain the benefits of using voice-grade twisted-pair cable. 100BASE-T4 signaling requires four pairs of Category 3 or better cable, installed according to ISO/IEC 11801: 1995, as specified in 23.6. This type of cable, and the connectors used with it, are simple to install and reconfigure. 100BASE-T4 does not transmit a continuous signal between packets, which makes it useful in battery powered applications. The 100BASE-T4 PHY is one of the 100BASE-T family of high-speed CSMA/CD network specifications.

23.1.1 Scope

This clause defines the type 100BASE-T4 Physical Coding Sublayer (PCS), type 100BASE-T4 Physical Medium Attachment (PMA) sublayer, and type 100BASE-T4 Medium Dependent Interface (MDI). Together, the PCS and PMA layers comprise a 100BASE-T4 Physical Layer (PHY). Provided in this document are full functional, electrical, and mechanical specifications for the type 100BASE-T4 PCS, PMA, and MDI. This clause also specifies the baseband medium used with 100BASE-T4.

23.1.2 Objectives

The following are the objectives of 100BASE-T4:

a) To support the CSMA/CD MAC.
b) To support the 100BASE-T MII, Repeater, and optional Auto-Negotiation.
c) To provide 100 Mb/s data rate at the MII.
d) To provide for operating over unshielded twisted pairs of Category 3, 4, or 5 cable, installed as horizontal runs in accordance with ISO/IEC 11801: 1995, as specified in 23.6, at distances up to 100 m (328 ft).
e) To allow for a nominal network extent of 200 m, including:
   1) Unshielded twisted-pair links of 100 m.
   2) Two-repeater networks of approximately a 200 m span.
f) To provide a communication channel with a mean ternary symbol error rate, at the PMA service interface, of less than one part in 10^8.

23.1.3 Relation of 100BASE-T4 to other standards

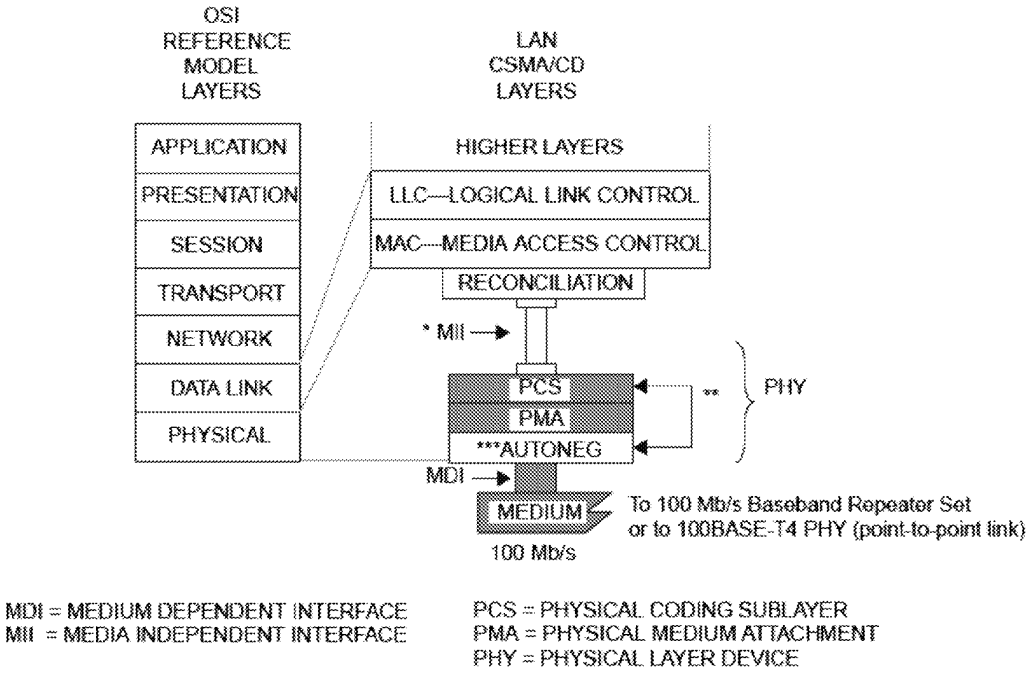
Relations between the 100BASE-T4 PHY and the ISO Open Systems Interconnection (OSI) reference model and the IEEE 802.3 CSMA/CD LAN model are shown in figure 23-1. The PHY Layers shown in figure 23-1 connect one clause 4 Media Access Control (MAC) layer to a clause 27 repeater. This clause also discusses other variations of the basic configuration shown in figure 23-1. This whole clause builds on clauses 1 through 4 of this standard.

23.1.4 Summary

The following paragraphs summarize the PCS and PMA clauses of this document.

23.1.4.1 Summary of Physical Coding Sublayer (PCS) specification

The 100BASE-T4 PCS couples a Media Independent Interface (MII), as described in clause 22, to a Physical Medium Attachment sublayer (PMA).



* MII is optional.
** AUTONEG communicates with the PMA sublayer through the PMA service interface messages PMA_LINK.request and PMA_LINK.indicate.
*** AUTONEG is optional.

Figure 23-1—Type 100BASE-T4 PHY relationship to the ISO Open Systems Interconnection (OSI) reference model and the IEEE 802.3 CSMA/CD LAN model

The PCS Transmit function accepts data nibbles from the MII. The PCS Transmit function encodes these nibbles using an 8B6T coding scheme (to be described) and passes the resulting ternary symbols to the PMA. In the reverse direction, the PMA conveys received ternary symbols to the PCS Receive function. The PCS Receive function decodes them into octets, and then passes the octets one nibble at a time up to the MII. The PCS also contains a PCS Carrier Sense function, a PCS Error Sense function, a PCS Collision Presence function, and a management interface.

Figure 23-2 shows the division of responsibilities between the PCS, PMA, and MDI layers.

Physical level communication between PHY entities takes place over four twisted pairs. This specification permits the use of Category 3, 4, or 5 unshielded twisted pairs, installed according to ISO/IEC 11801: 1995, as specified in 23.6. Figure 23-3 shows how the PHY manages the four twisted pairs at its disposal.

The 100BASE-T4 transmission algorithm always leaves one pair open for detecting carrier from the far end (see figure 23-3). Leaving one pair open for carrier detection in each direction greatly simplifies media access control. All collision detection functions are accomplished using only the unidirectional pairs TX_D1 and RX_D2, in a manner similar to 10BASE-T. This collision detection strategy leaves three pairs in each direction free for data transmission, which uses an 8B6T block code, schematically represented in figure 23-4.

8B6T coding, as used with 100BASE-T4 signaling, maps data octets into ternary symbols. Each octet is mapped to a pattern of 6 ternary symbols, called a 6T code group. The 6T code groups are fanned out to three independent serial channels. The effective data rate carried on each pair is one third of 100 Mb/s,

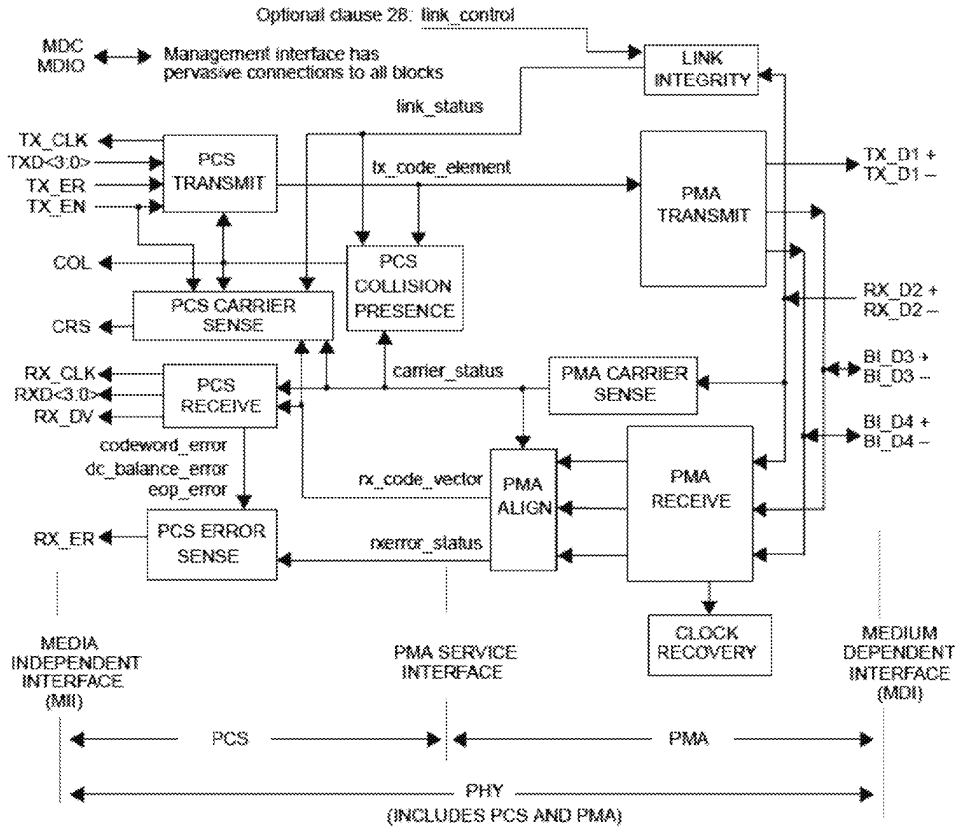


Figure 23-2—Division of responsibilities between 100BASE-T4 PCS and PMA

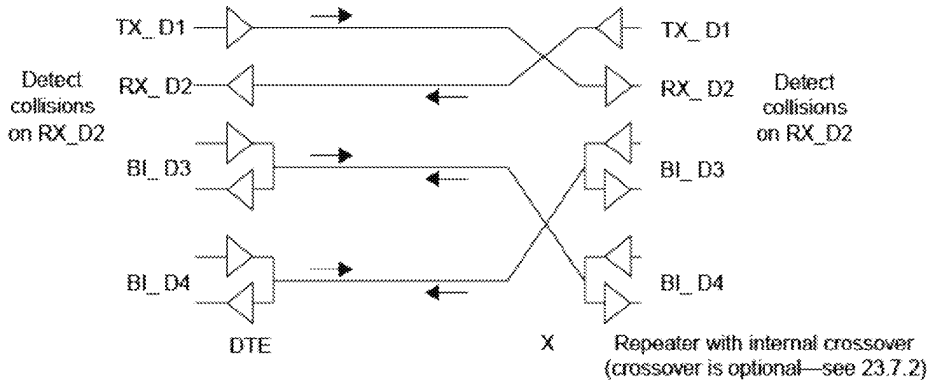


Figure 23-3—Use of wire pairs

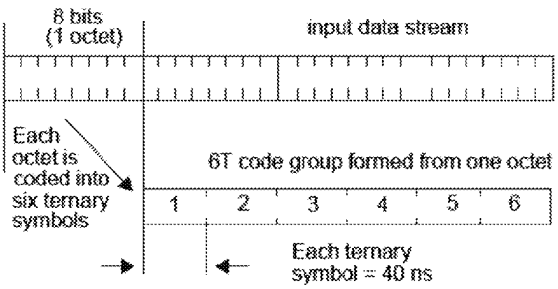


Figure 23-4—8B6T coding

which is 33.333... Mb/s. The ternary symbol transmission rate on each pair is 6/8 times 33.33 Mb/s, or precisely 25.000 MHz.

Refer to annex 23A for a complete listing of 8B6T code words.

The PCS functions and state diagrams are specified in 23.2. The PCS electrical interface to the MII conforms to the interface requirements of clause 21. The PCS interface to the PMA is an abstract message-passing interface specified in 23.3.

23.1.4.2 Summary of physical medium attachment (PMA) specification

The PMA couples messages from the PMA service interface onto the twisted-pair physical medium. The PMA provides communications, at 100 Mb/s, over four pairs of twisted-pair wiring up to 100 m in length.

The PMA Transmit function, shown in figure 23-2, comprises three independent ternary data transmitters. Upon receipt of a PMA_UNITDATA request message, the PMA synthesizes one ternary symbol on each of the three output channels (TX_D1, BI_D3, and BI_D4). Each output driver has a *ternary* output, meaning that the output waveform can assume any of three values, corresponding to the transmission of ternary symbols CS0, CS1 or CS-1 (see 23.4.3.1) on each of the twisted pairs.

The PMA Receive function comprises three independent ternary data receivers. The receivers are responsible for acquiring clock, decoding the Start of Stream Delimiter (SSD) on each channel, and providing data to the PCS in the synchronous fashion defined by the PMA_UNITDATA.indicate message. The PMA also contains functions for PMA Carrier Sense and Link Integrity.

PMA functions and state diagrams appear in 23.4. PMA electrical specifications appear in 23.5.

23.1.5 Application of 100BASE-T4

23.1.5.1 Compatibility considerations

All implementations of the twisted-pair link shall be compatible at the MDI. The PCS, PMA, and the medium are defined to provide compatibility among devices designed by different manufacturers. Designers are free to implement circuitry within the PCS and PMA (in an application-dependent manner) provided the MDI (and MII, when implemented) specifications are met.

23.1.5.2 Incorporating the 100BASE-T4 PHY into a DTE

The PCS is required when used with a DTE. The PCS provides functions necessary to the overall system operation (such as 8B6T coding) and cannot be omitted. Refer to figure 23-1.

When the PHY is incorporated within the physical bounds of a DTE, conformance to the MII interface is optional, provided that the observable behavior of the resulting system is identical to a system with a full MII implementation. For example, an integrated PHY may incorporate an interface between PCS and MAC that is logically equivalent to the MII, but does not have the full output current drive capability called for in the MII specification.

23.1.5.3 Use of 100BASE-T4 PHY for point-to-point communication

The 100BASE-T4 PHY, in conjunction with the MAC specified in clauses 1-4 (including parameterized values in 4.4.2.3 to support 100 Mb/s operation), may be used at both ends of a link for point-to-point applications between two DTEs. Such a configuration does not require a repeater. In this case each PHY may connect through an MII to its respective DTE. Optionally, either PHY (or both PHYs) may be incorporated into the DTEs without an exposed MII.

23.1.5.4 Support for Auto-Negotiation

The PMA service interface contains primitives used by the Auto-Negotiation algorithm (clause 28) to automatically select operating modes when connected to a like device.

23.2 PCS functional specifications

The 100BASE-T4 PCS couples a Media Independent Interface (MII), as described in clause 22, to a 100BASE-T4 Physical Medium Attachment sublayer (PMA).

At its interface with the MII, the PCS communicates via the electrical signals defined in clause 22.

The interface between PCS and the next lower level (PMA) is an abstract message-passing interface described in 23.3. The physical realization of this interface is left to the implementor, provided the requirements of this standard, where applicable, are met.

23.2.1 PCS functions

The PCS comprises one PCS Reset function and five simultaneous and asynchronous operating functions. The PCS operating functions are PCS Transmit, PCS Receive, PCS Error Sense, PCS Carrier Sense, and PCS Collision Presence. All operating functions start immediately after the successful completion of the PCS Reset function.

The PCS reference diagram, figure 23-5, shows how the five operating functions relate to the messages of the PCS-PMA interface. Connections from the management interface (signals MDC and MDIO) to other layers are pervasive, and are not shown in figure 23-5. The management functions are specified in clause 30. See also figure 23-6, which defines the structure of frames passed from PCS to PMA. See also figure 23-7, which presents a reference model helpful for understanding the definitions of PCS Transmit function state variables ohr1-4 and tsr.

23.2.1.1 PCS Reset function

The PCS Reset function shall be executed any time either of two conditions occur. These two conditions are "power on" and the receipt of a reset request from the management entity. The PCS Reset function initializes all PCS functions. The PCS Reset function sets pcs_reset ″ ON for the duration of its reset function. All state diagrams take the open-ended pcs_reset branch upon execution of the PCS Reset function. The reference diagrams do not explicitly show the PCS Reset function.

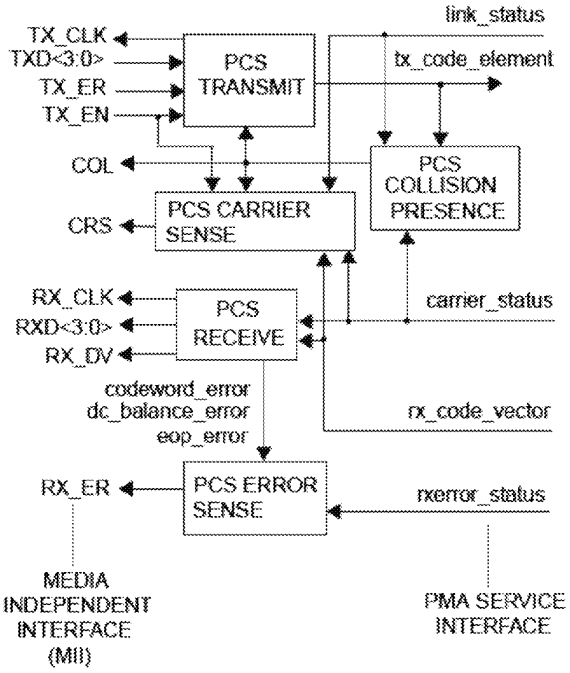


Figure 23-5—PCS reference diagram

23.2.1.2 PCS Transmit function

The PCS Transmit function shall conform to the PCS Transmit state diagram in figure 23-8.

The PCS Transmit function receives nibbles from the TXD signals of the MII, assembles pairs of nibbles to form octets, converts the octets into 6T code groups according to the 8B6T code table, and passes the resulting ternary data to the PMA using the PMA_UNITDATA request message. The state diagram of figure 23-8 depicts the PCS Transmit function operation. Definitions of state variables tsr, ohr, sosa, sosb, eop1-5, and tx_extend used in that diagram, as well as in the following text, appear in 23.2.4.1. The physical structure represented in figure 23-7 is not required; it merely serves to explain the meaning of the state diagram variables ohr and tsr in figure 23-8. Implementors are free to construct any logical devices having functionality identical to that described by this functional description and the PCS Transmit state diagram, figure 23-8.

PCS Transmit makes use of the tsr and ohr shift registers to manage nibble assembly and ternary symbol transmission. Nibbles from the MII go into tsr, which PCS Transmit reads as octets. PCS Transmit then encodes those octets and writes 6T code groups to the ohr registers. The PMA_UNITDATA.request message passes ternary symbols from the ohr registers to the PMA. In each state diagram block, the ohr loading operations are conducted first, then tx_code_vector is loaded and the state diagram waits 40 ns.

The first 5 octets assembled by the PCS Transmit function are encoded into the sosa code word and the next 3 octets assembled are encoded into the sosb code word. This guarantees that every packet begins with a valid preamble pattern. This is accomplished by the definition of tsr. In addition, the PCS Transmit state diagram also specifies that at the start of a packet all three output holding registers ohr1, ohr3 and ohr4 will be loaded with the same value (sosa). This produces the ternary symbols labeled P3 and P4 in figure 23-6.

At the conclusion of the MAC frame, the PCS Transmit function appends eop1-5. This is accomplished by defining a variable tx_extend to stretch the TX_EN signal, and defining tsr during this time to be a sequence of constants that decodes to the proper eop code groups.

The encoding operation shall use the 8B6T code table listed in annex 23A, and the dc balance encoding rules listed below. Encoding is performed separately for each transmit pair.

23.2.1.2.1 DC balance encoding rules

The encoding operation maintains dc balance on each transmit pair by keeping track of the cumulative weight of all 6T code groups (see *weight of 6T code group*, annex 21A) transmitted on that pair. For each pair, it initiates the cumulative weight to 0 when the PCS Transmit function is in the AWAITING DATA TO TRANSMIT state. All 6T code groups in the code table have weight 0 or 1. The dc balance algorithm conditionally negates transmitted 6T code groups, so that the code weights transmitted on the line include 0, +1, and –1. This dc balance algorithm ensures that the cumulative weight on each pair at the conclusion of each 6T code group is always either 0 or 1, so only one bit per pair is needed to store the cumulative weight. As used below, the phrase "invert the cumulative weight bit" means "if the cumulative weight bit is zero then set it to one, otherwise set it to zero."

After encoding any octet, except the constants sosa, sosb, eop1-5 or bad_code, update the cumulative weight bit for the affected pair according to rules a) through c):

a) If the 6T code group weight is 0, do not change the cumulative weight.
b) If the 6T code group weight is 1, and the cumulative weight bit is 0, set the cumulative weight bit to 1.
c) If the 6T code group weight is 1, and the cumulative weight bit is also 1, set the cumulative weight bit to 0, and then algebraically negate all the ternary symbol values in the 6T code group.

After encoding any of the constants sosa, sosb, or bad_code, update the cumulative weight bit for the affected pair according to rule d):

d) Do not change the cumulative weight. Never negate sosa, sosb or bad_code.

After encoding any of the constants eop1-5, update the cumulative weight bit for the affected pair according to rules e) and f):

e) If the cumulative weight is 0, do not change the cumulative weight; algebraically negate all the ternary symbol values in eop1-5.
f) If the cumulative weight is 1, do not change the cumulative weight.

NOTE—The inversion rules for eop1-5 are opposite rule b). That makes eop1-5 look very unlike normal data, increasing the number of errors required to synthesize a false end-of-packet marker.

23.2.1.3 PCS Receive function

The PCS Receive function shall conform to the PCS Receive state diagram in figure 23-9.

The PCS Receive function accepts ternary symbols from the PMA, communicated via the PMA_UNITDATA.indicate message, converts them using 8B6T coding into a nibble-wide format and passes them up to the MII. This function also generates RX_DV. The state diagram of figure 23-9 depicts the PCS Receive function. Definitions of state variables ih2, ih3, and ih4 used in that diagram, as well as in the following text, appear in 23.2.4.1.

The last 6 values of the rx_code_vector are available to the decoder. PCS Receive makes use of these stored rx_code_vector values as well as the ih2-4 registers to manage the assembly of ternary symbols into 6T code

groups, and the conversion of decoded data octets into nibbles. The last 6 ternary symbols for pair BI_D3 (as extracted from the last 6 values of rx_code_vector) are referred to in the state diagram as BI_D3[0:5]. Other pairs are referenced accordingly.

The PCS Receive state diagram starts the first time the PCS receives a PMA_UNITDATA.indicate message with rx_code_vector=DATA (as opposed to IDLE or PREAMBLE). The contents of this first PMA_UNITDATA.indicate (DATA) message are specified in 23.4.1.6.

After the sixth PMA_UNITDATA.indicate (DATA) message (state DECODE CHANNEL 3), there is enough information to decode the first data octet. The decoded data is transmitted across the MII in two parts, a least significant nibble followed by a most significant nibble (see clause 22).

During state COLLECT 4TH TERNARY SYMBOL the PCS Receive function raises RX_DV and begins shifting out the nibbles of the 802.3 MAC SFD, least significant nibble first (SFD:LO). The most significant nibble of the 802.3 MAC SFD, called SFD:HI, is sent across the MII during the next state, COLLECT 5TH TERNARY SYMBOL.

Once eop is signaled by the decode operation, the state diagram de-asserts RX_DV, preventing the end-of-packet bits from reaching the MII. At any time that RX_DV is de-asserted, RXD<3:0> shall be all zeroes.

The decode operation shall use the 8B6T code table listed in annex 23A, and the error-detecting rules listed in 23.2.1.3.1. Decoding and maintenance of the cumulative weight bit is performed separately for each receive pair.

23.2.1.3.1 Error-detecting rules

The decoding operation checks the dc balance on each receive pair by keeping track of the cumulative weight of all 6T code group received on that pair. For each pair, initialize the cumulative weight to 0 when the PCS Receive function is in the AWAITING INPUT state. As in the encoding operation, only one bit per pair is needed to store the cumulative weight.

Before decoding each octet, check the weight of the incoming code group and then apply rules a) through h) in sequence:

a) If the received code group is eop1 (or its negation), set eop=ON. Then check the other pairs for conformance to the end-of-packet rules as follows: Check the last four ternary symbols of the next pair, and the last two ternary symbols from the third pair for exact conformance with the end-of-packet pattern specified by PCS Transmit, including the cumulative weight negation rules. If the received data does not conform, set the internal variable eop_error=ON. Skip the other rules.
b) If the received code group weight is greater than 1 or less than –1, set the internal variable dc_balance_error=ON. Decode to all zeros. Do not change the cumulative weight.
c) If the received code group weight is zero, use the code table to decode. Do not change the cumulative weight.
d) If the received code group weight is +1, and the cumulative weight bit is 0, use the code table to decode. Invert the cumulative weight bit.
e) If the received code group weight is –1, and the cumulative weight bit is 1, algebraically negate each ternary symbol in the code group and then use the code table to decode. Invert the cumulative weight bit.
f) If the received code group weight is +1 and the cumulative weight bit is 1, set the internal variable dc_balance_error=ON. Decode to all zeros. Do not change the cumulative weight.
g) If the received code group weight is –1 and the cumulative weight bit is 0, set the internal variable dc_balance_error=ON. Decode to all zeros. Do not change the cumulative weight.
h) If the (possibly negated) code group is not found in the code table, set codeword_error =ON. Decode to all zeros. Do not change the cumulative weight.

The variables dc_balance_error, eop_error and codeword_error shall remain OFF at all times other than those specified in the above error-detecting rules.

The codeword_error=ON indication for a (possibly negated) code group not found in the code table shall set RX_ER during the transfer of both affected data nibbles across the MII.

The dc_balance_error=ON indication for a code group shall set RX_ER during the transfer of both affected data nibbles across the MII.

The eop_error=ON indication shall set RX_ER during the transfer of the last decoded data nibble of the previous octet across the MII. That is at least one RX_CLK period earlier than the requirement for codeword_error and dc_balance_error.

These timing requirements imply consideration of implementation delays not specified in the PCS Receive state diagram.

RX_DV is asserted coincident with the transmission across the MII of valid packet data, including the clause 4 MAC SFD, but not including the 100BASE-T4 end-of-packet delimiters eop1-5. When a packet is truncated due to early de-assertion of carrier_status, an RX_ER indication shall be generated and RX_DV shall be de-asserted, halting receive processing. The PCS Receive Function may use any of the existing signals codeword_error, dc_balance_error, or eop_error to accomplish this function.

23.2.1.4 PCS Error Sense function

The PCS Error Sense function performs the task of sending RX_ER to the MII whenever rxerror_status=ERROR is received from the PMA sublayer or when any of the PCS decoding error conditions occur. The PCS Error Sense function shall conform to the PCS Error Sense state diagram in figure 23-10.

Upon detection of any error, the error sense process shall report RX_ER to the MII before the last nibble of the clause 4 MAC frame has been passed across the MII. Errors attributable to a particular octet are reported to the MII coincident with the octet in which they occurred.

The timing of rxerror_status shall cause RX_ER to appear on the MII no later than the last nibble of the first data octet in the frame.

23.2.1.5 PCS Carrier Sense function

The PCS Carrier Sense function shall perform the function of controlling the MII signal CRS according to the rules presented in this clause.

While link_status = OK, CRS is asserted whenever rx_crs=ON or TX_EN=1, with timing as specified in 23.11.2, and table 23-6.

23.2.1.6 PCS Collision Presence function

A PCS collision is defined as the simultaneous occurrence of tx_code_vector↑IDLE and the assertion of carrier_status=ON while link_status=OK. While a PCS collision is detected, the MII signal COL shall be asserted, with timing as specified in 23.11.2 and table 23-6.

At other times COL shall remain de-asserted.

23.2.2 PCS interfaces

23.2.2.1 PCS–MII interface signals

The following signals are formally defined in 22.2.2. Jabber detection as specified in 22.2.4.2.12 is not required by this standard.

Table 23-1—MII interface signals

Signal name	Meaning
TX_CLK	Transmit Clock
TXD<3:0>	Transmit Data
TX_ER	Forces transmission of illegal code
TX_EN	Frames Transmit Data
COL	Collision Indication
CRS	Non-Idle Medium Indication
RX_CLK	Receive Clock
RXD<3:0>	Receive Data
RX_DV	Frames Receive SFD and DATA
RX_ER	Receive Error Indication
MDC	Management Data Clock
MDIO	Management Data

23.2.2.2 PCS–Management entity signals

The management interface has pervasive connections to all functions. Operation of the management control lines MDC and MDIO, and requirements for managed objects inside the PCS and PMA, are specified in clauses 22 and 30, respectively.

The loopback mode of operation shall be implemented in accordance with 22.2.4.1.2. The loopback mode of operation loops back transmit data to receive data, thus providing a way to check for the presence of a PHY.

No spurious signals shall be emitted onto the MDI when the PHY is held in power-down mode as defined in 22.2.4.1.5 (even if TX_EN is ON) or when released from power-down mode, or when external power is first applied to the PHY.

23.2.3 Frame structure

Frames passed from the PCS sublayer to the PMA sublayer shall have the structure shown in figure 23-6. This figure shows how ternary symbols on the various pairs are synchronized as they are passed by the PMA_UNITDATA.indicate and PMA_UNITDATA request messages. Time proceeds from left to right in the figure.

In the frame structure example, the last 6T code group, DATA N, happens to appear on transmit pair BI_D3. It could have appeared on any of the three transmit pairs, with the five words eop1 through eop5 appended afterward as the next five octets in sequence. The end of packet as recognized by the PCS is defined as the end of the last ternary symbol of cop1. At this point a receiver has gathered enough information to locate the last word in the packet and check the dc balance on each pair.

If the PMA service interface is exposed, data carried between PCS and PMA by the PMA_UNITDATA.indicate and PMA_UNITDATA request messages shall have a clock in each direction. Details of the clock

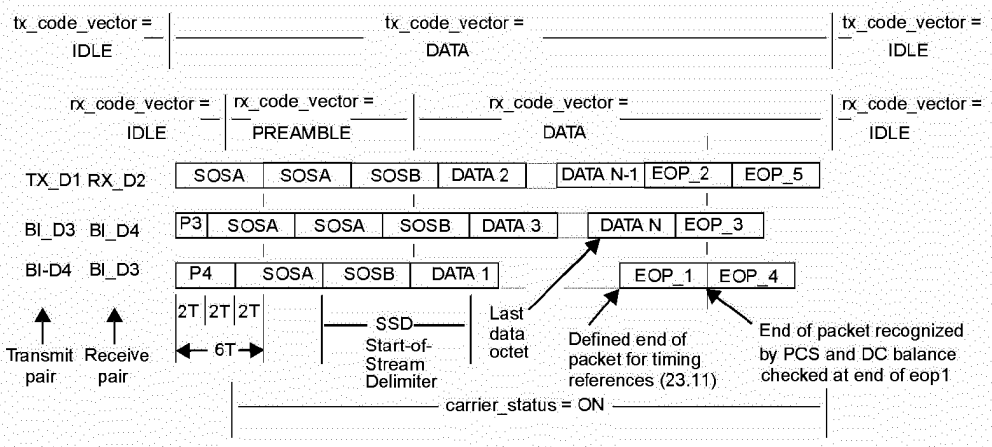


Figure 23-6—PCS sublayer to PMA sublayer frame structure

implementation are left to the implementor. The choice of binary encoding for each ternary symbol is left to the implementor.

The following frame elements appear in figure 23-6 (ternary symbols are transmitted leftmost first):

SOSA	The succession of six ternary symbols: `[ 1 -1 1 -1 1 -1]`, which is the result of encoding the constant sosa.
SOSB	The succession of six ternary symbols: `[ 1 -1 1 -1 -1 1]`, which is the result of encoding the constant sosb.
P3	The succession of two ternary symbols: `[ 1 -1]`.
P4	The succession of four ternary symbols: `[ 1 -1 1 -1]`.
DATA	A 6T code group that is the result of encoding a data octet in a packet that is not part of the clause 4 MAC prcamblc or SFD.
EOP1-5	A 6T code group that is the result of encoding one of the end-of-packet patterns eop1-5.

23.2.4 PCS state diagrams

The notation used in the state diagrams follows the conventions of 21.5. Transitions shown without source states are evaluated continuously and take immediate precedence over all other conditions.

23.2.4.1 PCS state diagram constants

Register tsr may take on any of the nine constant values listed below (sosa through eop5, bad_code, and zero_code). These values are used to describe the functional operation of the coding process.

NOTE—Implementors are under no obligation to implement these constants in any particular way. For example, some implementors may choose to implement these codes as special flag bits attached to MII TXD nibble registers. Other implementors may choose to implement insertion of these codes on the downstream side of the coder function, using precoded 6T sequences.

All 6T code words are sent leftmost ternary symbol first.

sosa	A constant that encodes to:	[1 -1 1 -1 1 -1].
sosb	A constant that encodes to:	[1 -1 1 -1 -1 1].
eop1	A constant that encodes to:	[1 1 1 1 1 1].
eop2	A constant that encodes to:	[1 1 1 1 -1 -1].
eop3	A constant that encodes to:	[1 1 -1 -1 0 0].
eop4	A constant that encodes to:	[-1 -1 -1 -1 -1 -1].
eop5	A constant that encodes to:	[-1 -1 0 0 0 0].
bad_code	A constant that encodes to:	[-1 -1 -1 1 1 1].
zero_code	A constant that encodes to:	[0 0 0 0 0 0].

23.2.4.2 PCS state diagram variables

codeword_error

Indicates reception of invalid 6T code group.

Values: ON and OFF

Set by: PCS Receive; error-detecting rules

dc_balance_error

Indicates reception of dc coding violation.

Values: ON and OFF

Set by: PCS Receive; error-detecting rules

eop

Indicates reception of eop1.

A state variable set by the decoding operation. Reset to OFF when in PCS Receive state AWAITING INPUT. When the decoder detects eop1 on any pair, it sets this flag ON. The timing of eop shall be adjusted such that the last nibble of the last decoded data octet in a packet is the last nibble sent across the MII by the PMA Receive state diagram with RX_DV set ON.

Values: ON and OFF

Set by: PCS Receive; error-detecting rules

eop_error

Indicates reception of data with improper end-of-packet coding.

Values: ON and OFF

Set by: PCS Receive; error-detecting rules

ih2, ih4, and ih3 (input holding registers)

A set of holding registers used for the purpose of holding decoded data octets in preparation for sending across the MII one nibble at a time. One register is provided for each of the three receive pairs RX_D2, BI_D4, and BI_D3, respectively.

Value: octet

Set by: PCS Receive

Each time the PCS Receive function decodes a 6T code group, it loads the result (an octet) into one of the ih2-4 registers. These three registers are loaded in round-robin fashion, one register being loaded every two ternary symbol times.

The PCS Receive state diagram reads nibbles as needed from the ih2-4 registers and stuffs them into RXD.

ohr1, ohr3, and ohr4 (output holding registers)

(See figure 23-7.) A set of shift registers used for the purpose of transferring coded 6T ternary symbol groups one ternary symbol at a time into the PMA. One register is provided for each of the three transmit pairs TX_D1, BI_D3, and BI_D4, respectively.

Value: 6T code group. Each of the six cells holds one ternary symbol (i.e., –1, 0, or 1).

Set by: PCS Transmit

Each time the PCS Transmit function encodes a data octet, it loads the result (a 6T code group) into one of the ohr registers. Three registers are loaded in round-robin fashion, one register being loaded every two ternary symbol times. The PCS shall transmit octets on the three transmit pairs in round-robin fashion, in the order TX_D1, BI_D3, and BI_D4, starting with TX_D1.

The PMA_UNITDATA request (DATA) message picks the least significant (rightmost) ternary symbol from each ohr register and sends it to the PMA, as shown below. (Note that 6T code words in annex 23A are listed with lsb on the left, not the right.)

tx_code_vector[TX_D1] = the LSB of ohr1, also called ohr1[0]

tx_code_vector[BI_D3] = the LSB of ohr3, also called ohr3[0]

tx_code_vector[BI_D4] = the LSB of ohr4, also called ohr4[0]

After each PMA_UNITDATA request message, all three ohr registers shift right by one ternary symbol, shifting in zero from the left. The PCS Transmit function loads a new 6T code group into each ohr immediately after the last ternary symbol of the previous group is shifted out.

At the beginning of a preamble, the PCS Transmit function loads the same value (sosa) into all three output holding registers, which causes alternating transitions to immediately appear on all three output pairs. The result on pairs BI_D3 and BI_D4 is depicted by code words P3 and P4 in figure 23-6.

pcs_reset

Causes reset of all PCS functions when ON.

Values: ON and OFF

Set by: PCS Reset

rx_crs

A latched asynchronous variable. Timing for the MII signal CRS is derived from rx_crs.

Values:	ON and OFF
Set ON when:	carrier_status changes to ON
Set OFF when	either of two events occurs: carrier_status changes to OFF, or detection of eop1, properly framed, on any of the lines RX_D2, BI_D4, or BI_D3

Additionally, if, 20 ternary symbol times after rx_crs falls, carrier_status remains set to ON then set rx_crs=ON.

NOTE—A special circuit for the detection of eop1 and subsequent de-assertion of rx_crs, faster than the full 8B6T decoding circuits, is generally required to meet the timing requirements for CRS listed in clause 23.11.

tsr (transmit shift register)

(See figure 23-7.) A shift register defined for the purpose of assembling nibbles from the MII TXD into octets.

Values:	The variable tsr always contains both the current nibble of TXD and the previous nibble of TXD. Valid values for tsr therefore include all octets. Register tsr may also take on any of the nine constant values listed in 23.2.4.1.
Nibble order:	When encoding the tsr octet, the previous TXD nibble is considered the least significant nibble.
Set by:	PCS Transmit

During the first 16 TX_CLK cycles after TX_EN is asserted, tsr shall assume the following values in sequence regardless of TXD: sosa, sosa, sosa, sosa, sosa, sosa, sosa, sosa, sosa, sosa, sosb, sosb, sosb, sosb, sosb, sosb. This action substitutes the 100BASE-T4 preamble for the clause 4 MAC preamble. The PCS Transmit state diagram samples the tsr only every other clock, which reduces the number of sosa and sosb constants actually coded to 5 and 3, respectively.

During the first 10 TX_CLK cycles after TX_EN is de-asserted, tsr shall assume the following values in sequence, regardless of TXD: eop1, eop1, eop2, eop2, eop3, eop3, eop4, eop4, eop5, eop5. This action appends the 100BASE-T4 end-of-packet delimiter to each pair. The PCS Transmit state diagram samples the tsr only every other clock, which reduces the number of eop1-5 constants actually coded to 1 each.

Except for the first 16 TX_CLK cycles after TX_EN is asserted, any time TX_ER and TX_EN are asserted, tsr shall assume the value bad_code with such timing as to cause both nibbles of the affected octet to be encoded as bad_code. If TX_ER is asserted at any time during the first 16 TX_CLK cycles after TX_EN is asserted, tsr shall during the 17th and 18th clock cycles assume the value bad_code.

If TX_EN is de-asserted on an odd nibble boundary, the PCS shall extend TX_EN by one TX_CLK cycle, and behave as if TX_ER were asserted during that additional cycle.

Except for the first 10 TX_CLK cycles after TX_EN is de-asserted, any time TX_EN is not asserted, tsr shall assume the value zero_code.

tx_extend

A latched, asynchronous state variable used to extend the TX_EN signal long enough to ensure complete transmission of all nonzero ternary symbols in eop1-5.

Values: ON and OFF

Set ON upon: rising edge of TX_EN

Set OFF upon: either of two conditions:
a) In the event of a collision (COL is asserted at any time during transmission) set tx_extend=OFF when TX_EN de-asserts.
b) In the event of no collision (COL remains de-asserted throughout transmission) set tx_extend=OFF upon completion of transmission of last ternary symbol in eop4.

NOTES

1—The 6T code group eop5 has four zeroes at the end. The 6T code group eop4 contains the last nonzero ternary symbol to be transmitted.

2—The effect of a collision, if present, is to truncate the frame at the original boundary determined by TX_EN. Noncolliding frames are extended, while colliding frames are not.

23.2.4.3 PCS state diagram timer

tw1_timer

A continuous free-running timer.

Values: The condition tw1_timer_done goes true when the timer expires.

Restart when: Immediately after expiration (restarting the timer resets condition tw1_timer_done).

Duration: 40 ns nominal.

TX_CLK shall be generated synchronous to tw1_timer (see tolerance required for TX_CLK in 23.5.1.2.10).

On every occurrence of tw1_timer_done, the state diagram advances by one block. The message PMA_UNITDATA request is issued concurrent with tw1_timer_done.

23.2.4.4 PCS state diagram functions

encode()

The encode operation of 23.2.1.2.

Argument: octet

Returns: 6T code group

decode()

The decode operation of 23.2.1.3.

Argument: 6T code group

Returns: octet

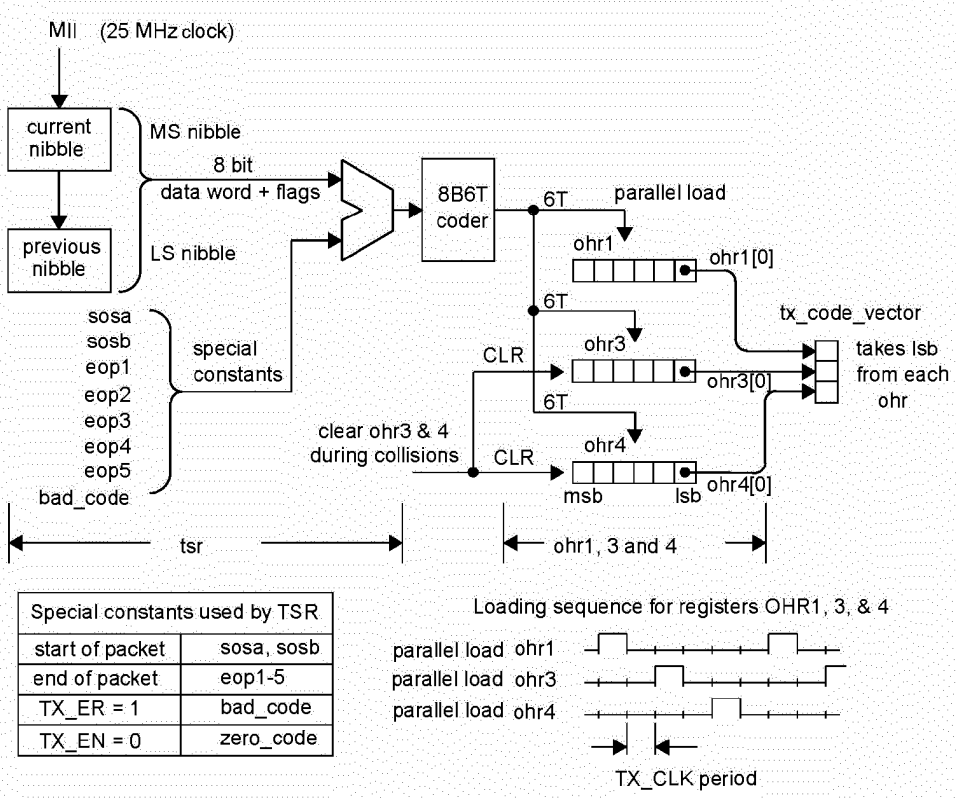


Figure 23-7—PCS Transmit reference diagram

23.2.4.5 PCS state diagrams

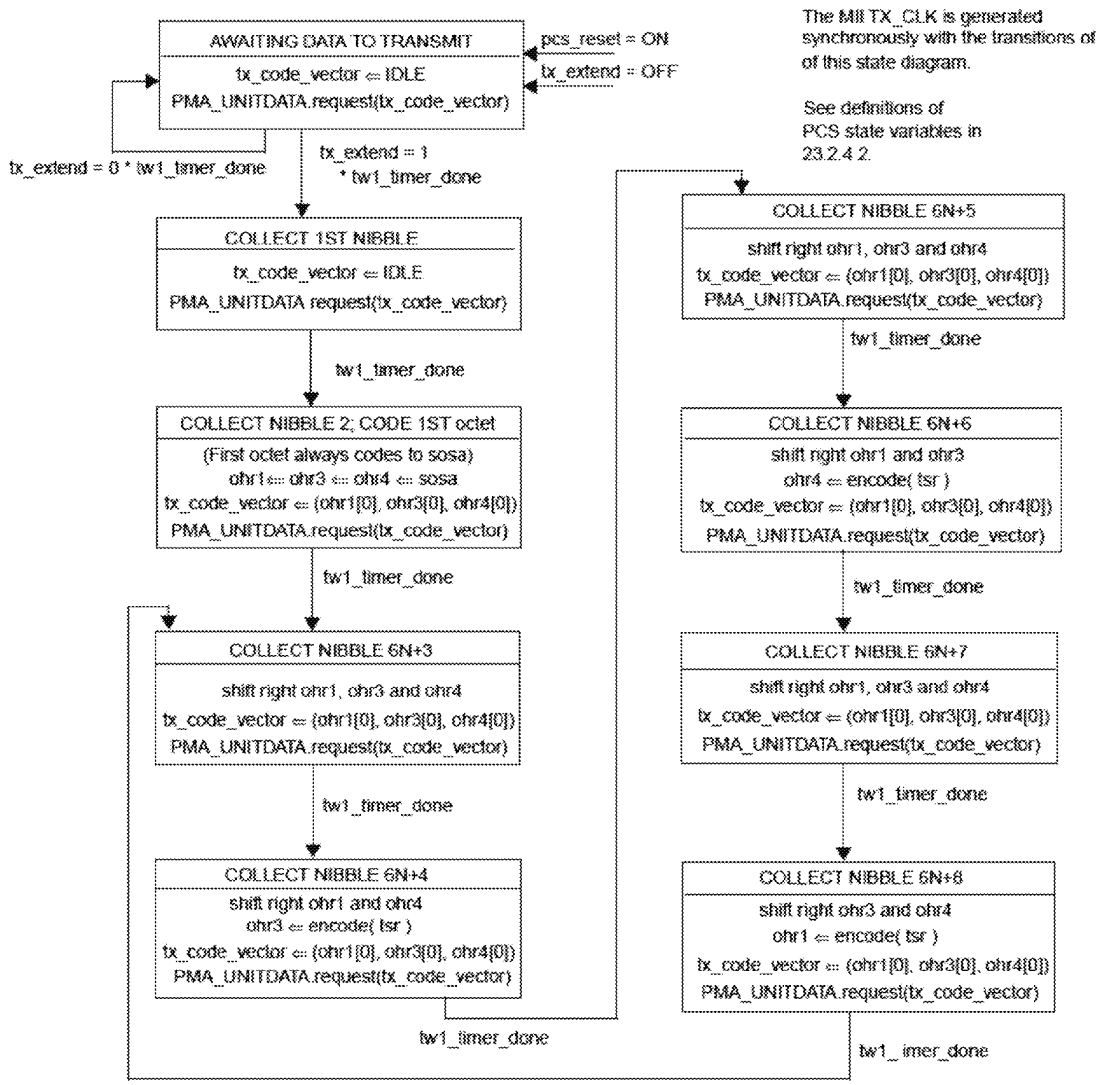


Figure 23-8—PCS Transmit state diagram

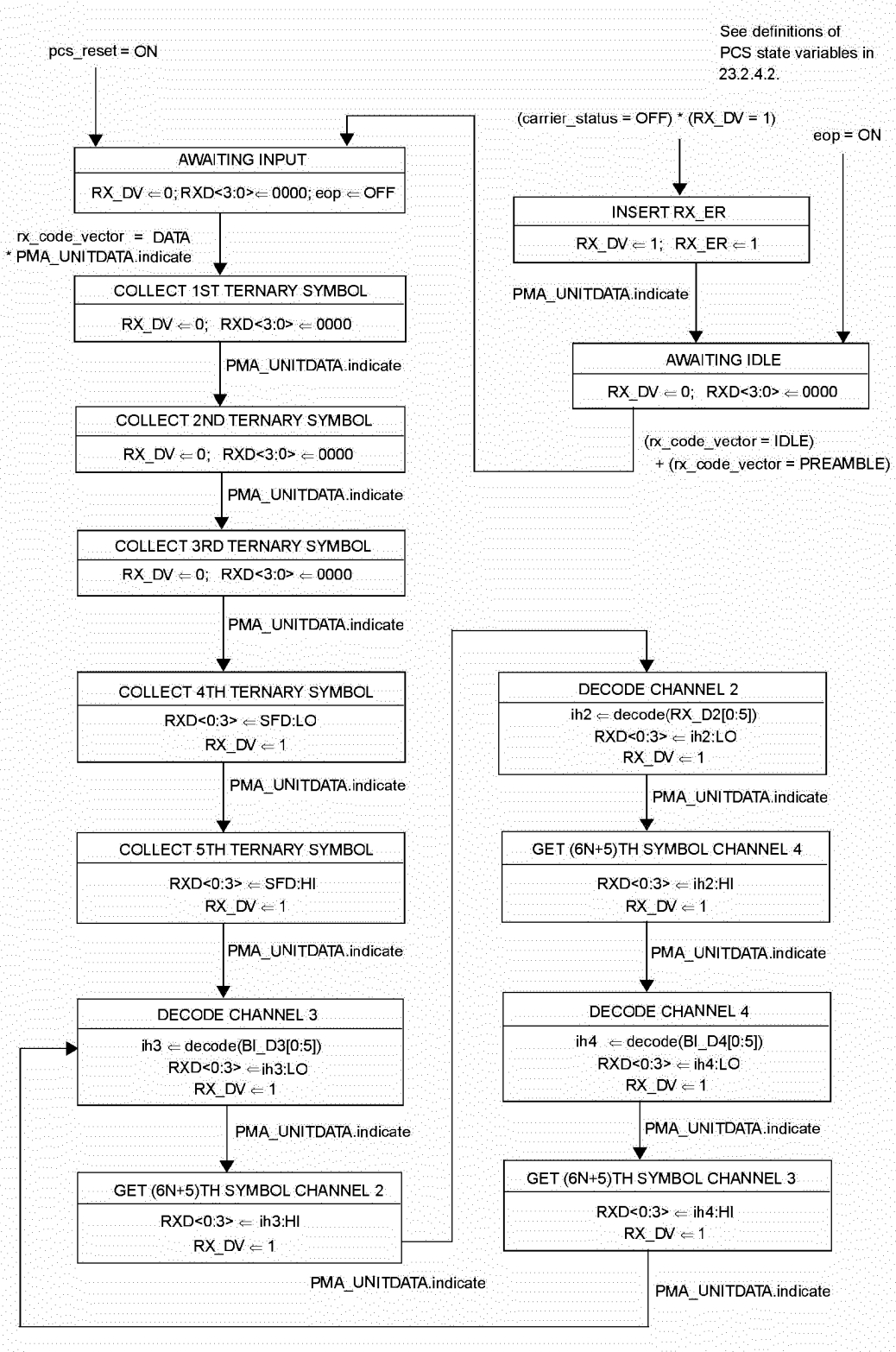


Figure 23-9—PCS Receive state diagram

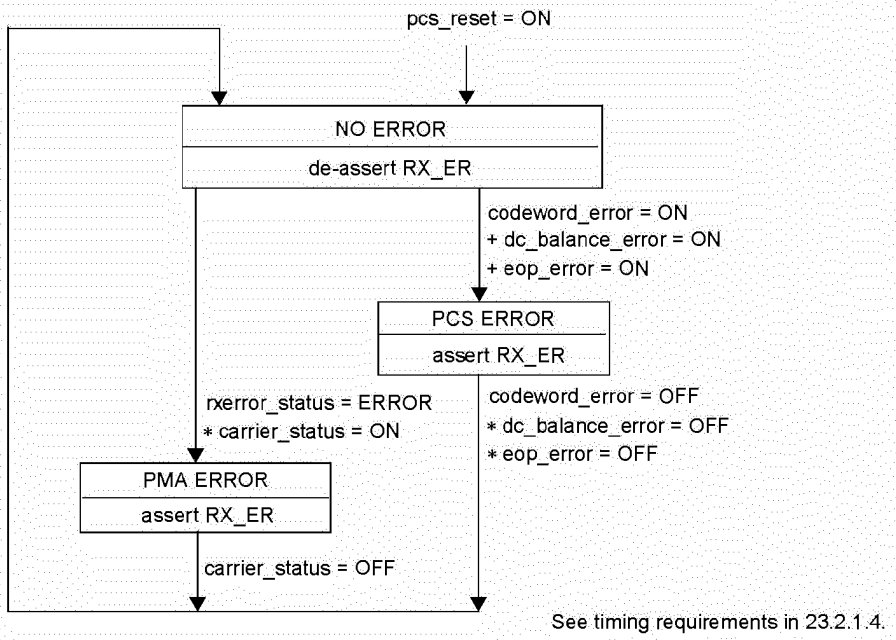


Figure 23-10—PCS Error Sense state diagram

23.2.5 PCS electrical specifications

The interface between PCS and PMA is an abstract message-passing interface, having no specified electrical properties.

Electrical characteristics of the signals passing between the PCS and MII may be found in clause 22.

23.3 PMA service interface

This clause specifies the services provided by the PMA to either the PCS or a Repeater client. These services are described in an abstract manner and do not imply any particular implementation.

The PMA Service Interface supports the exchange of code vectors between the PMA and its client (either the PCS or a Repeater). The PMA also generates status indications for use by the client.

The following primitives are defined:

PMA_TYPE.indicate
PMA_UNITDATA.request
PMA_UNITDATA.indicate
PMA_CARRIER.indicate
PMA_LINK.indicate
PMA_LINK request
PMA_RXERROR.indicate

23.3.1 PMA_TYPE.indicate

This primitive is generated by the PMA to indicate the nature of the PMA instantiation. The purpose of this primitive is to allow clients to support connections to the various types of 100BASE-T PMA entities in a generalized manner.

23.3.1.1 Semantics of the service primitive

PMA_TYPE.indicate (pma_type)

The pma_type parameter for use with the 100BASE-T4 PMA is T4.

23.3.1.2 When generated

The PMA shall continuously generate this primitive to indicate the value of pma_type.

23.3.1.3 Effect of receipt

The client uses the value of pma_type to define the semantics of the PMA_UNITDATA.request and PMA_UNITDATA.indicate primitives.

23.3.2 PMA_UNITDATA.request

This primitive defines the transfer of data (in the form of tx_code_vector parameters) from the PCS or repeater to the PMA.

23.3.2.1 Semantics of the service primitive

PMA_UNITDATA.request (tx_code_vector)

When transmitting data using 100BASE-T4 signaling, the PMA_UNITDATA.request conveys to the PMA simultaneously the logical output value for each of the three transmit pairs TX_D1, BI_D3, and BI_D4. The value of tx_code_vector during data transmission is therefore a three-element vector, with one element corresponding to each output pair. Each of the three elements of the tx_code_vector may take on one of three logical values: 1, 0, or –1, corresponding to the three ternary possibilities +, 0, and - listed for each ternary symbol in the 8B6T code table (see annex 23A).

Between packets, the 100BASE-T4 PMA layer sends the 100BASE-T4 idle signal, TP_IDL_100. The PCS informs the PMA layer that it is between packets, thus enabling the PMA idle signal, by setting the tx_code_vector parameter to IDLE.

For pma_type 100BASE-T4, the tx_code_vector parameter can take on either of two forms:

IDLE	A single value indicating to the PMA that there is no data to convey. The PMA generates link integrity pulses during the time that tx_code_vector = IDLE.
DATA	A vector of three ternary symbols, one for each of the three transmit pairs TX_D1, BI_D3, and BI_D4. The ternary symbol for each pair may take on one of three values, 1, 0, or –1.

The ternary symbols comprising tx_code_vector, when they are conveyed using the DATA format, are called, according to the pair on which each will be transmitted, tx_code_vector[BI_D4], tx_code_vector[TX_D1], and tx_code_vector[BI_D3].

23.3.2.2 When generated

The PCS or Repeater client generates PMA_UNITDATA.request synchronous with every MII TX_CLK.

For the purposes of state diagram descriptions, it may be assumed that at the time PMA_UNITDATA request is generated, the MII signals TX_EN, and TX_ER, and TXD instantly become valid and that they retain their values until the next PMA_UNITDATA request.

In the state diagrams, PMA_UNITDATA.request is assumed to occur at the conclusion of each tw1 wait function.

23.3.2.3 Effect of receipt

Upon receipt of this primitive, the PMA transmits the indicated ternary symbols on the MDI.

23.3.3 PMA_UNITDATA.indicate

This primitive defines the transfer of data (in the form of rx_code_vector parameters) from the PMA to the PCS or repeater during the time that link_status=OK.

23.3.3.1 Semantics of the service primitive

PMA_UNITDATA.indicate (rx_code_vector)

When receiving data using 100BASE-T4 signaling, the PMA_UNITDATA.indicate conveys to the PCS simultaneously the logical input value for each of the three receive pairs RX_D2, BI_D4, and BI_D3. The value of rx_code_vector during data reception is therefore a three-element vector, with one element corresponding to each input pair. Each of the three elements of the rx_code_vector may take on one of three logical values: 1, 0, or –1, corresponding to the three ternary possibilities +, 0, and - listed for each ternary symbol in the 8B6T code table (see annex 23A).

Between packets, the rx_code_vector is set by the PMA to the value IDLE.

From the time the PMA asserts carrier_status=ON until the PMA recognizes the SSD pattern (not all of the pattern need be received in order for the PMA to recognize the pattern), the PMA sets rx_code_vector to the value PREAMBLE.

For pma_type 100BASE-T4, the rx_code_vector parameter can take on any of three forms:

IDLE	A single value indicating that the PMA has no data to convey.
PREAMBLE	A single value indicating that the PMA has detected carrier, but has not received a valid SSD.
DATA	A vector of three ternary symbols, one for each of the three receive pairs RX_D2, BI_D3, and BI_D4. The ternary symbol for each pair may take on one of three values, 1, 0, or –1.

The ternary symbols comprising rx_code_vector, when they are conveyed using the DATA format, are called, according to the pair upon which each symbol was received, rx_code_vector[BI_D3], rx_code_vector[RX_D2], and rx_code_vector[BI_D4].

23.3.3.2 When generated

The PMA shall generate PMA_UNITDATA.indicate (DATA) messages synchronous with data received at the MDI.

23.3.3.3 Effect of receipt

The effect of receipt of this primitive is unspecified.

23.3.4 PMA_CARRIER.indicate

This primitive is generated by the PMA to indicate the status of the signal being received from the MDI. The purpose of this primitive is to give the PCS or repeater client the earliest reliable indication of activity on the underlying medium.

23.3.4.1 Semantics of the service primitive

PMA_CARRIER.indicate (carrier_status)

The carrier_status parameter can take on one of two values: OFF or ON, indicating whether the incoming signal should be interpreted as being between packets (OFF) or as a packet in progress (ON).

23.3.4.2 When generated

The PMA shall generate this primitive to indicate the value of carrier_status.

23.3.4.3 Effect of receipt

The effect of receipt of this primitive is unspecified.

23.3.5 PMA_LINK.indicate

This primitive is generated by the PMA to indicate the status of the underlying medium. The purpose of this primitive is to give the PCS or repeater client or Auto-Negotiation algorithm a means of determining the validity of received code elements.

23.3.5.1 Semantics of the service primitive

PMA_LINK.indicate (link_status)

The link_status parameter can take on one of three values: FAIL, READY, or OK:

FAIL	The link integrity function does not detect a valid 100BASE-T4 link.
READY	The link integrity function detects a valid 100BASE-T4 link, but has not been enabled by Auto-Negotiation.
OK	The 100BASE-T4 link integrity function detects a valid 100BASE-T4 link, and has been enabled by Auto-Negotiation.

23.3.5.2 When generated

The PMA shall generate this primitive to indicate the value of link_status.

23.3.5.3 Effect of receipt

The effect of receipt of this primitive is unspecified.

23.3.6 PMA_LINK.request

This primitive is generated by the Auto-Negotiation algorithm. The purpose of this primitive is to allow the Auto-Negotiation algorithm to enable and disable operation of the PHY.

23.3.6.1 Semantics of the service primitive

PMA_LINK request (link_control)

The link_control parameter can take on one of three values: SCAN_FOR_CARRIER, DISABLE, or ENABLE.

SCAN_FOR_CARRIER	Used by the Auto-Negotiation algorithm prior to receiving any fast link pulses. During this mode the PHY reports link_status=READY if it recognizes 100BASE-T4 carrier from the far end, but no other actions are enabled.
DISABLE	Used by the Auto-Negotiation algorithm to disable PHY processing in the event fast link pulses are detected. This gives the Auto-Negotiation algorithm a chance to determine how to configure the link.
ENABLE	Used by Auto-Negotiation to turn control over to the PHY for data processing functions. This is the default mode if Auto-Negotiation is not present.

23.3.6.2 Default value of parameter link_control

Upon power-on, reset, or release from power-down, the link_control parameter shall revert to ENABLE. If the optional Auto-Negotiation algorithm is not implemented, no PMA_LINK.request message will arrive and the PHY will operate indefinitely with link_control=ENABLE.

23.3.6.3 When generated

The Auto-Negotiation algorithm generates this primitive to indicate to the PHY how to behave.

Upon power-on, reset, or release from power down, the Auto-Negotiation algorithm, if present, issues the message PMA_LINK request (SCAN_FOR_CARRIER).

23.3.6.4 Effect of receipt

Whenever link_control=SCAN_FOR_CARRIER, the PHY shall enable the Link Integrity state diagram, but block passage into the state LINK_PASS, while holding rcv=DISABLE, and xmit=DISABLE. While link_control=SCAN_FOR_CARRIER, the PHY shall report link_status=READY if it recognizes 100BASE-T4 link integrity pulses coming from the far end, otherwise it reports link_status=FAIL.

Whenever link_control=DISABLE, the PHY shall report link_status=FAIL and hold the Link Integrity state diagram in the RESET state, while holding rcv=disable and xmit=DISABLE.

While link_control=ENABLE, the PHY shall allow the Link Integrity function to determine if the link is available and, if so, set rcv=ENABLE and xmit=ENABLE.

23.3.7 PMA_RXERROR.indicate

The primitive is generated in the PMA by the PMA Align function to indicate the status of the signal being received from the MDI. The purpose of this primitive is to give the PCS or repeater client an indication of a PMA detectable receive error.

23.3.7.1 Semantics of the service primitive

PMA_RXERROR.indicate (rxerror_status)

The rxerror_status parameter can take on one of two values: ERROR or NO_ERROR, indicating whether the incoming signal contains a detectable error (ERROR) or not (NO_ERROR).

23.3.7.2 When generated

The PMA shall generate this primitive to indicate whether or not each incoming packet contains a PMA detectable error (23.2.1.4).

23.3.7.3 Effect of receipt

The effect of receipt of this primitive is unspecified.

23.4 PMA functional specifications

The PMA couples messages from a PMA service interface (23.3) to the 100BASE-T4 baseband medium (23.6).

The interface between PCS and the baseband medium is the Medium Dependent Interface (MDI), specified in 23.7.

23.4.1 PMA functions

The PMA sublayer comprises one PMA Reset function and six simultaneous and asynchronous operating functions. The PMA operating functions are PMA Transmit, PMA Receive, PMA Carrier Sense, Link Integrity, PMA Align, and Clock Recovery. All operating functions are started immediately after the successful completion of the PMA Reset function. When the PMA is used in conjunction with a PCS, the RESET function may be shared between layers.

The PMA reference diagram, figure 23-11, shows how the operating functions relate to the messages of the PMA Service interface and the signals of the MDI. Connections from the management interface, comprising the signals MDC and MDIO, to other layers are pervasive, and are not shown in figure 23-11. The Management Interface and its functions are specified in clause 22.

23.4.1.1 PMA Reset function

The PMA Reset function shall be executed any time either of two conditions occur. These two conditions are power-on and the receipt of a reset request from the management entity. The PMA Reset function initializes all PMA functions. The PMA Reset function sets pma_reset <= ON for the duration of its reset function. All state diagrams take the open-ended pma_reset branch upon execution of the PMA Reset function. The reference diagrams do not explicitly show the PMA Reset function.

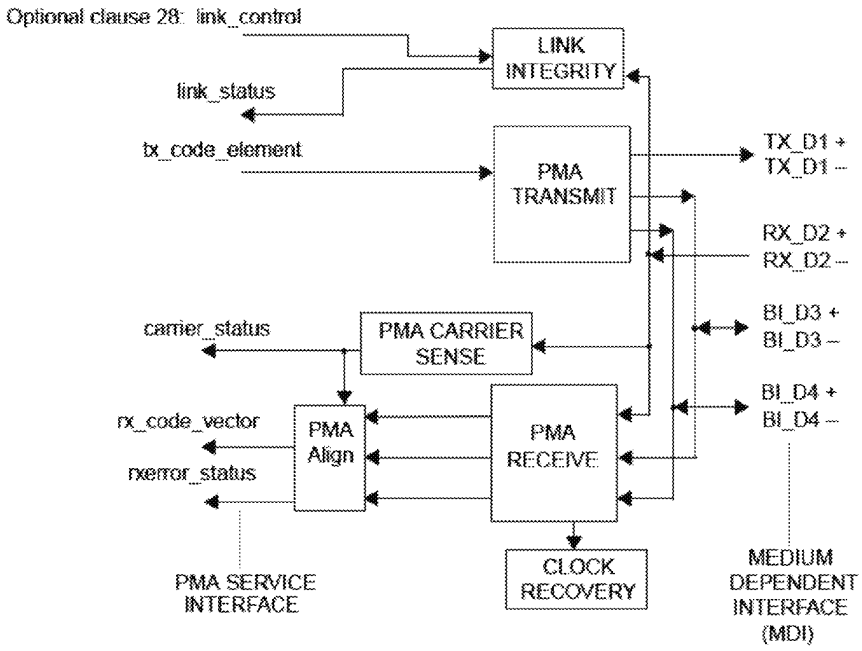


Figure 23-11—PMA reference diagram

23.4.1.2 PMA Transmit function

Except as provided for in the next paragraph, whenever (tx_code_vector=DATA)×(pma_carrier=OFF), the PMA shall transmit onto the MDI ternary symbols on pairs TX_D1, BI_D3, and BI_D4 equal to tx_code_vector[TX_D1], tx_code_vector[BI_D3], and tx_code_vector[BI_D4], respectively.

Whenever (tx_code_vector=DATA)×(pma_carrier=ON), the PMA shall transmit onto the MDI ternary symbols on pairs TX_D1, BI_D3, and BI_D4 equal to tx_code_vector[TX_D1], CS0, and CS0, respectively, and continue doing so until tx_code_vector=IDLE.

NOTE—This shuts off the transmitters on channels BI_D3 and BI_D4, and keeps them off, in the event of a collision. Shutting off the transmitters prevents overload and saturation of the transmitters, and also reduces the amount of near-end crosstalk present while monitoring for the end of carrier.

Whenever tx_code_vector=IDLE, an idle signal shall be transmitted on pair TX_D1 and silence on pairs BI_D3 and BI_D4. The idle signal consists of periods of silence (times where the differential output voltage remains at 0 mV ± 50 mV) broken by the transmission of link integrity test pulses.

The 100BASE-T4 idle signal is similar to the 10BASE-T idle signal, but with 100BASE-T4 ternary signal levels and a faster repetition rate. The 100BASE-T4 idle signal is called TP_IDL_100. The TP_IDL_100 signal shall be a repeating sequence formed from one 1.2 ms ± 0.6 ms period of silence (the time where the differential voltage remains at 0 mV ± 50 mV) and one link test pulse. Each link test pulse shall be a succession of two ternary symbols having logical values of –1 and 1 transmitted on pair TX_D1 using CS-1 and CS1 as defined in 23.4.3.1. Following a packet, the TP_IDL_100 shall start with a period of silence.

Transmission of TP_IDL_100 may be terminated at any time with respect to the link test pulse. It shall be terminated such that ternary symbols of the subsequent packet are not corrupted, and are not delayed any more than is specified in 23.11.

For any link test pulse occurring within 20 ternary symbol times of the beginning of a preamble, the zero crossing jitter (as defined in 23.5.1.2.5) of the link test pulse when measured along with the zero crossings of the preamble shall be less than 4 ns p-p.

NOTE—The above condition allows clock recovery implementations that optionally begin fast-lock sequences on part of a link integrity pulse to properly acquire lock on a subsequent preamble sequence.

Regardless of other considerations, when the transmitter is disabled (xmit=DISABLE), the PMA Transmit function shall transmit the TP_IDL_100 signal.

23.4.1.3 PMA Receive function

PMA Receive contains the circuits necessary to convert physically encoded ternary symbols from the physical MDI receive pairs (RX_D2, BI_D3 and BI_D4) into a logical format suitable for the PMA Align function. Each receive pair has its own dedicated PMA Receive circuitry.

The PHY shall receive the signals on the receive pairs (RX_D2, BI_D3, and BI_D4) and translate them into one of the PMA_UNITDATA.indicate parameters IDLE, PREAMBLE, or DATA with a ternary symbol error rate of less than one part in 10^8.

If both pma_carrier=ON and tx_code_vector=DATA, the value of rx_code_vector is unspecified until pma_carrier=OFF.

23.4.1.4 PMA Carrier Sense function

The PMA Carrier Sense function shall set pma_carrier=ON upon reception of the following pattern on pair RX_D2 at the receiving MDI, as measured using a 100BASE-T4 transmit test filter (23.5.1.2.3):

> Any signal greater than 467 mV, followed by any signal less than –225 mV, followed by any signal greater than 467 mV, all three events occurring within 2 ternary symbol times.

The operation of carrier sense is undefined for signal amplitudes greater than 4.5 V.

See 23.5.1.3.2 for a list of signals defined *not* to set pma_carrier=ON.

After asserting pma_carrier=ON, PMA Carrier Sense shall set pma_carrier=OFF upon receiving either of these conditions:

a) Seven consecutive ternary symbols of value CS0 on pair RX_D2.
b) (tx_code_vector=DATA) has not been true at any time since pma_carrier was asserted, *and* the 6T code group eop1 has been received, properly framed, on any of the lines RX_D2, BI_D4, or BI_D3, *and* enough time has passed to assure passage of all ternary symbols of eop4 across the PMA service interface.

NOTE—Designers may wish to take advantage of the fact that the minimum received packet fragment will include at least 24 ternary symbols of data on pair RX_D2. Therefore, once carrier is activated, it is not necessary to begin searching for seven consecutive zeroes until after the 24th ternary symbol has been received. During the time that the first 24 ternary symbols are being received, the near-end crosstalk from pairs BI_D3 and BI_D4, which are switched off during collisions, decays substantially.

While rcv=ENABLE, the PMA CARRIER function shall set carrier_status = pma_carrier.

While rcv↑ENABLE, the PMA CARRIER function shall set carrier_status = OFF.

This function operates independently of the Link Integrity function.

23.4.1.5 Link Integrity function

Link Integrity provides the ability to protect the network from the consequences of failure of the simplex link attached to RX_D2. While such a failure is present, transfer of data by the Transmit and Receive functions is disabled.

Link Integrity observes the incoming wire pair, RX_D2, to determine whether the device connected to the far end is of type 100BASE-T4. Based on its observations, Link Integrity sets two important internal variables:

a) pma_type variable is set to 100BASE-T4.
b) link_status variable is a parameter sent across the PMA Service interface.

The Link Integrity function shall comply with the state diagram of figure 23-12.

Four conditions gate the progression of states toward LINK_PASS: (1) reception of at least 31 link integrity test pulses; (2) reception of at least 96 more link integrity test pulses, or reception of carrier; (3) cessation of carrier, if it was present; (4) detection of equals link_control ENABLE.

While the PMA is not in the LINK_PASS state, the Link Integrity function sets rcv=DISABLE and xmit=DISABLE, thus disabling the bit transfer of the Transmit and Receive functions.

If a visible indicator is provided on the PHY to indicate the link status, it is recommended that the color be green and that the indicator be labeled appropriately. It is further recommended that the indicator be on when the PHY is in the LINK_PASS state and off otherwise.

23.4.1.6 PMA Align function

The PMA Align function accepts received ternary symbols from the PMA Receive function, along with pma_carrier. PMA Align is responsible for realigning the received ternary symbols to eliminate the effects of unequal pair propagation time, commonly called pair skew. PMA Align also looks for the SSD pattern to determine the proper alignment of 6T code groups, and then forwards PMA_UNITDATA.indicate (DATA) messages to the PCS. The SSD pattern includes referencing patterns on each of the three receive lines that may be used to establish the proper relationship of received ternary symbols (see figure 23-6).

NOTE—The skew between lines is not expected to change measurably from packet to packet.

At the beginning of each received frame, the PMA Carrier Sense function asserts pma_carrier=ON. During the preamble, the Clock Recovery function begins synchronizing its receive clock. Until clock is synchronized, data coming from the low-level PMA Receive function is meaningless. The PMA Align function is responsible for waiting for the receiver clock to stabilize and then properly recognizing the 100BASE-T4 coded SSD pattern. The PMA Align function shall send PMA_UNITDATA.indicate (PREAMBLE) messages to the PCS from the time pma_carrier=ON is asserted until the PMA is ready to transfer the first PMA_UNITDATA.indicate (DATA) message. Once the PMA Align function locates a SSD pattern, it begins forwarding PMA_UNITDATA.indicate (DATA) messages to the PCS, starting with the first ternary symbol of the first data word on pair BI_D3, as defined in figure 23-6. This first PMA_UNITDATA.indicate (DATA) message shall transfer the following ternary symbols, as specified in the frame structure diagram, figure 23-6:

rx_code_vector[BI_D3]first ternary symbol of first data code group

rx_code_vector[RX_D2]second ternary symbol prior to start of second data code group

rx_code_vector[BI_D4]fourth ternary symbol prior to start of third data code group

PMA Align shall continue sending PMA_UNITDATA.indicate (DATA) messages until pma_carrier=OFF. While pma_carrier=OFF, PMA Align shall emit PMA_UNITDATA.indicate (IDLE) messages.

If no valid SSD pattern is recognized within 22 ternary symbol times of the assertion of pma_carrier=ON, the PMA Align function shall set rxerror_status=ERROR. The PMA Align function is permitted to begin sending PMA_UNITDATA.indicate (DATA) messages upon receipt of a partially recognized SSD pattern, but it is required to set rxerror_status=ERROR if the complete SSD does not match perfectly the expected ternary symbol sequence. Rxerror_status shall be reset to NO_ERROR when pma_carrier=OFF.

The PMA Align function is permitted to use the first received packet of at least minimum size after RESET or the transition to LINK_PASS to learn the nominal skew between pairs, adjust its equalizer, or perform any other initiation functions. During this first packet, the PMA Align function shall emit PMA_UNITDATA.indicate (PREAMBLE) messages, but may optionally choose to never begin sending PMA_UNITDATA.indicate (DATA) messages.

The PMA Align function shall tolerate a maximum skew between any two pairs of 60 ns in either direction without crror.

To protect the network against the consequences of mistaken packet framing, the PMA Align function shall detect the following error and report it by setting rxerror_status=ERROR (optionally, those error patterns already detected by codeword_error, dc_balance_error, or eop_error do not also have to be detected by rxerror_status): *In a series of good packets, any one packet that has been corrupted with three or fewer ternary symbols in error causing its sosb 6T code groups on one or more pairs to appear in the wrong location.*

Several approaches are available for meeting this requirement, including, but not limited to, a) comparing the relative positions of sosb 6T code groups on successive packets; b) measuring the time between the first preamble pulse and reception of sosb on each pair; c) counting the number of zero crossings from the beginning of the preamble until sosb; and d) monitoring for exception strings like "11" and "–1–1–1" in conjunction with one or more of the above techniques.

Regardless of other considerations, when the receive function is disabled (rcv=DISABLE), the PMA Align function shall emit PMA_UNITDATA.indicate (IDLE) messages and no others.

23.4.1.7 Clock Recovery function

The Clock Recovery function couples to all three receive pairs. It provides a synchronous clock for sampling each pair. While it may not drive the MII directly, the Clock Recovery function is the underlying root source of RX_CLK.

The Clock Recovery function shall provide a clock suitable for synchronously decoding ternary symbols on each line within the bit error tolerance provided in 23.4.1.3. During each preamble, in order to properly recognize the frame delimiting pattern formed by code word sosb on each pair, the received clock signal must be stable and ready for use in time to decode the following ternary symbols: the 16th ternary symbol of pair RX_D2, the 18th ternary symbol of pair BI_D4, and the 14th ternary symbol of pair BI_D3.

23.4.2 PMA interface messages

The messages between the PMA and PCS are defined above in 23.3, PMA Service Interface. Communication between a repeater unit and PMA also uses the PMA Service Interface. Communication through the MDI is summarized in tables 23-2 and 23-3.

Table 23-2—MDI signals transmitted by the PHY

Signal	Allowed pair	Meaning
CS1	TX_D1, BI_D3 BI_D4	A waveform that conveys the ternary symbol 1. Nominal voltage level +3.5 V.
CS0	TX_D1, BI_D3 BI_D4	A waveform that conveys the ternary symbol 0. Nominal voltage level 0 V.
CS-1	TX_D1, BI_D3 BI_D4	A waveform that conveys the ternary symbol –1. Nominal voltage level –3.5 V.
TP_IDL_100	TX_D1	Idle signal. Indicates transmitter is currently operating at 100 Mb/s.

Table 23-3—Signals received at the MDI

Signal	Allowed pair	Meaning
CS1	RX_D2, BI_D3 BI_D4	A waveform that conveys the ternary symbol 1. Nominal transmitted voltage level +3.5 V.
CS0	RX_D2, BI_D3 BI_D4	A waveform that conveys the ternary symbol 0. Nominal transmitted voltage level 0 V.
CS-1	RX_D2, BI_D3 BI_D4	A waveform that conveys the ternary symbol –1. Nominal transmitted voltage level –3.5 V.
TP_IDL_100	RX_D2	Idle signal. Indicates transmitter is currently operating at 100 Mb/s.

TP_IDL_100 is defined in 23.4.1.2. The waveforms used to convey CS1, CS0, and CS-1 are defined in 23.5.1.2.

TP_IDL_100 is defined in 23.4.1.2. The encodings for CS1, CS0, and CS-1 are defined in 23.5.1.2.

Re-timing of CS1, CS0, and CS-1 signals within the PMA is required.

23.4.3 PMA state diagrams

The notation used in the state diagrams follows the conventions of 21.5. Transitions shown without source states are evaluated continuously and take immediate precedence over all other conditions.

23.4.3.1 PMA constants

CS0

A waveform that conveys the ternary symbol 0.

Value: CS0 has a nominal voltage of 0 V. See 23.5.1.2.

CS1

A waveform that conveys the ternary symbol 1.

Value: CS1 has a nominal peak voltage of +3.5 V. See 23.5.1.2.

CS-1

A waveform that conveys the ternary symbol –1.

Value: CS-1 has a nominal peak voltage of –3.5 V. See 23.5.1.2.

link_100_max

A constant.

Value: Greater than 5.0 ms and less than 7.0 ms.

Used by link_max_timer to detect the absence of 100BASE-T4 link test pulses on pair RX_D2.

link_100_min

A constant.

Value: Greater than 0.15 ms and less than 0.45 ms.

Used by cnt_link to detect link test pulses on pair RX_D2 that are too close together to be valid 100BASE-T4 link test pulses.

23.4.3.2 State diagram variables

pma_reset

Causes reset of all PCS functions.

Values: ON and OFF

Set by: PMA Reset

pma_carrier

A version of carrier_status used internally by the PMA sublayer. The variable pma_carrier always functions regardless of the link status. The value of pma_carrier is passed on through the PMA service interface as carrier_status when rcv=ENABLE. At other times, the passage of pma_carrier information to the PMA service interface is blocked.

Values: ON, OFF

Set by: PMA CARRIER

rcv

Controls the flow of data from the PMA to PCS through the PMA_UNITDATA.indicate message.

Values: ENABLE (receive is enabled)
DISABLE (the PMA always sends PMA_UNITDATA.indicate (IDLE), and carrier_status is set to OFF)

xmit

Controls the flow of data from PCS to PMA through the PMA_UNITDATA.request message.

Values: ENABLE (transmit is enabled)
DISABLE (the PMA interprets all PMA_UNITDATA.request messages as PMA_UNITDATA.request (IDLE). The PMA transmits no data, but continues sending TP_IDL_100).

23.4.3.3 State diagram timers

link_max_timer

A re-triggerable timer.

Values: The condition link_max_timer_done goes true when the timer expires.

Restart when: Timer is restarted for its full duration by every occurrence of either a link test pulse on pair RX_D2 or the assertion of pma_carrier=ON (restarting the timer resets the condition link_max_timer_done).

Duration: link_100_max

Used by Link Integrity to detect the absence of 100BASE-T4 link test pulses on pair RX_D2.

23.4.3.4 State diagram counters

cnt_link

Counts number of 100BASE-T4 link test pulses (see 23.5.1.3.1) received on pair RX_D2.

Values: nonnegative integers

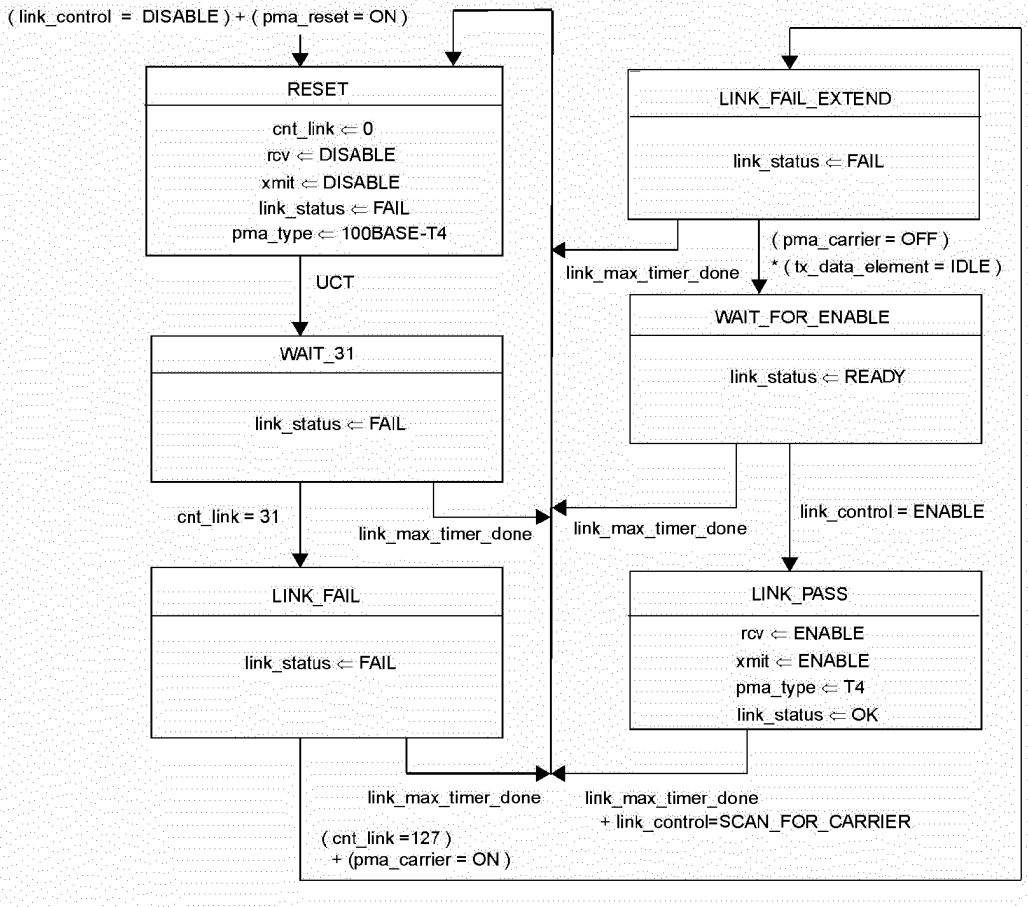
Reset to zero: On either of two conditions:

a) While in any state other than LINK_PASS, reset counter to zero if successive link test pulses are received within link_100_min.
b) While in any state, reset to zero if link_max_timer expires.

While in the LINK_PASS state, ignore pulses received within link_100_min (i.e., do not count them).

23.4.3.5 Link Integrity state diagram

The Link Integrity state diagram is shown in figure 23-12.



NOTE—The variables link_control and link_status are designated as link_control_[T4] and link_status_[T4], respectively, by the Auto-Negotiation Arbitration state diagram (figure 28-16).

Figure 23-12—Link integrity state diagram

23.5 PMA electrical specifications

This clause defines the electrical characteristics of the PHY at the MDI.

The ground reference point for all common-mode tests is the MII ground circuit. Implementations without an MII use the chassis ground. The values of all components in test circuits shall be accurate to within ±1% unless otherwise stated.

23.5.1 PMA-to-MDI interface characteristics

23.5.1.1 Isolation requirement

The PHY shall provide electrical isolation between the DTE, or repeater circuits including frame ground, and all MDI leads. This electrical separation shall withstand at least one of the following electrical strength tests:

a) 1500 V rms at 50 Hz to 60 Hz for 60 s, applied as specified in subclause 5.3.2 of IEC 950: 1991.
b) 2250 Vdc for 60 s, applied as specified in subclause 5.3.2 of IEC 950: 1991.
c) A sequence of ten 2400 V impulses of alternating polarity, applied at intervals of not less than 1 s. The shape of the impulses shall be 1.2/50 ∝s (1.2 ∝s virtual front time, 50 ∝s virtual time or half value), as defined in IEC 60.

There shall be no insulation breakdown, as defined in subclause 5.3.2 of IEC 950: 1991, during the test. The resistance after the test shall be at least 2 M | , measured at 500 Vdc.

23.5.1.2 Transmitter specifications

The PMA shall provide the Transmit function specified in 23.4.1.2 in accordance with the electrical specifications of this clause.

Where a load is not specified, the transmitter shall meet requirements of this clause when each transmit output is connected to a differentially connected 100 | resistive load.

23.5.1.2.1 Peak differential output voltage

While repetitively transmitting the ternary sequence [0 0 1 0 0 0 0 0 −1 0 0 0] (leftmost ternary symbol first), and while observing the differential transmitted output at the MDI, for any pair, with no intervening cable, the absolute value of both positive and negative peaks shall fall within the range of 3.15 V to 3.85 V (3.5 V ± 10%).

23.5.1.2.2 Differential output templates

While repetitively transmitting the ternary sequence [0 0 1 0 0 0 0 0 −1 0 0 0], and while observing the transmitted output at the MDI, the observed waveform shall fall within the normalized transmit template listed in table 23-4. Portions of this table are represented graphically in figure 23-13. The entire normalized transmit template shall be scaled by a single factor between 3.15 and 3.85. It is a functional requirement that linear interpolation be used between points. The template time axis may be shifted horizontally to attain the most favorable match. In addition to this simple test pattern, all other pulses, including link integrity pulses and also including the first pulse of each packet preamble, should meet this same normalized transmit template, with appropriate shifting and linear superposition of the CS1 and CS-1 template limits. Transmitters are allowed to insert additional delay in the transmit path in order to meet the first pulse requirement, subject to the overall timing limitations listed in 23.11, Timing summary.

While transmitting the TP_IDL_100 signal, and while observing the transmitted output at the MDI, the observed waveform shall fall within the normalized link pulse template listed in table 23-4. Portions of this table are represented graphically in figure 23-14. The entire template shall be scaled by the same factor used for the normalized transmit template test. It is a functional requirement that linear interpolation be used between template points. The template time axis may be shifted horizontally to attain the most favorable match.

After transmitting seven or more consecutive CS0 waveforms during the TP_IDL_100 signal, each pair, as observed using the 100BASE-T4 Transmit Test Filter (23.5.1.2.3) connected to the MDI, shall attain a state within 50 mV of zero.

When the TX_D1, BI_D3, or BI_D4 pair is driven with a repeating pattern (`1 -1 1 -1 ...`) any harmonic measured at the MDI output shall be at least 27 dB below the fundamental at 12.5 MHz.

NOTES

1—The specification on maximum spectral components is not intended to ensure compliance with regulations concerning RF emissions. The implementor should consider any applicable local, national, or international regulations. Additional filtering of spectral components may therefore be necessary.

2—The repetitive pattern [`0 0 1 0 0 0 0 0 -1 0 0 0`] (leftmost ternary symbol first) may be synthesized using the 8B6T coding rules from a string of repeating data octets with value 73 hex. The repetitive pattern [`1 -1 1 -1 1 -1`] (leftmost ternary symbol first) may be synthesized using the 8B6T coding rules from a string of repeating data octets with value 92 hex.

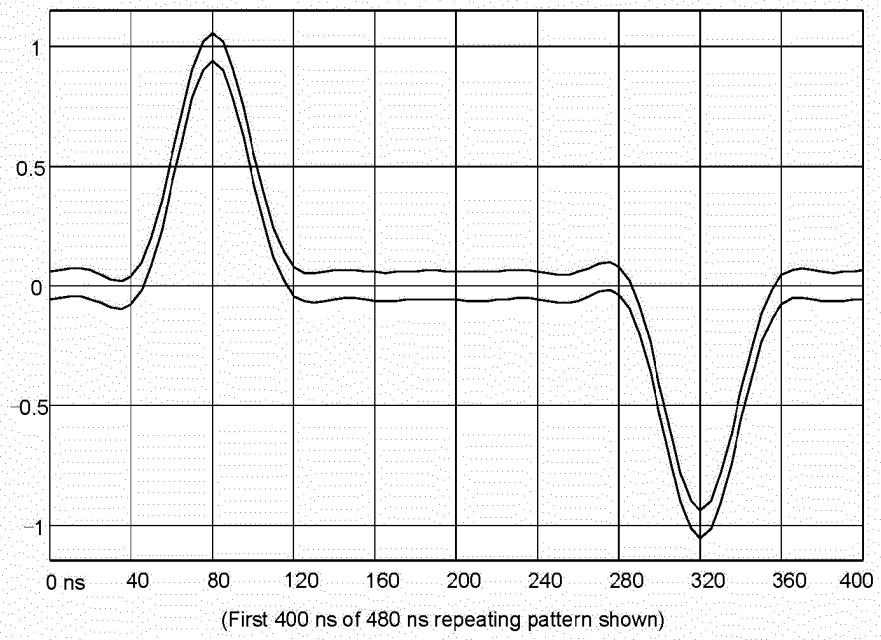


Figure 23-13—Normalized transmit template as measured at MD

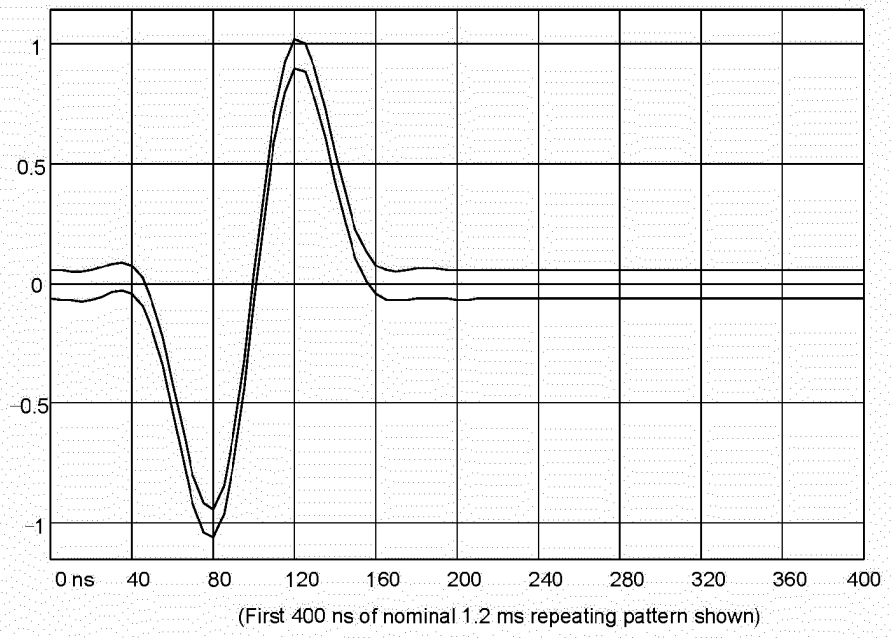


Figure 23-14—Normalized link pulse template as measured at MDI

The ideal template values may be automatically generated from the following equations:

Laplace transform of
Ideal transmit response $\quad IdealResponse(s) = \frac{Ideal(s)}{LPF(s)}$

Where $Ideal(s)$ is a 100% raised cosine system response

Where $LPF(s)$ is a 3-pole Butterworth low pass filter response with –3 dB point at 25 MHz

Convert *IdealResponse(s)* from frequency domain to time domain

Use at least 8 samples per ternary symbol for the conversion

Superimpose alternating positive and negative copies of the ideal time response, seperated by 6 ternary symbol times, to form the ideal transmit voltage waveform.

The template limits are formed by offsetting the ideal transmit voltage waveform by plus and minus 6% of its peak.

23.5.1.2.3 Differential output ISI (intersymbol interference)

While observing a pseudo-random 8B6T coded data sequence (with every 6T code group represented at least once) preceded by at least 128 octets and followed by at least 128 octets of data, and while observing the transmitted output through a 100BASE-T4 Transmit Test Filter (one implementation of which is depicted in figure 23-16), the ISI shall be less than 9%. The ISI for this test is defined by first finding the largest of the three peak-to-peak ISI error voltages marked in figure 23-15 as TOP ISI, MIDDLE ISI, and BOTTOM ISI.

The largest of these peak-to-peak ISI error voltages is then divided by the overall peak-to-peak signal voltage. (The technique of limiting the ratio of worst ISI to overall peak-to-peak voltage at 9% accomplishes the same end as limiting the ratio of worst ISI to nominal peak-to-peak at 10%.)

Table 23-4—Normalized voltage templates as measured at the MDI

Time, ns	Normalized transmit template, pos. limit	Normalized transmit template, neg. limit	Normalized link template, pos. limit	Normalized link template, neg. limit
0	0.060	–0.061	0.061	–0.060
5	0.067	–0.054	0.056	–0.065
10	0.072	–0.049	0.052	–0.069
15	0.072	–0.049	0.052	–0.069
20	0.063	–0.058	0.058	–0.063
25	0.047	–0.074	0.071	–0.050
30	0.030	–0.091	0.086	–0.035
35	0.023	–0.098	0.094	–0.027
40	0.041	–0.080	0.080	–0.041
45	0.099	–0.022	0.027	–0.094
50	0.206	0.085	–0.076	–0.197
55	0.358	0.237	–0.231	–0.352
60	0.544	0.423	–0.428	–0.549
65	0.736	0.615	–0.640	–0.761
70	0.905	0.784	–0.829	–0.950
75	1.020	0.899	–0.954	–1.075
80	1.060	0.940	–0.977	–1.098
85	1.020	0.899	–0.876	–0.997
90	0.907	0.786	–0.653	–0.774
95	0.744	0.623	–0.332	–0.453
100	0.560	0.439	0.044	–0.077
105	0.384	0.263	0.419	0.298
110	0.239	0.118	0.738	0.617
115	0.137	0.016	0.959	0.838
120	0.077	–0.044	1.060	0.940
125	0.053	–0.068	1.044	0.923
130	0.050	–0.071	0.932	0.811
135	0.057	–0.064	0.759	0.638
140	0.064	–0.057	0.565	0.444
145	0.067	–0.054	0.383	0.262
150	0.065	–0.056	0.238	0.117
155	0.061	–0.060	0.138	0.017
160	0.057	–0.064	0.081	–0.040
165	0.055	–0.066	0.057	–0.064
170	0.056	–0.065	0.054	–0.067
175	0.059	–0.062	0.058	–0.063

Table 23-4—Normalized voltage templates as measured at the MDI *(Continued)*

Time, ns	Normalized transmit template, pos. limit	Normalized transmit template, neg. limit	Normalized link template, pos. limit	Normalized link template, neg. limit
180	0.062	–0.059	0.063	–0.058
185	0.064	–0.057	0.064	–0.057
190	0.064	–0.057	0.063	–0.058
195	0.062	–0.059	0.060	–0.061
200	0.060	–0.061	0.058	–0.063
205	0.057	–0.064	0.058	–0.063
210	0.056	–0.065	0.059	–0.062
215	0.058	–0.063	0.060	–0.061
220	0.061	–0.060	0.062	–0.059
225	0.064	–0.057	0.062	–0.059
230	0.066	–0.055	0.062	–0.059
235	0.065	–0.056	0.061	–0.060
240	0.061	–0.060	0.060	–0.061
245	0.054	–0.067	0.060	–0.061
250	0.049	–0.072	0.060	–0.061
255	0.049	–0.072	0.060	–0.061
260	0.058	–0.063	0.061	–0.060
265	0.074	–0.047	0.061	–0.060
270	0.091	–0.030	0.061	–0.060
275	0.099	–0.022	0.061	–0.060
280	0.080	–0.041	0.060	–0.061
285	0.022	–0.099	0.060	–0.061
290	–0.085	–0.206	0.060	–0.061
295	–0.238	–0.359	0.060	–0.061
300	–0.423	–0.544	0.061	–0.060
305	–0.615	–0.736	0.061	–0.060
310	–0.783	–0.904	0.061	–0.060
315	–0.899	-1.020	0.061	–0.060
320	–0.940	-1.061	0.060	–0.061
325	–0.899	-1.020	0.060	–0.061
330	–0.786	–0.907	0.060	–0.061
335	–0.623	–0.744	0.060	–0.061
340	–0.439	–0.560	0.061	–0.060
345	–0.263	–0.384	0.061	–0.060
350	–0.118	–0.239	0.061	–0.060
355	–0.016	–0.137	0.061	–0.060

Table 23-4—Normalized voltage templates as measured at the MDI *(Continued)*

Time, ns	Normalized transmit template, pos. limit	Normalized transmit template, neg. limit	Normalized link template, pos. limit	Normalized link template, neg. limit
360	0.044	–0.077	0.060	–0.061
365	0.068	–0.053	0.060	–0.061
370	0.070	–0.051	0.060	–0.061
375	0.064	–0.057	0.060	–0.061
380	0.057	–0.064	0.061	–0.060
385	0.054	–0.067	0.061	–0.060
390	0.056	–0.065	0.061	–0.060
395	0.060	–0.061	0.061	–0.060
400	0.064	–0.057	0.060	–0.061
405	0.065	–0.056	0.060	–0.061
410	0.064	–0.057	0.060	–0.061
415	0.061	–0.060	0.060	–0.061
420	0.059	–0.062	0.061	–0.060
425	0.058	–0.063	0.061	–0.060
430	0.059	–0.062	0.061	–0.060
435	0.060	–0.061	0.061	–0.060
440	0.061	–0.060	0.060	–0.061
445	0.062	–0.059	0.060	–0.061
450	0.062	–0.059	0.060	–0.061
455	0.061	–0.060	0.060	–0.061
460	0.060	–0.061	0.061	–0.060
465	0.059	–0.062	0.061	–0.060
470	0.060	–0.061	0.061	–0.060
475	0.060	–0.061	0.061	–0.060
480	0.061	–0.060	0.060	–0.061

It is a mandatory requirement that the peak-to-peak ISI, and the overall peak-to-peak signal voltage, be measured at a point in time halfway between the nominal zero crossings of the observed eye pattern.

It is a mandatory requirement that the 100BASE-T4 Transmit Test Filter perform the function of a third-order Butterworth filter with its –3 dB point at 25.0 MHz.

One acceptable implementation of a 100BASE-T4 Transmit Test Filter appears in figure 23-16. That implementation uses the 100BASE-T4 Transmit Test Filter as a line termination. The output of the filter is terminated in 100 | . It is a mandatory requirement that such implementations of the 100BASE-T4 Transmit Test Filter be designed such that the reflection loss of the filter, when driven by a 100 | source, exceeds 17 dB across the frequency range 2 to 12.5 MHz.

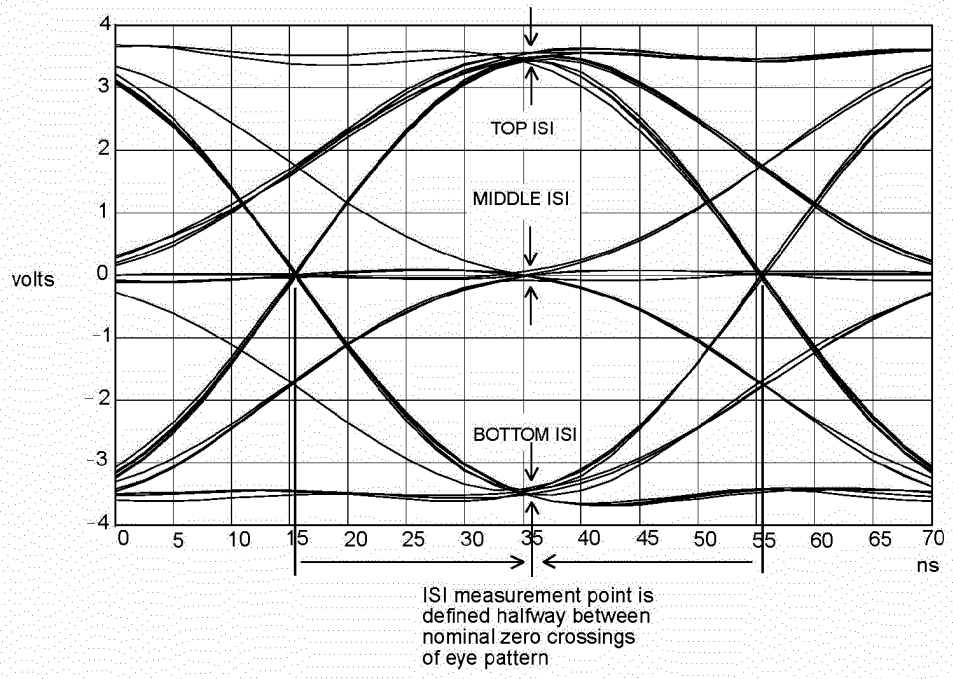


Figure 23-15—Definition of sampling points for ISI measurement

Equivalent circuits that implement the same overall transfer function are also acceptable. For example, the 100BASE-T4 Transmit Test Filter may be tapped onto a line in parallel with an existing termination. It is a mandatory requirement that such implementations of the 100BASE-T4 Transmit Test Filter be designed with an input impedance sufficiently high that the reflection loss of the parallel combination of filter and 100 | termination, when driven by 100 | , exceeds 17 dB across the frequency range 2 to 12.5 MHz.

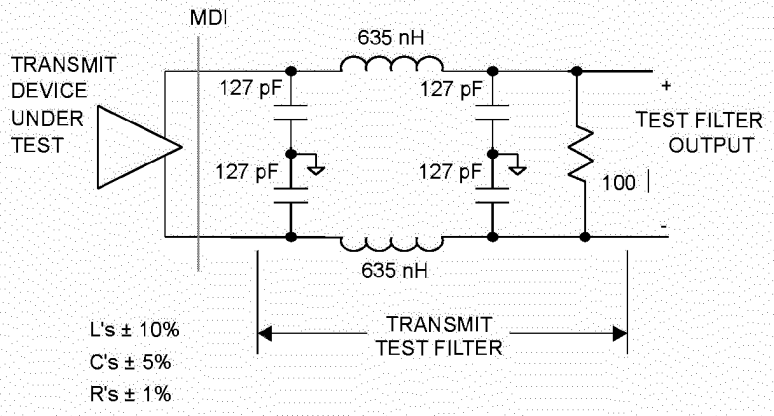
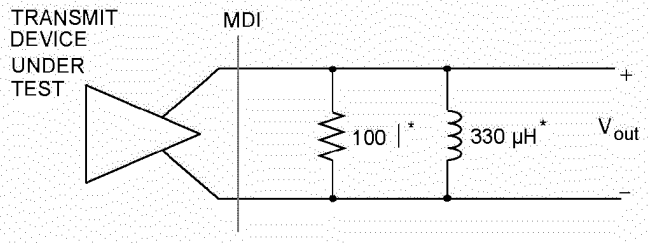


Figure 23-16—Acceptable implementation of transmit test filter

23.5.1.2.4 Transmitter differential output impedance

The differential output impedance as measured at the MDI for each transmit pair shall be such that any reflection due to differential signals incident upon the MDI from a balanced cable having an impedance of 100 | is at least 17 dB below the incident signal, over the frequency range of 2.0 MHz to 12.5 MHz. This return loss shall be maintained at all times when the PHY is fully powered.

With every transmitter connected as in figure 23-17, and while transmitting a repeating sequence of packets as specified in table 23-3, the amount of droop on any transmit pair as defined in figure 23-18 during the transmission of eop1 and eop4 shall not exceed 6.0%.



* ± 1% as measured at 100 kHz

Figure 23-17—Output impedance test setup

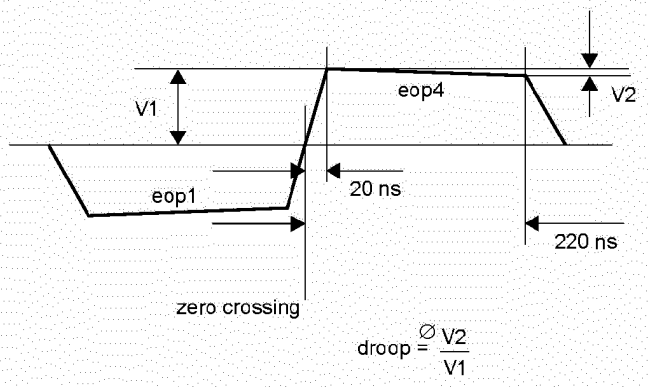
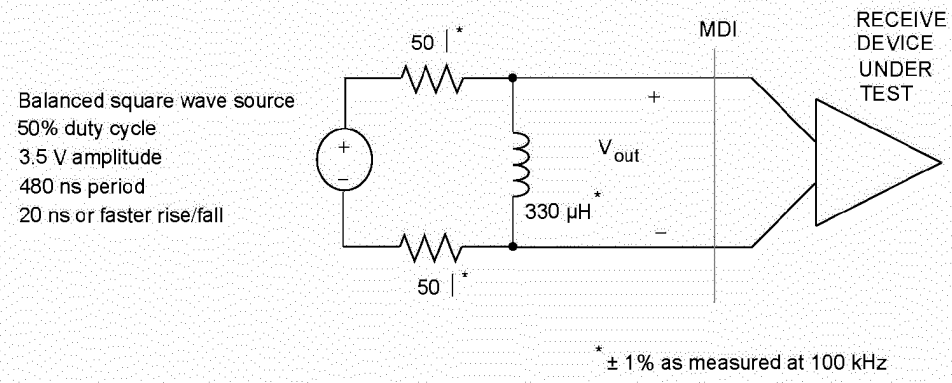


Figure 23-18—Measurement of output droop



* ± 1% as measured at 100 kHz

Figure 23-19—Input impedance test setup

Table 23-5—Sequence of packets for droop test

Packet sequence (Transmit this sequence of packets in a repetitive loop)	Packet length (Number of data octets)	Data, hex (All octets in each packet are the same)
first packet	64	AA
second packet	65	AA
third packet	66	AA

23.5.1.2.5 Output timing jitter

While repetitively transmitting a random sequence of valid 8B6T code words, and while observing the output of a 100BASE-T4 Transmit Test Filter connected at the MDI to any of the transmit pairs as specified in 23.5.1.2.3, the measured jitter shall be no more than 4 ns p-p. For the duration of the test, each of the other transmit pairs shall be connected to either a 100BASE-T4 Transmit Test Filter or a 100 | resistive load.

NOTES

1—Jitter is the difference between the actual zero crossing point in time and the ideal time. For various ternary transitions, the zero crossing time is defined differently. For transitions between +1 and –1 or vice versa, the zero crossing point is defined as that point in time when the voltage waveform crosses zero. For transitions between zero and the other values, or from some other value to zero, the zero crossing time is defined as that point in time when the voltage waveform crosses the boundary between logical voltage levels, halfway between zero volts and the logical +1 or logical –1 ideal level.

2—The ideal zero crossing times are contained in a set of points $\{t_n\}$ where $t_n = t_0 + n/f$, where n is an integer, and f is in the range 25.000 MHz ± 0.01%. A collection of zero crossing times satisfies the jitter requirement if there exists a pair (t_0, f) such that each zero crossing time is separated from some member of $\{t_n\}$ by no more than 4 ns.

23.5.1.2.6 Transmitter impedance balance

The common-mode to differential-mode impedance balance of each transmit output shall exceed

$$29 - 17\log\left(\frac{f}{10}\right)\text{dB}$$

where f is the frequency (in MHz) over the frequency range 2.0 MHz to 12.5 MHz. The balance is defined as

$$20\log\left(\frac{E_{cm}}{E_{dif}}\right)$$

where E_{cm} is an externally applied sine-wave voltage as shown in figure 23-20.

NOTE—The balance of the test equipment (such as the matching of the test resistors) must be insignificant relative to the balance requirements.

23.5.1.2.7 Common-mode output voltage

The implementor should consider any applicable local, national, or international regulations. Driving unshielded twisted pairs with high-frequency, common-mode voltages may result in interference to other equipment. FCC conducted and radiated emissions tests may require that, while transmitting data, the magnitude of the total common-mode output voltage, $E_{cm(out)}$, on any transmit circuit, be less than a few millivolts when measured as shown in figure 23-21.

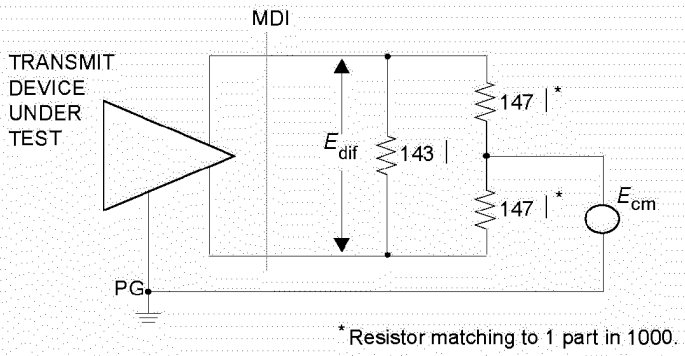


Figure 23-20—Transmitter impedance balance and common-mode rejection test circuit

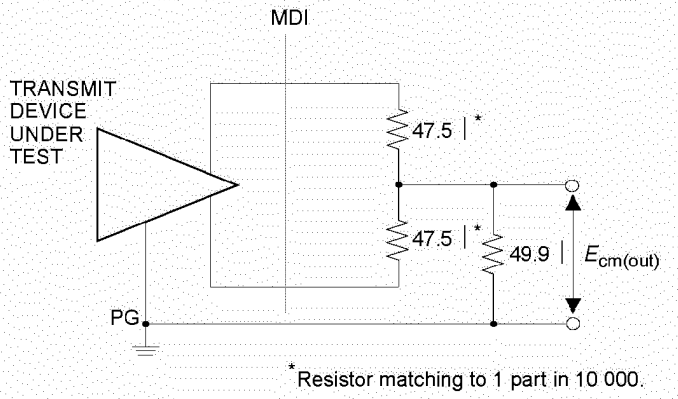


Figure 23-21—Common-mode output voltage test circuit

23.5.1.2.8 Transmitter common-mode rejection

The application of E_{cm} as shown in figure 23-20 shall not change the differential voltage at any transmit output, E_{dif}, by more than 100 mV for all data sequences while the transmitter is sending data. Additionally, the edge jitter added by the application of E_{cm} shall be no more than 1.0 ns. E_{cm} shall be a 15 V peak 10.1 MHz sine wave.

23.5.1.2.9 Transmitter fault tolerance

Transmitters, when either idle or nonidle, shall withstand without damage the application of short circuits across any transmit output for an indefinite period of time and shall resume normal operation after such faults are removed. The magnitude of the current through such a short circuit shall not exceed 420 mA.

Transmitters, when either idle or nonidle, shall withstand without damage a 1000 V common-mode impulse applied at E_{cm} of either polarity (as indicated in figure 23-22). The shape of the impulse shall be 0.3/50 μs (300 ns virtual front time, 50 μs virtual time of half value), as defined in IEC 60.

23.5.1.2.10 Transmit clock frequency

The ternary symbol transmission rate on each pair shall be 25.000 MHz ± 0.01%.

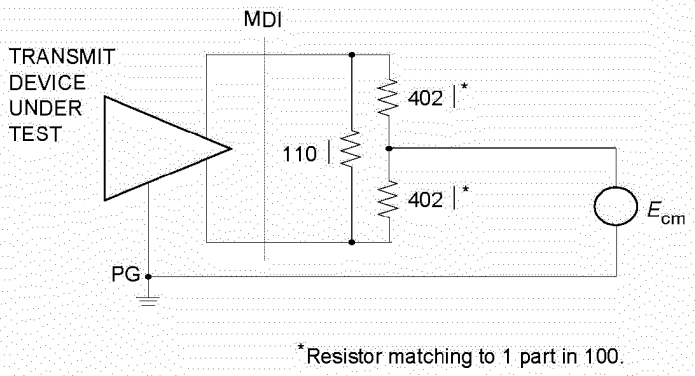


Figure 23-22—Transmitter fault tolerance test circuit

23.5.1.3 Receiver specifications

The PMA shall provide the Receive function specified in 23.4.1.3 in accordance with the electrical specifications of this clause. The patch cables and interconnecting hardware used in test configurations shall meet Category 5 specifications as in ISO/IEC 11801: 1995.

The term *worst-case UTP model*, as used in this clause, refers to lumped-element cable model shown in figure 23-23 that has been developed to simulate the attenuation and group delay characteristics of 100 m of worst-case Category 3 PVC UTP cable.

This constant resistance filter structure has been optimized to best match the following amplitude and group delay characteristics, where the argument f is in hertz, and the argument x is the cable length in meters. For the worst-case UTP model, argument x was set to 100 m, and the component values determined for a best least mean squared fit of both real and imaginary parts of $H(f, x)$ over the frequency range 2 to 15 MHz.

NOTE—This group delay model is relative and does not includes the fixed delay associated with 100 m of Category 3 cable. An additional 570 ns of fixed delay should be added in order to obtain the absolute group delay.

$$PropagationImag(f, x) = j(-10)\sqrt{\frac{f}{10^7}}\left(\frac{x}{100}\right)$$

$$PropagationReal(f, x) = -\left(7.1\sqrt{\frac{f}{10^6}} + 0.70\frac{f}{10^6}\right)\left(\frac{x}{305}\right)$$

$$\frac{PropagationImag(f, x) + PropagationReal(f, x)}{20}$$

$$H(f, x) = 10$$

23.5.1.3.1 Receiver differential input signals

Differential signals received on the receive inputs that were transmitted within the constraints of 23.5.1.2, and have then passed through a worst-case UTP model, shall be correctly translated into one of the PMA_UNITDATA.indicate messages and sent to the PCS. In addition, the receiver, when presented with a

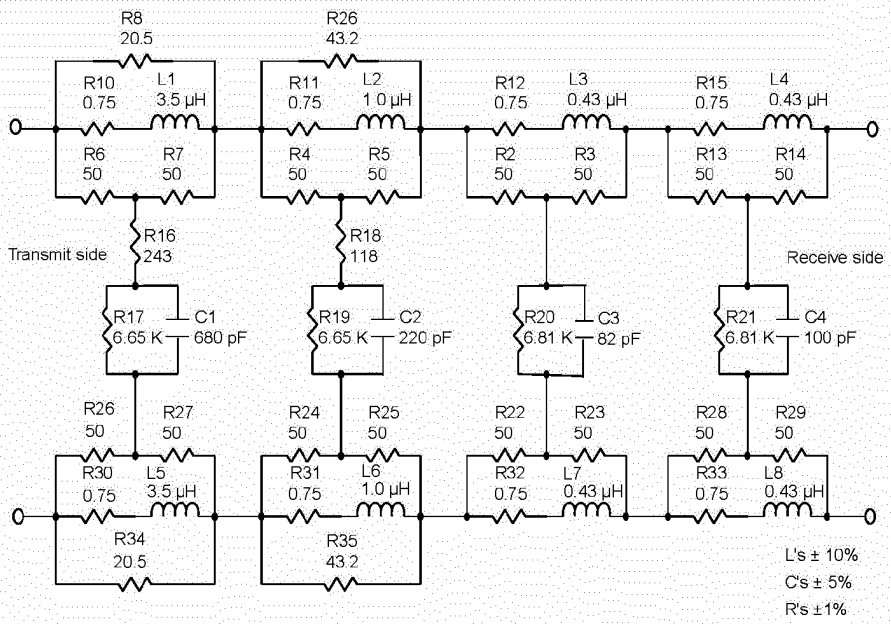


Figure 23-23—Worst-case UTP model

link test pulse generated according to the requirements of 23.4.1.2 and followed by at least 3T of silence on pair RX_D2, shall accept it as a link test pulse.

Both data and link test pulse receive features shall be tested in at least two configurations: using the worst-case UTP model, and with a connection less than one meter in length between transmitter and receiver.

A receiver is allowed to discard the first received packet after the transition into state LINK_PASS, using that packet for the purpose of fine-tuning its receiver equalization and clock recovery circuits.

NOTE—Implementors may find it practically impossible to meet the requirements of this subclause without using some form of adaptive equalization.

23.5.1.3.2 Receiver differential noise immunity

The PMA, when presented with 8B6T encoded data meeting the requirements of 23.5.1.3.1, shall translate this data into PMA_UNITDATA.indicate (DATA) messages with a bit loss of no more than that specified in 23.4.1.3.

The PMA Carrier Sense function shall *not* set pma_carrier=ON upon receiving any of the following signals on pair RX_D2 at the receiving MDI, as measured using a 100BASE-T4 transmit test filter (23.5.1.2.3):

a) All signals having a peak magnitude less than 325 mV.
b) All continuous sinusoidal signals of amplitude less than 8.7 V peak-to-peak and frequency less than 1.7 MHz.
c) All sine waves of single cycle or less duration, starting with phase 0Ÿor 180Ÿ, and of amplitude less than 8.7 V peak-to-peak, where the frequency is between 1.7 MHz and 15 MHz. For a period of 7 BT before and after this single cycle, the signal shall be less than 325 mV.

d) Fast link pulse burst (FLP burst), as defined in clause 28.
e) The link integrity test pulse signal TP_IDL_100.

23.5.1.3.3 Receiver differential input impedance

The differential input impedance as measured at the MDI for each receive input shall be such that any reflection due to differential signals incident upon each receive input from a balanced cable having an impedance of 100 | is at least 17 dB below the incident signal, over the frequency range of 2.0 MHz to 12.5 MHz. This return loss shall be maintained at all times when the PHY is fully powered.

With each receiver connected as in figure 23-19, and with the source adjusted to simulate eop1 and eop4 (50% duty cycle square wave with 3.5 V amplitude, period of 480 ns, and risetime of 20 ns or faster), the amount of droop on each receive pair as defined in figure 23-18 shall not exceed 6.0%.

23.5.1.3.4 Common-mode rejection

While receiving packets from a compliant 100BASE-T4 transmitter connected to all MDI pins, a receiver shall send the proper PMA_UNITDATA.indicate messages to the PCS for any differential input signal E_s that results in a signal E_{dif} that meets 23.5.1.3.1 even in the presence of common-mode voltages E_{cm} (applied as shown in figure 23-24). E_{cm} shall be a 25 V peak-to-peak square wave, 500 kHz or lower in frequency, with edges no slower than 4 ns (20%–80%), connected to each of the receive pairs RX_D2, BI_D3, and BI_D4.

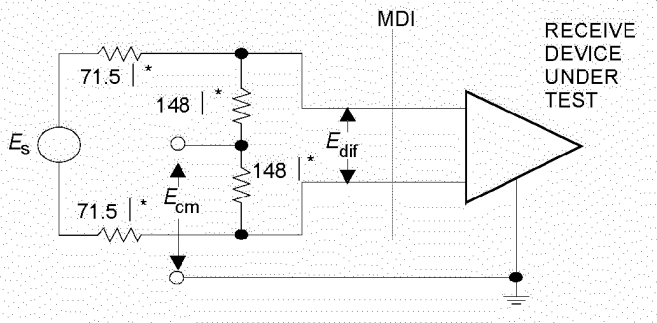


Figure 23-24—Receiver common-mode rejection test circuit

23.5.1.3.5 Receiver fault tolerance

The receiver shall tolerate the application of short circuits between the leads of any receive input for an indefinite period of time without damage and shall resume normal operation after such faults are removed. Receivers shall withstand without damage a 1000 V common-mode impulse of either polarity (E_{cm} as indicated in figure 23-25). The shape of the impulse shall be 0.3/50 μs (300 ns virtual front time, 50 μs virtual time of half value), as defined in IEC 60.

23.5.1.3.6 Receiver frequency tolerance

The receive feature shall properly receive incoming data with a ternary symbol rate within the range 25.000 MHz ± 0.01%.

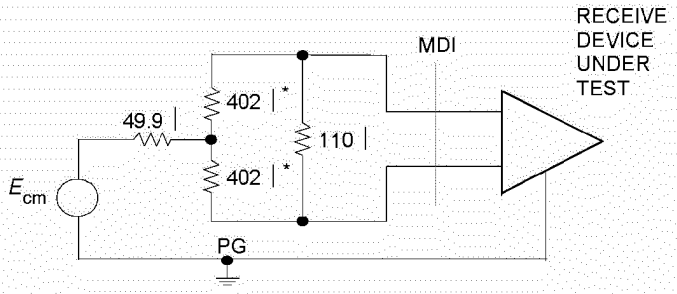


Figure 23-25—Common-mode impulse test circuit

23.5.2 Power consumption

After 100 ms following PowerOn, the current drawn by the PHY shall not exceed 0.75 A when powered through the MII.

The PHY shall be capable of operating from all voltage sources allowed by clause 22, including those current limited to 0.75 A, as supplied by the DTE or repeater through the resistance of all permissible MII cables.

The PHY shall not introduce extraneous signals on the MII control circuits during normal power-up and power-down.

While in power-down mode the PHY is not required to meet any of the 100BASE-T4 performance requirements.

23.6 Link segment characteristics

23.6.1 Cabling

Cabling and installation practices generally suitable for use with this standard appear in ISO/IEC 11801: 1995. Exceptions, notes, and additional requirements are as listed below.

a) 100BASE-T4 uses a star topology. Horizontal cabling is used to connect PHY entities.
b) 100BASE-T4 is an ISO/IEC 11801: 1995 class C application, with additional installation requirements and transmission parameters specified in 23.6.2 through 23.6.4. The highest fundamental frequency transmitted by 8B6T coding is 12.5 MHz. The aggregate data rate for three pairs using 8B6T coding is 100 Mb/s.
c) 100BASE-T4 shall use four pairs of balanced cabling, Category 3 or better, with a nominal characteristic impedance of 100 Ω.
d) When using Category 3 cable for the link segment, clause 23 recommends, but does not require, the use of Category 4 or better connecting hardware, patch cords and jumpers. The use of Category 4 or better connecting hardware increases the link segment composite NEXT loss, composite ELFEXT loss and reduces the link segment insertion loss. This lowers the link segment crosstalk noise, which in turn decreases the probability of errors.
e) The use of shielded cable is outside the scope of this standard.

23.6.2 Link transmission parameters

Unless otherwise specified, link segment testing shall be conducted using source and load impedances of 100 | .

23.6.2.1 Insertion loss

The insertion loss of a simplex link segment shall be no more than 12 dB at all frequencies between 2 and 12.5 MHz. This consists of the attenuation of the twisted pairs, connector losses, and reflection losses due to impedance mismatches between the various components of the simplex link segment. The insertion loss specification shall be met when the simplex link segment is terminated in source and load impedances that satisfy 23.5.1.2.4 and 23.5.1.3.3.

NOTE—The loss of PVC-insulated cable exhibits significant temperature dependence. At temperatures greater than 40 °C, it may be necessary to use a less temperature-dependent cable, such as many Fluorinated Ethylene Propylene (FEP), Polytetrafluoroethylene (PTFE), or Perfluoroalkoxy (PFA) plenum-rated cables.

23.6.2.2 Differential characteristic impedance

The magnitude of the differential characteristic impedance of a 3 m length of twisted pair used in a simplex link shall be between 85 | and 115 | for all frequencies between 2 MHz and 12.5 MHz.

23.6.2.3 Coupling parameters

In order to limit the noise coupled into a simplex link segment from adjacent simplex link segments, Near-End Crosstalk (NEXT) loss and Equal Level Far-End Crosstalk (ELFEXT) loss are specified for each simplex link segment. In addition, since three simplex links (TX_D1, Bl_D3, and Bl_D4) are used to send data between PHYs and one simplex link (RX_D2) is used to carry collision information as specified in 23.1.4, Multiple-Disturber NEXT loss and Multiple-Disturber ELFEXT loss are also specified.

23.6.2.3.1 Differential Near-End Crosstalk (NEXT) loss

The differential Near-End Crosstalk (NEXT) loss between two simplex link segments is specified in order to ensure that collision information can be reliably received by the PHY receiver. The NEXT loss between each of the three data carrying simplex link segments and the collision sensing simplex link segment shall be at least $24.5 - 15\times\log_{10}(f/12.5)$ (where f is the frequency in MHz) over the frequency range 2.0 MHz to 12.5 MHz.

23.6.2.3.2 Multiple-disturber NEXT (MDNEXT) loss

Since three simplex links are used to send data between PHYs and one simplex link is used to carry collision information, the NEXT noise that is coupled into the collision, sensing simplex link segment is from multiple (three) signal sources, or disturbers. The MDNEXT loss between the three data carrying simplex link segments and the collision sensing simplex link segment shall be at least $21.4 - 15\times\log_{10}(f/12.5)$ dB (where f is the frequency in MHz) over the frequency range 2.0 to 12.5 MHz. Refer to 12.7.3.2 and Appendix A3, Example Crosstalk Computation for Multiple Disturbers, for a tutorial and method for estimating the MDNEXT loss for an n-pair cable.

23.6.2.3.3 Equal Level Far-End Crosstalk (ELFEXT) loss

Equal Level Far-End Crosstalk (ELFEXT) loss is specified in order to limit the crosstalk noise at the far end of a simplex link segment to meet the BER objective specified in 23.1.2 and the noise specifications of 23.6.3. Far-End Crosstalk (FEXT) noise is the crosstalk noise that appears at the far end of a simplex link segment which is coupled from an adjacent simplex link segment with the noise source (transmitters) at the near end. ELFEXT loss is the ratio of the data signal to FEXT noise at the output of a simplex link segment (receiver input). To limit the FEXT noise from adjacent simplex link segments, the ELFEXT loss between two data car-

rying simplex link segments shall be greater than $23.1 - 20\times\log_{10}(f/12.5)$ dB (where f is the frequency in MHz) over the frequency range 2.0 MHz to 12.5 MHz. ELFEXT loss at frequency f and distance l is defined as

$$\text{ELFEXT\_Loss}(f,l) = 20 \times \log_{10}\left(\frac{V_{pds}}{V_{pcn}}\right) - \text{SLS\_Loss (dB)}$$

where

V_{pds} is the peak voltage of disturbing signal (near-end transmitter)
V_{pcn} is the peak crosstalk noise at the far end of disturbed simplex link segment
SLS_Loss is the insertion loss of the disturbing simplex link segment

23.6.2.3.4 Multiple-disturber ELFEXT (MDELFEXT) loss

Since three simplex links are used to transfer data between PHYs, the FEXT noise that is coupled into an data carrying simplex link segment is from multiple (two) signal sources, or disturbers. The MDELFEXT loss between a data carrying simplex link segment and the other two data carrying simplex link segments shall be greater than $20.9 - 20\times\log_{10}(f/12.5)$ (where f is the frequency in MHz) over the frequency range 2.0 MHz to 12.5 MHz. Refer to 12.7.3.2 and Appendix A3, Example Crosstalk Computation for Multiple Disturbers, for a tutorial and method for estimating the MDELFEXT loss for an n-pair cable.

23.6.2.4 Delay

Since T4 sends information over three simplex link segments in parallel, the absolute delay of each and the differential delay are specified to comply with network round-trip delay limits and ensure the proper decoding by receivers, respectively.

23.6.2.4.1 Maximum link delay

The propagation delay of a simplex link segment shall not exceed 570 ns at all frequencies between 2.0 MHz and 12.5 MHz.

23.6.2.4.2 Maximum link delay per meter

The propagation delay per meter of a simplex link segment shall not exceed 5.7 ns/m at all frequencies between 2.0 MHz and 12.5 MHz.

23.6.2.4.3 Difference in link delays

The difference in propagation delay, or skew, under all conditions, between the fastest and the slowest simplex link segment in a link segment shall not exceed 50 ns at all frequencies between 2.0 MHz and 12.5 MHz. It is a further functional requirement that, once installed, the skew between all pair combinations due to environmental conditions shall not vary more than ± 10 ns, within the above requirement.

23.6.3 Noise

The noise level on the link segments shall be such that the objective error rate is met. The noise environment consists generally of two primary contributors: self-induced near-end crosstalk, which affects the ability to detect collisions, and far-end crosstalk, which affects the signal-to-noise ratio during packet reception.

23.6.3.1 Near-End Crosstalk

The MDNEXT (Multiple-Disturber Near-End Crosstalk) noise on a link segment depends on the level of the disturbing signals on pairs TX_D1, BI_D3, and BI_D4, and the crosstalk loss between those pairs and the disturbed pair, RX_D2.

The MDNEXT noise on a link segment shall not exceed 325 mVp.

This standard is compatible with the following assumptions:

a) Three disturbing pairs with 99th percentile pair-to-pair NEXT loss greater than 24.5 dB at 12.5 MHz (i.e., Category 3 cable).
b) Six additional disturbers (2 per simplex link) representing connectors at the near end of the link segment with 99th percentile NEXT loss greater than 40 dB at 12.5 MHz (i.e., Category 3 connectors installed in accordance with 23.6.4.1).
c) All disturbers combined according to the MDNEXT Monte Carlo procedure outlined in Appendix A3, Example Crosstalk Computation for Multiple Disturbers.

The MDNEXT noise is defined using three maximum level 100BASE-T4 transmitters sending uncorrellated continuous data sequences while attached to the simplex link segments TX_D1, BI_D3, and BI_D4 (disturbing links), and the noise measured at the output of a filter connected to the simplex link segment RX_D2. (disturbed link). Each continuous data sequence is a pseudo-random bit pattern having a length of at least 2047 bits that has been coded according to the 8B6T coding rules in 23.2.1.2. The filter is the 100BASE-T4 Transmit Test Filter specified in 23.5.1.2.3.

23.6.3.2 Far-End Crosstalk

The MDFEXT (Multiple-Disturber Far-End Crosstalk) noise on a link segment depends on the level of the disturbing signals on pairs TX_D1, BI_D3, and BI_D4, and the various crosstalk losses between those pairs.

The MDFEXT noise on a link segment shall not exceed 87 mVp.

This standard is compatible with the following assumptions:

a) Two disturbing pairs with 99th percentile ELFEXT (Equal Level Far-End Crosstalk) loss greater than 23 dB at 12.5 MHz.
b) Nine additional disturbers (three per simplex link) representing connectors in the link segment with 99th percentile NEXT loss greater than 40 dB at 12.5 MHz.
c) All disturbers combined according to the MDNEXT Monte Carlo procedure outlined in Appendix A3, Example Crosstalk Computation for Multiple Disturbers.

The MDFEXT noise is defined using two maximum level 100BASE-T4 transmitters sending uncorrellated continuous data sequences while attached to two simplex link segments (disturbing links) and the noise measured at the output of a filter connected to the far end of a third simplex link segment (disturbed link). Each continuous data sequence is a pseudo-random bit pattern having a length of at least 2047 bits that has been coded according to the 8B6T coding rules in 23.2.1.2. The filter is the 100BASE-T4 Transmit Test Filter specified in 23.5.1.2.3.

23.6.4 Installation practice

23.6.4.1 Connector installation practices

The amount of untwisting in a pair as a result of termination to connecting hardware should be no greater than 25 mm (1.0 in) for Category 3 cables. This is the same value recommended in ISO/IEC 11801: 1995 for Category 4 connectors.

23.6.4.2 Disallow use of Category 3 cable with more than four pairs

Jumper cables, or horizontal runs, made from more than four pairs of Category 3 cable are not allowed.

23.6.4.3 Allow use of Category 5 jumpers with up to 25 pairs

Jumper cables made from up to 25 pairs of Category 5 cable, for the purpose of mass-terminating port connections at a hub, are allowed. Such jumper cables, if used, shall be limited in length to no more than 10 m total.

23.7 MDI specification

This clause defines the MDI. The link topology requires a crossover function between PMAs. Implementation and location of this crossover are also defined in this clause.

23.7.1 MDI connectors

Eight-pin connectors meeting the requirements of section 3 and figures 1-5 of IEC 603-7: 1990 shall be used as the mechanical interface to the balanced cabling. The plug connector shall be used on the balanced cabling and the jack on the PHY. These connectors are depicted (for informational use only) in figures 23-26 and 23-27. The table 23-6 shows the assignment of PMA signals to connector contacts for PHYs with and without an internal crossover.

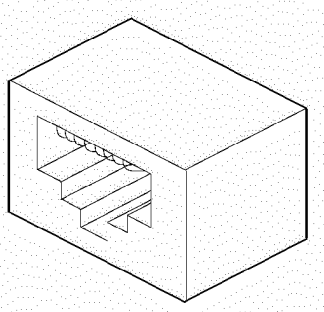


Figure 23-26—MDI connector

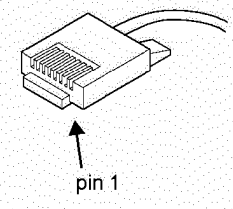


Figure 23-27—Balanced cabling connector

23.7.2 Crossover function

It is a functional requirement that a crossover function be implemented in every link segment. The crossover function connects the transmitters of one PHY to the receivers of the PHY at the other end of the link segment. Crossover functions may be implemented internally to a PHY or elsewhere in the link segment. For a PHY that does not implement the crossover function, the MDI labels in the last column of table 23-4 refer to its own internal circuits (second column). For PHYs that do implement the internal crossover, the MDI labels in the last column of table 23-4 refer to the internal circuits of the remote PHY of the link segment.

Table 23-6—MDI connection and labeling requirements

Contact	PHY without internal crossover (recommended for DTE) internal PMA signals	PHY with internal crossover (recommended for repeater) internal PMA signals	MDI labeling requirement
1	TX_D1+	RX_D2+	TX_D1+
2	TX_D1–	RX_D2–	TX_D1–
3	RX_D2+	TX_D1+	RX_D2+
4	BI_D3+	BI_D4+	BI_D3+
5	BI_D3–	BI_D4–	BI_D3–
6	RX_D2–	TX_D1–	RX_D2–
7	BI_D4+	BI_D3+	BI_D4+
8	BI_D4–	BI_D3–	BI_D4–

Additionally, the MDI connector for a PHY that implements the crossover function shall be marked with the graphical symbol "X". Internal and external crossover functions are shown in figure 23-28. The crossover function specified here for pairs TX_D1 and RX_D2 is compatible with the crossover function specified in 14.5.2 for pairs TD and RD.

When a link segment connects a DTE to a repeater, it is recommended the crossover be implemented in the PHY local to the repeater. If both PHYs of a link segment contain internal crossover functions, an additional external crossover is necessary. It is recommended that the crossover be visible to an installer from one of the PHYs. When both PHYs contain internal crossovers, it is further recommended in networks in which the topology identifies either a central backbone segment or a central repeater that the PHY furthest from the central element be assigned the external crossover to maintain consistency.

Implicit implementation of the crossover function within a twisted-pair cable, or at a wiring panel, while not expressly forbidden, is beyond the scope of this standard.

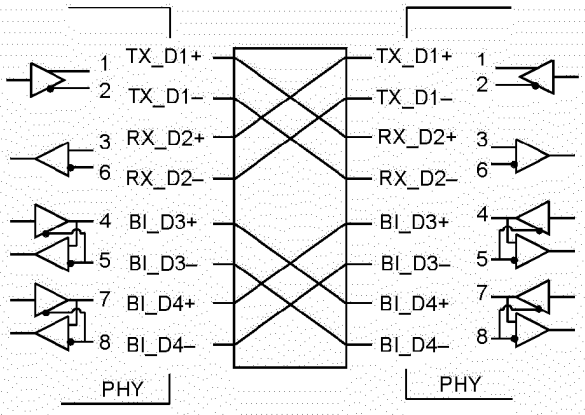
23.8 System considerations

The repeater unit specified in clause 27 forms the central unit for interconnecting 100BASE-T4 twisted-pair links in networks of more than two nodes. It also provides the means for connecting 100BASE-T4 twisted-pair links to other 100 Mb/s baseband segments. The proper operation of a CSMA/CD network requires that network size be limited to control round-trip propagation delay as specified in clause 29.

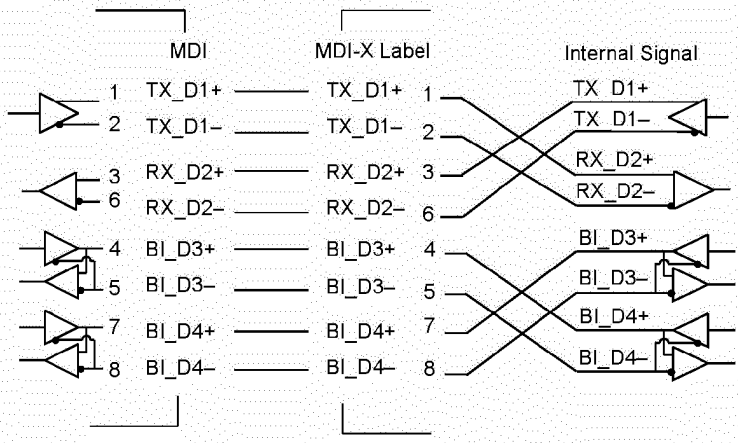
23.9 Environmental specifications

23.9.1 General safety

All equipment meeting this standard shall conform to IEC 950: 1991.



a) Two PHYs with external crossover function



b) PHY with internal crossover function

Figure 23-28—Crossover function

23.9.2 Network safety

This clause sets forth a number of recommendations and guidelines related to safety concerns; the list is neither complete nor does it address all possible safety issues. The designer is urged to consult the relevant local, national, and international safety regulations to ensure compliance with the appropriate requirements.

LAN cable systems described in this clause are subject to at least four direct electrical safety hazards during their installation and use. These hazards are as follows:

a) Direct contact between LAN components and power, lighting, or communications circuits
b) Static charge buildup on LAN cables and components
c) High-energy transients coupled onto the LAN cable system
d) Voltage potential differences between safety grounds to which various LAN components are connected

Such electrical safety hazards must be avoided or appropriately protected against for proper network installation and performance. In addition to provisions for proper handling of these conditions in an operational system, special measures must be taken to ensure that the intended safety features are not negated during installation of a new network or during modification or maintenance of an existing network.

23.9.2.1 Installation

It is a mandatory functional requirement that sound installation practice, as defined by applicable local codes and regulations, be followed in every instance in which such practice is applicable.

23.9.2.2 Grounding

Any safety grounding path for an externally connected PHY shall be provided through the circuit ground of the MII connection.

WARNING—It is assumed that the equipment to which the PHY is attached is properly grounded, and not left floating nor serviced by a "doubly insulated, ac power distribution system." The use of floating or insulated equipment, and the consequent implications for safety, are beyond the scope of this standard.

23.9.2.3 Installation and maintenance guidelines

It is a mandatory functional requirement that, during installation and maintenance of the cable plant, care be taken to ensure that noninsulated network cable conductors do not make electrical contact with unintended conductors or ground.

23.9.2.4 Telephony voltages

The use of building wiring brings with it the possibility of wiring errors that may connect telephony voltages to 100BASE-T4 equipment. Other than voice signals (which are low voltage), the primary voltages that may be encountered are the "battery" and ringing voltages. Although there is no universal standard, the following maximums generally apply.

Battery voltage to a telephone line is generally 56 Vdc applied to the line through a balanced 400 | source impedance.

Ringing voltage is a composite signal consisting of an ac component and a dc component. The ac component is up to 175 V peak at 20 Hz to 60 Hz with a 100 | source resistance. The dc component is 56 Vdc with a 300 | to 600 | source resistance. Large reactive transients can occur at the start and end of each ring interval.

Although 100BASE-T4 equipment is not required to survive such wiring hazards without damage, application of any of the above voltages shall not result in any safety hazard.

NOTE—Wiring errors may impose telephony voltages differentially across 100BASE-T4 transmitters or receivers. Because the termination resistance likely to be present across a receiver's input is of substantially lower impedance than an off-hook telephone instrument, receivers will generally appear to the telephone system as off-hook telephones. Therefore, full-ring voltages will be applied for only short periods. Transmitters that are coupled using transformers will similarly appear like off-hook telephones (though perhaps a bit more slowly) due to the low resistance of the transformer coil.

23.9.3 Environment

23.9.3.1 Electromagnetic emission

The twisted-pair link shall comply with applicable local and national codes for the limitation of electromagnetic interference.

23.9.3.2 Temperature and humidity

The twisted-pair link is expected to operate over a reasonable range of environmental conditions related to temperature, humidity, and physical handling (such as shock and vibration). Specific requirements and values for these parameters are considered to be beyond the scope of this standard.

It is recommended that manufacturers indicate in the literature associated with the PHY the operating environmental conditions to facilitate selection, installation, and maintenance.

23.10 PHY labeling

It is recommended that each PHY (and supporting documentation) be labeled in a manner visible to the user with at least these parameters:

a) Data rate capability in Mb/s
b) Power level in terms of maximum current drain (for external PHYs)
c) Any applicable safety warnings

See also 23.7.2.

23.11 Timing summary

23.11.1 Timing references

All MII signals are defined (or corrected to) the DTE end of a zero length MII cable.

NOTE—With a finite length MII cable, TX_CLK appears in the PHY one cable propagation delay *earlier* than at the MII. This advances the transmit timing. Receive timing is retarded by the same amount.

The phrase *adjusted for pair skew*, when applied to a timing reference on a particular pair, means that the designated timing reference has been adjusted by adding to it the difference between the time of arrival of preamble on the latest of the three receive pairs and the time of arrival of preamble on that particular pair.

PMA_UNITDATA request

Figures 23-29, 30, 31, and 32. The implementation of this abstract message is not specified. Conceptually, this is the time at which the PMA has been given full knowledge and use of the ternary symbols to be transmitted.

PMA_UNITDATA.indicate

Figure 23-33. The implementation of this abstract message is not specified. Conceptually, this is the time at which the PCS has been given full knowledge and use of the ternary symbols received.

WAVEFORM

Figure 23-29. Point in time at which output waveform has moved 1/2 way from previous nominal output level to present nominal output level.

TX_EN

Figure 23-30. First rising edge of TX_CLK following the rising edge of TX_EN.

NOT_TX_EN

Figures 23-31 and 32. First rising edge of TX_CLK following the falling edge of TX_EN.

CRS

Figure 23-33. Rising edge of CRS.

CARRIER_STATUS

Figure 23-33. Rising edge of carrier_status.

NOT_CARRIER_STATUS

Figure 23-34. Falling edge of carrier_status.

RX_DV

No figure. First rising edge of RX_CLK following rising edge of RX_DV.

COL

No figure. Rising edge of COL signal at MII.

NOT_COL

No figure. Falling edge of COL signal at MII.

PMA_ERROR

No figure. Time at which rxerror_status changes to ERROR.

23.11.2 Definitions of controlled parameters

PMA_OUT

Figure 23-29. Time between PMA_UNITDATA request (tx_code_vector) and the WAVEFORM timing reference for each of the three transmit channels TX_D1, BI_D3, or BI_D4.

TEN_PMA

Figures 23-30, 31, and 32. Time between TX_EN timing reference and MA_UNITDATA request (tx_code_vector).

TEN_CRS

Figure 23-30. Time between TX_EN timing reference and the loopback of TX_EN to CRS as measured at the CRS timing reference point.

NOT_TEN_CRS

Figures 23-31 and 32. Time between NOT_TX_EN timing reference and the loopback of TX_EN to CRS as measured at the NOT_CRS timing reference point. In the event of a collision (COL is raised at any point during a packet) the minimum time for NOT_TEN_CRS may optionally be as short as 0.

RX_PMA_CARRIER

Figure 23-33. Time between the WAVEFORM timing reference, adjusted for pair skew, of first pulse of a normal preamble (or first pulse of a preamble preceded by a link test pulse or a partial link test pulse) and the CARRIER_STATUS timing reference.

RX_CRS

Figure 23-33. Time between the WAVEFORM timing reference, adjusted for pair skew, of first pulse of a normal preamble (or first pulse of a preamble preceded by a link test pulse or a partial link test pulse) and the CRS timing reference.

NOTE—The input waveform used for this test is an ordinary T4 preamble, generated by a compliant T4 transmitter. As such, the delay between the first and third pulses of the preamble (which are used by the carrier sense logic) is very nearly 80 ns.

RX_NOT_CRS

For a data packet, the time between the WAVEFORM timing reference, adjusted for pair skew, of the first pulse of eop1, and the de-assertion of CRS. For a collision fragment, the time between the WAVEFORM timing reference, adjusted for pair skew, of the ternary symbol on pair TX_D2, which follows the last ternary data symbol received on pair RX_D2, and the de-assertion of CRS.

Both are limited to the same value. For a data packet, detection of the six ternary symbols of eopo1 is accomplished in the PCS layer. For a collision fragment, detection of the concluding seven ternary zeroes is accomplished in the PMA layer, and passed to the PCS in the form of the carrier_status indication.

FAIRNESS

The difference between RX_NOT_CRS at the conclusion of one packet and RX_CRS on a subsequent packet. The packets used in this test may arrive with an IPG anywhere in the range of 80 to 160.

RX_PMA_DATA

Figure 23-33. Time between the WAVEFORM timing reference, adjusted for pair skew, of first pulse of a normal preamble (or first pulse of a preamble preceded by a link test pulse or a partial link test pulse) and the particular PMA_UNITDATA.indicate that transfers to the PCS the first ternary symbol of the first 6T code group from receive pair BI_D3.

EOP_CARRIER_STATUS

Figure 23-34. For a data packet, the time between the WAVEFORM timing reference, adjusted for pair skew, of first pulse of eop1 and the NOT_CARRIER_STATUS timing reference.

EOC_CARRIER_STATUS

Figure 23-35. In the case of a colliding packet, the time between the WAVEFORM timing reference, adjusted for pair skew, of the ternary symbol on pair RX_D2, which follows the last ternary data symbol received on pair RX_D2 and the NOT_CARRIER_STATUS timing reference.

RX_RXDV

No figure. Time between WAVEFORM timing reference, adjusted for pair skew, of first pulse of a normal preamble (or first pulse of a preamble preceded by a link test pulse or a partial link test pulse) and the RX_DV timing reference.

RX_PMA_ERROR

No figure. In the event of a preamble in error, the time between the WAVEFORM timing reference adjusted for pair skew, of first pulse of that preamble (or first pulse of the preamble preceded by a link test pulse or a partial link test pulse), and the PMA_ERROR timing reference.

RX_COL

No figure. In the event of a collision, the time between the WAVEFORM timing reference adjusted for pair skew, of first pulse of a normal preamble (or first pulse of a preamble preceded by a link test pulse or a partial link test pulse), and the COL timing reference.

RX_NOT_COL

No figure. In the event of a collision in which the receive signal stops before the locally transmitted signal, the time between the WAVEFORM timing reference adjusted for pair skew, of the ternary symbol on pair RX_D2, which follows the last ternary data symbol received on pair RX_D2 and the NOT_COL timing reference point.

TX_NOT_COL

No figure. In the event of a collision in which the locally transmitted signal stops before the received signal, the time between the NOT_TX_EN timing reference and the loopback of TX_EN to COL as measured at the NOT_COL timing reference point.

TX_SKEW

Greatest absolute difference between a) the waveform timing reference of the first pulse of a preamble as measured on output pair TX_D1; b) the waveform timing reference of the first pulse of a preamble as measured on output pair BI_D3; and c) the waveform timing reference of the first pulse of a preamble as measured on output pair BI_D4. Link test pulses, if present during the measurement, must be separated from the preamble by at least 100 ternary symbols.

CRS_PMA_DATA

Time between the timing reference for CARRIER STATUS and the transferral, via PMA_UNITDATA.indicate, of the first ternary symbol of the 6T code group marked DATA1 in figure 23-6.

COL_to_BI_D3/D4_OFF

No figure. In the case of a colliding packet, the time between the WAVE FORM timing reference, adjusted for pair skew, of the first pulse of preamble (or the first pulse of the preamble preceded by a link test pulse or a partial link test pulse) on RX_D2, and the first ternary zero transmitted on BI_D3 and on BI_D4.

NOTE—Subclause 23.4.1.2 mandates that transmission on pairs BI_D3 and BI_D4 be halted in the event of a collision.

23.11.3 Table of required timing values

While in the LINK_PASS state, each PHY timing parameter shall fall within the Low and High limits listed in table 23-7. All units are in bit times. A bit time equals 10 ns.

Table 23-7—Required timing values

Controlled parameter	Low limit (bits)	High limit (bits)	Comment
PMA_OUT	1	9.5	
TEN_PMA + PMA_OUT	7	17.5	
TEN_CRS	0	+4	
NOT_TEN_CRS	0	36	
RX_PMA_CARRIER	0	15.5	
RX_CRS	0	27.5	
RX_NOT_CRS	0	51.5	
FAIRNESS	0	28	
RX_PMA_DATA	67	90.5	
EOP_CARRIER_STATUS	51	74.5	
EOC_CARRIER_STATUS	3	50.5	
RX_RXDV	81	114.5	
RX_PMA_ERROR	RX_PMA_DATA	RX_PMA_DATA + 20	Allowed limits equal the actual RX_PMA_DATA time for the device under test plus from 0 to 20 BT
RX_COL	0	27.5	SAME AS RX_CRS
RX_NOT_COL	0	51.5	SAME AS RX_NOT_CRS
TX_NOT_COL	0	36	
TX_SKEW	0	0.5	
CRS_PMA_DATA	0	78.5	
COL_to_BI_D3/D4_OFF	0	40	

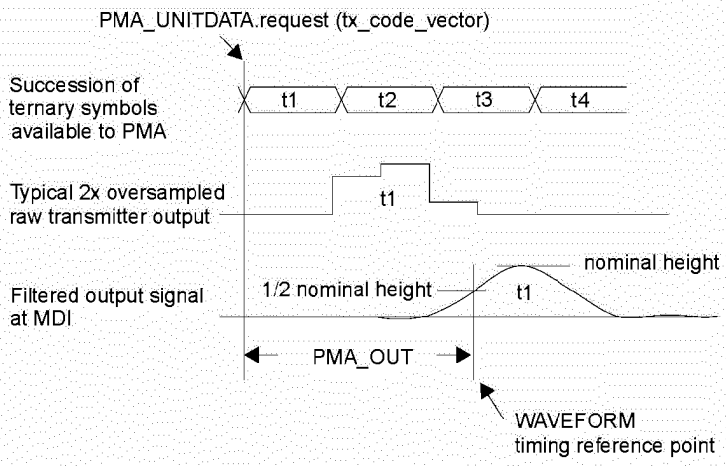


Figure 23-29—PMA TRANSMIT timing while tx_code_vector = DATA

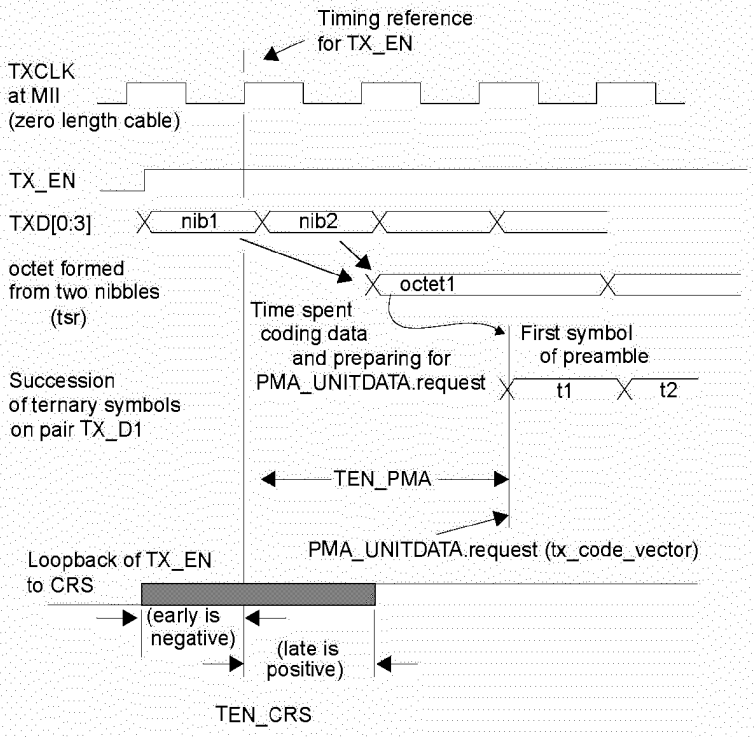


Figure 23-30—PCS TRANSMIT timing at start of packet

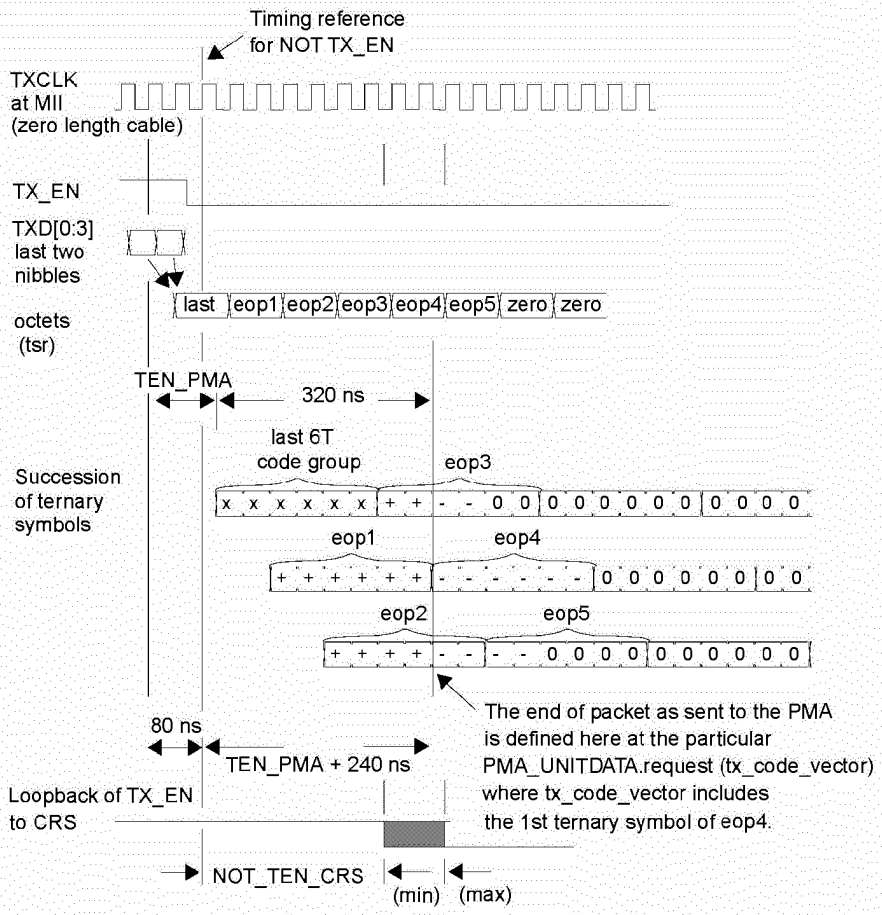


Figure 23-31—PCS TRANSMIT timing end of normal packet

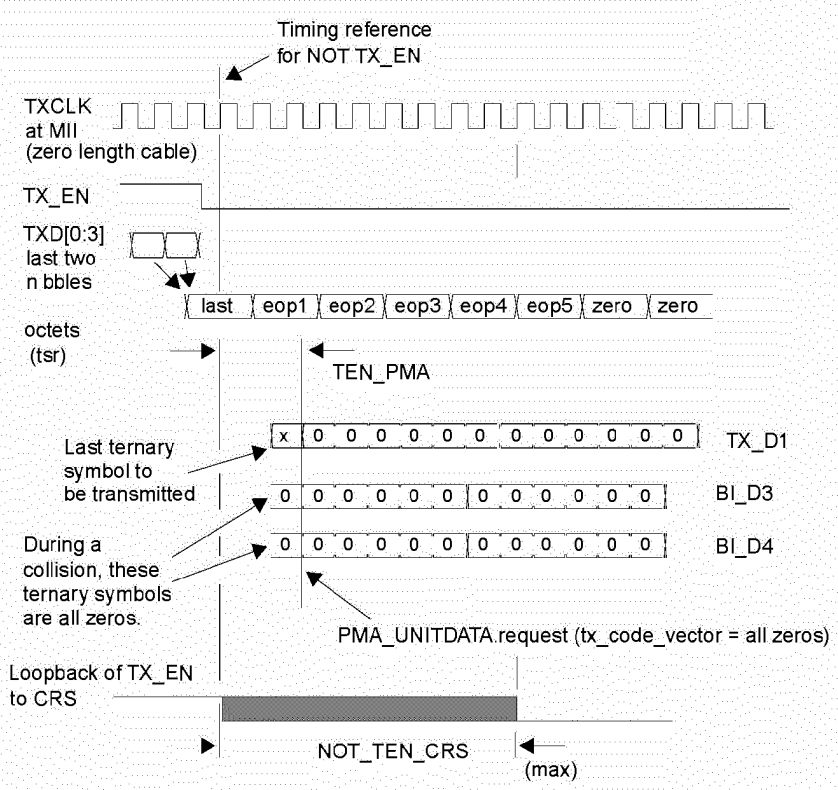


Figure 23-32—PCS TRANSMIT timing end of colliding packet

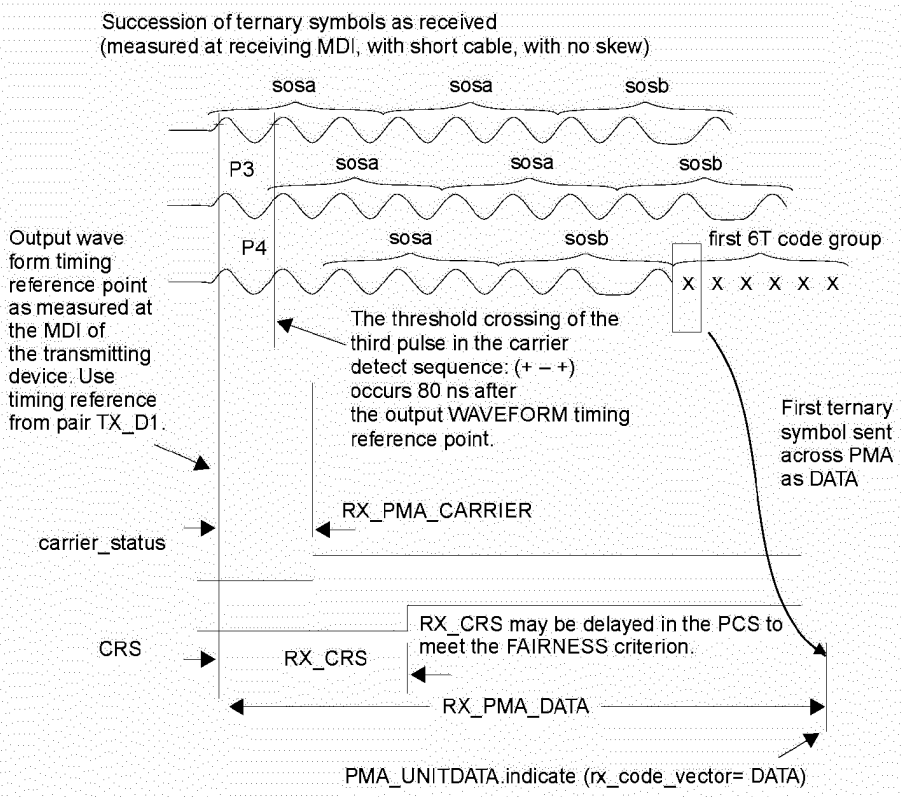
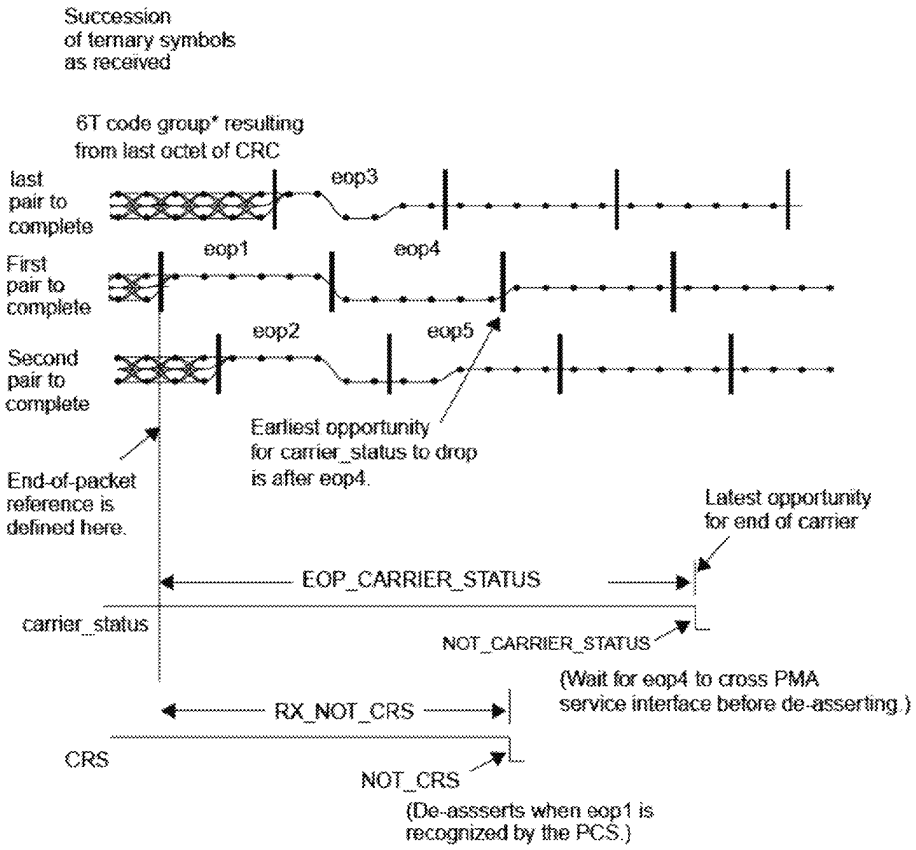


Figure 23-33—PMA RECEIVE timing start of packet



*RX_DV de-asserts after sending the last nibble of this decoded octet across the MII. CRS may de-assert prior to that time.

Figure 23-34—PMA RECEIVE timing end of normal packet

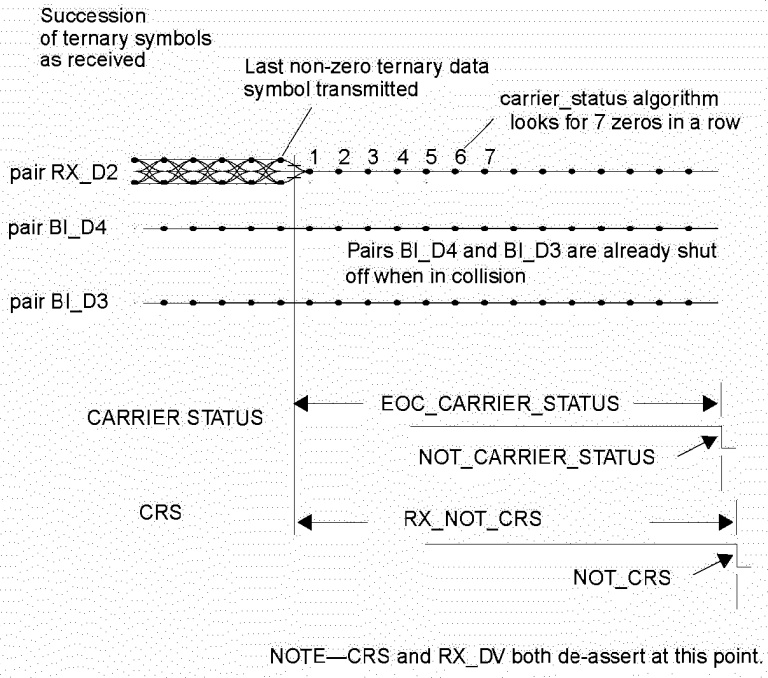


Figure 23-35—PMA RECEIVE timing end of colliding packet

23.12 Protocol Implementation Conformance Statement (PICS) proforma for clause 23, Physical Coding Sublayer (PCS), Physical Medium Attachment (PMA) sublayer and baseband medium, type 100BASE-T4[28]

23.12.1 Introduction

The supplier of a protocol implementation that is claimed to conform to clause 23, Physical Coding Sublayer (PCS), Physical Medium Attachment (PMA) sublayer and baseband medium, type 100BASE-T4, shall complete the following Protocol Implementation Conformance Statement (PICS) proforma.

A detailed description of the symbols used in the PICS proforma, along with instructions for completing the PICS proforma, can be found in clause 21.

23.12.2 Identification

23.12.2.1 Implementation identification

Supplier	
Contact point for enquiries about the PICS	
Implementation Name(s) and Version(s)	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Names(s)	
NOTES 1—Only the first three items are required for all implementations; other information may be completed as appropriate in meeting the requirements for the identification. 2—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

23.12.2.2 Protocol summary

Identification of protocol standard	IEEE Std 802.3, 1998 Edition, clause 23, Physical Coding Sublayer (PCS), Physical Medium Attachment (PMA) sublayer and baseband medium, type 100BASE-T4
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required? No [ ] Yes [ ] (See clause 21; the answer Yes means that the implementation does not conform to IEEE Std 802.3, 1998 Edition.)	
Date of Statement	

[28] *Copyright release for PICS proformas* Users of this standard may freely reproduce the PICS proforma in this annex so that it can be used for its intended purpose and may further publish the completed PICS.

23.12.3 Major capabilities/options

Item	Feature	Subclause	Status	Support	Value/Comment
*MII	Exposed MII interface	23.1.5.3	O		Devices supporting this option must also support the PCS option
*PCS	PCS functions	23.1.5.2	O		Required for integration with DTE or MII
*PMA	Exposed PMA service interface	23.1.5.2	O		Required for integration into symbol level repeater core
*XVR	Internal wiring crossover	23.7.2	O		Usually implemented in repeater, usually not in DTE
*NWY	Support for optional Auto-Negotiation (clause 28)	23.1.5.6	O		Required if Auto-Negotiation is implemented
*INS	Installation / cable		O		Items marked with INS include installation practices and cable specifications not applicable to a PHY manufacturer

23.12.4 PICS proforma tables for the Physical Coding Sublayer (PCS), Physical Medium Attachment (PMA) sublayer and baseband medium, type 100BASE-T4

23.12.4.1 Compatibility considerations

Item	Feature	Subclause	Status	Support	Value/Comment
CCO-1	Compatibility at the MDI	23.1.5.1	M		

23.12.4.2 PCS Transmit functions

Item	Feature	Subclause	Status	Support	Value/Comment
PCT-1	PCS Transmit function	23.2.1.2	PCS:M		Complies with state diagram figure 23-8
PCT-2	Data encoding	23.2.1.2	PCS:M		8B6T with DC balance encoding rules
PCT-3	Order of ternary symbol transmission	Appendix 23-A	PCS:M		Leftmost symbol of each 6T code group first

23.12.4.3 PCS Receive functions

Item	Feature	Subclause	Status	Support	Value/Comment
PCR1	PCS Receive function	23.2.1.3	PCS:M		Complies with state diagram figure 23-9
PCR2	Value of RXD<3:0> while RXDV is de-asserted	23.2.1.3	PCS:M		All zeroes
PCR3	Data decoding	23.2.1.3	PCS:M		8B6T with error detecting rules
PCR4	Value of dc_balance_error, eop_error and codeword_error at times other than those specified in the error detecting rules.	23.2.1.3	PCS:M		OFF
PCR5	Codeword_error indication sets RX_ER when	23.2.1.3	PCS:M		During transfer of both affected data nibbles across the MII
PCR6	Dc_balance_error sets RX_ER when	23.2.1.3	PCS:M		During transfer of both affected nibbles across the MII
PCR7	Eop_error sets RX_ER when	23.2.1.3	PCS:M		During transfer of last decoded data nibble across the MII
PCR8	Action taken if carrier_status is truncated dur to early de-assertion of carrier_status	23.2.1.3	PCS:M		Assert RX_ER, and then de-assert RX_DV

23.12.4.4 Other PCS functions

Item	Feature	Subclause	Status	Support	Value/Comment
PCO1	PCS Reset function executed when	23.2.1.1	PCS:M		Power-on, or the receipt of a reset request from the management entity
PCO2	PCS Error Sense function	23.2.1.4	PCS:M		Complies with state diagram figure 23-10
PCO3	Signaling of RX_ER to MII	23.2.1.4	PCS:M		Before last nibble of clause 4 MAC frame has passed across MII
PCO4	Timing of rxerror_status	23.2.1.4	PCS:M		Causes RX_ER to appear on the MII no later than last nibble of first data octet
PCO5	PCS Carrier Sense function	23.2.1.5	PCS:M		Controls MII signal CRS according to rules in 23.2.1.5
PCO6	MII signal COL is asserted when	23.2.1.6	PCS:M		Upon detection of a PCS collision
PCO7	At other times COL remains	23.2.1.6	PCS:M		De-asserted
PCO8	Loopback implemented in accordance with 22.4.1.2	23.2.2.4	PCS:M		Redundantly specified in 22.2.4.1.2

Item	Feature	Subclause	Status	Support	Value/Comment
PCO9	No spurious signals emitted on the MDI during or after power down	23.2.2.4	M		
PCO10	PMA frame structure	23.2.3	M		Conformance to figure 23-6
PCO11	PMA_UNITDATA messages	23.2.3	PMA:M		Must have a clock for both directions

23.12.4.5 PCS state diagram variables

Item	Feature	Subclause	Status	Support	Value/Comment
PCS1	Timing of eop adjusted such that the last nibble sent across the MII with RX_DV asserted is	23.2.4.1.5	PCS:M		Last nibble of last decoded data octet in a packet
PCS2	Transmission of octets on the three transmit pairs	23.2.4.1.8	PCS:M		Transmission order is: TX_D1, then BI_D3, and then BI_D4
PCS3	Value of tsr during first 16 TX_CLK cycles after TX_EN is asserted	23.2.4.1.11	PCS:M		sosa, sosa, sosa, sosa, sosa, sosa, sosa, sosa, sosa, sosa, sosb, sosb, sosb, sosb, sosb, sosb
PCS4	Value of tsr during first 10 TX_CLK cycles after TX_EN is de-asserted	23.2.4.1.11	PCS:M		eop1, eop1, eop2, eop2, eop3, eop3, eop4, eop4, eop5, eop5
PCS5	TX_ER causes transmission of	23.2.4.1.11	PCS:M		bad_code
PCS6	TX_ER received during the first 16 TX_CLK cycles causes	23.2.4.1.11	PCS:M		Transmission of **bad_code** during 17th and 18th clock cycles
PCS7	Action taken in event TX_EN falls on an odd nibble boundary	23.2.4.1.11	PCS:M		Extension of TX_EN by one TX_CLK cycle, and transmission of bad_code
PCS8	Transmission when TX_EN is not asserted	23.2.4.1.11	PCS:M		zero_code
PCS9	TX_CLK generated synchronous to	23.2.4.1.12	PCS:M		tw1_timer

23.12.4.6 PMA service interface

Item	Feature	Subclause	Status	Support	Value/Comment
PMS1	Continuous generation of PMA_TYPE	23.3.1.2	M		
PMS2	Generation of PMA_UNITDATA.indicate (DATA) messages	23.3.3.2	M		synchronous with data received at the MDI
PMS3	Generation of PMA_CARRIER.indicate message	23.3.4.2	M		ON/OFF
PMS4	Generation of PMA_LINK.indicate message	23.3.5.2	M		FAIL/READY/OK
PMS5	Link_control defaults on power-on or reset to	23.3.6.2	M		ENABLE
PMS6	Action taken in SCAN_FOR_CARRIER mode	23.3.6.4	NWY:M		Enables link integrity state diagram, but blocks passage into LINK_PASS
PMS7	Reporting of link_status while in SCAN_FOR_CARRRIER mode	23.3.6.4	NWY:M		FAIL / READY
PMS8	Reporting of link_status while in DISABLE mode	23.3.6.4	NWY:M		FAIL
PMS9	Action taken in ENABLE mode	23.3.6.4	NWY:M		enables data processing functions
PMS10	Generation of PMA_RXERROR	23.3.7.2	M		ERROR / NO_ERROR

23.12.4.7 PMA Transmit functions

Item	Feature	Subclause	Status	Support	Value/Comment
PMT1	Transmission while (tx_code_vector=DATA) * (pma_carrier=OFF)	23.4.1.2	M		tx_code_vector[TX_D1] tx_code_vector[BI_D3] tx_code_vector[BI_D4]
PMT2	Transmission from time (tx_code_vector=DATA) * (pma_carrier=ON), until (tx_code_vector=IDLE	23.4.1.2	M		tx_code_vector[TX_D1] CS0 CS0
PMT3	Transmission while tx_code_vector=IDLE	23.4.1.2	M		Idle signal TP_DIL_100
PMT4	Duration of silence between link test pulses	23.4.1.2	M		1.2 ms ± 0.6 ms
PMT5	Link test pulse composed of	23.4.1.2	M		CS-1, CS1 transmitted on TX_D1

Item	Feature	Subclause	Status	Support	Value/Comment
PMT6	Following a packet, TP_IDL_100 signal starts with	23.4.1.2	M		Period of silence
PMT7	Effect of termination of TP_IDL_100	23.4.1.2	M		No delay or corruption of subsequent packet
PMT8	Zero crossing jitter of link test pulse	23.4.1.2	M		Less than 4 ns p-p
PMT9	Action taken when xmit=disable	23.4.1.2	M		Transmitter behaves as if tx_code_vector=IDLE

23.12.4.8 PMA Receive functions

Item	Feature	Subclause	Status	Support	Value/Comment
PMR1	Reception and translation of data with ternary symbol error rate less than	23.4.1.3	M		One part in 10^8
PMR2	Assertion of pma_carrier=ON upon reception of test signal	23.4.1.4	M		Test signal is a succession of three data values, produced synchronously with a 25 MHz clock, both preceded and followed by 100 symbols of silence. The three values are: 467 mV, –225 mV, and then 467 mV again
PMR3	condition required to turn off pma_carrier	23.4.1.4	M		Either of a) Seven consecutive zeroes b) Reception of eop1 per 23.4.1.4
PMR4	Value of carrier_status while rcv=ENABLE	23.4.1.4	M		pma_carrier
PMR5	Value of carrier_status while rcv=DISABLE	23.4.1.4	M		OFF

23.12.4.9 Link Integrity functions

Item	Feature	Subclause	Status	Support	Value/Comment
LIF1	Link Integrity function complies with	23.4.1.5	M		State diagram figure 23-12

23.12.4.10 PMA Align functions

Item	Feature	Subclause	Status	Support	Value/Comment
ALN1	Generation of PMA_UNITDATA.indicate (PREAMBLE) messages	23.4.1.6	M		
ALN2	Ternary symbols transferred by first PMA_UNITDATA.indicate (DATA) message	23.4.1.6	M		rx_code_vector[BI_D3]:first ternary symbol of first data code group rx_code_vector[RX_D2]:two ternary symbols prior to start of second data code group rx_code_vector[BI_D4]:four ternary symbols prior to start of third data code group

Item	Feature	Subclause	Status	Support	Value/Comment
ALN3	PMA_UNITDATA.indicate (DATA) messages continue until carrier_status=OFF	23.4.1.6	M		
ALN4	While carrier_status=OFF, PMA emits message	23.4.1.6	M		PMA_UNITDATA.indicate (IDLE)
ALN5	Failure to recognize SSD generates rxerror_status=ERROR	23.4.1.6	M		
ALN6	Action taken when carrier_status=OFF	23.4.1.6	M		Clear rxerror_status
ALN7	Action taken if first packet is used for alignment	23.4.1.6	M		PMA emits PMA_UNITDATA.indicate (PREAMBLE)
ALN8	Tolerance of line skew	23.4.1.6	M		60 ns
ALN9	Detection of misplaced **sosb** 6T code group caused by 3 or fewer ternary symbols in error	23.4.1.6	M		
ALN10	Action taken if **rcv**=disable	23.4.1.6	M		PMA emits PMA_UNITDATA.indicate (IDLE)

23.12.4.11 Other PMA functions

Item	Feature	Subclause	Status	Support	Value/Comment
PMO1	PMA Reset function	23.4.1.1	M		
PMO2	Suitable clock recovery	23.4.1.7	M		

23.12.4.12 Isolation requirements

Item	Feature	Subclause	Status	Support	Value/Comment
ISO1	Values of all components used in test circuits	23.5	M		Accurate to within ±1% unless required otherwise
ISO2	Electrical isolation meets	23.5.1.1	M		1500 V at 50–60 Hz for 60 s per IEC 950: 1991 *or* 2250 Vdc for 60 s per IEC 950: 1991 *or* Ten 2400 V pulses per IEC 60
ISO3	Insulation breakdown during isolation test	23.5.1.1	M		None per IEC 950: 1991
ISO4	Resistance after isolation test	23.5.1.1	M		At least 2 M

23.12.4.13 PMA electrical requirements

Item	Feature	Subclause	Status	Support	Value/Comment
PME1	Conformance to all transmitter specifications in 23.5.1.2	23.5.1.2	M		
PME2	Transmitter load unless otherwise specified	23.5.1.2	M		100 Ω
PME3	Peak differential output voltage	23.5.1.2.1	M		3.15–3.85 V
PME4	Differential transmit template at MDI	23.5.1.2.2	M		Table 23-2
PME5	Differential MDI output template voltage scaling	23.5.1.2.2	M		3.15– 3.85 V
PME6	Interpolation between points on transmit template	23.5.1.2.2	M		Linear
PME7	Differential link pulse template at MDI	23.5.1.2.2	M		Table 23-2
PME8	Differential link pulse template scaling	23.5.1.2.2	M		Same value as used for differential transmit template scaling
PME9	Interpolation between point on link pulse template	23.5.1.2.2	M		Linear
PME10	State when transmitting seven or more consecutive CS0 during TP_IDL-100 signal	23.5.1.2.2	M		–50 mV to 50 mV
PME11	Limit on magnitude of harmonics measured at MDI	23.5.1.2.2	M		27 dB below fundamental
PME12	Differential output ISI	23.5.1.2.3	M		Less than 9%
PME13	Measurement of ISI and peak-to-peak signal voltage	23.5.1.2.3	M		Halfway between nominal zero crossing of the observed eye pattern
PME14	Transfer function of 100BASE-T4 transmit test filter	23.5.1.2.3	M		Third-order Butterworth filter with –3 dB point at 25.0 MHz
PME15	Reflection loss of 100BASE-T4 transmit test filter and 100 W load across the frequency range 2–12.5 MHz	23.5.1.2.3	M		Exceeds 17 dB
PME16	Differential output impedance	23.5.1.2.4	M		Provide return loss into 100 Ω of 17 dB from 2.0 to 12.5 MHz
PME17	Maintenance of return loss	23.5.1.2.4	M		At all times PHY is fully powered
PME18	Droop as defined in figure 23-18 during transmission of eop1 and eop4	23.5.1.2.4	M		Less than 6%
PME19	Output timing jitter	23.5.1.2.5	M		No more than 4 ns peak-to-peak

Item	Feature	Subclause	Status	Support	Value/Comment
PME20	Measurement of output timing jitter	23.5.1.2.5	M		Other transmit outputs connected to 100BASE-T4 ISI test filter or 100 | load
PME21	Minimum transmitter impedance balance	23.5.1.2.6	M		$29 - 17\log\left(\frac{f}{10}\right)$ dB
PME22	Transmitter common-mode rejection; effect of E_{cm} as shown in figure 23-20 upon E_{dif}	23.5.1.2.8	M		Less than 100 mV
PME23	Transmitter common-mode rejection; effect of E_{cm} as shown in figure 23-20 upon edge jitter	23.5.1.2.8	M		Less than 1.0 ns
PME24	E_{cm} used for common-mode rejection tests	23.5.1.2.8	M		15 V peak, 10.1 MHz sine wave
PME25	Transmitter faults; response to indefinite application of short circuits	23.5.1.2.9	M		Withstand without damage and resume operation after fault is removed
PME26	Transmitter faults; response to 1000 V common-mode impulse per IEC 60	23.5.1.2.9	M		Withstand without damage
PME27	Shape of impulse used for common-mode impulse test	23.5.1.2.9	M		0.3/50 ∝s as defined in IEC 60
PME28	Ternary symbol transmission rate	23.5.1.2.10	M		25.000 MHz ± 0.01%
PME29	Conformance to all receiver specifications in 23.5.1.3	23.5.1.3	M		
PME30	Action taken upon receipt of differential signals that were transmitted within the constraints of 23.5.1.2 and have passed through worst-case UTP model	23.5.1.3.1	M		Correctly translated into PMA_UNITDATA messages
PME31	Action taken upon receipt of link test pulse	23.5.1.3.1	M		Accept as a link test pulse
PME32	Test configuration for data reception and link test pulse tests	23.5.1.3.1	M		Using worst-case UTP model, and with a connection less than one meter in length
PME33	Bit loss	23.5.1.3.2	M		No more than that specified in 23.5.1.3.1
PME34	Reaction of pma_carrier to signal less than 325 mV peak	23.5.1.3.2	M		Must not set pma_carrier=ON
PME35	Reaction of pma_carrier to continuous sinusoid less than 1.7 MHz	23.5.1.3.2	M		Must not set pma_carrier=ON
PME36	Reaction of pma_carrier to single cycle or less	23.5.1.3.2	M		Must not set pma_carrier=ON

Item	Feature	Subclause	Status	Support	Value/Comment
PME37	Reaction of pma_carrier to fast link pulse as defined in clause 28	23.5.1.3.2	M		Must not set pma_carrier=ON
PME38	Reaction of pma_carrier to link integrity test pulse signal TP_IDL_100	23.5.1.3.2	M		Must not set pma_carrier=ON
PME39	Differential input impedance	23.5.1.3.3	M		Provide return loss into 100 | of 17 dB from 2.0 to 12.5 MHz
PME40	Maintenance of return loss	23.5.1.3.3	M		At all times PHY is fully powered
PME41	Droop as defined in figure 23-18 during reception of test signal defined in figure 23-19	23.5.1.3.3	M		Less than 6%
PME42	Receiver common-mode rejection; effect of E_{cm} as shown in figure 23-24	23.5.1.3.4	M		Receiver meets 23.5.1.3.1
PME43	E_{cm} used for common-mode rejection tests	23.5.1.3.4	M		25 V peak-to-peak square wave, 500 kHz or lower in frequency, with edges no slower than 4 ns
PME44	Receiver faults; response to indefinite application of short circuits	23.5.1.3.5	M		Withstand without damage and resume operation after fault is removed
PME45	Receiver faults; response to 1000 V common mode impulse per IEC 60	23.5.1.3.5	M		Withstand without damage
PME46	Shape of impulse used for common mode impulse test	23.5.1.3.5	M		0.3/50 ∝s as defined in IEC 60
PME47	Receiver properly receives data have a worst-case ternary symbol range	23.5.1.3.6	M		25.00 MHz ± 0.01%
PME48	Steady-state current consumption	23.5.2	MII:M		0.75 A maximum
PME49	PHY operating voltage range	23.5.2	MII:M		Includes worst voltage available from MII
PME50	Extraneous signals induced on the MII control circuits during normal power-up and power-down	23.5.2	M		None

23.12.4.14 Characteristics of the link segment

Item	Feature	Subclause	Status	Support	Value/Comment
LNK1	Cable used	23.6.1	INS:M		Four pairs of balanced cabling, Category 3 or better, with a nominal characteristic impedance of 100 ±
LNK2	Source and load impedance used for cable testing (unless otherwise specified)	23.6.2	INS:M		100 ±
LNK3	Insertion loss of simplex link segment	23.6.2.1	INS:M		Less than 12 dB
LNK4	Source and load impedances used to measure cable insertion loss	23.6.2.1	INS:M		Meet 23.5.1.2.4 and 23.5.1.3.3
LNK5	Characteristic impedance over the range 2–12.5 MHz	26.6.2.2	INS:M		85–115 ±
LNK6	NEXT loss between 2 and 12.5 MHz	23.6.2.3.1	INS:M		Greater than $24.5 - 15\log\left(\frac{f}{12.5}\right)$ dB
LNK7	MDNEXT loss between 2 and 12.5 MHz	23.6.2.3.2	INS:M		Greater than $21.4 - 15\log\left(\frac{f}{12.5}\right)$ dB
LNK8	ELFEXT loss between 2 and 12.5 MHz	23.6.2.3.3	INS:M		Greater than $23.1 - 15\log\left(\frac{f}{12.5}\right)$ dB
LNK9	MDELFEXT loss between 2 and 12.5 MHz	23.6.2.3.4	INS:M		Greater than $20.9 - 15\log\left(\frac{f}{12.5}\right)$ dB
LNK10	Propagation delay	23.6.2.4.1	INS:M		Less than 570 ns
LNK11	Propagation delay per meter	23.6.2.4.2	INS:M		Less than 5.7 ns/m
LNK12	Skew	23.6.2.4.3	INS:M		Less than 50 ns
LNK13	Variation in skew once installed	23.6.243.3	INS:M		Less than ± 10 ns, within constraint of LNK8
LNK14	Noise level	23.6.3	INS:M		Such that objective error rate is met
LNK15	MDNEXT noise	23.6.3.1	INS:M		Less than 325 mVp
LNK16	MDFEXT noise	23.6.3.2	INS:M		Less than 87 mVp
LNK17	Maximum length of Category 5, 25-pair jumper cables	23.6.3.2	INS:M		10 m

23.12.4.15 MDI requirements

Item	Feature	Subclause	Status	Support	Value/Comment
MDI1	MDI connector	23.7.1	M		IEC 603-7: 1990
MDI2	Connector used on PHY	23.7.1	M		Jack (as opposed to plug)
MDI3	Crossover in every twisted-pair link	23.7.2	INS:M		
MDI4	MDI connector that implements the crossover function	23.7.2	XVR:M		Marked with "X"

23.12.4.16 General safety and environmental requirements

Item	Feature	Subclause	Status	Support	Value/Comment
SAF1	Conformance to safety specifications	23.9.1	M		IEC 950: 1991
SAF2	Installation practice	23.9.2.1	INS:M		Sound practice, as defined by applicable local codes
SAF3	Any safety grounding path for an externally connected PHY shall be provided through the circuit ground of the MII connection	23.9.2.2	M		
SAF4	Care taken during installation to ensure that noninsulated network cable conductors do not make electrical contact with unintended conductors or ground	23.9.2.3	INS:M		
SAF5	Application of voltages specified in 23.9.2.4 does not result in any safety hazard	23.9.2.4	M		
SAF6	Conformance with local and national codes for the limitation of electromagnetic interference	23.9.3.1	INS:M		

23.12.4.17 Timing requirements

Item	Feature	Subclause	Status	Support	Value/Comment
TIM1	PMA_OUT	23.11.3	PMA:M		1 to 9.5 BT
TIM2	TEN_PMA + PMA_OUT	23.11.3	PCS:M		7 to 17.5 BT
TIM3	TEN_CRS	23.11.3	PCS:M		0 to +4 BT

Item	Feature	Subclause	Status	Support	Value/Comment
TIM4	NOT_TEN_CRS	23.11.3	PCS:M		28 to 36 BT
TIM5	RX_PMA_CARRIER	23.11.3	PMA:M		Less than 15.5 BT
TIM6	RX_CRS	23.11.3	PCS:M		Less than 27.5 BT
TIM7	RX_NOT_CRS	23.11.3	PCS:M		0 to 51.5 BT
TIM8	FAIRNESS	23.11.3	PCS:M		0 to 28 BT
TIM9	RX_PMA_DATA	23.11.3	PMA:M		67 to 90.5 BT
TIM10	EOP_CARRIER_STATUS	23.11.3	M		51 to 74.5 BT
TIM11	EOC_CARRIER_STATUS	23.11.3	M		3 to 50.5 BT
TIM12	RX_RXDV	23.11.3	PCS:M		81 to 114.5 BT
TIM13	RX_PMA_ERROR	23.11.3	M		Allowed limits equal the actual RX_PMA_DATA time for the device under test plus from 0 to 20 BT
TIM14	RX_COL	23.11.3	PCS:M		Less than 27.5 BT
TIM15	RX_NOT_COL	23.11.3	PCS:M		Less than 51.5 BT
TIM16	TX_NOT_COL	23.11.3	PCS:M		Less than 36 BT
TIM17	TX_SKEW	23.11.3	M		Less than 0.5 BT
TIM18	CRS_PMA_DATA	23.11.3	PMA:M		Less than 78.5 BT
TIM19	COL_to_BI_D3/4_OFF	23.11.3	PMA:M		Less than 40 BT

24. Physical Coding Sublayer (PCS) and Physical Medium Attachment (PMA) sublayer, type 100BASE-X

24.1 Overview

24.1.1 Scope

This clause specifies the Physical Coding Sublayer (PCS) and the Physical Medium Attachment (PMA) sublayer that are common to a family of 100 Mb/s Physical Layer implementations, collectively known as 100BASE-X. There are currently two embodiments within this family: 100BASE-TX and 100BASE-FX. 100BASE-TX specifies operation over two copper media: two pairs of shielded twisted-pair cable (STP) and two pairs of unshielded twisted-pair cable (Category 5 UTP).[21] 100BASE-FX specifies operation over two optical fibers. The term 100BASE-X is used when referring to issues common to both 100BASE-TX and 100BASE-FX.

100BASE-X leverages the Physical Layer standards of ISO 9314 and ANSI X3T12 (FDDI) through the use of their Physical Medium Dependent (PMD) sublayers, including their Medium Dependent Interfaces (MDI). For example, ANSI X3.263: 199X (TP-PMD) defines a 125 Mb/s, full-duplex signaling system for twisted-pair wiring that forms the basis for 100BASE-TX as defined in clause 25. Similarly, ISO 9314-3: 1990 defines a system for transmission on optical fiber that forms the basis for 100BASE-FX as defined in clause 26.

100BASE-X maps the interface characteristics of the FDDI PMD sublayer (including MDI) to the services expected by the CSMA/CD MAC. 100BASE-X can be extended to support any other full duplex medium requiring only that the medium be PMD compliant.

24.1.2 Objectives

The following are the objectives of 100BASE-X:

a) Support the CSMA/CD MAC.
b) Support the 100BASE-T MII, repeater, and optional Auto-Negotiation.
c) Provide 100 Mb/s data rate at the MII.
d) Support cable plants using Category 5 UTP, 150 Ω STP or optical fiber, compliant with ISO/IEC 11801: 1995.
e) Allow for a nominal network extent of 200–400 m, including:
   1) unshielded twisted-pair links of 100 m;
   2) two repeater networks of approximately 200 m span;
   3) one repeater networks of approximately 300 m span (using fiber); and
   4) DTE/DTE links of approximately 400 m (using fiber).
f) Preserve full-duplex behavior of underlying PMD channels.

24.1.3 Relationship of 100BASE-X to other standards

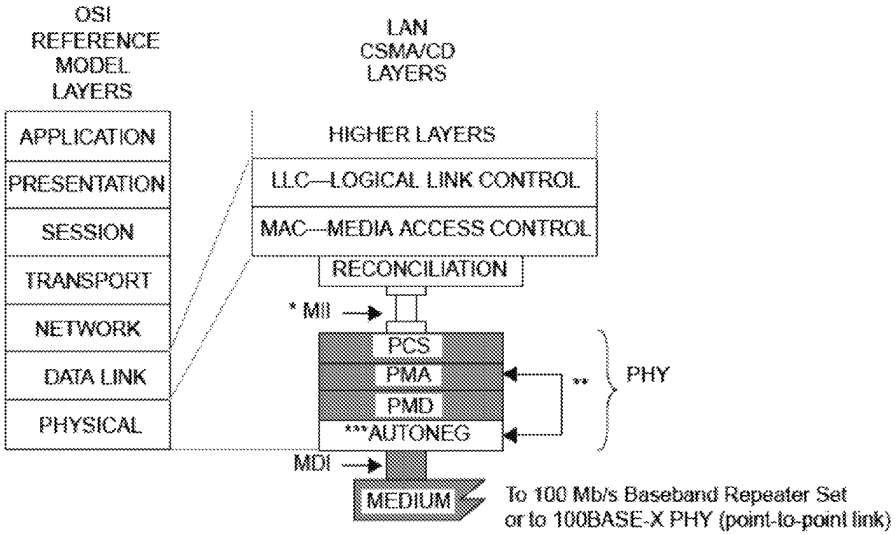
Figure 24-1 depicts the relationships among the 100BASE-X sublayers (shown shaded), other 100BASE-T sublayers, the CSMA/CD MAC, and the IEEE 802.2 LLC.

24.1.4 Summary of 100BASE-X sublayers

The following provides an overview of the 100BASE-X sublayers that are embodied in the 100BASE-X Physical sublayer (PHY).[22]

[21] ISO/IEC 11801: 1995 makes no distinction between shielded or unshielded twisted-pair cables, referring to both as balanced cables.

[22] The 100BASE-X PHY should not be confused with the FDDI PHY, which is a sublayer functionally aligned to the 100BASE-T PCS.



MDI = MEDIUM DEPENDENT INTERFACE
MII = MEDIA INDEPENDENT INTERFACE
PCS = PHYSICAL CODING SUBLAYER
PMA = PHYSICAL MEDIUM ATTACHMENT
PHY = PHYSICAL LAYER DEVICE
PMD = PHYSICAL MEDIUM DEPENDENT

* MII is optional.
** AUTONEG communicates with the PMA sublayer through the PMA service interface messages PMA_LINK.request and PMA_LINK.indicate.
*** AUTONEG is optional.

Figure 24-1—Type 100BASE-X PHY relationship to the ISO Open Systems Interconnection (OSI) reference model and the IEEE 802.3 CSMA/CD LAN model

24.1.4.1 Physical Coding Sublayer (PCS)

The PCS interface is the Media Independent Interface (MII) that provides a uniform interface to the Reconciliation sublayer for all 100BASE-T PHY implementations (e.g., 100BASE-X and 100BASE-T4). 100BASE-X, as other 100BASE-T PHYs, is modeled as providing services to the MII. This is similar to the use of an AUI interface.

The 100BASE-X PCS realizes all services required by the MII, including:

a) Encoding (decoding) of MII data nibbles to (from) five-bit code-groups (4B/5B);
b) Generating Carrier Sense and Collision Detect indications;
c) Serialization (deserialization) of code-groups for transmission (reception) on the underlying serial PMA, and
d) Mapping of Transmit, Receive, Carrier Sense and Collision Detection between the MII and the underlying PMA.

24.1.4.2 Physical Medium Attachment (PMA) sublayer

The PMA provides a medium-independent means for the PCS and other bit-oriented clients (e.g., repeaters) to support the use of a range of physical media. The 100BASE-X PMA performs the following functions:

a) Mapping of transmit and receive code-bits between the PMA's client and the underlying PMD;
b) Generating a control signal indicating the availability of the PMD to a PCS or other client, also synchronizing with Auto-Negotiation when implemented;
c) Optionally, generating indications of activity (carrier) and carrier errors from the underlying PMD;
d) Optionally, sensing receive channel failures and transmitting the Far-End Fault Indication; and detecting the Far-End Fault Indication; and
e) Recovery of clock from the NRZI data supplied by the PMD.

24.1.4.3 Physical Medium Dependent (PMD) sublayer

100BASE-X uses the FDDI signaling standards ISO 9314-3: 1990 and ANSI X3.263: 199X (TP-PMD). These signaling standards, called PMD sublayers, define 125 Mb/s, full-duplex signaling systems that accommodate multi-mode optical fiber, STP and UTP wiring. 100BASE-X uses the PMDs specified in these standards with the PMD Service Interface specified in 24.4.1.

The MDI, logically subsumed within the PMD, provides the actual medium attachment, including connectors, for the various supported media.

100BASE-X does not specify the PMD and MDI other than including the appropriate standard by reference along with the minor adaptations necessary for 100BASE-X. Figure 24-2 depicts the relationship between 100BASE-X and the PMDs of ISO 9314-3: 1990 (for 100BASE-FX) and ANSI X3.263: 199X (for 100BASE-TX). The PMDs (and MDIs) for 100BASE-TX and 100BASE-FX are specified in subsequent clauses of this standard.

24.1.5 Inter-sublayer interfaces

There are a number of interfaces employed by 100BASE-X. Some (such as the PMA and PMD interfaces) use an abstract service model to define the operation of the interface. The PCS Interface is defined as a set of physical signals, in a medium-independent manner (MII). Figure 24-3 depicts the relationship and mapping of the services provided by all of the interfaces relevant to 100BASE-X.

It is important to note that, while this specification defines interfaces in terms of bits, nibbles, and code-groups, implementations may choose other data path widths for implementation convenience. The only exceptions are: a) the MII, which, when implemented, uses a nibble-wide data path as specified in clause 22, and b) the MDI, which uses a serial, physical interface.

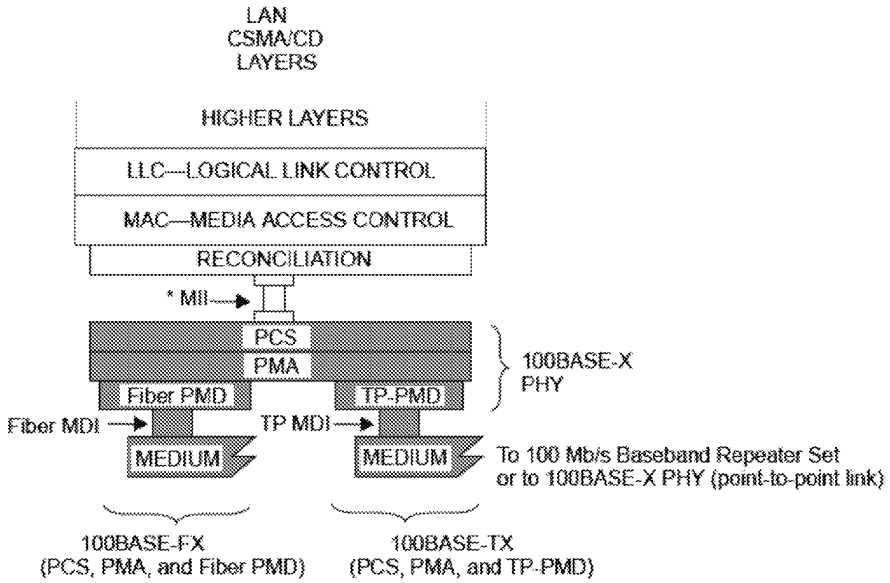
24.1.6 Functional block diagram

Figure 24-4 provides a functional block diagram of the 100BASE-X PHY.

24.1.7 State diagram conventions

The body of this standard is comprised of state diagrams, including the associated definitions of variables, constants, and functions. Should there be a discrepancy between a state diagram and descriptive text, the state diagram prevails.

The notation used in the state diagrams follows the conventions of 21.5; state diagram timers follow the conventions of 14.2.3.2.



MDI = MEDIUM DEPENDENT INTERFACE
MII = MEDIA INDEPENDENT INTERFACE
PCS = PHYSICAL CODING SUBLAYER
PMA = PHYSICAL MEDIUM ATTACHMENT
PHY = PHYSICAL LAYER DEVICE
Fiber PMD = PHYSICAL MEDIUM DEPENDENT SUBLAYER FOR FIBER
TP-PMD = PHYSICAL MEDIUM DEPENDENT SUBLAYER FOR TWISTED PAIRS

NOTE—The PMD sublayers are mutually independent.
* MII is optional.

Figure 24-2—Relationship of 100BASE-X and the PMDs

24.2 Physical Coding Sublayer (PCS)

24.2.1 Service Interface (MII)

The PCS Service Interface allows the 100BASE-X PCS to transfer information to and from the MAC (via the Reconciliation sublayer) or other PCS client, such as a repeater. The PCS Service Interface is precisely defined as the Media Independent Interface (MII) in clause 22.

In this clause, the setting of MII variables to TRUE or FALSE is equivalent, respectively, to "asserting" or "de-asserting" them as specified in clause 22.

24.2.2 Functional requirements

The PCS comprises the Transmit, Receive, and Carrier Sense functions for 100BASE-T. In addition, the collisionDetect signal required by the MAC (COL on the MII) is derived from the PMA code-bit stream. The PCS shields the Reconciliation sublayer (and MAC) from the specific nature of the underlying channel. Specifically for receiving, the 100BASE-X PCS passes to the MII a sequence of data nibbles derived from incoming code-groups, each comprised of five code-bits, received from the medium. Code-group alignment and MAC packet delimiting is performed by embedding special non-data code-groups. The MII uses a nibble-wide, synchronous data path, with packet delimiting being provided by separate TX_EN and RX_DV

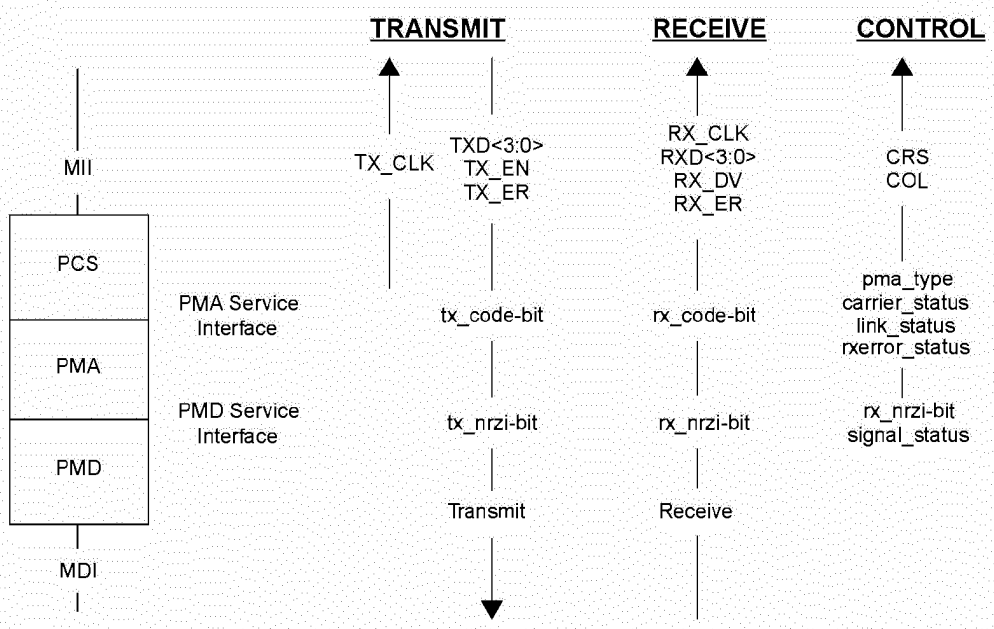


Figure 24-3—Interface mapping

signals. The PCS provides the functions necessary to map these two views of the exchanged data. The process is reversed for transmit.

The following provides a detailed specification of the functions performed by the PCS, which comprise five parallel processes (Transmit, Transmit Bits, Receive, Receive Bits, and Carrier Sense). Figure 24-4 includes a functional block diagram of the PCS.

The Receive Bits process accepts continuous code-bits via the PMA_UNITDATA.indicate primitive. Receive monitors these bits and generates RXD <3:0>, RX_DV and RX_ER on the MII, and the internal flag, receiving, used by the Carrier Sense and Transmit processes.

The Transmit process generates continuous code-groups based upon the TXD <3:0>, TX_EN, and TX_ER signals on the MII. These code-groups are transmitted by Transmit Bits via the PMA_UNITDATA request primitive. The Transmit process generates the MII signal COL based on whether a reception is occurring simultaneously with transmission. Additionally, it generates the internal flag, transmitting, for use by the Carrier Sense process.

The Carrier Sense process asserts the MII signal CRS when either transmitting or receiving is TRUE. Both the Transmit and Receive processes monitor link_status via the PMA_LINK.indicate primitive, to account for potential link failure conditions.

24.2.2.1 Code-groups

The PCS maps four-bit nibbles from the MII into five-bit code-groups, and vice versa, using a 4B/5B block coding scheme. A code-group is a consecutive sequence of five code-bits interpreted and mapped by the PCS. Implicit in the definition of a code-group is an establishment of code-group boundaries by an alignment function within the PCS Receive process. It is important to note that, with the sole exception of the SSD, which is used to achieve alignment, code-groups are undetectable and have no meaning outside the 100BASE-X physical protocol data unit, called a "stream."

The coding method used, derived from ISO 9314-1: 1989, provides

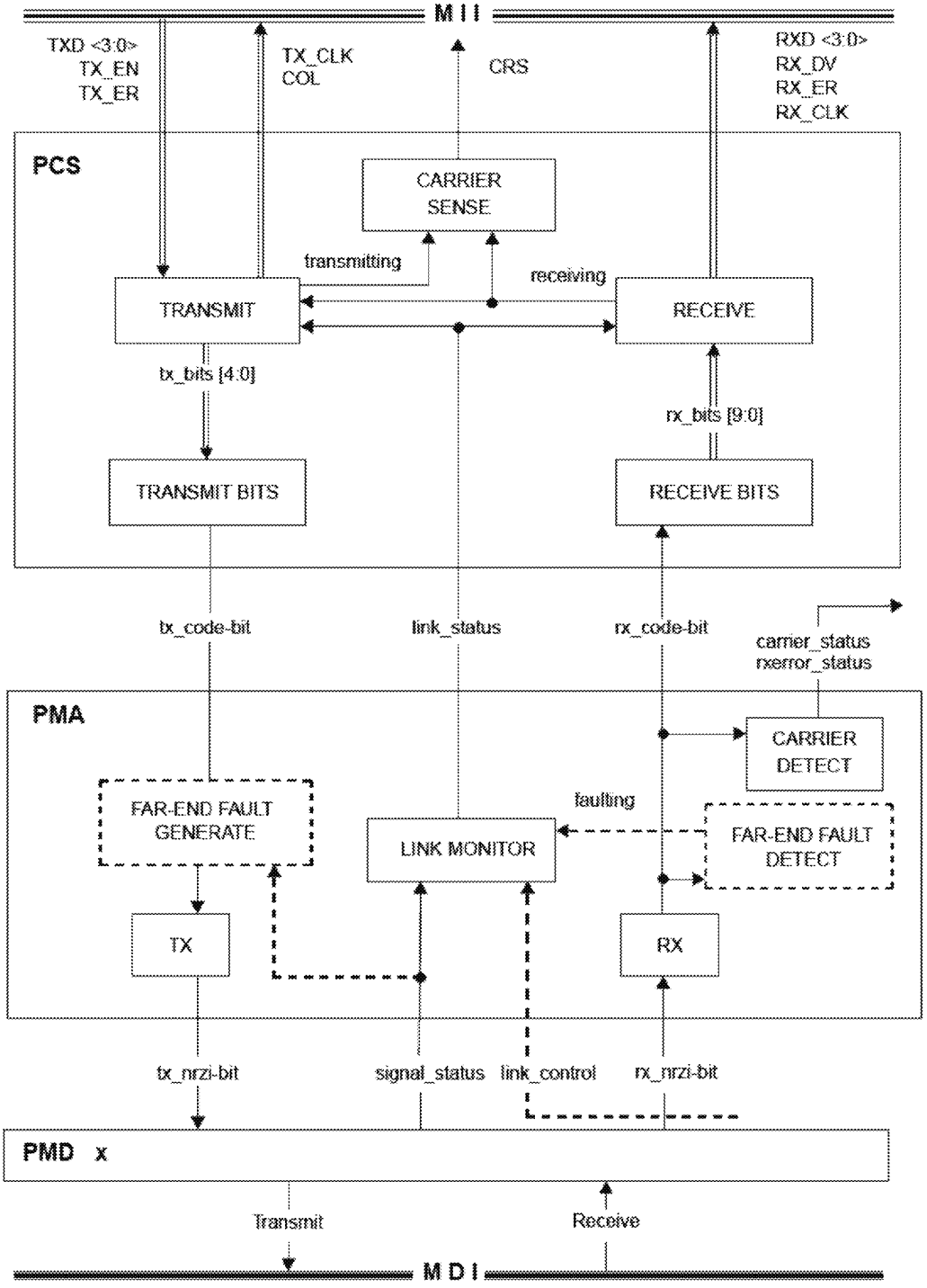


Figure 24-4—Functional block diagram

a) Adequate codes (32) to provide for all Data code-groups (16) plus necessary control code-groups;
b) Appropriate coding efficiency (4 data bits per 5 code-bits; 80%) to effect a 100 Mb/s Physical Layer interface on a 125 Mb/s physical channel as provided by FDDI PMDs; and
c) Sufficient transition density to facilitate clock recovery (when not scrambled).

Table 24-1 specifies the interpretation assigned to each five bit code-group, including the mapping to the nibble-wide (TXD or RXD) Data signals on the MII. The 32 code-groups are divided into four categories, as shown.

For clarity in the remainder of this clause, code-group names are shown between /slashes/. Code-group sequences are shown in succession, e.g.: /1/2/....

The indicated code-group mapping is identical to ISO 9314-1: 1989, with four exceptions:

a) The FDDI term *symbol* is avoided in order to prevent confusion with other 100BASE-T terminology. In general, the term *code-group* is used in its place.
b) The /S/ and /Q/ code-groups are not used by 100BASE-X and are interpreted as INVALID.
c) The /R/ code-group is used in 100BASE-X as the second code-group of the End-of-Stream delimiter rather than to indicate a Reset condition.
d) The /H/ code-group is used to propagate receive errors rather than to indicate the Halt Line State.

24.2.2.1.1 Data code-groups

A Data code-group conveys one nibble of arbitrary data between the MII and the PCS. The sequence of Data code-groups is arbitrary, where any Data code-group can be followed by any other Data code-group. Data code-groups are coded and decoded but not interpreted by the PCS. Successful decoding of Data code-groups depends on proper receipt of the Start-of-Stream delimiter sequence, as defined in table 24-1.

24.2.2.1.2 Idle code-groups

The Idle code-group (/I/) is transferred between streams. It provides a continuous fill pattern to establish and maintain clock synchronization. Idle code-groups are emitted from, and interpreted by, the PCS.

24.2.2.1.3 Control code-groups

The Control code-groups are used in pairs (/J/K/, /T/R/) to delimit MAC packets. Control code-groups are emitted from, and interpreted by, the PCS.

24.2.2.1.4 Start-of-Stream Delimiter (/J/K/)

A Start-of-Stream Delimiter (SSD) is used to delineate the boundary of a data transmission sequence and to authenticate carrier events. The SSD is unique in that it may be recognized independently of previously established code-group boundaries. The Receive function within the PCS uses the SSD to establish code-group boundaries. A SSD consists of the sequence /J/K/.

On transmission, the first 8 bits of the MAC preamble are replaced by the SSD, a replacement that is reversed on reception.

24.2.2.1.5 End-of-Stream delimiter (/T/R/)

An End-of-Stream delimiter (ESD) terminates all normal data transmissions. Unlike the SSD, an ESD cannot be recognized independent of previously established code-group boundaries. An ESD consists of the sequence /T/R/.

Table 24-1—4B/5B code-groups

	PCS code-group [4:0] 4 3 2 1 0	Name	MII (TXD/RXD) <3:0> 3 2 1 0	Interpretation
DATA	1 1 1 1 0	0	0 0 0 0	Data 0
	0 1 0 0 1	1	0 0 0 1	Data 1
	1 0 1 0 0	2	0 0 1 0	Data 2
	1 0 1 0 1	3	0 0 1 1	Data 3
	0 1 0 1 0	4	0 1 0 0	Data 4
	0 1 0 1 1	5	0 1 0 1	Data 5
	0 1 1 1 0	6	0 1 1 0	Data 6
	0 1 1 1 1	7	0 1 1 1	Data 7
	1 0 0 1 0	8	1 0 0 0	Data 8
	1 0 0 1 1	9	1 0 0 1	Data 9
	1 0 1 1 0	A	1 0 1 0	Data A
	1 0 1 1 1	B	1 0 1 1	Data B
	1 1 0 1 0	C	1 1 0 0	Data C
	1 1 0 1 1	D	1 1 0 1	Data D
	1 1 1 0 0	E	1 1 1 0	Data E
	1 1 1 0 1	F	1 1 1 1	Data F
	1 1 1 1 1	I	undefined	IDLE; used as inter-stream fill code
CONTROL	1 1 0 0 0	J	0 1 0 1	Start-of-Stream Delimiter, Part 1 of 2; always used in pairs with K
	1 0 0 0 1	K	0 1 0 1	Start-of-Stream Delimiter, Part 2 of 2; always used in pairs with J
	0 1 1 0 1	T	undefined	End-of-Stream Delimiter, Part 1 of 2; always used in pairs with R
	0 0 1 1 1	R	undefined	End-of-Stream Delimiter, Part 2 of 2; always used in pairs with T
INVALID	0 0 1 0 0	H	Undefined	Transmit Error; used to force signaling errors
	0 0 0 0 0	V	Undefined	Invalid code
	0 0 0 0 1	V	Undefined	Invalid code
	0 0 0 1 0	V	Undefined	Invalid code
	0 0 0 1 1	V	Undefined	Invalid code
	0 0 1 0 1	V	Undefined	Invalid code
	0 0 1 1 0	V	Undefined	Invalid code
	0 1 0 0 0	V	Undefined	Invalid code
	0 1 1 0 0	V	Undefined	Invalid code
	1 0 0 0 0	V	Undefined	Invalid code
	1 1 0 0 1	V	Undefined	Invalid code

24.2.2.1.6 Invalid code-groups

The /H/ code-group indicates that the PCS's client wishes to indicate a Transmit Error to its peer entity. The normal use of this indicator is for repeaters to propagate received errors. Transmit Error code-groups are emitted from the PCS, at the request of the PCS's client through the use of the TX_ER signal, as described in 24.2.4.2.

The presence of any invalid code-group on the medium, including /H/, denotes a collision artifact or an error condition. Invalid code-groups are not intentionally transmitted onto the medium by DTE's. The PCS indicates the reception of an Invalid code-group on the MII through the use of the RX_ER signal, as described in 24.2.4.4.

24.2.2.2 Encapsulation

The 100BASE-X PCS accepts frames from the MAC through the Reconciliation sublayer and MII. Due to the continuously signaled nature of the underlying PMA, and the encoding performed by the PCS, the 100BASE-X PCS encapsulates the MAC frame (100BASE-X Service Data Unit, SDU) into a Physical Layer stream (100BASE-X Protocol Data Unit, PDU).

Except for the two code-group SSD, data nibbles within the SDU (including the non-SSD portions of the MAC preamble and SFD) are not interpreted by the 100BASE-X PHY. The conversion from a MAC frame to a Physical Layer stream and back to a MAC frame is transparent to the MAC.

Figure 24-5 depicts the mapping between MAC frames and Physical Layer streams.

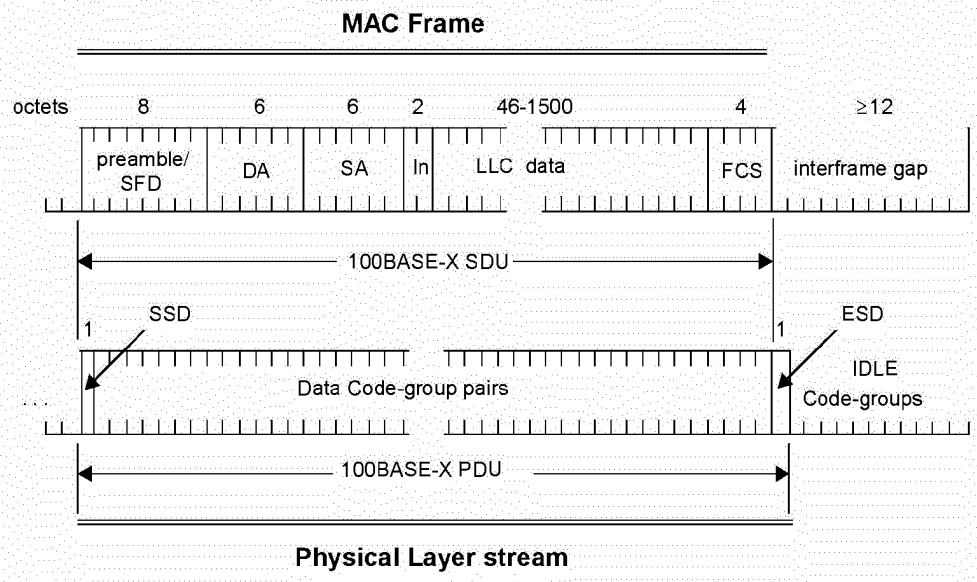


Figure 24-5—PCS encapsulation

A properly formed stream can be viewed as comprising three elements:

a) *Start-of-Stream Delimiter*. The start of a Physical Layer stream is indicated by a SSD, as defined in 24.2.2.1. The SSD replaces the first octet of the preamble from the MAC frame and vice versa.
b) *Data Code-groups*. Between delimiters (SSD and ESD), the PCS conveys Data code-groups corresponding to the data nibbles of the MII. These Data code-groups comprise the 100BASE-X Service Data Unit (SDU). Data nibbles within the SDU (including those corresponding to the MAC preamble and SFD) are not interpreted by the 100BASE-X PCS.
c) *End-of-Stream Delimiter*. The end of a properly formed stream is indicated by an ESD, as defined in 24.2.2.1. The ESD is transmitted by the PCS following the de-assertion of TX_EN on the MII, which corresponds to the last data nibble composing the FCS from the MAC. It is transmitted during the period considered by the MAC to be the interframe gap (IFG). On reception, ESD is interpreted by the PCS as terminating the SDU.

Between streams, IDLE code-groups are conveyed between the PCS and PMA.

24.2.2.3 Data delay

The PCS maps a non-aligned code-bit data path from the PMA to an aligned, nibble-wide data path on the MII, both for Transmit and Receive. Logically, received bits must be buffered to facilitate SSD detection and alignment, coding translation, and ESD detection. These functions necessitate an internal PCS delay of at least two code-groups. In practice, alignment may necessitate even longer delays of the incoming code-bit stream.

When the MII is present as an exposed interface, the MII signals TX_CLK and RX_CLK, not depicted in the following state diagrams, shall be generated by the PCS in accordance with clause 22.

24.2.2.4 Mapping between MII and PMA

Figure 24-6 depicts the mapping of the nibble-wide data path of the MII to the five-bit-wide code-groups (internal to the PCS) and the code-bit path of the PMA interface.

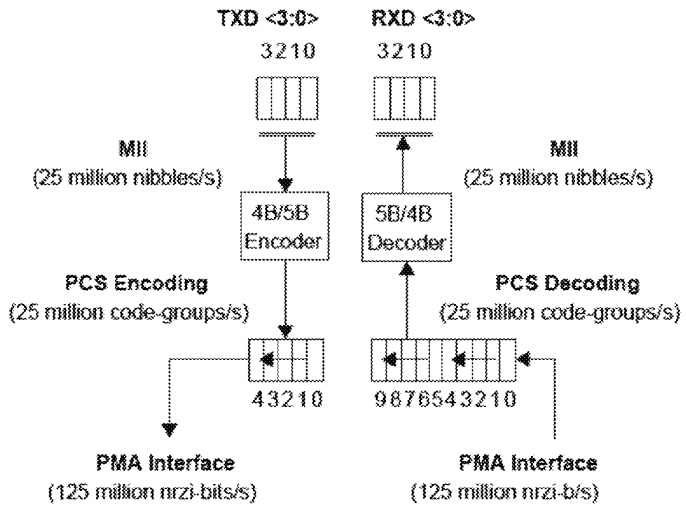


Figure 24-6—PCS reference diagram

Upon receipt of a nibble from the MII, the PCS encodes it into a five-bit code-group, according to 24.2.2.1. Code-groups are serialized into code-bits and passed to the PMA for transmission on the underlying medium, according to figure 24-6. The first transmitted code-bit of a code-group is bit 4, and the last code-bit transmitted is bit 0. There is no numerical significance ascribed to the bits within a code-group; that is, the code-group is simply a five-bit pattern that has some predefined interpretation.

Similarly, the PCS deserializes code-bits received from the PMA, according to figure 24-6. After alignment is achieved, based on SSD detection, the PCS converts code-groups into MII data nibbles, according to 24.2.2.1.

24.2.3 State variables

24.2.3.1 Constants

DATA
: The set of 16 code-groups corresponding to valid DATA, as specified in 24.2.2.1. (In the Receive state diagram, the set operators $\in$ and $\notin$ are used to represent set membership and non-membership, respectively.)

ESD
: The code-group pair corresponding to the End-of-Stream delimiter, as specified in 24.2.2.1.

ESD1
: The code-group pair corresponding to the End-of-Stream delimiter, Part 1 (/T/), as specified in 24.2.2.1.

ESD2
: The code-group pair corresponding to the End-of-Stream delimiter, Part 2 (/R/), as specified in 24.2.2.1.

HALT
: The Transmit Error code-group (/H/), as specified in 24.2.2.1.

IDLE
: The IDLE code-group, as specified in 24.2.2.1.

IDLES
: A code-group pair comprised of /I/I/; /I/ as specified in 24.2.2.1.

SSD
: The code-group pair corresponding to the Start-of-Stream delimiter, as specified in 24.2.2.1.

SSD1
: The code-group corresponding to the Start-of-Stream delimiter, Part 1 (/J/), as specified in 24.2.2.1.

SSD2
: The code-group corresponding to the Start-of-Stream delimiter, Part 2 (/K/), as specified in 24.2.2.1.

24.2.3.2 Variables

In the following, values for the MII parameters are definitively specified in clause 22.

COL
: The COL signal of the MII as specified in clause 22.

CRS
: The CRS signal of the MII as specified in clause 22.

link_status
The link_status parameter as communicated by the PMA_LINK.indicate primitive.

Values: FAIL; the receive channel is not intact
READY; the receive channel is intact and ready to be enabled by Auto-Negotiation
OK; the receive channel is intact and enabled for reception

receiving
A boolean set by the Receive process to indicate non-IDLE activity (after squelch). Used by the Carrier Sense process, and also interpreted by the Transmit process for indicating a collision.

Values: TRUE; unsquelched carrier being received
FALSE; carrier not being received

rx_bits [9:0]
A vector of the 10 most recently received code-bits from the PMA as assembled by Receive Bits and processed by Receive. rx_bits [0] is the most recently received (newest) code-bit; rx_bits [9] is the least recently received code-bit (oldest). When alignment has been achieved, it contains the last two code-groups.

rx_code-bit
The rx_code-bit parameter as communicated by the most recent PMA_UNITDATA.indicate primitive (that is, the value of the most recently received code-bit from the PMA).

RX_DV
The RX_DV signal of the MII as specified in clause 22. Set by the Receive process, RX_DV is also interpreted by the Receive Bits process as an indication that rx_bits is code-group aligned.

RX_ER
The RX_ER signal of the MII as specified in clause 22.

RXD <3:0>
The RXD <3:0> signal of the MII as specified in clause 22.

transmitting
A boolean set by the Transmit Process to indicate a transmission in progress. Used by the Carrier Sense process.

Values: TRUE; the PCS's client is transmitting
FALSE; the PCS's client is not transmitting

tx_bits [4:0]
A vector of code-bits representing a code-group prepared for transmission by the Transmit Process and transmitted to the PMA by the Transmit Bits process.

TX_EN
The TX_EN signal of the MII as specified in clause 22.

TX_ER
The TX_ER signal of the MII as specified in clause 22.

TXD <3:0>
The TXD <3:0> signal of the MII as specified in clause 22.

24.2.3.3 Functions

nibble DECODE (code-group)
In Receive, this function takes as its argument a five-bit code-group and returns the corresponding MII RXD <3:0> nibble, per table 24-1.

code-group ENCODE (nibble)
In the Transmit process, this function takes as its argument an MII TXD <3:0> nibble, and returns the corresponding five-bit code-group per table 24-1.

SHIFTLEFT (rx_bits)
In Receive Bits, this function shifts rx_bits left one bit placing rx_bits [8] in rx_bits [9], rx_bits [7] in rx_bits [8] and so on until rx_bits [1] gets rx_bits [0].

24.2.3.4 Timers

code-bit_timer

In the Transmit Bits process, the timer governing the output of code-bits from the PCS to the PMA and thereby to the medium with a nominal 8 ns period. This timer shall be derived from a fixed frequency oscillator with a base frequency of 125 MHz ± 0.005% and phase jitter above 20 kHz less than ± 8°.

24.2.3.5 Messages

gotCodeGroup.indicate

A signal sent to the Receive process by the Receive Bits process after alignment has been achieved signifying completion of reception of the next code-group in rx_bits(4:0), with the preceding code-group moved to rx_bits [9:5]. rx_bits [9:5] may be considered as the "current" code-group.

PMA_UNITDATA.indicate (rx_code-bit)

A signal sent by the PMA signifying that the next code-bit from the medium is available in rx_code-bit.

sentCodeGroup.indicate

A signal sent to the Transmit process from the Transmit Bits process signifying the completion of transmission of the code-group in tx_bits [4:0].

24.2.4 State diagrams

24.2.4.1 Transmit Bits

Transmit Bits is responsible for taking code-groups prepared by the Transmit process and transmitting them to the PMA using PMA_UNITDATA request, the frequency of which determines the transmit clock. Transmit deposits these code-groups in tx_bits with Transmit Bits signaling completion of a code-group transmission with sentCodeGroup.indicate.

The PCS shall implement the Transmit Bits process as depicted in figure 24-7 including compliance with the associated state variables as specified in 24.2.3.

24.2.4.2 Transmit

The Transmit process sends code-groups to the PMA via tx_bits and the Transmit Bits process. When initially invoked, and between streams (delimited by TX_EN on the MII), the Transmit process sources continuous Idle code-groups (/I/) to the PMA. Upon the assertion of TX_EN by the MII, the Transmit process passes an SSD (/J/K/) to the PMA, ignoring the TXD <3:0> nibbles during these two code-group times. Following the SSD, each TXD <3:0> nibble is encoded into a five-bit code-group until TX_EN is deasserted. If, while TX_EN is asserted, the TX_ER signal is asserted, the Transmit process passes Transmit Error code-groups (/H/) to the PMA. Following the de-assertion of TX_EN, an ESD (/T/R/) is generated, after which the transmission of Idle code-groups is resumed by the IDLE state.

Collision detection is implemented by noting the occurrence of carrier receptions during transmissions, following the model of 10BASE-T. The indication of link_status ↑ OK by the PMA at any time causes an immediate transition to the IDLE state and supersedes any other Transmit process operations.

The PCS shall implement the Transmit process as depicted in figure 24-8 including compliance with the associated state variables as specified in 24.2.3.

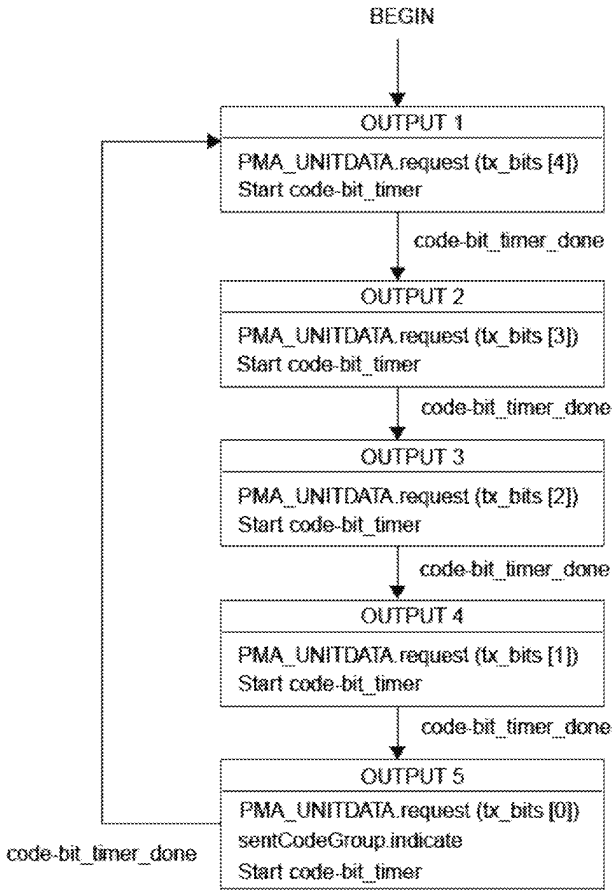


Figure 24-7—Transmit Bits state diagram

24.2.4.3 Receive Bits

The Receive Bits process collects code-bits from the PMA interface passing them to the Receive process via rx_bits. rx_bits [9:0] represents a sliding, 10-bit window on the PMA code-bits, with newly received code-bits from the PMA (rx_code-bit) being shifted into rx_bits [0]. This is depicted in figure 24-9. Bits are collected serially until Receive indicates alignment by asserting RX_DV, after which Receive Bits signals Receive for every five code-bits accumulated. Serial processing resumes with the de-assertion of RX_DV.

The PCS shall implement the Receive Bits process as depicted in figure 24-10 including compliance with the associated state variables as specified in 24.2.3.

24.2.4.4 Receive

The Receive process state machine can be viewed as comprising two sections: prealigned and aligned. In the prealigned states, IDLE, CARRIER DETECT, and CONFIRM K, the Receive process is waiting for an indication of channel activity followed by a SSD. After successful alignment, the incoming code-groups are decoded while waiting for stream termination.

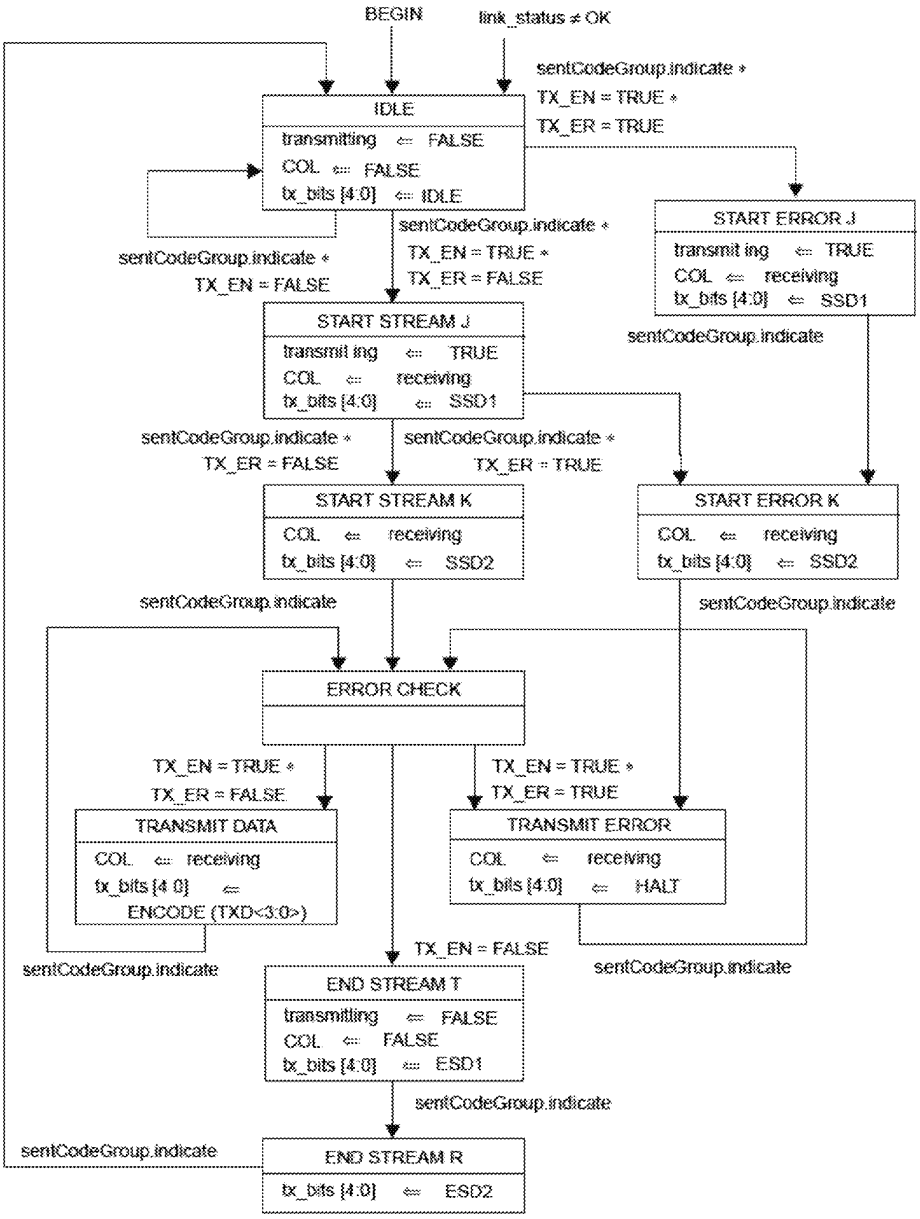


Figure 24-8—Transmit state diagram

24.2.4.4.1 Detecting channel activity

The detection of activity on the underlying channel is used both by the MAC (via the MII CRS signal and the Reconciliation sublayer) for deferral purposes, and by the Transmit process for collision detection. Activity, signaled by the assertion of receiving, is indicated by the receipt of two non-contiguous ZEROS within any 10 code-bits of the incoming code-bit stream.

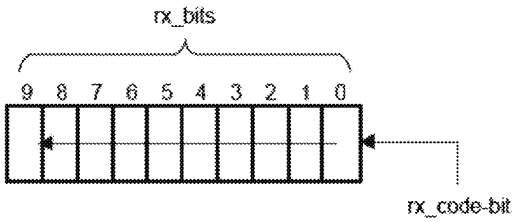


Figure 24-9—Receive Bits reference diagram

24.2.4.4.2 Code-group alignment

After channel activity is detected, the Receive process first aligns the incoming code-bits on code-group boundaries for subsequent data decoding. This is achieved by scanning the rx_bits vector for a SSD (/J/K/). The MII RX_DV signal remains deasserted during this time, which ensures that the Reconciliation sublayer will ignore any signals on RXD <3:0>. Detection of the SSD causes the Receive process to enter the START OF STREAM J state.

Well-formed streams contain SSD (/J/K/) in place of the first eight preamble bits. In the event that something else is sensed immediately following detection of carrier, a False Carrier Indication is signaled to the MII by asserting RX_ER and setting RXD to 1110 while RX_DV remains de-asserted. The associated carrier event, as terminated by 10 ONEs, is otherwise ignored.

24.2.4.4.3 Stream decoding

The Receive process substitutes a sequence of alternating ONE and ZERO data-bits for the SSD, which is consistent with the preamble pattern expected by the MAC.

The Receive process then performs the DECODE function on the incoming code-groups, passing decoded data to the MII, including those corresponding to the remainder of the MAC preamble and SFD. The MII signal RX_ER is asserted upon decoding any code-group following the SSD that is neither a valid Data code-group nor a valid stream termination sequence.

24.2.4.4.4 Stream termination

There are two means of effecting stream termination in the Receive process (figure 24-11).

A normal stream termination is caused by detection of an ESD (/T/R/) in the rx_bits vector. In order to preserve the ability of the MAC to properly delimit the FCS at the end of the frame (that is, to avoid incorrect AlignmentErrors in the MAC) the internal signal receiving (and through it, the MII CRS signal, per clause 22) is de-asserted immediately following the last code-bit in the stream that maps to the FCS. Note that the condition link_status ≠ OK during stream reception (that is, when receiving = TRUE) causes an immediate transition to the LINK FAILED state and supersedes any other Receive process operations.

A premature stream termination is caused by the detection of two Idle code-groups (/I/I) in the rx_bits vector prior to an ESD. Note that RX_DV remains asserted during the nibble corresponding to the first five contiguous ONEs while RX_ER is signaled on the MII. RX_ER is also asserted in the LINK FAILED state, which ensures that RX_ER remains asserted for sufficient time to be detected.

Stream termination causes a transition to the IDLE state.

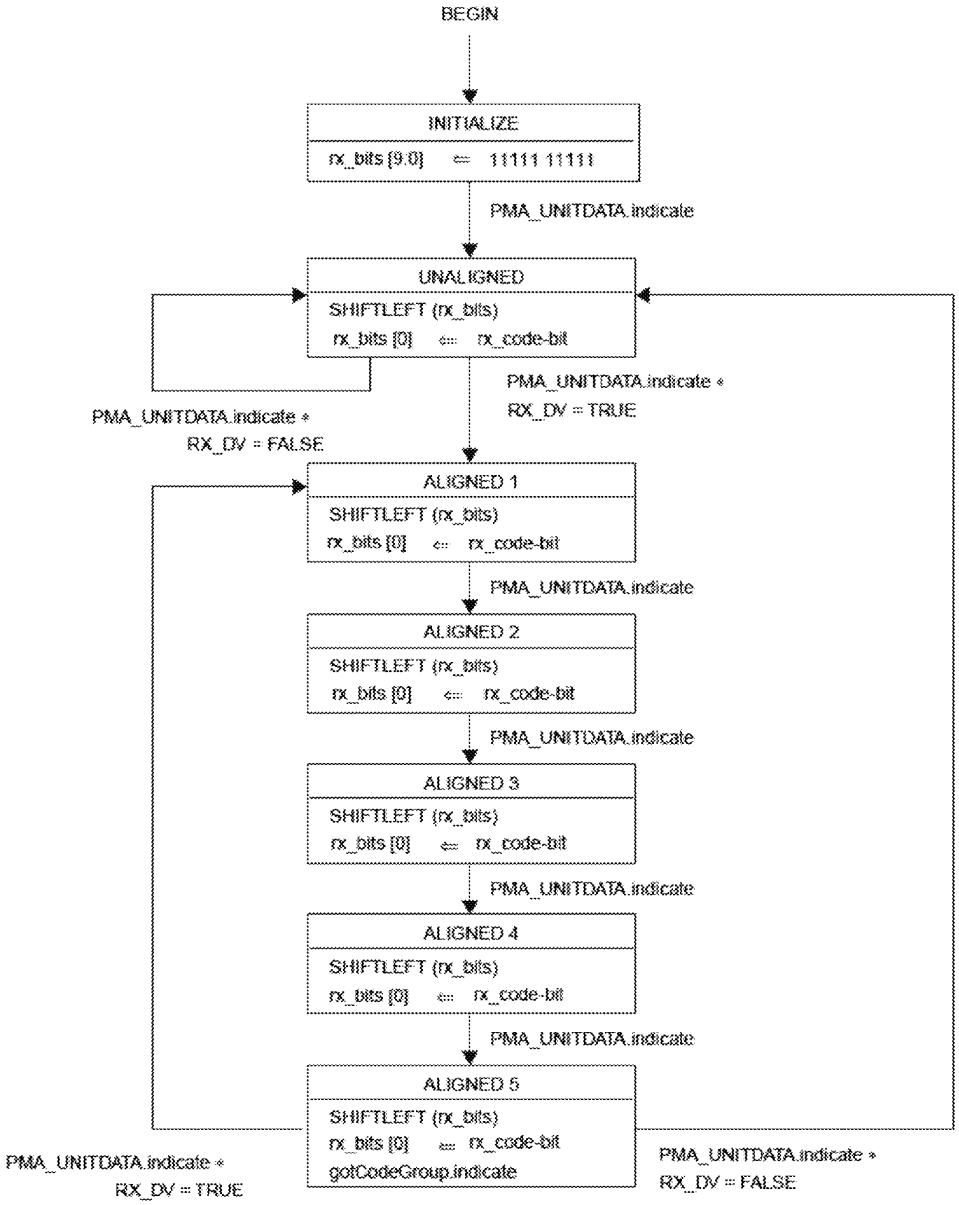


Figure 24-10—Receive Bits state diagram

The PCS shall implement the Receive process as depicted in figure 24-11 including compliance with the associated state variables as specified in 24.2.3.

24.2.4.5 Carrier Sense

The Carrier Sense process generates the signal CRS on the MII, which (via the Reconciliation sublayer) the MAC uses for frame receptions and for deferral. The process operates by performing a logical OR operation on the internal messages receiving and transmitting, generated by the Receive and Transmit processes, respectively.

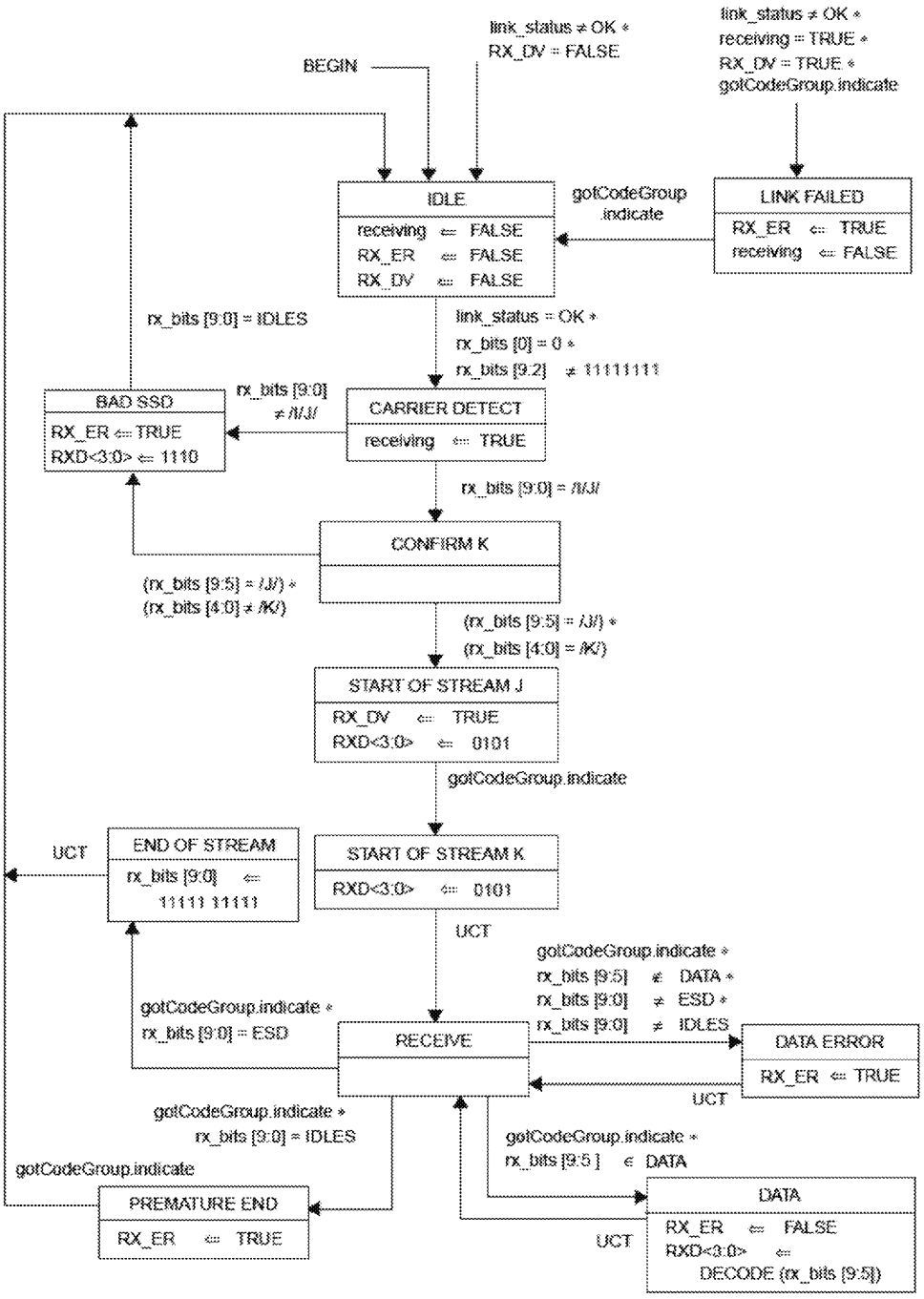


Figure 24-11—Receive state diagram

The PCS shall implement the Carrier Sense process as depicted in figure 24-12 including compliance with the associated state variables as specified in 24.2.3.

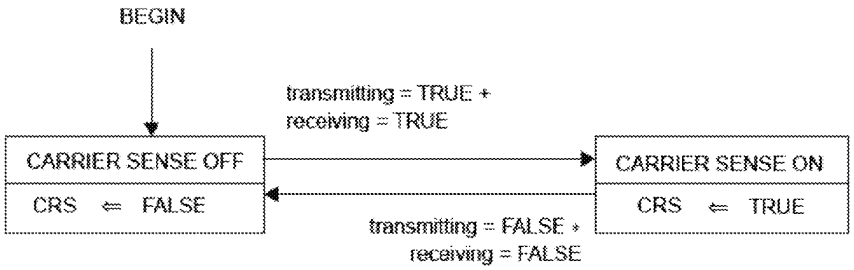


Figure 24-12—Carrier Sense state diagram

24.3 Physical Medium Attachment (PMA) sublayer

24.3.1 Service interface

The following specifies the service interface provided by the PMA to the PCS or another client, such as a repeater. These services are described in an abstract manner and do not imply any particular implementation.

The PMA Service Interface supports the exchange of code-bits between the PCS and/or Repeater entities. The PMA converts code-bits into NRZI format and passes these to the PMD, and vice versa. It also generates additional status indications for use by its client.

The following primitives are defined:

PMA_TYPE.indicate
PMA_UNITDATA.request
PMA_UNITDATA.indicate
PMA_CARRIER.indicate
PMA_LINK.indicate
PMA_LINK.request
PMA_RXERROR.indicate

24.3.1.1 PMA_TYPE.indicate

This primitive is generated by the PMA to indicate the nature of the PMA instantiation. The purpose of this primitive is to allow clients to support connections to the various types of 100BASE-T PMA entities in a generalized manner.

24.3.1.1.1 Semantics of the service primitive

PMA_TYPE.indicate (pma_type)

The pma_type parameter for use with a 100BASE-X PMA is "X".

24.3.1.1.2 When generated

The PMA continuously generates this primitive to indicate the value of pma_type.

24.3.1.1.3 Effect of receipt

The effect of receipt of this primitive by the client is unspecified by the PMA sublayer.

24.3.1.2 PMA_UNITDATA.request

This primitive defines the transfer of data (in the form of code-bits) from the PMA's client to the PMA.

24.3.1.2.1 Semantics of the service primitive

PMA_UNITDATA.request (tx_code-bit)

This primitive defines the transfer of data (in the form of code-bits) from the PCS or other client to the PMA. The tx_code-bit parameter can take one of two values: ONE or ZERO.

24.3.1.2.2 When generated

The PCS or other client continuously sends, at a nominal 125 Mb/s rate, the appropriate code-bit for transmission on the medium.

24.3.1.2.3 Effect of receipt

Upon receipt of this primitive, the PMA generates a PMD_UNITDATA request primitive, requesting transmission of the indicated code-bit, in NRZI format (tx_nrzi-bit), on the MDI.

24.3.1.3 PMA_UNITDATA.indicate

This primitive defines the transfer of data (in the form of code-bits) from the PMA to the PCS or other client.

24.3.1.3.1 Semantics of the service primitive

PMA_UNITDATA.indicate (rx_code-bit)

The data conveyed by PMA_UNITDATA.indicate is a continuous code-bit sequence at a nominal 125 Mb/s rate. The rx_code-bit parameter can take one of two values: ONE or ZERO.

24.3.1.3.2 When generated

The PMA continuously sends code-bits to the PCS or other client corresponding to the PMD_UNITDATA.indicate primitives received from the PMD.

24.3.1.3.3 Effect of receipt

The effect of receipt of this primitive by the client is unspecified by the PMA sublayer.

24.3.1.4 PMA_CARRIER.indicate

This primitive is generated by the PMA to indicate that a non-squelched, non-IDLE code-bit sequence is being received from the PMD. The purpose of this primitive is to give clients the earliest reliable indication of activity on the underlying continuous-signaling channel.

24.3.1.4.1 Semantics of the service primitive

PMA_CARRIER.indicate (carrier_status)

The carrier_status parameter can take on one of two values, ON or OFF, indicating whether a non-squelched, non-IDLE code-bit sequence (that is, carrier) is being received (ON) or not (OFF).

24.3.1.4.2 When generated

The PMA generates this primitive to indicate a change in the value of carrier_status.

24.3.1.4.3 Effect of receipt

The effect of receipt of this primitive by the client is unspecified by the PMA sublayer.

24.3.1.5 PMA_LINK.indicate

This primitive is generated by the PMA to indicate the status of the underlying PMD receive link.

24.3.1.5.1 Semantics of the service primitive

PMA_LINK.indicate (link_status)

The link_status parameter can take on one of three values: READY, OK, or FAIL, indicating whether the underlying receive channel is intact and ready to be enabled by Auto-Negotiation (READY), intact and enabled (OK), or not intact (FAIL). Link_status is set to FAIL when the PMD sets signal_status to OFF; when Auto-Negotiation (optional) sets link_control to DISABLE; or when Far-End Fault Detect (optional) sets faulting to TRUE. When link_status ↑ OK, then rx_code-bit and carrier_status are undefined.

24.3.1.5.2 When generated

The PMA generates this primitive to indicate a change in the value of link_status.

24.3.1.5.3 Effect of receipt

The effect of receipt of this primitive by the client is unspecified by the PMA sublayer.

24.3.1.6 PMA_LINK.request

This primitive is generated by the Auto-Negotiation algorithm, when implemented, to allow it to enable and disable operation of the PMA. See clause 28. When Auto-Negotiation is not implemented, the primitive is never invoked and the PMA behaves as if link_control = ENABLE.

24.3.1.6.1 Semantics of the service primitive

PMA_LINK request (link_control)

The link_control parameter takes on one of three values: SCAN_FOR_CARRIER, DISABLE, or ENABLE. Auto-Negotiation sets link_control to SCAN_FOR_CARRIER prior to receiving any fast link pulses, permitting the PMA to sense a 100BASE-X signal. Auto-Negotiation sets link_control to DISABLE when it senses an Auto-Negotiation partner (fast link pulses) and must temporarily disable the 100BASE-X PHY while negotiation ensues. Auto-Negotiation sets link_control to ENABLE when full control is passed to the 100BASE-X PHY.

24.3.1.6.2 When generated

Auto-Negotiation generates this primitive to indicate a change in link_control as described in clause 28.

24.3.1.6.3 Effect of receipt

This primitive affects operation of the PMA Link Monitor function as described in 24.3.4.4.

24.3.1.7 PMA_RXERROR.indicate

This primitive is generated by the PMA to indicate that an error has been detected during a carrier event.

24.3.1.7.1 Semantics of the service primitive

PMA_RXERROR.indicate (rxerror_status)

The rxerror_status parameter can take on one of two values: ERROR or NO_ERROR, indicating whether the received carrier event contains a detectable error (ERROR) or not (NO_ERROR). A carrier event is considered to be in error when it is not started by a Start-of-Stream Delimiter.

24.3.1.7.2 When generated

The PMA generates this primitive whenever a new, non-squelched carrier event is not started by a Start-of-Stream Delimiter.

24.3.1.7.3 Effect of receipt

The effect of receipt of this primitive by the client is unspecified by the PMA sublayer.

24.3.2 Functional requirements

The 100BASE-X PMA comprises the following functions:

a) Mapping of transmit and receive code-bits between the PMA Service Interface and the PMD Service Interface;
b) Link Monitor, which maps the PMD_SIGNAL.indicate primitive to the PMA_LINK.indicate primitive, indicating the availability of the underlying PMD;
c) Carrier Detection, which generates the PMA_CARRIER.indicate and PMA_RXERROR.indicate primitives from inspection of received PMD signals; and
d) Far-End Fault (optional), comprised of the Far-End Fault Generate and Far-End Fault Detect processes, which sense receive channel failures and send the Far-End Fault Indication, and sense the Far-End Fault Indication.

Figure 24-4 includes a functional block diagram of the PMA.

24.3.2.1 Far-End fault

Auto-Negotiation provides a Remote Fault capability useful for detection of asymmetric link failures; i.e., channel error conditions detected by the far-end station but not the near-end station. Since Auto-Negotiation is specified only for media supporting eight-pin modular connectors, such as used by 100BASE-TX over unshielded twisted pair, Auto-Negotiation's Remote Fault capability is unavailable to other media for which it may be functionally beneficial, such as 100BASE-TX over shielded twisted pair or 100BASE-FX. A remote fault capability for 100BASE-FX is particularly useful due to this medium's applicability over longer distances (making end-station checking inconvenient) and for backbones (in which detection of link failures can trigger redundant systems).

For these reasons, 100BASE-X provides an optional Far-End Fault facility when Auto-Negotiation cannot be used. Far-End Fault shall not be implemented for media capable of supporting Auto-Negotiation.

When no signal is being received, as indicated by the PMD's signal detect function, the Far-End Fault feature permits the station to transmit a special Far-End Fault Indication to its far-end peer. The Far-End Fault Indication is sent only when a physical error condition is sensed on the receive channel. In all other situations, including reception of the Far-End Fault Indication itself, the PMA passes through tx_code-bit. (Note that the Far-End Fault architecture is such that IDLEs are automatically transmitted when the Far-End Fault Indication is detected. This is necessary to re-establish communication when the link is repaired.)

The Far-End Fault Indication is comprised of three or more repeating cycles, each of 84 ONEs followed by a single ZERO. This signal is sent in-band and is readily detectable but is constructed so as to not satisfy the 100BASE-X carrier sense criterion. It is therefore transparent to the PMA's client and to stations not implementing Far-End Fault.

As shown in figure 24-4, Far-End Fault is implemented through the Far-End Fault Generate, Far-End Fault Detect and the Link Monitor processes.

The Far-End Fault Generate process, which is interposed between the incoming tx_code-bit stream and the TX process, is responsible for sensing a receive channel failure (signal_status=OFF) and transmitting the Far-End Fault Indication in response. The transmission of the Far-End Fault Indication may start or stop at any time depending only on signal_status.

The Far-End Fault Detect process continuously monitors rx_code-bits from the RX process for the Far-End Fault Indication. Detection of the Far-End Fault Indication disables the station by causing the Link Monitor process to deassert link_status, which in turn causes the station to source IDLEs. Far-End Fault detection can also be used by management functions not specified in this clause.

24.3.2.2 Comparison to previous 802.3 PMAs

Previous 802.3 PMA's perform the additional functions of SQE Test and Jabber. Neither of these functions is implemented in the 100BASE-X PMA.

SQE Test is provided in other Physical Layers to check the integrity of the Collision Detection mechanism independently of the Transmit and Receive capabilities of the Physical Layer. Since 100BASE-X effects collision detection by sensing receptions that occur during transmissions, collision detection is dependent on the health of the receive channel. By checking the ability to properly receive signals from the PMD, the Link Monitor function therefore functionally subsumes the functions previously implemented by SQE Test.

The Jabber function prevents a DTE from causing total network failure under certain classes of faults. When using mixing media (e.g., coaxial cables or passive optical star couplers), this function must naturally be implemented in the DTE. 100BASE-X requires the use of an active repeater, with one DTE or repeater attached to each port. As an implementation optimization, the Jabber function has therefore been moved to the repeater in 100BASE-X.

24.3.3 State variables

24.3.3.1 Constants

FEF_CYCLES

The number of consecutive cycles (of FEF_ONES ONEs and a single ZERO) necessary to indicate the Far-End Fault Indication. This value is 3.

FEF_ONES

The number of consecutive ONEs to be transmitted for each cycle of the Far-End Fault Indication. This value is 84.

24.3.3.2 Variables

carrier_status

The carrier_status parameter to be communicated by the Carrier Detect process through the PMA_CARRIER.indicate primitive. Carrier is defined as receipt of 2 noncontiguous ZEROes in 10 code-bits.

Values: ON; carrier is being received
OFF; carrier is not being received

faulting

The faulting variable set by the Far-End Fault Detect process, when implemented, indicating whether or not a Far-End Fault Indication is being sensed. This variable is used by the Link Monitor process to force link_status to FAIL.When Far-End Fault is not implemented, this variable is always FALSE.

Values: TRUE; Far-End Fault Indication is being sensed
FALSE; Far-End Fault Indication is not being sensed

link_control

The link_control parameter as communicated by the PMA_LINK.request primitive. When Auto-Negotiation is not implemented, the value of link_control is always ENABLE. See clause 28 for a complete definition.

link_status

The link_status parameter as communicated by the Link Monitor process through the PMA_LINK.indicate primitive.

Values: FAIL; the receive channel is not intact
READY; the receive channel is intact and ready to be enabled by Auto-Negotiation
OK; the receive channel is intact and enabled for reception

r_bits [9:0]

In Carrier Detect, a vector of the 10 most recently received code-bits from the PMD RX process. r_bits [0] is the most recently received (newest) code-bit; r_bits [9] is the least recently received code-bit (oldest). r_bits is an internal variable used exclusively by the Carrier Detect process.

rx_code-bit

The rx_code-bit parameter as delivered by the RX process, which operates in synchronism with the PMD_UNITDATA.indicate primitive. rx_code-bit is the most recently received code-bit from the PMD after conversion from NRZI.

rxcrror_status

The rxcrror_status parameter to be communicated by the Carrier Detect process through the PMA_RXERROR.indicate primitive.

Values: NO_ERROR; no error detected in the carrier event being received
ERROR; the carrier event being received is in error

signal_status

The signal_status parameter as communicated by the PMD_SIGNAL.indicate primitive.

Values: ON; the quality and level of the received signal is satisfactory
OFF; the quality and level of the received signal is not satisfactory

tx_code-bit_in

In Link Fault Generate, the tx_code-bit parameter as conveyed to the PMA from the PMA client by the PMA_UNITDATA request.

tx_code-bit_out

In Link Fault Generate, the tx_code-bit parameter to be passed to the TX process. Note that this is called tx_code-bit by the TX process.

24.3.3.3 Functions

SHIFTLEFT (rx_bits)

In Carrier Detect, this function shifts rx_bits left one bit placing rx_bits [8] in rx_bits [9], rx_bits [7] in rx_bits [8] and so on until rx_bits [1] gets rx_bits [0].

24.3.3.4 Timers

stabilize_timer

An implementation-dependent delay timer between 330 µs and 1000 µs, inclusive, to ensure that the link is stable.

24.3.3.5 Counters

num_cycles

In Link Fault Detect, a counter containing the number of consecutive Far-End Fault cycles currently sensed. This counter gets reset on intialization or when the bit stream fails to qualify as a potential Far-End Fault Indication. It never exceeds FEF_CYCLES.

num_ones

This represents two separate and independent counters: In Link Fault Generate, a counter containing the number of consecutive ONEs already sent during this cycle of the Far-End Fault Indication. In Link Fault Detect, a counter containing the number of consecutive ONEs currently sensed; it gets reset whenever a ZERO is detected or when the bit stream fails to qualify as a potential Far-End Fault Indication. These counters never exceed FEF_ONES.

24.3.3.6 Messages

PMD_UNITDATA.indicate (rx_nrzi-bit)

A signal sent by the PMD signifying that the next nrzi-bit is available from the medium. nrzi-bit is converted (instantaneously) to code-bit by the RX process and used by the Carrier Detect process.

5xPMD_UNITDATA.indicates

In Carrier Detect, this shorthand notation represents repetition of the preceding state five times synchronized with five successive PMD_UNITDATA.indicates.

PMA_UNITDATA request (tx_code-bit)

A signal sent by the PMA's client signifying that the next nrzi-bit is available for transmission. For this process, the tx_code-bit parameter is interpreted as tx_code-bit_in.

24.3.4 Process specifications and state diagrams

24.3.4.1 TX

The TX process passes data from the PMA's client directly to the PMD. The PMA shall implement the TX process as follows: Upon receipt of a PMA_UNITDATA request (tx_code-bit), the PMA performs a conversion to NRZI format and generates a PMD_UNITDATA request (tx_nrzi-bit) primitive with the same logical value for the tx_nrzi-bit parameter. Note that tx_code-bit is equivalent to tx_code-bit_out of the Link Fault Generate process when implemented.

24.3.4.2 RX

The RX process passes data from the PMD directly to the PMA's client and to the Carrier Detect process. The PMA shall implement the RX process as follows: Upon receipt of a PMD_UNITDATA.indicate (rx_nrzi-bit),