Trials@uspto.gov
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Paper 67
Entered: August 2, 2018

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

APPLE INC.,
Petitioner,

v.

CALIFORNIA INSTITUTE OF TECHNOLOGY,
Patent Owner.

Case IPR2017-00701
Patent 7,421,032 B2

Before KEN B. BARRETT, TREVOR M. JEFFERSON, and JOHN A. HUDALLA, *Administrative Patent Judges*.

BARRETT, *Administrative Patent Judge.*

FINAL WRITTEN DECISION
Inter Partes Review
35 U.S.C. § 318(a) and 37 C.F.R. § 42.73

I. INTRODUCTION

A. Background and Summary

Apple Inc. ("Petitioner") filed a Petition requesting *inter partes* review of U.S. Patent No. 7,421,032 B2, issued September 2, 2008 ("the '032 patent," Ex. 1101). Paper 3 ("Pet."). The Petition challenges the patentability of claims 1–10 of the '032 patent on the ground of obviousness under 35 U.S.C. § 103. California Institute of Technology ("Patent Owner") filed a Preliminary Response to the Petition. Paper 13 ("Prelim. Resp."). We instituted *inter partes* review (Paper 14, "Inst. Dec.") of claims 1 and 4–10 based on Ping, MacKay, Divsalar, and Luby97. However, the instituted review did not include Petitioner's obviousness challenge of claims 2 and 3 based on those same references.

Patent Owner filed a Response to the Petition (Paper 32, "PO Resp."), and Petitioner filed a Reply (Paper 45, "Pet. Reply"). Pursuant to our authorization (Paper 43), Patent Owner filed a Sur-Reply (Paper 55, "PO Sur-Reply").

An oral hearing was held on May 8, 2018, and a transcript of the hearing is included in the record. Paper 66 ("Tr.").

As authorized in our Order of February 10, 2018 (Paper 41), Patent Owner filed a motion for sanctions related to Petitioner's cross-examination of Patent Owner's witnesses, Dr. Mitzenmacher and Dr. Divsalar (Paper 42), and Petitioner filed an opposition (Paper 47).

Additionally, Patent Owner filed a Motion to Exclude evidence (Paper 52), to which Petitioner filed an Opposition (Paper 54), and Patent Owner filed a Reply (Paper 58).

On April 24, 2018, the Supreme Court held that a decision to institute under 35 U.S.C. § 314 may not institute on fewer than all claims challenged in the petition. *SAS Inst., Inc. v. Iancu*, 138 S. Ct. 1348 (U.S. Apr. 24, 2018). On May 3, 2018, we issued an order modifying our institution decision to institute on all of the challenged claims and all of the grounds presented in the Petition. Paper 60. Subsequently, the parties filed a joint motion to limit the Petition to the claims and grounds that were originally instituted. Paper 64. We granted the motion. Paper 65. As a result, the remaining instituted claims and grounds are the same as they had been at the time of the Institution Decision. *See id.* at 3.

We have jurisdiction under 35 U.S.C. § 6. This Final Written Decision is entered pursuant to 35 U.S.C. § 318(a). After consideration of the parties' arguments and evidence, and for the reasons discussed below, we determine that Petitioner has *not* shown by a preponderance of the evidence that claims 1 and 4–10 of the '032 patent are unpatentable.

B. Related Proceedings

One or both parties identify, as matters involving or related to the '032 patent, *Cal. Inst. of Tech. v. Broadcom Ltd.*, No. 2:16-cv-03714 (C.D. Cal. filed May 26, 2016) and *Cal. Inst. of Tech. v. Hughes Commc'ns, Inc.*, 2:13-cv-07245 (C.D. Cal. filed Oct. 1, 2013), and Patent Trial and Appeal Board cases IPR2015-00059, IPR2015-00060, IPR2015-00061, IPR 2015-00067, IPR2015-00068, IPR2015-00081, IPR2017-00210, IPR2017-00211, IPR2017-00219, IPR2017-00297, IPR2017-00423, IPR2017-00700, and IPR2017-00728. Pet. 3, Paper 7.

C. The '032 Patent

The '032 patent is titled "Serial Concatenation of Interleaved Convolutional Codes Forming Turbo-Like Codes." Ex. 1101, [54]. The '032 patent explains some of the prior art with reference to its Figure 1, reproduced below.

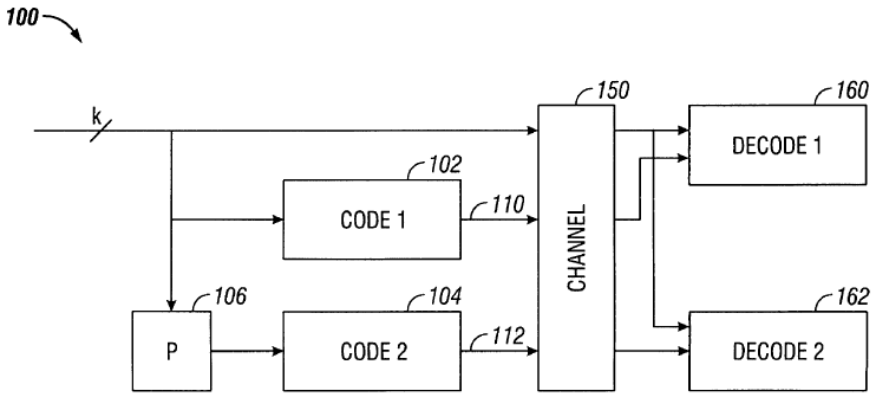

Figure 1 is a schematic diagram of a prior "turbo code" system. *Id.* at 2:16–17. The '032 patent specification describes Figure 1 as follows:

> A block of k information bits is input directly to a first coder 102. A k bit interleaver 106 also receives the k bits and interleaves them prior to applying them to a second coder 104. The second coder produces an output that has more bits than its input, that is, it is a coder with rate that is less than 1. The coders 102, 104 are typically recursive convolutional coders.
>
> Three different items are sent over the channel 150: the original k bits, first encoded bits 110, and second encoded bits 112. At the decoding end, two decoders are used: a first constituent decoder 160 and a second constituent decoder 162. Each receives both the original k bits, and one of the encoded portions 110, 112. Each decoder sends likelihood estimates of the decoded bits to the other decoders. The estimates are used to decode the uncoded information bits as corrupted by the noisy channel.

Id. at 1:41–56.

A coder 200, according to a first embodiment of the invention, is described with reference to Figure 2, reproduced below.

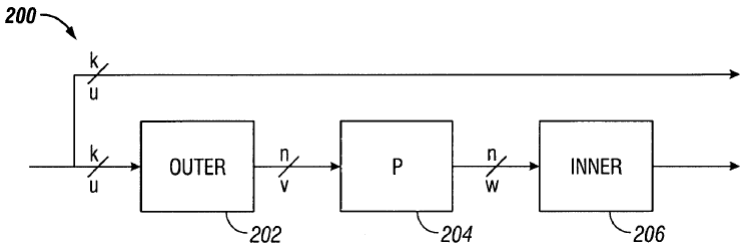

Figure 2 of the '032 patent is a schematic diagram of coder 200.

> The coder 200 may include an outer coder 202, an interleaver 204, and inner coder 206. . . . The outer coder 202 receives the uncoded data. The data may be partitioned into blocks of fixed size, say k bits. The outer coder may be an (n,k) binary linear block coder, where n>k. The coder accepts as input a block u of k data bits and produces an output block v of n data bits. The mathematical relationship between u and v is $v=T_0u$, where T_0 is an n×k matrix, and the rate[1] of the coder is k/n.
>
> The rate of the coder may be irregular, that is, the value of T_0 is not constant, and may differ for sub-blocks of bits in the data block. In an embodiment, the outer coder 202 is a repeater that repeats the k bits in a block a number of times q to produce a block with n bits, where n=qk. Since the repeater has an irregular output, different bits in the block may be repeated a different number of times. For example, a fraction of the bits in the block may be repeated two times, a fraction of bits may be repeated three times, and the remainder of bits may be repeated four times. These fractions define a degree sequence, or degree profile, of the code.
>
> The inner coder 206 may be a linear rate-1 coder, which means that the n-bit output block x can be written as $x=T_Iw$, where T_I is a nonsingular n×n matrix. The inner coder 210 can

[1] We understand that the "rate" of an encoder refers to the ratio of the number of input bits to the number of resulting encoded output bits related to those input bits.

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