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BEFORE THE PATENT TRIAL AND APPEAL BOARD

LG Electronics, Inc. Petitioner,

> v. FastVDO LLC Patent Owner.

Patent No. 5,850,482

Inter Parte Review No.

U.S. Patent No. 5,218,622 to Fazel et. al.

Exhibit 1006

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US005218622A

United States Patent [19]

Fazel et al.

- [54] SYSTEM OF ENCODING DIGITAL SIGNALS INTENDED FOR TRANSMISSION AND/OR STORAGE AND A CORRESPONDING DECODING SYSTEM
- [75] Inventors: Khaled Fazel, Vincennes; Jean-Jacques Lhuillier, Saint-Maur, both of France
- [73] Assignee: U.S. Philips Corporation, New York, N.Y.
- [21] Appl. No.: 630,700
- [22] Filed: Dec. 20, 1990
- [30] Foreign Application Priority Data

Dec. 29, 1989 [F.	R] France	 89 17452
Feb. 16, 1990 [F]	R] France	 90 01891
Mar. 16, 1990 [F]	R] France	 90 03406

- [51] Int. Cl.⁵ H04N 11/02 [52]
- 371/37.1 [58] Field of Search 375/25, 31, 34, 122;
- 358/133, 138, 426, 427, 430; 341/65, 67; 371/37.1, 41

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U.S. PATENT DOCUMENTS

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4,782,387	11/1988	Sabri et al	358/138
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5,218,622 [11] Patent Number:

[45] Date of Patent: Jun. 8, 1993

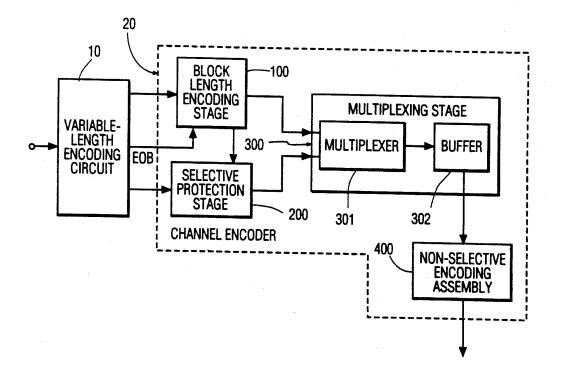
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Primary Examiner-Benedict V. Safourek Attorney, Agent, or Firm-Michael E. Marion

[57] ABSTRACT

A system of encoding digital signals comprising a source encoder followed by a transmission channel encoder, which is characterized in that in the case in which the source encoder is a variable-length encoding circuit (10), the channel encoder comprises a series arrangement of a sub-assembly of encoding with selective protection and a sub-assembly of encoding without selective protection. The signals being arranged in information component blocks. The system includes a stage for encoding lengths of blocks for determining along the block an accumulated length of code words supplied by said source encoder and ensuring the encoding of block lengths thus determined, a stage for selective protection of said blocks and a stage for multiplexing the signals supplied by said length encoding and selective protection stages. The corresponding decoding system comprises a transmission channel decoder followed by a source decoder, the channel decoder comprising a series arrangement of a sub-assembly for decoding with non-selective protection and a subassembly for decoding with n levels of selective protection.

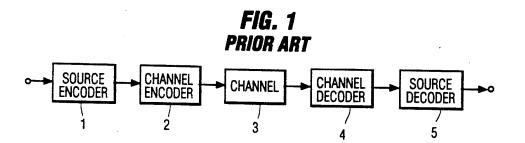
12 Claims, 4 Drawing Sheets

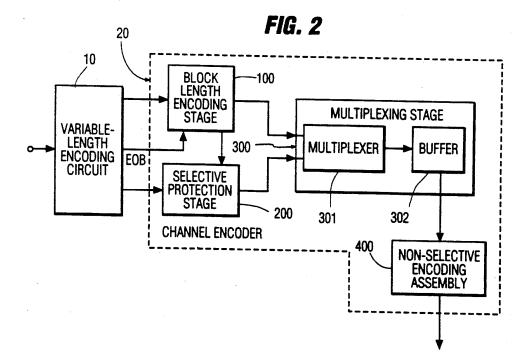


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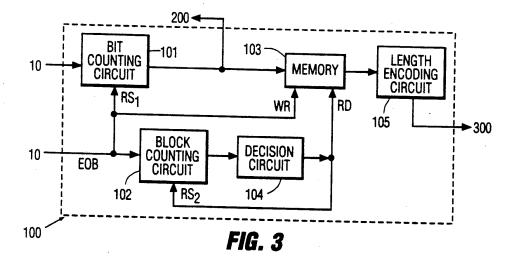
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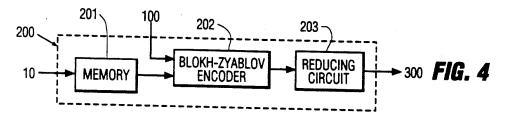


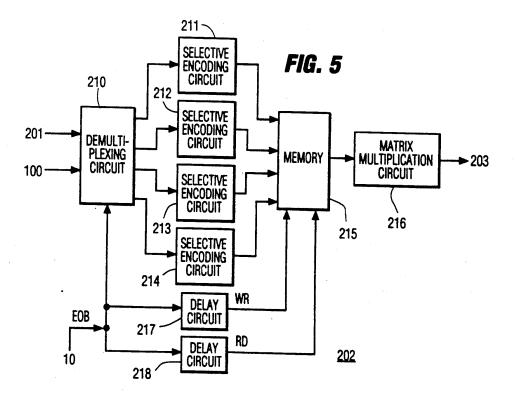


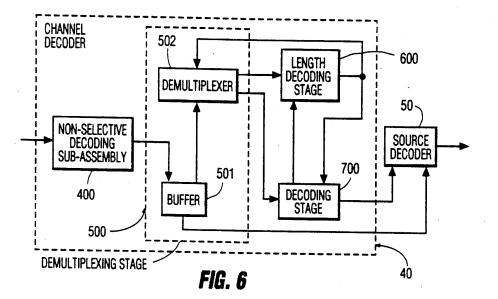
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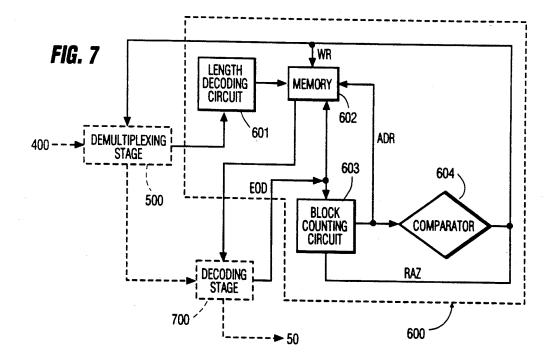
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