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INVENTORS: Chau, Kwok Kit

TITLE: MPEG decoder system and method
having a unified memory for transport
decode and system controller functions

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FILED: 13 NOV 1996
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102			

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FILED: LOS ANGELES, CA.

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***** APPLICATIONS *****

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119 conditions met	<input type="checkbox"/> yes <input checked="" type="checkbox"/> no	→	US	16	20	3	\$770.00	5201 01300

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PATENT LAW DEPT
MILPITAS, CA 95035

SYSTEM AND METHOD HAVING A UNIFIED MEMORY FOR TRANSPORT AND SYSTEM CONTROLLER FUNCTIONS

U.S. DEPT. OF COMM. / PAT. & TM—PTO-438L (Rev.12-84)

OF APPLICATION SEPARATELY		M. Cal Applications Examiner	
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1998		Total Claims	Print Claim
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PHO K. NGUYEN PRIMARY EXAMINER GROUP 2400 Shu Nguyen Primary Examiner		Print Fig. 3	
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PTO-438A
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(FACE)

5,870,087

MPEG DECODER SYSTEM AND METHOD HAVING A UNIFIED
MEMORY FOR TRANSPORT DECODE AND SYSTEM CONTROLLER
FUNCTIONS

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09-18-1997	Information Disclosure Statement (IDS) Filed
09-18-1997	Information Disclosure Statement (IDS) Filed
02-04-1998	Case Docketed to Examiner in GAU
04-27-1998	Case Docketed to Examiner in GAU
05-11-1998	Mail Non-Final Rejection
05-11-1998	Non-Final Rejection
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06-16-1998	Date Forwarded to Examiner
09-02-1998	Mail Notice of Allowance
09-02-1998	Notice of Allowance Data Verification Completed
10-26-1998	Issue Fee Payment Verified
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11-09-1998	Drawing(s) Matched to Application
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01-11-1999	Issue Notification Mailed
02-09-1999	Recordation of Patent Grant Mailed
02-22-2016	Petition Requesting Trial
06-29-2016	File Marked Found
08-22-2016	Request for Trial Granted in Part

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PATENT APPLICATION



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	1. Application <i>16pts.</i> papers.	
	2. <i>IDS</i>	<i>Sept 18 97</i>
<i>5-11-98</i>	3. <i>Rejection (3 mos)</i>	<i>MAY 1 1998 T.H.B.</i>
	4. <i>Amend A</i>	<i>6-8-98</i>
<i>8-21-98</i>	5. <i>Notice of Allowance</i>	<i>SEP 02 1998 T.H.B.</i>
<i>11/2/98</i>	6. <i>Formal Drawings (16 sheets) set 1</i>	<i>10/26/98</i>
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(REV. 8-81)

U.S. GOVERNMENT PRINTING OFFICE 1007-100-100

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PHU K. NGUYEN

ISSUE CLASSIFICATION SLIP

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PATENT AND TRADEMARK OFFICE

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SYMBOLS
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SEARCHED			
Class	Sub.	Date	Exmr.
345	302		
345	418	5/6/98	cc ✓
345	302 418	6/17/98	a ✓
707	101 102 103 104	6/17/98	✓
update searched		8/25/98	cc ✓

SEARCH NOTES		
	Date	Exmr.

[illegible]

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Page 6



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United States Patent [19]
Chau

[11] **Patent Number:** **5,870,087**
[45] **Date of Patent:** **Feb. 9, 1999**

[54] **MPEG DECODER SYSTEM AND METHOD
HAVING A UNIFIED MEMORY FOR
TRANSPORT DECODE AND SYSTEM
CONTROLLER FUNCTIONS**

[75] **Inventor:** **Kwok Kit Chau**, Los Altos, Calif.

[73] **Assignee:** **LSI Logic Corporation**, Milpitas,
Calif.

[21] **Appl. No.:** **748,269**

[22] **Filed:** **Nov. 13, 1996**

[51] **Int. Cl.⁶** **G06T 13/00**

[52] **U.S. Cl.** **345/302**

[58] **Field of Search** 345/302, 418;
707/101, 102, 103, 104

[56] **References Cited**

U.S. PATENT DOCUMENTS

5,675,511 10/1997 Prasad et al. 345/302
5,692,213 11/1997 Goldberg et al. 345/302
5,767,846 6/1998 Nakamura et al. 345/302

Primary Examiner—Phu K. Nguyen

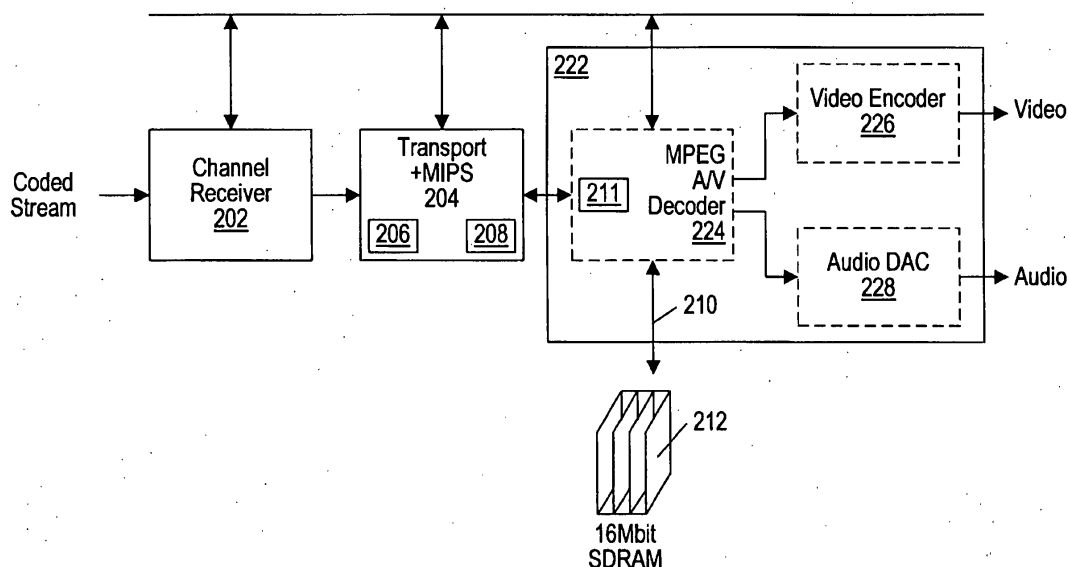
Assistant Examiner—Cliff N. Vo

Attorney, Agent, or Firm—Conley, Rose & Tayon; Jeffrey C.
Hood

[57] **ABSTRACT**

An MPEG decoder system and method for performing video decoding or decompression which includes a unified memory for multiple functions according to the present invention. The video decoding system includes transport logic, a system controller, and MPEG decoder logic. The video decoding system of the present invention includes a single unified memory which stores code and data for the transport, system controller and MPEG decoder functions. The single unified memory is preferably a 16 Mbit memory. The MPEG decoder logic includes a memory controller which couples to the single unified memory, and each of the transport logic, system controller and MPEG decoder logic access the single unified memory through the memory controller. The video decoding system implements various frame memory saving schemes, such as compression or dynamic allocation, to more efficiently use the memory. In one embodiment, the memory is not required to store reconstructed frame data during B-frame reconstruction, thus considerably reducing the required amount of memory for this function. Alternatively, the memory is only required to store a portion of the reconstructed frame data. In addition, these savings in memory allow portions of the memory to also be used for transport and system controller functions. The present invention thus provides a video decoding system with reduced memory requirements.

20 Claims, 16 Drawing Sheets



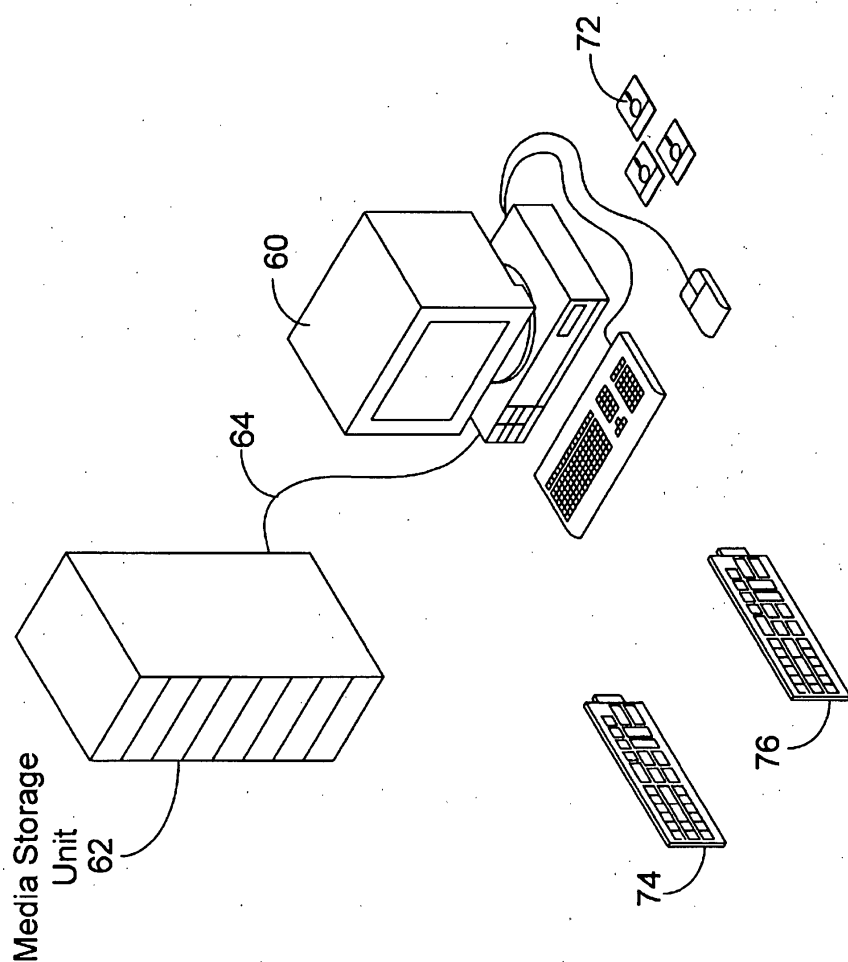


FIG. 1

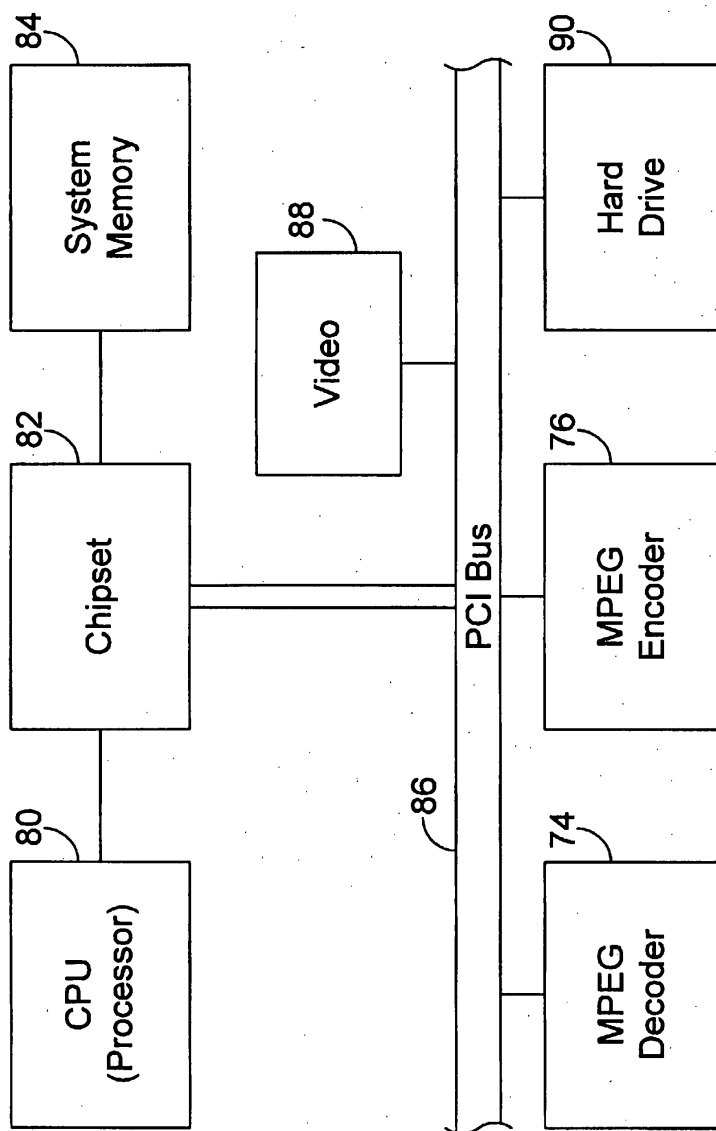


FIG. 2

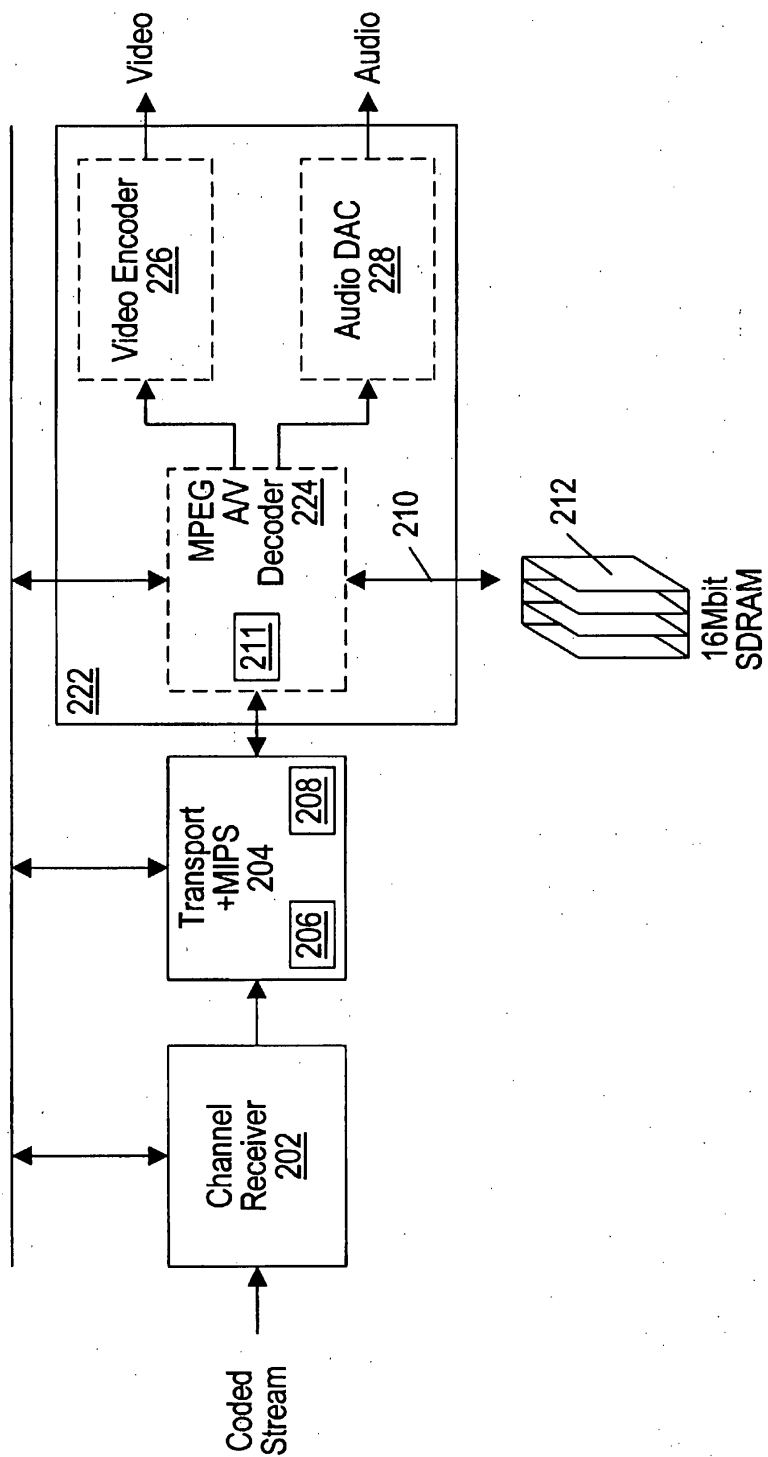


FIG. 3

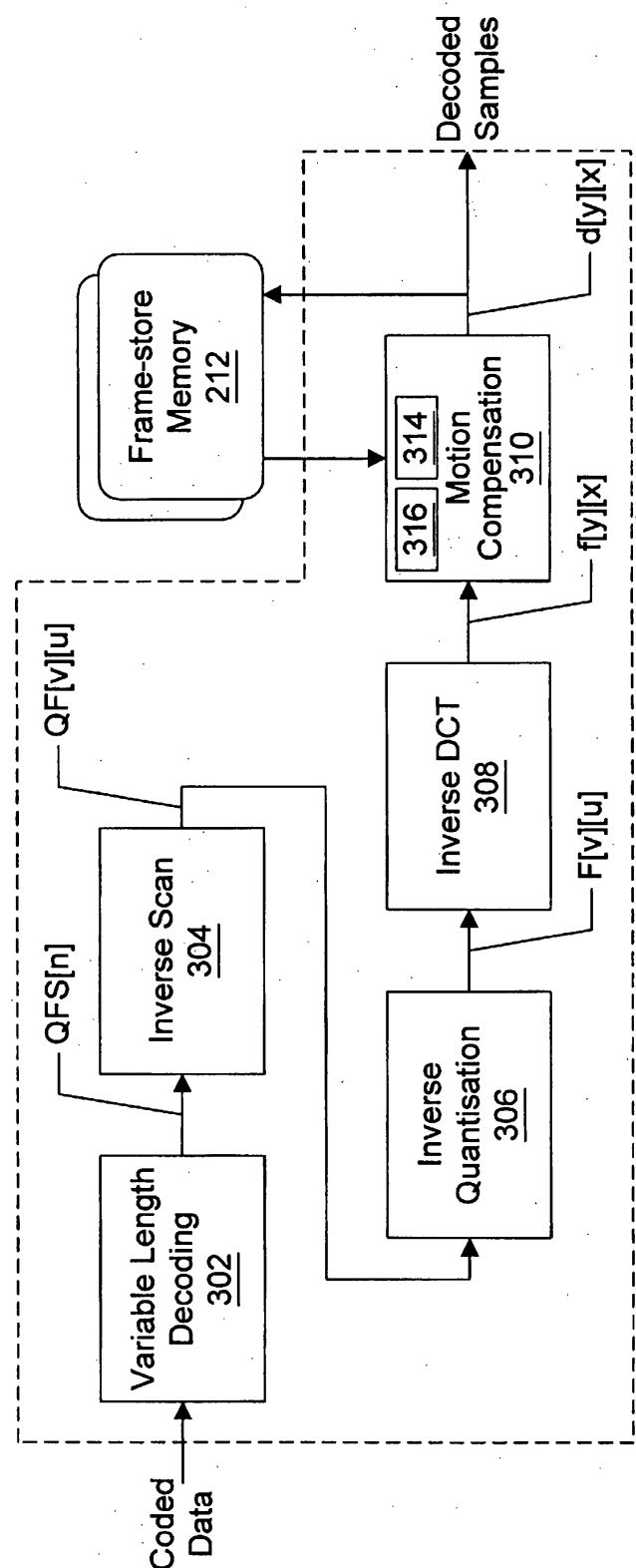
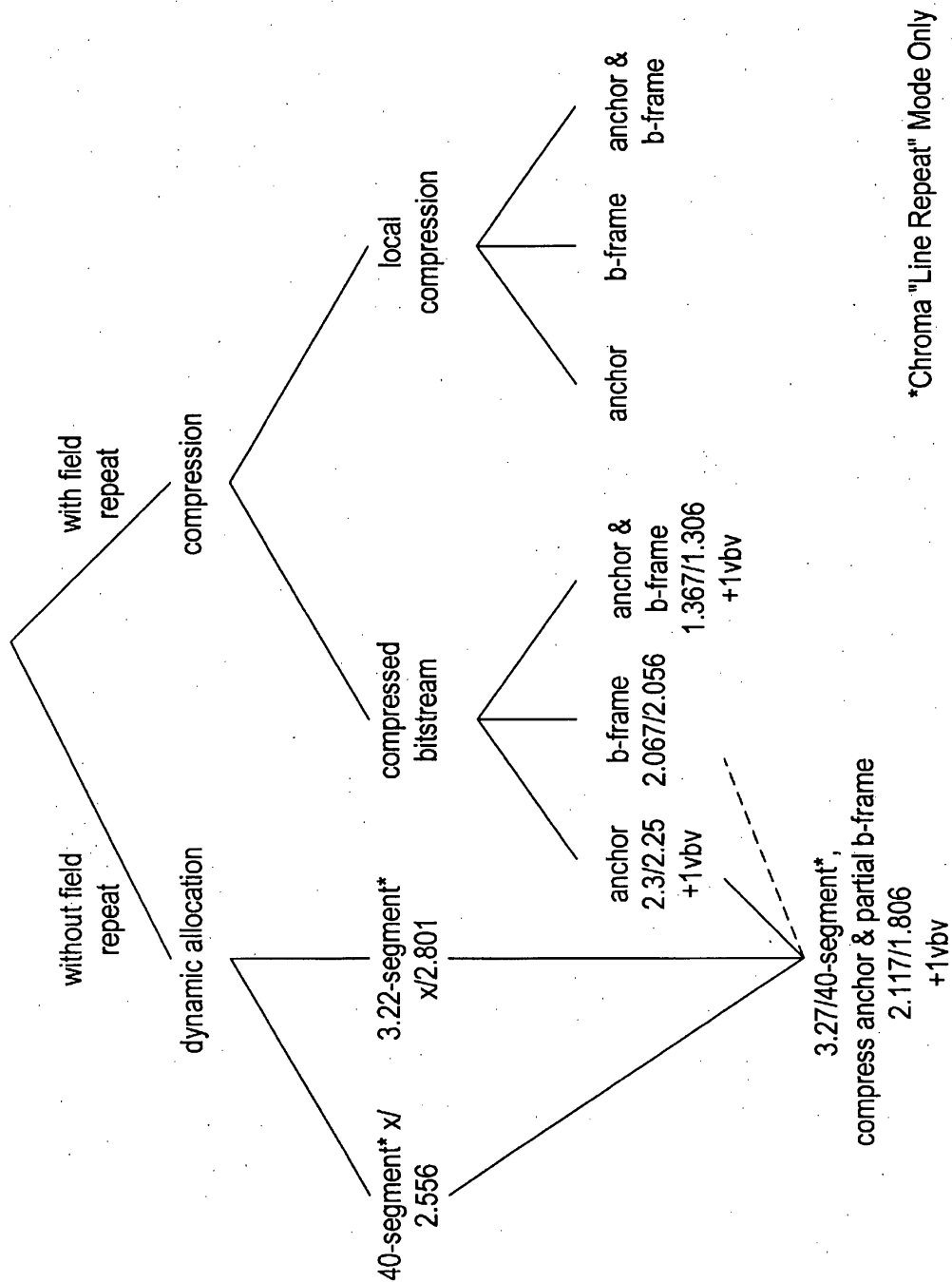


FIG. 4



*Chroma "Line Repeat" Mode Only

FIG. 5

Table 1
MPEG Decoder: Memory Partition

	L64005		Compress Displayed Anchor	
	NTSC	PAL	NTSC	PAL
frame store (number of frames)	12,441,600 (3,000)	12,718,080 (2,556)	9,538,560 (2,300)	11,197,440 (2,250)
vbv buffer	1,805,008	1,805,008	3,610,016	3,610,016
video non-instantaneous decode	430,765	520,575		
video-display sync	500,000	600,000		
audio buffer	28,672	28,672		
audio-video latency difference	19,200	23,040		
audio-display sync	12,800	15,360		
video transport buffer	4,096	4,096		
audio transport buffer	4,096	4,096		
4ms jitter at 15Mbps	60,000	60,000		
sub-total for channel buffer	2,864,637	3,060,847	4,669,645	4,865,855
packet header overhead	20,000	20,000		
OSD	675,840	808,192		
sub-total for software & data	775,139	170,097		
Grand Total	16,777,216	16,777,216	1,873,171	(114,271)
frame store + channel buffer	15,306,237	15,778,927	14,208,205	16,063,295

FIG. 6A

Table 1
MPEG Decoder: Memory Partition

Compress Anchor & Segment B		Compress B-Frame		Compress Anchor & B-Frame	
NTSC: 3.267 segments 8,778,240 (2.117)	PAL: 40 segments 8,985,600 (1.806)	NTSC 8,570,880 (2.067)	PAL 10,229,760 (2.056)	NTSC 5,667,840 (1.367)	PAL 6,497,280 (1.306)
3,610,016	3,610,016			3,610,016	3,610,016
4,669,645	4,865,855			4,669,645	4,865,855
2,633,491	2,097,569	4,645,859	2,658,417	5,743,891	4,585,889
13,447,885	13,851,455	11,435,517	13,290,607	10,337,485	11,363,135

FIG. 6B

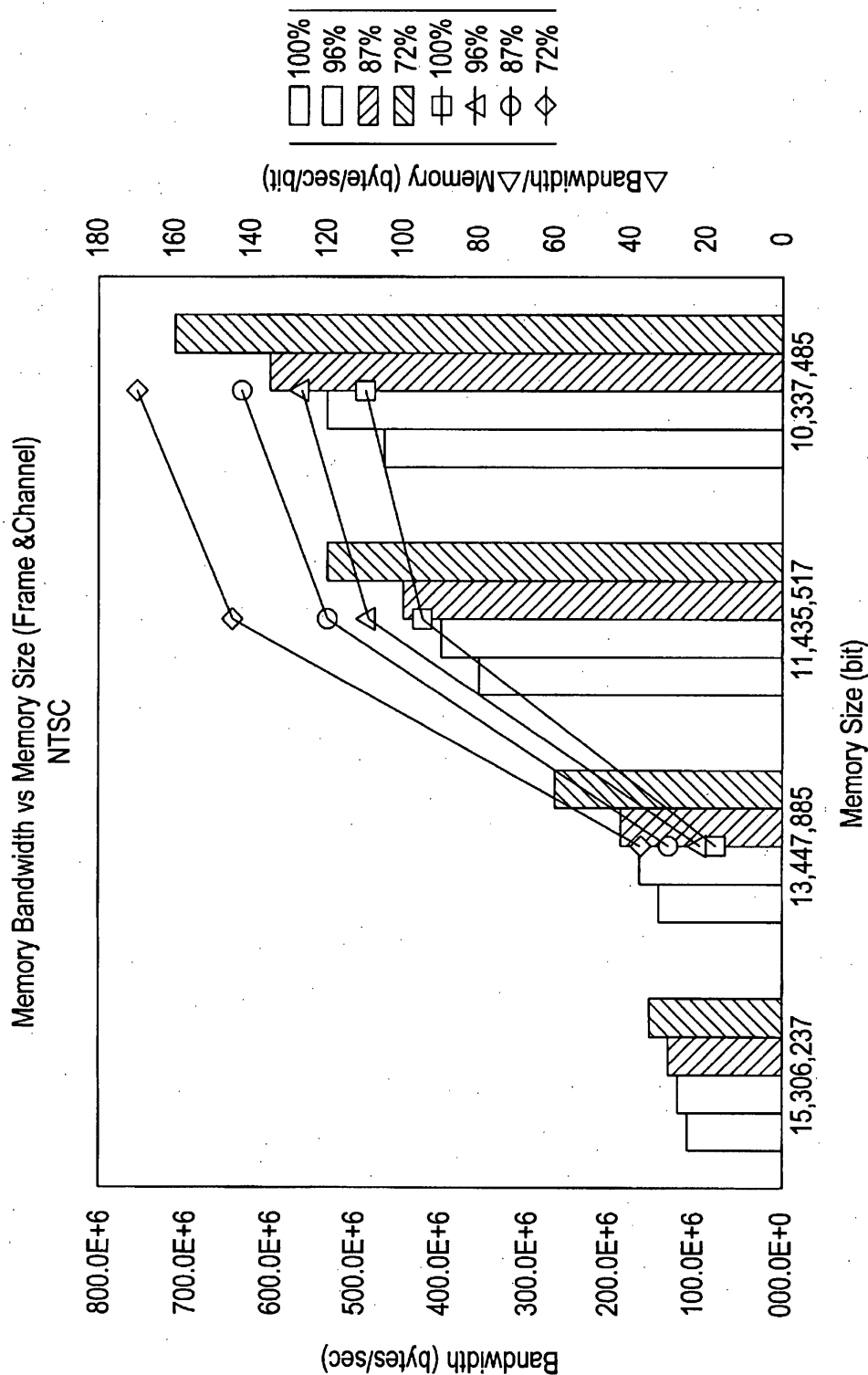


FIG. 7

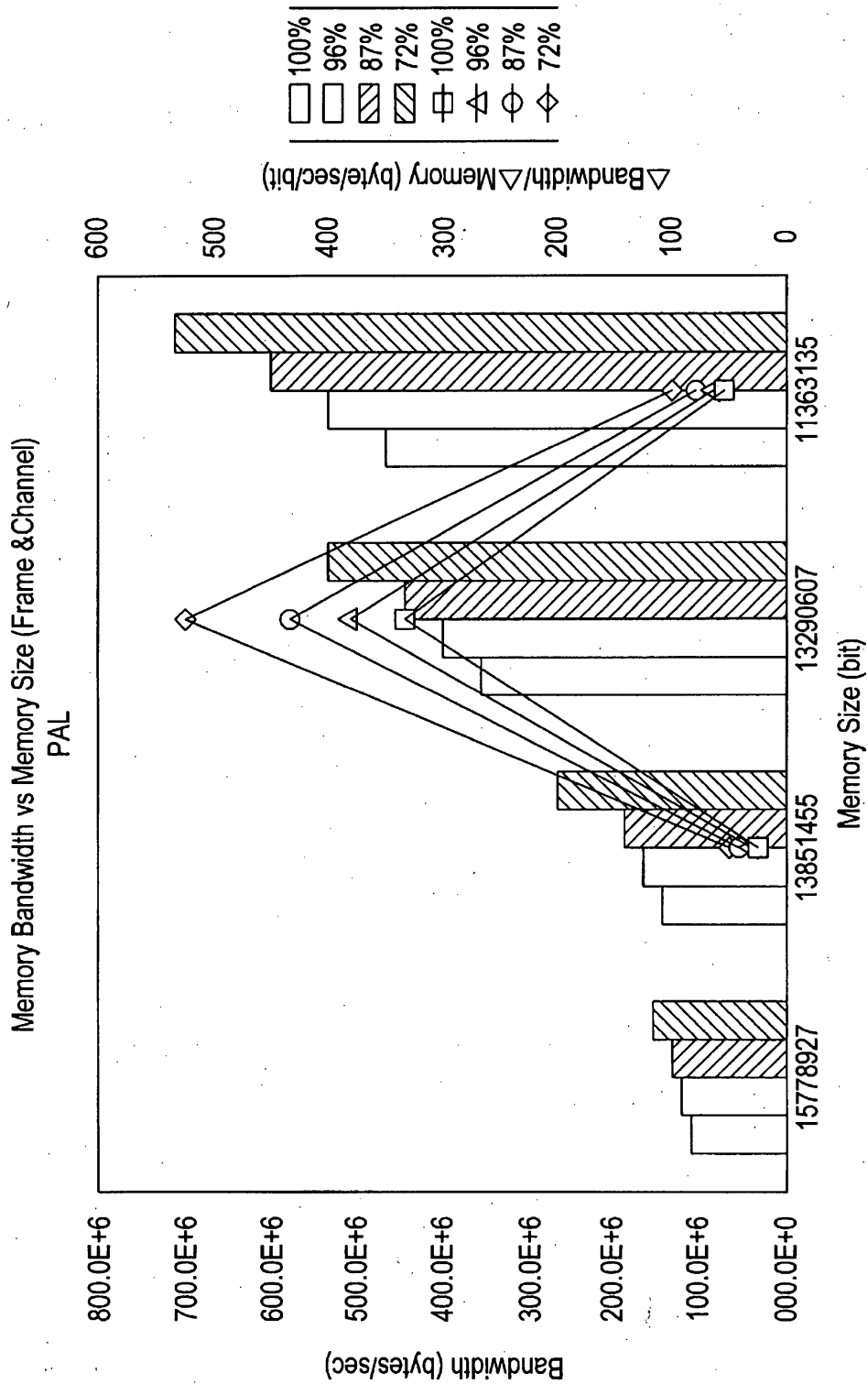


FIG. 8

	bit	
	NTSC	PAL
Video Frames (incl. compressed)	10,583,248	10,790,608
VBV Buffer	1,805,008	1,805,008
Video Decode Buffer	430,765	520,575
Video-Display Sync Buffer	500,000	600,000
Audio Buffer	28,672	28,672
Audio-Video Latency Buffer	19,200	23,040
Audio-Display Sync Buffer	12,800	15,360
Transport Buffer	8,192	8,192
Jitter Buffer (4ms)	60,000	60,000
PES Header Overhead	20,000	20,000
OSD	675,840	808,192
MIPS Code and Data	2,633,491	2,097,569

FIG. 9

	Bandwidth (Mbyte/sec)	
	NTSC	PAL
Channel In/Out	18.82	15.98
Motion Compensation	72.70	72.59
Store	38.29	38.23
Display & OSD	30.38	30.38
TOTAL	160.19	157.18

- With 16x1M SDRAM running at 100 MHz, Bandwidth Available is 200Mbyte/sec
- Expecting 20Mbyte/sec for MIPS Code and Data

FIG. 10

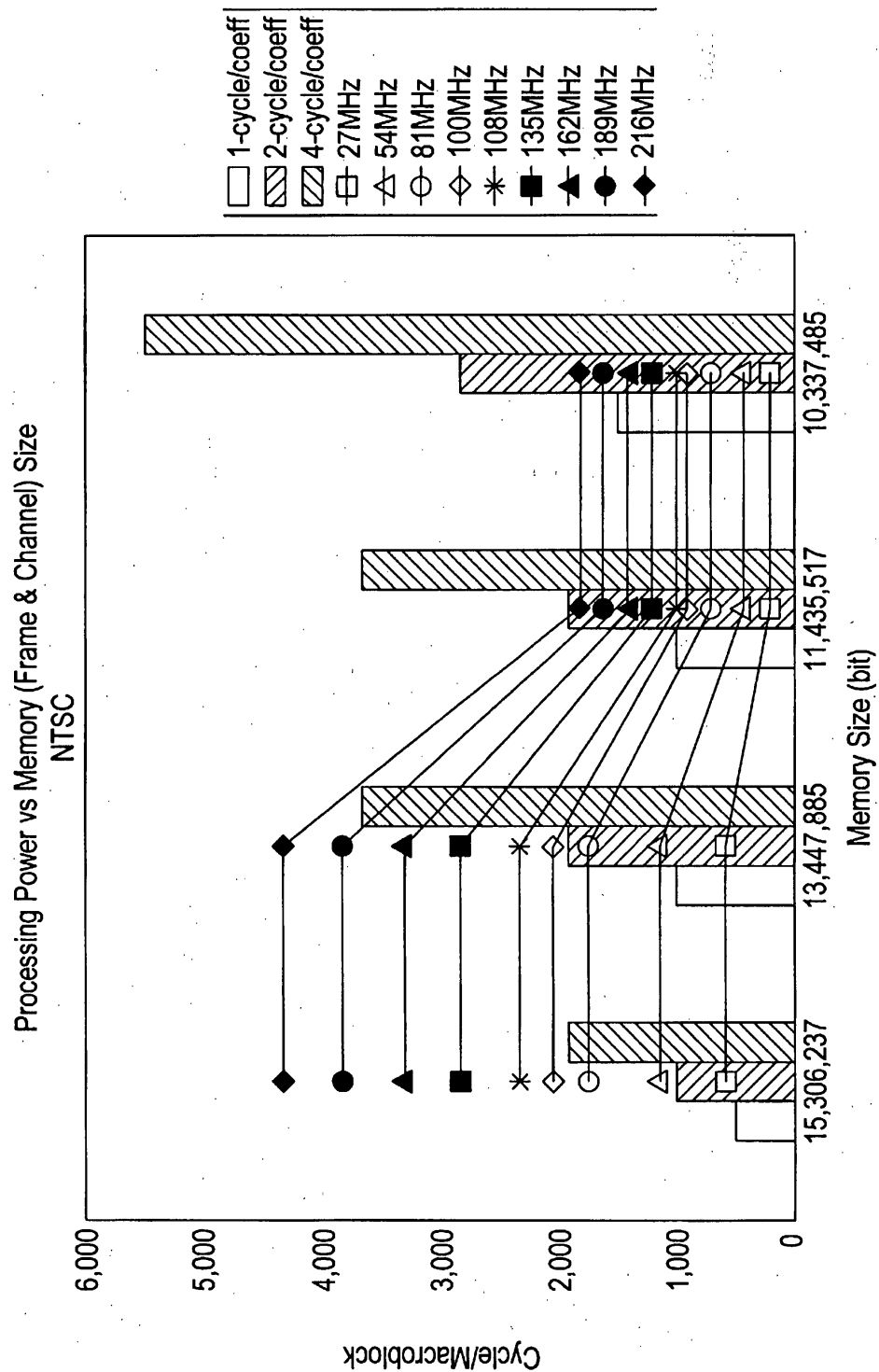


FIG. 11

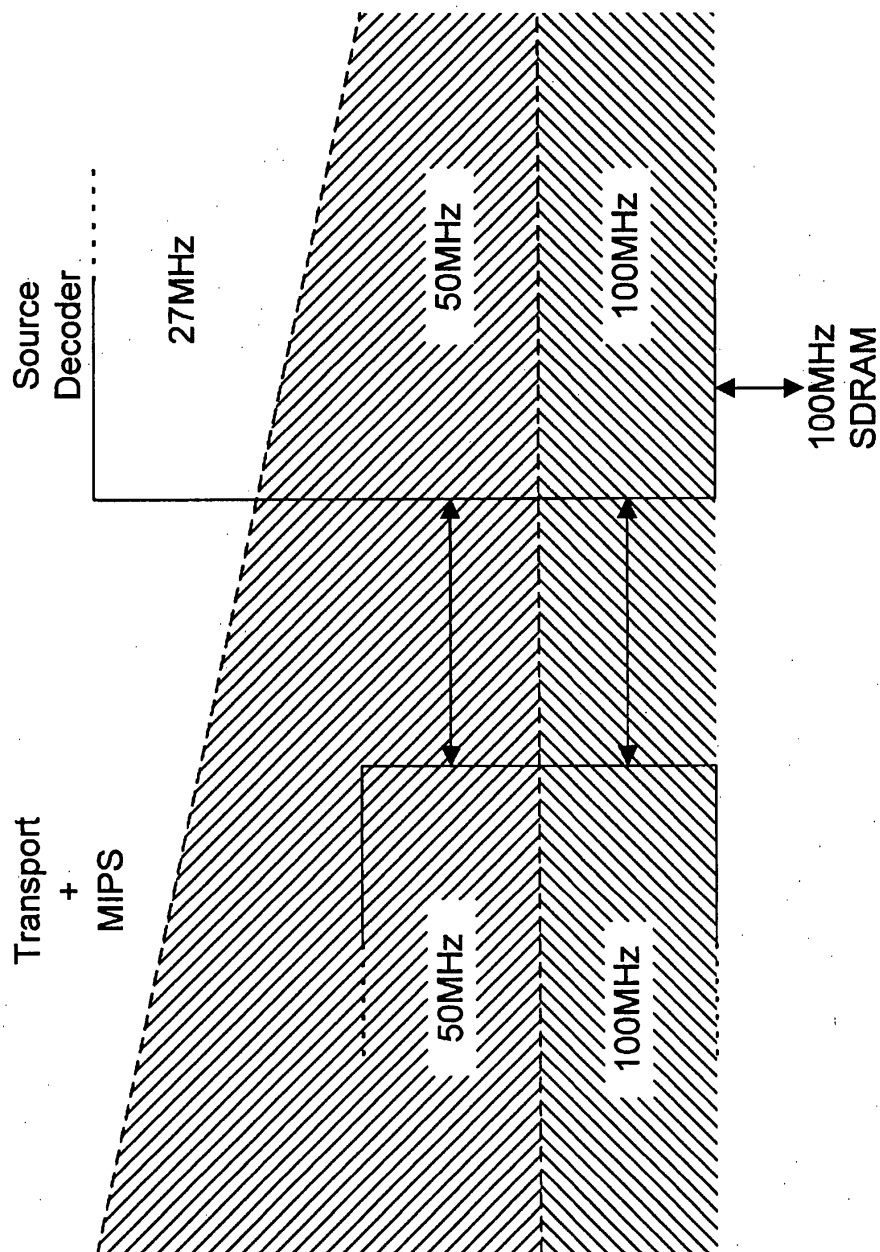


FIG. 12

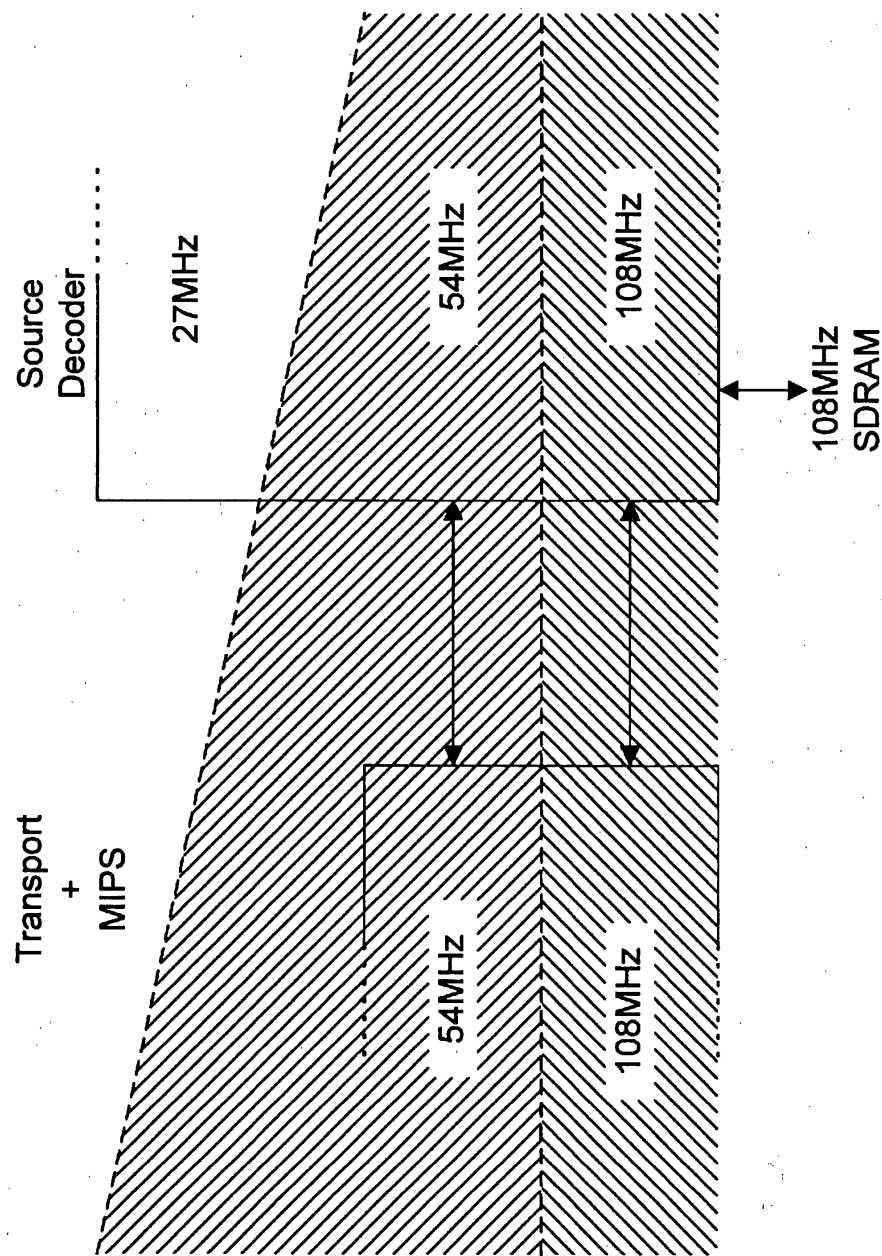


FIG. 13

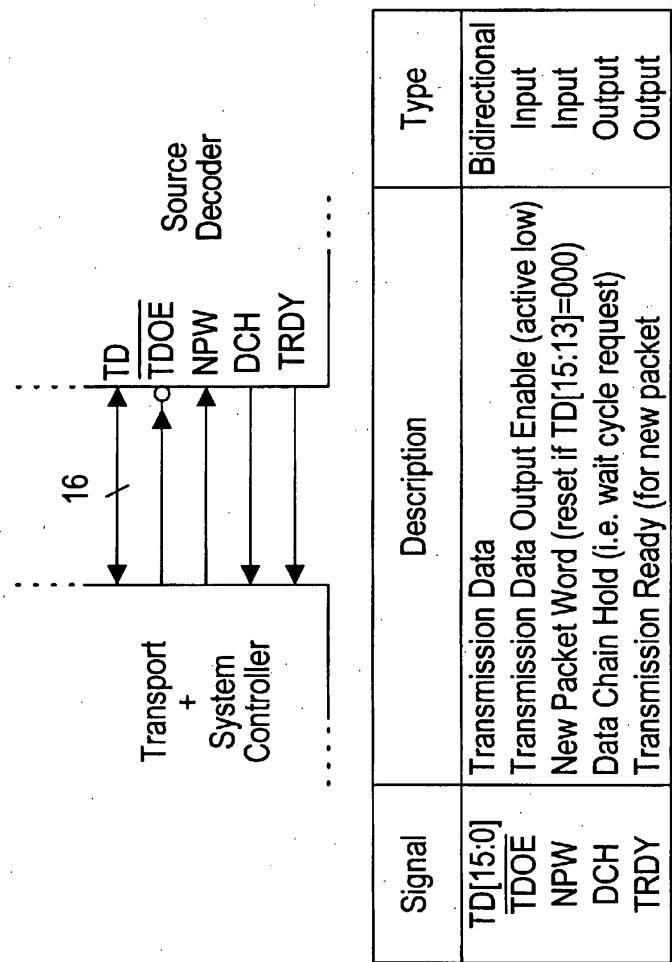


FIG. 14

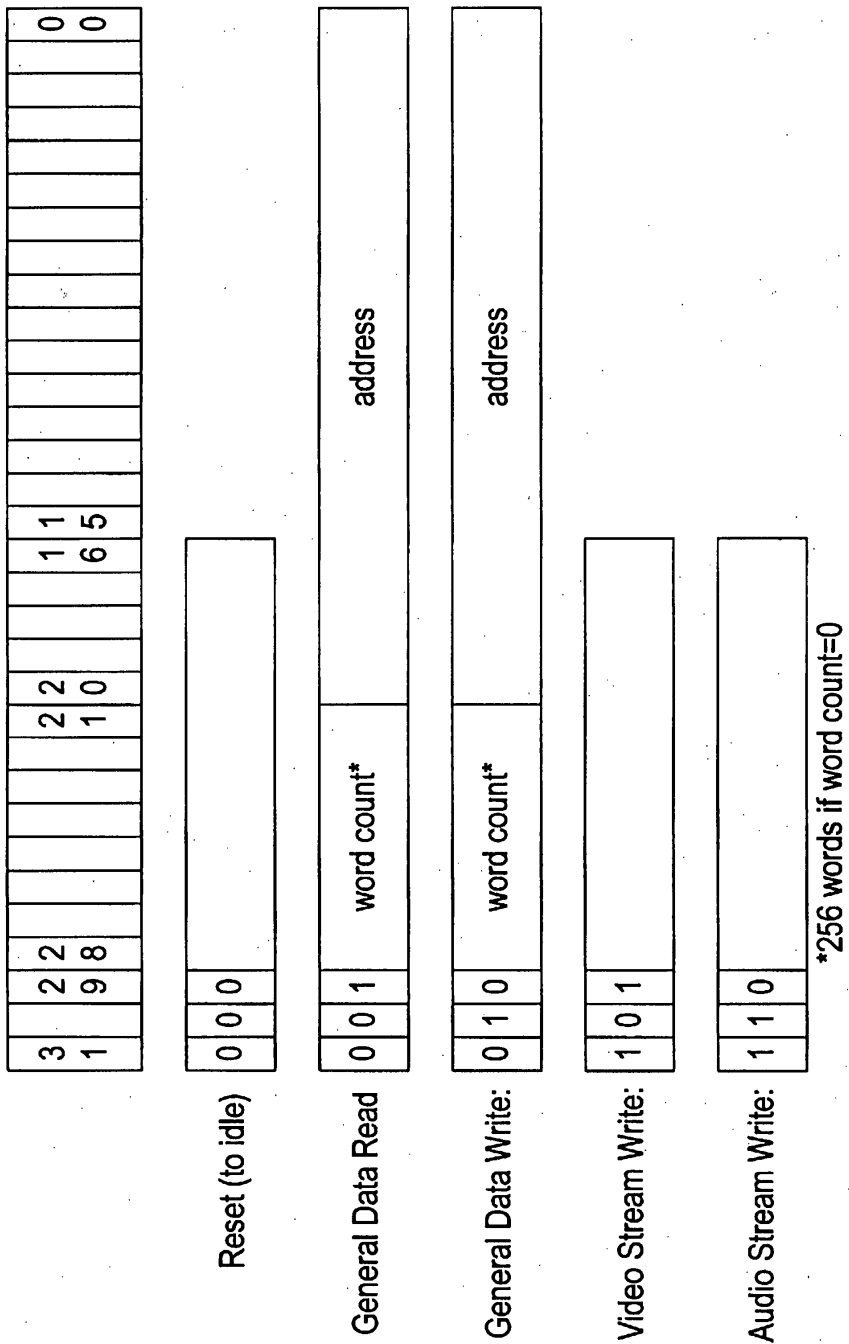


FIG. 15

MPEG DECODER SYSTEM AND METHOD HAVING A UNIFIED MEMORY FOR TRANSPORT DECODE AND SYSTEM CONTROLLER FUNCTIONS

INCORPORATION BY REFERENCE

The following references are hereby incorporated by reference.

The ISO/IEC MPEG specification referred to as ISO/IEC 13818 is hereby incorporated by reference in its entirety.

U.S. patent application Ser. No. 08/654,321 titled "Method and Apparatus for Segmenting Memory to Reduce the Memory Required for Bidirectionally Predictive-Coded Frames" and filed May 28, 1996 is hereby incorporated by reference in its entirety as though fully and completely set forth herein.

U.S. patent application Ser. No. 08/653,845 titled "Method and Apparatus for Reducing the Memory Required for Decoding Bidirectionally Predictive-Coded Frames During Pull-Down" and filed May 28, 1996 is hereby incorporated by reference in its entirety as though fully and completely set forth herein.

U.S. patent application Ser. No. 08/689,300 titled "Method and Apparatus for Decoding B Frames in Video Codecs with Minimal Memory" and filed Aug. 8, 1996 now U.S. Pat. No. 5,818,533, whose inventors are David R. Auld and Kwok Chau, is hereby incorporated by reference in its entirety as though fully and completely set forth herein.

1. Field of the Invention

The present invention relates generally to digital video compression, and more particularly to an MPEG decoder system which includes a single unified memory for MPEG transport, decode and system controller functions.

2. Description of the Related Art

Full-motion digital video requires a large amount of storage and data transfer bandwidth. Thus, video systems use various types of video compression algorithms to reduce the amount of necessary storage and transfer bandwidth. In general, different video compression methods exist for still graphic images and for full-motion video. Intraframe compression methods are used to compress data within a still image or single frame using spatial redundancies within the frame. Interframe compression methods are used to compress multiple frames, i.e., motion video, using the temporal redundancy between the frames. Interframe compression methods are used exclusively for motion video, either alone or in conjunction with intraframe compression methods.

Intraframe or still image compression techniques generally use frequency domain techniques, such as the discrete cosine transform (DCT). Intraframe compression typically uses the frequency characteristics of a picture frame to efficiently encode a frame and remove spatial redundancy. Examples of video data compression for still graphic images are JPEG (Joint Photographic Experts Group) compression and RLE (run-length encoding). JPEG compression is a group of related standards that provide either lossless (no image quality degradation) or lossy (imperceptible to severe degradation) compression. Although JPEG compression was originally designed for the compression of still images rather than video, JPEG compression is used in some motion video applications. The RLE compression method operates by testing for duplicated pixels in a single line of the bit map and storing the number of consecutive duplicate pixels rather than the data for the pixels themselves.

In contrast to compression algorithms for still images, most video compression algorithms are designed to com-

press full motion video. As mentioned above, video compression algorithms for motion video use a concept referred to as interframe compression to remove temporal redundancies between frames. Interframe compression involves storing only the differences between successive frames in the data file. Interframe compression stores the entire image of a key frame or reference frame, generally in a moderately compressed format. Successive frames are compared with the key frame, and only the differences between the key frame and the successive frames are stored. Periodically, such as when new scenes are displayed, new key frames are stored, and subsequent comparisons begin from this new reference point. It is noted that the interframe compression ratio may be kept constant while varying the video quality. Alternatively, interframe compression ratios may be content-dependent, i.e., if the video clip being compressed includes many abrupt scene transitions from one image to another, the compression is less efficient. Examples of video compression which use an interframe compression technique are MPEG, DVI and Indeo, among others.

MPEG BACKGROUND

A compression standard referred to as MPEG (Moving Pictures Experts Group) compression is a set of methods for compression and decompression of full motion video images which uses the interframe and intraframe compression techniques described above. MPEG compression uses both motion compensation and discrete cosine transform (DCT) processes, among others, and can yield compression ratios of more than 30:1.

The two predominant MPEG standards are referred to as MPEG-1 and MPEG-2. The MPEG-1 standard generally concerns frame data reduction using block-based motion compensation prediction (MCP), which generally uses temporal differential pulse code modulation (DPCM). The MPEG-2 standard is similar to the MPEG-1 standard, but includes extensions to cover a wider range of applications, including interlaced digital video such as high definition television (HDTV).

Interframe compression methods such as MPEG are based on the fact that, in most video sequences, the background remains relatively stable while action takes place in the foreground. The background may move, but large portions of successive frames in a video sequence are redundant. MPEG compression uses this inherent redundancy to encode or compress frames in the sequence.

An MPEG stream includes three types of pictures, referred to as the Intra (I) frame, the Predicted (P) frame, and the Bi-directional Interpolated (B) frame. The I or Intraframes contain the video data for the entire frame of video and are typically placed every 10 to 15 frames. Intraframes provide entry points into the file for random access, and are generally only moderately compressed. Predicted frames are encoded with reference to a past frame, i.e., a prior Intraframe or Predicted frame. Thus P frames only include changes relative to prior I or P frames. In general, Predicted frames receive a fairly high amount of compression and are used as references for future Predicted frames. Thus, both I and P frames are used as references for subsequent frames. Bi-directional pictures include the greatest amount of compression and require both a past and a future reference in order to be encoded. Bi-directional frames are never used as references for other frames.

In general, for the frame(s) following a reference frame, i.e., P and B frames that follow a reference I or P frame, only small portions of these frames are different from the corre-

sponding portions of the respective reference frame. Thus, for these frames, only the differences are captured, compressed and stored. The differences between these frames are typically generated using motion vector estimation logic, as discussed below.

When an MPEG encoder receives a video file, the MPEG encoder generally first creates the I frames. The MPEG encoder may compress the I frame using an intraframe compression technique. The MPEG encoder divides respective frames into a grid of 16x16 pixel squares called macroblocks in order to perform motion estimation/compensation. Thus, for a respective target picture or frame, i.e., a frame being encoded, the encoder searches for an exact, or near exact, match between the target picture macroblock and a block in a neighboring picture referred to as a search frame. For a target P frame the encoder searches in a prior I or P frame. For a target B frame, the encoder searches in a prior or subsequent I or P frame. When a match is found, the encoder transmits a vector movement code or motion vector. The vector movement code or motion vector only includes information on the difference between the search frame and the respective target picture. The blocks in target pictures that have no change relative to the block in the reference picture or I frame are ignored. Thus the amount of data that is actually stored for these frames is significantly reduced.

After motion vectors have been generated, the encoder then encodes the changes using spatial redundancy. Thus, after finding the changes in location of the macroblocks, the MPEG algorithm further calculates and encodes the difference between corresponding macroblocks. Encoding the difference is accomplished through a math process referred to as the discrete cosine transform or DCT. This process divides the macroblock into four sub blocks, seeking out changes in color and brightness. Human perception is more sensitive to brightness changes than color changes. Thus the MPEG algorithm devotes more effort to reducing color data than brightness.

Therefore, MPEG compression is based on two types of redundancies in video sequences, these being spatial, which is the redundancy in an individual frame, and temporal, which is the redundancy between consecutive frames. Spatial compression is achieved by considering the frequency characteristics of a picture frame. Each frame is divided into non-overlapping blocks, and each block is transformed via the discrete cosine transform (DCT). After the transformed blocks are converted to the "DCT domain", each entry in the transformed block is quantized with respect to a set of quantization tables. The quantization step for each entry can vary, taking into account the sensitivity of the human visual system (HVS) to the frequency. Since the HVS is more sensitive to low frequencies, most of the high frequency entries are quantized to zero. In this step where the entries are quantized, information is lost and errors are introduced to the reconstructed image. Run length encoding is used to transmit the quantized values. To further enhance compression, the blocks are scanned in a zig-zag ordering that scans the lower frequency entries first, and the non-zero quantized values, along with the zero run lengths, are entropy encoded.

When an MPEG decoder receives an encoded stream, the MPEG decoder reverses the above operations. Thus the MPEG decoder performs inverse scanning to remove the zig zag ordering, inverse quantization to de-quantize the data, and the inverse DCT to convert the data from the frequency domain back to the pixel domain. The MPEG decoder also performs motion compensation using the transmitted motion vectors to recreate the temporally compressed frames.

When frames are received which are used as references for other frames, such as I or P frames, these frames are decoded and stored in memory. When a temporally compressed or encoded frame is received, such as a P or B frame, motion compensation is performed on the frame using the prior decoded I or P reference frames. The temporally compressed or encoded frame, referred to as a target frame, will include motion vectors which reference blocks in prior decoded I or P frames stored in the memory. The MPEG decoder examines the motion vector, determines the respective reference block in the reference frame, and accesses the reference block pointed to by the motion vector from the memory.

A typical MPEG decoder includes motion compensation logic which includes local or on-chip memory. The MPEG decoder also includes an external memory which stores prior decoded reference frames. The MPEG decoder accesses the reference frames or anchor frames stored in the external memory in order to reconstruct temporally compressed frames. The MPEG decoder also typically stores the frame being reconstructed in the external memory.

An MPEG decoder system also typically includes transport logic which operates to demultiplex received data into a plurality of individual multimedia streams. An MPEG decoder system also generally includes a system controller which controls operations in the system and executes programs or applets.

Prior art MPEG video decoder systems have generally used a frame store memory for the MPEG decoder motion compensation logic which stores the reference frames or anchor frames as well as the frame being reconstructed. Prior art MPEG video decoder systems have also generally included a separate memory for the transport and system controller functions. It has generally not been possible to combine these memories, due to size limitations. For example, current memory devices are fabricated on an 4 Mbit granularity. In prior art systems, the memory requirements for the transport and system controller functions as well as the decoder motion compensation logic would exceed 16 Mbits of memory, thus requiring 20 or 24 Mbits of memory. This additional memory adds considerable cost to the system.

The amount of memory is a major cost item in the production of video decoders. Thus, it is desired to reduce the memory requirements of the decoder system as much as possible to reduce its size and cost. Since practical memory devices are implemented using particular convenient discrete sizes, it is important to stay within a particular size if possible for commercial reasons. For example, it is desired to keep the memory requirements below a particular size of memory, such as 16 Mb, since otherwise a memory device of 20 or 24 Mb would have to be used, resulting in greater cost and extraneous storage area. As mentioned above, it has heretofore not been possible to combine the memory required for the transport and system controller functions with the memory required for the MPEG decoder logic due to the memory size requirements.

Therefore, a new video decoder system and method is desired which efficiently uses memory and combines the memory subsystem for reduced memory requirements and hence reduced cost.

SUMMARY OF THE INVENTION

The present invention comprises an MPEG decoder system and method for performing video decoding or decompression which includes a unified memory for multiple

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functions according to the present invention. The video decoding system includes transport logic, a system controller, and MPEG decoder logic. The video decoding system of the present invention includes a single unified memory which stores code and data for the transport logic, system controller and MPEG decoder functions. The single unified memory is preferably a 16 Mbit memory. The present invention thus requires only a single memory, and thus has reduced memory requirements compared to prior art designs.

The video decoding system includes transport logic which operates to demultiplex received data into a plurality of individual multimedia streams. The video decoding system also includes a system controller which controls operations in the system and executes programs or applets. The video decoding system further includes decoding logic, preferably MPEG decoder logic, which performs motion compensation between temporally compressed frames of a video sequence during video decoding or video decompression. The memory includes a plurality of memory portions, including a video frame portion for storing video frames, a system controller portion for storing code and data executable by the system controller, and a transport buffer for storing data used by the transport logic. The MPEG decoder logic preferably includes a memory controller which couples to the single unified memory. Each of the transport logic, system controller, and MPEG decoder logic accesses the single unified memory through the memory controller.

The video decoding system implements various frame memory saving schemes, such as compression or dynamic allocation, to reduce the required amount of frame store memory. Also, in one embodiment, the memory is not required to store reconstructed frame data during motion compensation, thus considerably reducing the required amount of memory for this function. Alternatively, the memory is only required to store a portion of the reconstructed frame data. These savings in memory allow portions of the memory to also be used for transport and system controller functions.

The present invention thus provides a video decoding system with reduced memory requirements.

BRIEF DESCRIPTION OF THE DRAWINGS

A better understanding of the present invention can be obtained when the following detailed description of the preferred embodiment is considered in conjunction with the following drawings, in which:

FIG. 1 illustrates a computer system which performs video decoding and which includes a motion compensation logic having a frame memory which stores reference block data according to the present invention;

FIG. 2 is a block diagram illustrating the computer system of FIG. 1;

FIG. 3 is a block diagram illustrating an MPEG decoder system including a unified memory for MPEG transport, system controller, and decode functions according to the present invention;

FIG. 4 is a block diagram illustrating the MPEG decoder logic in the system of FIG. 3;

FIG. 5 illustrates various frame memory saving schemes used in various embodiments of the invention;

FIGS. 6a and 6b illustrate a table listing the memory partitions under different display schemes;

FIG. 7 illustrates the relationship of memory bandwidth vs. memory size in the NTSC decoding scheme;

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FIG. 8 illustrates the relationship of memory bandwidth vs. memory size in the PAL encoding scheme;

FIG. 9 illustrates the memory partitions according to the preferred embodiment of the invention;

FIG. 10 illustrates the estimated memory bandwidth distribution in the preferred embodiment of the invention;

FIG. 11 illustrates the "worst case" relationship of processing power vs. memory size in the NTSC decoding scheme;

FIG. 12 illustrates the clock domains in the system;

FIG. 13 illustrates clock operating frequencies according to the preferred embodiment of the invention;

FIG. 14 illustrates an example of the packet data interface between the transport controller and the source decoder; and

FIG. 15 illustrates packet header formats used in the preferred embodiment.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

Video Compression System

Referring now to FIG. 1, a system for performing video decoding or decompression and including a unified memory according to the present invention is shown. The video decoding system of the present invention includes a single unified memory which stores code and data for the transport, system controller and MPEG decoder functions. This simplifies the design and reduces the memory requirements in the system.

As shown, in one embodiment the video decoding or decompression system is comprised in a general purpose computer system 60. The video decoding system may comprise any of various types of systems, including a computer system, set-top box, television, or other device.

The computer system 60 is preferably coupled to a media storage unit 62 which stores digital video files which are to be decompressed or decoded by the computer system 60. The media storage unit 62 may also store the resultant decoded or decompressed video file. In the preferred embodiment, the computer system 60 receives a compressed video file or bitstream and generates a normal uncompressed digital video file. In the present disclosure, the term "compressed video file" refers to a video file which has been compressed according to any of various video compression algorithms which use motion estimation techniques, including the MPEG standard, among others, and the term "uncompressed digital video file" refers to a stream of decoded or uncompressed video.

As shown, the computer system 60 preferably includes a video decoder 74 which performs video decoding or decompression operations. The video decoder 74 is preferably an MPEG decoder. The computer system 60 optionally may also include an MPEG encoder 76. The MPEG decoder 74 and MPEG encoder 76 are preferably adapter cards coupled to a bus in the computer system, but are shown external to the computer system 60 for illustrative purposes. The computer system 60 also includes software, represented by floppy disks 72, which may perform portions of the video decompression or decoding operation and/or may perform other operations, as desired.

The computer system 60 preferably includes various standard components, including one or more processors, one or more buses, a hard drive and memory. Referring now to FIG. 2, a block diagram illustrating the components comprised in the computer system of FIG. 1 is shown. It is noted that FIG. 2 is illustrative only, and other computer architectures may be used, as desired. As shown, the computer

system includes at least one processor 80 coupled through chipset logic 82 to a system memory 84. The chipset 82 preferably includes a PCI (Peripheral Component Interconnect) bridge for interfacing to PCI bus 86, or another type of bus bridge for interfacing to another type of expansion bus. In FIG. 2, MPEG decoder 74 and MPEG encoder 76 are shown connected to PCI bus 86. Various other components may be comprised in the computer system, such as video 88 and hard drive 90.

As mentioned above, in the preferred embodiment of FIG. 1 the computer system 60 includes or is coupled to one or more digital storage or media storage devices. For example, in the embodiment of FIG. 1, the computer system 60 couples to media storage unit 62 through cable 64. The media storage unit 62 preferably comprises a RAID (Redundant Array of Inexpensive Disks) disk array, or includes one or more CD-ROM drives and/or one or more Digital Video Disk (DVD) storage units, or other media, for storing digital video to be decompressed and/or for storing the resultant decoded video data. The computer system may also include one or more internal RAID arrays, CD-ROM drives and/or may couple to one or more separate Digital Video Disk (DVD) storage units. The computer system 60 also may connect to other types of digital or analog storage devices or media, as desired.

Alternatively, the compressed digital video file may be received from an external source, such as a remote storage device or remote computer system. In this embodiment, the computer system preferably includes an input device, such as an ATM (Asynchronous Transfer Mode) adapter card or an ISDN (Integrated Services Digital Network) terminal adapter, or other digital data receiver, for receiving the digital video file. The digital video file may also be stored or received in analog format and converted to digital data, either externally to the computer system 60 or within the computer system 60.

As mentioned above, the MPEG decoder 74 in the computer system 60 performs video decoding or video decompression functions. As discussed further below, the video decoding system includes transport logic which operates to demultiplex received data into a plurality of individual multimedia streams. The video decoding system also includes a system controller which controls operations in the system and executes programs or applets comprised in the stream. The video decoding system further includes decoding logic, preferably MPEG decoder logic, which performs motion compensation between temporally compressed frames of a video sequence during video decoding or video decompression. The video decoding system of the present invention includes a single unified memory which stores code and data for the transport, system controller and MPEG decoder functions. This simplifies the design and reduces the memory requirements in the system. The MPEG decoder 74 thus performs functions with improved efficiency and reduced memory requirements according to the present invention.

It is noted that the system for decoding or decompressing video data may comprise two or more interconnected computers, as desired. The system for decoding or decompressing video data may also comprise other hardware, such as a set top box, either alone or used in conjunction with a general purpose programmable computer. It is noted that any of various types of systems may be used for decoding or decompressing video data according to the present invention, as desired.

FIG. 3—MPEG Decoder Block Diagram

Referring now to FIG. 3, a block diagram illustrating an MPEG decoder system architecture according to one

embodiment of the present invention is shown. As shown, the MPEG decoder system includes a channel receiver 202 for receiving a coded stream. As mentioned above, in the preferred embodiment, the coded stream is an MPEG encoded stream. The MPEG encoded stream may include interactive program content comprised within this stream, as desired. The channel receiver 202 receives the coded stream and provides the coded stream to a transport and system controller block 204.

The transport and system controller block 204 includes transport logic 206 which operates to demultiplex the received MPEG encoded stream into a plurality of multimedia data streams. In other words, the encoded stream preferably includes a plurality of multiplexed encoded channels or multimedia data streams which are combined into a single stream, such as a broadcast signal provided from a broadcast network. The transport logic 206 in the transport and system controller block 204 operates to demultiplex this multiplexed stream into one or more programs, wherein each of the programs comprise individual multimedia data streams including video and/or audio components.

It is noted that the MPEG stream may comprise one of two types of streams including either a transport stream or a program stream. A transport stream comprises a 188 byte stream which includes error correction and which is designed for an error prone environment. A program stream, on the other hand, is designed for an error free environment and this does not include error correction capabilities.

The transport and system controller block 204 also includes a system controller 208 which monitors the MPEG system and is programmable to display audio/graphics on the screen and/or execute interactive applets or programs which are embedded in the MPEG stream. The system controller 208 also preferably controls operations in the MPEG decoder system. In the preferred embodiment, the system controller 208 comprises a MIPS RISC CPU which is programmed to perform system controller functions.

The transport and system controller block 204 couples through a memory controller 211 in MPEG decoder 224 to an external memory 212, also referred to as the single unified memory 212. The transport logic 206 and system controller logic 208 comprised in the transport and system controller block 204 utilize the external memory 212 to store and/or receive code and data. In the preferred embodiment, the external memory 212 is a 16 MB synchronous dynamic random access memory (SDRAM).

As shown, the transport and system controller block 204 couples to an MPEG decoder block 222. The MPEG decoder block 222 includes an MPEG audio visual decoder 224, as shown. The MPEG audio visual decoder 224 receives data from the transport and system controller block 204 and operates to perform MPEG decoding to produce a decoded or decompressed signal. The visual component of the decompressed signal is output from the MPEG A/V decoder 224 and is provided to a video encoder 226. The video encoder 226 operates to convert the digital video stream into a format more appropriate for transmission or display, such as NTSC or PAL format. The video encoder logic 226 includes digital to analog (D/A) converters for converting the decoded digital video stream into an analog stream. This analog video stream is then provided as an output of the system as shown.

The audio component of the decoded or decompressed MPEG stream is provided to an audio digital to analog converter (DAC) 228. The audio DAC 228 operates to perform digital to analog conversion on the digital audio signal output from the MPEG A/V decoder 224. The result-

ing analog audio signals are provided as an output to the system as shown.

As shown, the external memory 212 is coupled to the MPEG A/V decoder 224. The MPEG A/V decoder 224 includes a memory controller 211 which controls access to the single unified memory 212. As noted above, each of the transport logic 206 and system controller logic 208 comprised in the transport and system controller block 204 access the external memory 212 through the memory controller 211.

The MPEG A/V decoder 224 utilizes the external memory 212 in the MPEG decode process. Thus the MPEG A/V decoder 224 uses the same memory 212 as the transport and system controller blocks. As is well-known in the art, the MPEG A/V decoder 224 uses the external memory 212 to store decoded reference frames or anchor frames which are used during motion compensation or reconstruction of temporally compressed frames. The MPEG A/V decoder 224 may also use the external memory 212 to store a portion or all of the reconstructed frames.

Reconstructed Frame Data Memory Saving Schemes

It is noted that reconstruction of a temporally compressed frame during MPEG decoding typically uses a full 16 MB of external memory. However, the MPEG decoder system 74 of the preferred embodiment uses one or more of various methods to reduce the amount of memory required for storing reconstructed frame data. For example, current prior art video decoder implementations use at least one frame of memory to store the reconstructed B-picture prior to display. In other words, prior art decoders require that there be a full frame store into which to reconstruct the B frame or picture.

In one embodiment of the invention, the video decoder system 74 uses as little as 2.528 frame stores when there is no pulldown during B-frames. In this embodiment, the system uses an improved method to reduce the required amount of memory, whereby the memory used to store the first field is used again for reconstruction as soon as that part of the picture has been displayed. This method reduces the amount of memory needed for B-frame reconstruction to about 0.528 frames. For more information on this method, please see U.S. patent application Ser. No. 08/654,321 titled "Method and Apparatus for Segmenting Memory to Reduce the Memory Required for Bidirectionally Predictive-Coded Frames" and filed May 27, 1996, which is hereby incorporated by reference in its entirety as though fully and completely set forth herein.

In another embodiment of the invention, the video decoder system 74 uses as little as 2.75 frames when there is pulldown. In this embodiment, a method is used to reduce the memory required for decoding and displaying B frames during 3:2 pull-down. This method uses the fact that B frames are not used to predict other frames, so that once the B frame data is retrieved for display, it may be discarded. To enable re-use of memory, data from the top and bottom fields is separated into different segments of memory. Thus, once retrieval begins of the data in a segment, that segment becomes free for reconstruction. However, this initial scheme is not completely sufficient for the top field of every other frame during 3:2 pull-down, since the top field must be somehow made available again for re-display. Rather than requiring additional memory to save the top field of every other frame, the top field is reconstructed again during the period when reconstruction is typically stalled. In this manner, the amount of memory required is reduced, and the field requiring re-display for 3:2 pull-down is simply reconstructed again. For more information on this method for reducing the required amount of memory when pull-down is

being performed, please see U.S. patent application Ser. No. 08/653,845 titled "Method and Apparatus for Reducing the Memory Required for Decoding Bidirectionally Predictive-Coded Frames During Pull-Down" and filed May 27, 1996, which is hereby incorporated by reference in its entirety as though fully and completely set forth herein.

The above methods used to reduce memory requirements, which are disclosed in the above-referenced patent applications, are optimal, i.e., use the least possible memory, where the picture is decoded only once. In another embodiment, The MPEG decoder 74 includes frame reconstruction or decoder logic which operates to reconstruct a bi-directionally encoded (B) frame without requiring storage of the frame being constructed in the external memory 112. In this embodiment, the MPEG decoder 74 operates to decode or reconstruct the frame twice, once during each field display period. This obviates the necessity of storing the reconstructed B frame data, thus reducing memory requirements.

In this embodiment, the MPEG decoder system includes a picture reconstruction unit, a picture display unit, a pointer register, and a temporary buffer (all not shown). The picture memory 212 includes separate buffers used for anchor pictures or reference frames (A1, A2) and a rate buffer which stores the temporally compressed frame, referred to as C. The pointer register stores the location of the first byte of the compressed picture, which is stored in the rate buffer. According to this embodiment, the picture memory 212 is not required to store data from the reconstructed frame.

The picture reconstruction unit operates to decode or reconstruct the B frame twice, once each during a first field time and a second field time. The first field time substantially corresponds to the time when the first or top field of the picture is displayed, and the second field time substantially corresponds to the time when the second or bottom field of the picture is displayed.

During the first field time, compressed picture data is read from the rate buffer into the picture reconstruction unit, where the picture is decoded. The top field data from the picture reconstruction unit is written to the temporary buffer, and the bottom field data is discarded. After one slice of the picture has been decoded, the data in the temporary buffer is retrieved by the picture display unit and is output for display. This process continues for the entire picture in order to display all of the first field. Thus, the entire picture is decoded or reconstructed, and only data from the top field is written to the temporary buffer for display.

During the second field time, the same compressed picture is again read from the rate buffer. The picture reconstruction unit again decodes the compressed picture. In the second field time, the picture reconstruction unit writes the bottom field data to the temporary buffer, and the top field data is discarded. After one slice of the picture has been decoded, the data in the temporary buffer is output by the picture display unit for display. This process continues for the entire picture in order to display all of the second field.

The reconstructed picture is never written to the memory during reconstruction of B-frames. It is also noted that the temporary buffer is about 32 times smaller than the external frame store required in the best implementation of prior art methods. This allows the temporary buffer to be comprised on the same monolithic substrate as the decoder itself.

Therefore, in this embodiment the video decoder system reconstructs the B-picture twice, once in each field time. This eliminates the storage requirement of the reconstructed B-frame entirely and thus allows this memory space to be used for transport and system controller functions.

In another embodiment, the MPEG decoder system of the preferred embodiment uses a dynamic segment allocation scheme and/or compression techniques which reduce the external memory requirement. These memory saving techniques are discussed further below.

Therefore, the video decoding system 74 includes transport logic 206 which operates to demultiplex received data into a plurality of individual multimedia streams. The video decoding system also includes a system controller 208 which controls operations in the system and executes programs or applets comprised in the stream. The video decoding system 74 further includes decoding logic 224, preferably MPEG decoder logic, performs motion compensation between temporally compressed frames of a video sequence during video decoding or video decompression. The video decoding system of the present invention includes a single unified memory which stores code and data for the transport, system controller and MPEG decoder functions. This simplifies the design and reduces the memory requirements in the system.

As discussed above, prior art MPEG decoder systems include different memory systems for the transport and system controller logic 204 and the MPEG decoder logic 224. These separate memories are required because of the separate bandwidth and processing requirements for each memory, as well as the memory size requirements of each block. According to the system and method of the present invention, the present invention includes a single or unified memory which is used for each of the transport and system controller block 204 and the MPEG A/V decoder logic 224. FIG. 4—MPEG Decoder Block Diagram

Referring now to FIG. 4, a block diagram illustrating the MPEG A/V decoder logic 224 in the MPEG decoder 74 which performs motion compensation according to the present invention is shown. As shown, the video decoder logic 224 receives an encoded or compressed digital video stream and outputs an uncompressed digital video stream. The compressed digital video stream is a bitstream of compressed video data which is used to present a video sequence, such as a television segment or movie, onto a screen, such as a television or a computer system. In the preferred embodiment, the compressed digital video stream is compressed using the MPEG-2 compression algorithm, and the video decoder 74 is thus preferably an MPEG-2 decoder. Since the operation of MPEG decoders is well known in the art, details of their operation which are not necessary to the operation of the present invention are omitted for simplicity.

As shown in FIG. 3, the decoder logic 224 comprises a Variable Length Decoding block 302 coupled to provide an output to an Inverse Scan block 304, which is coupled to provide an output to an Inverse Quantization block 306, which is coupled to provide an output to an Inverse DCT block 308, which is coupled to provide an output to a motion compensation block 310. The motion compensation block 310 provides an output comprising decoded samples. A frame store memory 212 is coupled to the output of the motion compensation block 310 to receive and store decoded frame data. The motion compensation block 310 is coupled to an output of the frame store memory 212 to receive reference block data from the frame store memory 212 during motion compensation.

As shown in FIG. 3, the Variable Length Decoding block 302 receives coded data and performs variable length decoding. As is well known, the MPEG standard provides that data is compressed for transmission using variable length codes. Thus the Variable Length Decoding block 302 decodes this

data and produces an output, referred to as QFS[n]. The QFS[n] output of the Variable Length Decoding block 302 is provided to the Inverse Scan block 304. The Inverse Scan block 304 reverses the zig zag scan ordering of the received data (is this right) and produces an output referred to as QF[v][u]. The output QF[v][u] is provided to the Inverse Quantization block 306. The Inverse Quantization block 306 performs inverse quantization or de-quantizes the data to produce de-quantized data, referred to as F[v][u]. The output F[v][u] of the Inverse Quantization block 306 is provided to the Inverse DCT block 308, which performs the inverse discrete cosine transform to convert the data from the frequency domain back to the pixel domain. The inverse DCT block 308 produces an output referred to as f[y][x]. The output f[y][x] of the inverse DCT block 308 is provided to the motion compensation block 310.

The output f[y][x] from the inverse DCT block 308 comprises temporally encoded frames of pixel data. The motion compensation block 310 decompresses the temporally compressed frames using motion compensation techniques. As described above, an MPEG encoded stream comprises I, P and B frames. P and B frames are temporally compressed relative to other frames. P frames are temporally compressed relative to prior I or P frames, and B frames are temporally compressed relative to prior I or P frames. When a frame is temporally compressed, the frame is partitioned into macroblocks, referred to as target blocks, and then the compression method searches in neighboring frames for blocks which are most similar to the block being encoded. When the best fit block is found, the respective target block is encoded by a motion vector which points to this best fit reference block in the reference frame. The difference between the block being encoded and the best fit block is also computed and transferred in the MPEG stream.

Output pixel values from the motion compensation block 310 are provided to a frame store memory 212. The frame store memory 212 is thus coupled to the motion compensation block 310 and stores one or more reference frames of video data. These reference frames of video data are used in performing motion compensation on temporally compressed frames, such as P and B frames. In general, an MPEG stream includes encoded reference frame data which is transmitted before temporally compressed data that depends on the prior transmitted reference frame data. Thus, incoming temporally encoded frame data, such as P and B frame data, comprises motion vectors which point to reference blocks in a prior transmitted reference frame of video data, which has been stored in the frame store memory 212. The motion compensation block 310 analyzes each motion vector from the incoming temporally compressed data and retrieves a reference block from the frame store memory 212 in response to each motion vector. The motion compensation block 310 includes a local memory or on-chip memory 116 which stores the retrieved reference block. The motion compensation block 110 then uses this retrieved reference block to decompress the temporally compressed data.

In the preferred embodiment, the frame store memory 212 is 1Mx16 SDRAM, such as Samsung KM416S1120AT-12, having an operating frequency of 81 MHz or 108 MHz and a burst size of 4 words. As discussed above, the frame store memory 112 is also used according to the present invention to store code and data for the transport logic 206 and the system controller logic 208.

FIG. 5—Memory Saving Schemes

FIG. 5 illustrates various frame memory saving schemes used in various embodiments of the invention. As shown, in European systems which do not include a field repeat,

dynamic memory segment allocation techniques are used to more efficiently use the memory space. In other words, memory segments or areas are dynamically allocated to minimize unused space. These dynamic memory segment allocation techniques range from a 40 segment technique ($\times/2.556$) to a 3.22 (3) segment technique ($\times/2.801$). As the memory segment size decreases, a larger amount of granularity is provided, and the memory can be used in a more "detailed" or specific fashion. The dynamic allocation scheme operates to dynamically allocate segments of memory of different size to more efficiently use the available memory and correspondingly result in little or no unused space.

In U.S. systems with field repeat, compression techniques are preferably used to reduce memory requirements. These compression techniques include a "compressed bitstream" technique and a "local compression" technique.

The compressed bitstream technique operates to store frame data in its received MPEG compressed format, instead of storing the frame data in a decoded or decompressed format. When this compressed data is read from memory, the compressed memory is decoded or decompressed "on the fly". As shown, the compressed bitstream technique may involve storing only one of the anchor frames in a compressed format, storing only the B frames in a compressed format, or storing both the anchor and B frames in a compressed format.

The local compression technique comprises re-encoding the decoded or compressed bitstream, preferably using a standard compression standard such as DPCM or MPEG. Thus, once frames have been decoded or reconstructed, the frame data is re-encoded prior to storage in memory. As shown, the local compression may involve compressing one of the anchor frames only, the B frames only, or both the anchor and B frames.

FIGS. 6a and 6b—Memory Partitions

FIGS. 6A and 6B illustrate a table listing the memory partitions under different memory reduction schemes. As shown, the table of FIG. 1 illustrates the memory requirements for both the NTSC and PAL decoding schemes for a standard LSI L64005 part, a method which compresses the displayed anchor frame, a method which compresses both the anchor and the segment storing the B frame, a method which compresses only the B frame, and a method which compresses both the anchor and entire B frame. LSI part no. L64005 is a device produced by LSI Logic that has no memory reduction for NTSC and has dynamic allocation for PAL.

As shown, in the NTSC format using LSI part No. L64005, the frame store memory requires 12,441,600 bits of memory for storing three full frames. The channel buffer requires 2,864,637 bits of memory for various functions. As shown in the table, these functions include the vbv (video buffer verifier) buffer, the video non-instantaneous decode function, the video display sync function, the audio buffer, the audio-video latency difference function, the audio-display sync function, the video transport buffer, the audio transport buffer, and the jitter buffer (4 ms jitter at 15 Mbps). Each of the above functions collectively requires 2,864,637 bits for the channel buffer. The packet header overhead requires 20,000 bits of memory, the on-screen display (OSD) requires 675,840 bits of memory. This provides a subtotal for the software and data storage of 775,139 bits. The total required storage for the NTSC format is 16,777,216 bits of memory. As shown, the frame store and channel buffer collectively require 15,306,237 bits of memory.

As shown, the PAL decoding scheme using L64005 is similar. As shown the PAL decoding scheme requires

12,718,080 bits of memory to store 2.556 frames of memory. The channel buffer's subtotal for the PAL decoding scheme requires 3,060,847 bits of memory. The packet header overhead for the pal scheme is also 20,000 bits, and the onscreen display requires 808,192 bits. The subtotal for software and data storage in the PAL decoding scheme is 170,097 bits. Thus, the PAL decoding scheme using L64005 requires a total of 16,777,216 bits. As shown, for the PAL format, the frame store and channel buffer collectively require 15,778,927 bits of memory.

As shown, when the displayed anchor is compressed, the NTSC format requires 9,538,560 bits for the frame store, which is required to store the equivalent of 2.3 frames. The total for the frame store and channel buffer requirements is 14,208,205 bits, as well as 1,873,171 bits for the software and data. For the PAL decoding scheme with a compressed display anchor, 11,197,440 bits are required for the frame store. The frame store and channel buffer collectively require 16,063,295 bits, and the software and data requirement is (114,271). Thus, there are 114,271 bits "over budget" over a 16 Mbit target.

Where the anchor and the B segment are both compressed, for the NTSC decoding scheme, assuming 3.267 segments, the frame store is reduced to 8,778,240 bits and is required to store only 2.117 frames. Under this method, the frame store and channel buffer collectively require 13,447,885 bits of memory, and the subtotal for the software and data requirement is 2,633,491 bits of memory. In the PAL decoding scheme where the method compresses an anchor and segment B, assuming 40 segments, the frame store requires 8,985,600 bits and requires 1.806 frames to be stored. This method requires 13,851,455 bits to collectively store the frame store and channel buffer data, and the subtotal for software and data storage is 2,097,569 bits.

When the memory compresses only the B frame to optimize memory storage, in the NTSC format, the frame store required is 8,570,880 bits of memory and stores an equivalent of 2.067 frames. Under this method, the frame store and channel buffer require a total of 11,435,517 bits and a subtotal for software and data storage of 4,645,859 bits. In the PAL decoding scheme where the B frame only is compressed, the frame store requires 10,229,760 bits and thus stores 2.056 equivalent number of frames. In this method, the frames store and channel buffer collectively require 13,290,607 bits of memory, and the subtotal for software and data storage requires 2,658,417 bits of memory.

Where the system compresses both the anchor and the B frame to optimize memory, in the NTSC format, the frame store required is 5,667,840 bits of memory and stores an equivalent of 1.367 frames. Under this method, the frame store and channel buffer require a total of 10,337,485 bits and a subtotal for software and data storage of 5,743,891 bits. In the PAL decoding scheme where both the anchor frame and B frame are compressed, the frame store requires 6,497,280 bits and thus stores 1.306 equivalent number of frames. In this method, the frames store and channel buffer collectively require 11,363,135 bits of memory, and the subtotal for software and data storage requires 4,585,889 bits of memory.

FIG. 7—Memory Bandwidth vs. Memory Size in the NTSC Decoding Scheme

FIG. 7 illustrates the relationship of memory bandwidth vs. memory size in the NTSC decoding scheme. The memory size on the x axis of the graph is the memory size required for the frame store memory and the channel buffer. As shown, as the memory size decreases from left to right,

the required amount of memory and/or processing bandwidth increases. Thus, a greater amount of memory transfer and/or processing bandwidth is required as the memory size is reduced. FIG. 7 illustrates four different plots for each memory size, where these plots comprise 100%, 96%, and 87%, and 72% of useable bandwidth. The various lines illustrated in the graph of FIG. 7 illustrate the change in bandwidth versus the change in memory size, i.e., the $\Delta\text{bandwidth}/\Delta\text{memory}$, which comprises the units bytes/second/bit. As shown, the optimum memory size in the NTSC format is 13,447,885 bits.

FIG. 8—Memory Bandwidth vs. Memory Size in the NTSC Decoding Scheme

FIG. 8 illustrates the relationship of memory bandwidth vs. memory size in the PAL decoding scheme. As with FIG. 7, the memory size on the x axis of the graph is the memory size required for the frame store memory and the channel buffer. As shown, as the memory size decreases from left to right, the required amount of memory and/or processing bandwidth increases. Thus, a greater amount of memory transfer and/or processing bandwidth is required as the memory size is reduced. FIG. 8 also illustrates four different plots for each memory size, where these plots comprise 100%, 96%, and 87%, and 72% of useable bandwidth. The various lines illustrated in the graph of FIG. 8 illustrate the change in bandwidth versus the change in memory size, i.e., the $\Delta\text{bandwidth}/\Delta\text{memory}$, which comprises the units bytes/second/bit. As shown, the $\Delta\text{bandwidth}/\Delta\text{memory}$ peaks at 13,851,455 bits, which is the optimum memory size in the PAL format.

FIG. 9—Memory Partitions

FIG. 9 illustrates the memory partitions of the external memory 212 for each of the NTSC and PAL encoding formats according to one embodiment of the invention. FIG. 9 illustrates the number of bytes of memory size allocated for different purposes in the unified memory 212, including number of bits for video frames, the vbv buffer, the video decode buffer, the video-display synch buffer, the audio buffer, the audio-video latency buffer, the audio-display synch buffer, the transport buffer, the jitter buffer, the PES header overhead memory, the OSD, and the system controller code and data storage. It is noted that FIG. 9 illustrates the memory partition according to one embodiment of the invention, and it is noted that the memory 212 may be allocated differently, as desired. As shown, the memory size requirement are substantially comparable. In this example, the NTSC format uses 10,583,248 bytes for storing video frames, and the PAL format uses 10,790,608 bytes for storing video frames.

FIG. 10—Decoding Memory Bandwidth

FIG. 10 illustrates the estimated memory bandwidth distribution in the preferred embodiment of the invention for the NTSC and PAL formats. FIG. 10 illustrates the estimated memory bandwidth distribution using the memory partition embodiment of FIG. 9. The estimated memory bandwidth distribution shown in FIG. 10 presumes a 16x1 MB SDRAM running at 100 MHz, wherein bandwidth is available at 200 MB per second. This memory bandwidth distribution also presumes a requirement of 20 Mbytes per second for code and data executed by the system controller 208 in the transport and system controller block 204. As noted above, the system controller 208 is preferably a MIPS RISC CPU. As shown, the NTSC scheme requires 160.19 MB per second bandwidth, whereas the PAL decoding scheme requires 157.18 MB per second of bandwidth. The bandwidth requirements for each of the NTSC and PAL formats are substantially comparable with the exception that the

NTSC format requires a greater amount of memory bandwidth for the channel in/out function than does the PAL format.

FIG. 11—Processing Power vs. Memory Size (NTSC)

FIG. 11 illustrates the "worst case" relationship of processing power vs. memory size in the NTSC decoding scheme. In FIG. 11, the lines represent available cycles per macroblock for a decoder operating at 27 to 216 MHz. The bars represent the required cycles per macroblock reconstructed for 1 to 4 cycle/coefficient throughput. For example, a 100 MHz decoder can operate with 13,447,885 memory points at 1 and 2-cycle/coefficient throughput only (not the slow 4-cycle/coefficient). However, as shown, the processing power tends to increase as the memory decreases in size from 13,447,885 bytes to 11,435,517 bytes. The 11,435,517 and 19,337,485 memory points require a large amount of processing power, and thus even 216 MHz processing speed is not sufficient with 2-cycle/coefficient throughput.

FIGS. 12 and 13—Clock Domains

FIG. 12 illustrates the clock domains in the system, i.e., the various possible clock rates for the external memory 212 according to one embodiment of the invention. The video decoder system in the preferred embodiment includes a source decoder which operates at 27 Megahertz. The source decoder clock frequency of 27 Megahertz is required according to modern video encoding schemes. However, current memory operating frequencies are not designed for video applications, i.e., are not designed to operate at multiples of 27 MHz. As shown, the memory 212 operates near multiples of this source decoder frequency such as 50 MHz or 100 MHz.

FIG. 13 illustrates clock operating frequencies according to the preferred embodiment of the invention. In this embodiment, the external memory 212 is SDRAM or other suitable memory operating at 108 MHz, or a higher multiple. As shown, the transport and system controller block 204 preferably operates at either 54 MHz or 108 MHz. The source decoder 224 preferably also operates at 54 MHz or 108 MHz. Thus, as shown in FIG. 13, in the preferred embodiment the memory and hardware elements operate at multiples of the 27 MHz required clock frequency, i.e., either 54 Megahertz or 108 Megahertz.

FIG. 14—Packet Data Interface

FIG. 14 illustrates an example of the packet data interface between the transport and system controller block 204 and the source decoder 224. As shown, the transport and system controller block 204 and the source decoder 224 communicate 16 bit transmission data, referred to as TD[15:0], in a bi-directional manner. The transmission data signals TD[15:0] comprise a data bus for transmitting data between the transport and system control logic 204 and the source decoder 224. The transport and system controller block 204 provides a transmission data output enable (TDOE) signal which is provided as an input to the source decoder 224. The transport and system controller block 204 also provides a new packet word (NPW) signal as an input to the source decoder 224. The source decoder 224 provides two outputs to the transport and system controller block 204, these being a data chain hold (DCH) signal, which is a wait cycle request, and a TRDY (transmission ready) signal which indicates that the logic is ready for a new packet.

FIG. 15—Packet Header Formats

FIG. 15 illustrates packet header formats used in the preferred embodiment. As shown, different packet header values are used to indicate a reset, a general data read, a general data write, a video stream write, and an audio stream write. The general data read and general data write packets each include fields for word count and address.

Conclusion

Therefore, the present invention comprises a video decoder system and method which includes a single unified memory for MPEG transport, decode, and system controller functions. This reduces the required amount of memory, thus simplifying system design and reducing system cost.

Although the system and method of the present invention has been described in connection with the described embodiments, it is not intended to be limited to the specific form set forth herein, but on the contrary, it is intended to cover such alternatives, modifications, and equivalents, as can be reasonably included within the spirit and scope of the invention as defined by the appended claims.

I claim:

1. An MPEG decoder system which includes a single memory for use by transport, decode and system controller functions, comprising:
 - a channel receiver for receiving and MPEG encoded stream;
 - transport logic coupled to the channel receiver which demultiplexes one or more multimedia data streams from the encoded stream;
 - a system controller coupled to the transport logic which controls operations within the MPEG decoder system;
 - an MPEG decoder coupled to receive one or more multimedia data streams output from the transport logic, wherein the MPEG decoder operates to perform MPEG decoding on the multimedia data streams; and
 - a memory coupled to the MPEG decoder, wherein the memory is used by the MPEG decoder during MPEG decoding operations, wherein the memory stores code and data useable by the system controller which enables the system controller to perform control functions within the MPEG decoder system, wherein the memory is used by the transport logic for demultiplexing operations;
- wherein the MPEG decoder is operable to access the memory during MPEG decoding operations;
- wherein the transport logic is operable to access the memory to store and retrieve data during demultiplexing operations; and
- wherein the system controller is operable to access the memory to retrieve code and data during system control functions.
2. The MPEG decoder system of claim 1, wherein the MPEG decoder includes a memory controller coupled to the memory;
 - wherein the transport logic is coupled to the memory controller and is operable to access the memory through the memory controller; and
 - wherein the system controller is coupled to the memory controller and is operable to access the memory through the memory controller.
3. The MPEG decoder system of claim 2, wherein the memory controller is operable to store compressed data in the memory to reduce memory storage requirements.
4. The MPEG decoder system of claim 2, wherein the memory controller is operable to dynamically allocate segments of memory space in the memory to optimize memory use.
5. The MPEG decoder system of claim 1, wherein the memory stores anchor frame data during reconstruction of temporally compressed frames.
6. The MPEG decoder system of claim 1, wherein said memory has a memory size which does not exceed 16 Mbit.

7. The MPEG decoder system of claim 1, wherein said memory includes a plurality of memory portions, wherein said memory includes a video frame portion for storing video frames, a system controller portion for storing code and data executable by the system controller, and a transport buffer portion for storing data used by the transport logic.

8. The MPEG decoder system of claim 7, wherein said memory further includes a video decode buffer portion for storing decoded video data, a video display sync buffer, and an on-screen display buffer.

9. The MPEG decoder system of claim 8, wherein said memory further includes one or more audio buffers for storing audio data.

10. A method for performing video decoding in an MPEG decoder system which includes a single memory for use by transport, decode and system controller functions, the method comprising:

- receiving an MPEG encoded stream;
 - demultiplexing one or more multimedia data streams from the encoded stream, wherein said demultiplexing one or more multimedia data streams from the encoded stream operates using a first unified memory;
 - performing MPEG decoding on the multimedia data streams, wherein said performing MPEG decoding operates using said first unified memory; and
 - a system controller controlling operations within the MPEG decoder system, wherein said controlling operations accesses code and data from said first unified memory;
- wherein said demultiplexing one or more multimedia data streams, said performing MPEG decoding, and said controlling operations each use said first unified memory.

11. The method of claim 10,

- wherein said demultiplexing one or more multimedia data streams from the encoded stream includes accessing multimedia data stream data from said first unified memory;
- wherein said performing MPEG decoding on the multimedia data streams includes accessing video frame data from said first unified memory; and
- wherein said controlling operations includes accessing code and data from said first unified memory.

12. The method of claim 11, wherein the MPEG decoder system includes a memory controller coupled to the first unified memory;

- wherein said accessing multimedia data stream data from said first unified memory comprises accessing said multimedia data stream data through the memory controller;
- wherein said accessing video frame data from said first unified memory comprises accessing said video frame data through the memory controller; and
- wherein said accessing code and data from said first unified memory comprises accessing said code and data through the memory controller.

13. The method of claim 10, wherein the MPEG decoder system includes a memory controller coupled to the first unified memory, the method further comprising:

- the memory controller storing compressed data in the first unified memory to reduce memory storage requirements.

14. The method of claim 10, wherein the MPEG decoder system includes a memory controller coupled to the first unified memory, the method further comprising:

19

the memory controller dynamically allocating segments of memory space in the first unified memory to optimize memory use.

15. The method of claim 10, wherein said first unified memory has a memory size which does not exceed 16 Mbit. 5

16. A video decoder system which includes a single memory for use by transport, decode and system controller functions, comprising:

a channel receiver for receiving an encoded video stream; transport logic coupled to the channel receiver which demultiplexes one or more multimedia data streams from the encoded stream; 10

a system controller coupled to the transport logic which controls operations within the video decoder system; 15

a video decoder coupled to receive one or more multimedia data streams output from the transport logic, wherein the video decoder operates to perform video decoding on the multimedia data streams; and

a memory coupled to the video decoder, wherein the memory is used by the video decoder during video decoding operations, wherein the memory stores code and data useable by the system controller which enables the system controller to perform control functions within the video decoder system, wherein the memory is used by the transport logic for demultiplexing operations; 20 25

wherein the video decoder is operable to access the memory during video decoding operations;

20

wherein the transport logic is operable to access the memory to store and retrieve data during demultiplexing operations; and

wherein the system controller is operable to access the memory to retrieve code and data during system control functions.

17. The video decoder system of claim 16, wherein the video decoder includes a memory controller coupled to the memory; 10

wherein the transport logic is coupled to the memory controller and is operable to access the memory through the memory controller; and

wherein the system controller is coupled to the memory controller and is operable to access the memory through the memory controller.

18. The video decoder system of claim 17, wherein the memory controller is operable to store compressed data in the memory to reduce memory storage requirements.

19. The video decoder system of claim 17, wherein the memory controller is operable to dynamically allocate segments of memory space in the memory to optimize memory use. 20

20. The video decoder system of claim 16, wherein said memory has a memory size which does not exceed 16 Mbit.

* * * * *

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:
Kwok Kit Chau

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For: MPEG DECODER SYSTEM AND
METHOD HAVING A UNIFIED
MEMORY FOR TRANSPORT, DECODE
AND SYSTEM CONTROLLER
FUNCTIONS

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Dear Sir:

Enclosed for filing in the above-referenced Patent Application are the following:

1. A Specification consisting of a title page, a 29 page Disclosure, 5 pages of Claims (Claims 1 - 20) and a one page Abstract of the Disclosure;
2. Informal drawings consisting of 16 sheets (Figs. 1 through 15);
3. A Combined Declaration and Power of Attorney executed by the inventors;
4. An Assignment document and coversheet and \$40.00 to cover the filing fee;
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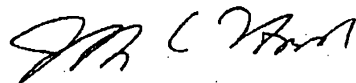
A check in the amount of the total filing fee is enclosed. However, if the check is missing or insufficient, the Commissioner is authorized to charge any additional fees which may be required, or credit any overpayment, to Conley, Rose & Tayon, P.C. Deposit Account No. 03-2769/5201-01600/JCH. Two duplicate copies of this sheet are enclosed.

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Pursuant to 37 C.F.R. §1.53(b) and (d), the Applicants request the Patent and Trademark Office to accept the application and accord a serial number and filing date as of the date this Application is deposited with the U. S. Postal Service for Express Mail.

Respectfully submitted,



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Title: MPEG Decoder System and Method Having a Unified Memory for
Transport, Decode and System Controller Functions

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Title: MPEG Decoder System and Method Having a Unified Memory for Transport Decode and System Controller Functions

Inventor: Kwok Chau

Incorporation by Reference

The following references are hereby incorporated by reference.

The ISO/IEC MPEG specification referred to as ISO/IEC 13818 is hereby incorporated by reference in its entirety.

U.S. Patent Application Serial No. 08/654,321 titled "Method and Apparatus for Segmenting Memory to Reduce the Memory Required for Bidirectionally Predictive-Coded Frames" and filed May 27, 1996 is hereby incorporated by reference in its entirety as though fully and completely set forth herein.

U.S. Patent Application Serial No. 08/653,845 titled "Method and Apparatus for Reducing the Memory Required for Decoding Bidirectionally Predictive-Coded Frames During Pull-Down" and filed May 27, 1996 is hereby incorporated by reference in its entirety as though fully and completely set forth herein.

U.S. Patent Application Serial No. 08/689,500 titled "System and Method for Decoding B Frames in Video Codecs with Minimal Memory" and filed August 7, 1996, now U.S. Pat. No. 5,818,533 whose inventors are David R. Auld and Kwok Chau, is hereby incorporated by reference in its entirety as though fully and completely set forth herein.

Field of the Invention

The present invention relates generally to digital video compression, and more particularly to an MPEG decoder system which includes a single unified memory for MPEG transport, decode and system controller functions.

Description of the Related Art

Full-motion digital video requires a large amount of storage and data transfer bandwidth. Thus, video systems use various types of video compression algorithms to reduce the amount of necessary storage and transfer bandwidth. In general, different

video compression methods exist for still graphic images and for full-motion video. Intraframe compression methods are used to compress data within a still image or single frame using spatial redundancies within the frame. Interframe compression methods are used to compress multiple frames, i.e., motion video, using the temporal redundancy between the frames. Interframe compression methods are used exclusively for motion video, either alone or in conjunction with intraframe compression methods.

Intraframe or still image compression techniques generally use frequency domain techniques, such as the discrete cosine transform (DCT). Intraframe compression typically uses the frequency characteristics of a picture frame to efficiently encode a frame and remove spatial redundancy. Examples of video data compression for still graphic images are JPEG (Joint Photographic Experts Group) compression and RLE (run-length encoding). JPEG compression is a group of related standards that provide either lossless (no image quality degradation) or lossy (imperceptible to severe degradation) compression. Although JPEG compression was originally designed for the compression of still images rather than video, JPEG compression is used in some motion video applications. The RLE compression method operates by testing for duplicated pixels in a single line of the bit map and storing the number of consecutive duplicate pixels rather than the data for the pixels themselves.

In contrast to compression algorithms for still images, most video compression algorithms are designed to compress full motion video. As mentioned above, video compression algorithms for motion video use a concept referred to as interframe compression to remove temporal redundancies between frames. Interframe compression involves storing only the differences between successive frames in the data file. Interframe compression stores the entire image of a key frame or reference frame, generally in a moderately compressed format. Successive frames are compared with the key frame, and only the differences between the key frame and the successive frames are stored. Periodically, such as when new scenes are displayed, new key frames are stored, and subsequent comparisons begin from this new reference point. It is noted that the interframe compression ratio may be kept constant while varying the video quality. Alternatively, interframe compression ratios may be content-dependent, i.e., if the video

clip being compressed includes many abrupt scene transitions from one image to another, the compression is less efficient. Examples of video compression which use an interframe compression technique are MPEG, DVI and Indeo, among others.

5 MPEG Background

A compression standard referred to as MPEG (Moving Pictures Experts Group) compression is a set of methods for compression and decompression of full motion video images which uses the interframe and intraframe compression techniques described above. MPEG compression uses both motion compensation and discrete cosine
10 transform (DCT) processes, among others, and can yield compression ratios of more than 30:1.

The two predominant MPEG standards are referred to as MPEG-1 and MPEG-2. The MPEG-1 standard generally concerns frame data reduction using block-based motion compensation prediction (MCP), which generally uses temporal differential pulse code
15 modulation (DPCM). The MPEG-2 standard is similar to the MPEG-1 standard, but includes extensions to cover a wider range of applications, including interlaced digital video such as high definition television (HDTV).

Interframe compression methods such as MPEG are based on the fact that, in most video sequences, the background remains relatively stable while action takes place in the
20 foreground. The background may move, but large portions of successive frames in a video sequence are redundant. MPEG compression uses this inherent redundancy to encode or compress frames in the sequence.

An MPEG stream includes three types of pictures, referred to as the Intra (I) frame, the Predicted (P) frame, and the Bi-directional Interpolated (B) frame. The I or
25 Intraframes contain the video data for the entire frame of video and are typically placed every 10 to 15 frames. Intraframes provide entry points into the file for random access, and are generally only moderately compressed. Predicted frames are encoded with reference to a past frame, i.e., a prior Intraframe or Predicted frame. Thus P frames only include changes relative to prior I or P frames. In general, Predicted frames receive a
30 fairly high amount of compression and are used as references for future Predicted frames.

Thus, both I and P frames are used as references for subsequent frames. Bi-directional pictures include the greatest amount of compression and require both a past and a future reference in order to be encoded. Bi-directional frames are never used as references for other frames.

5 In general, for the frame(s) following a reference frame, i.e., P and B frames that follow a reference I or P frame, only small portions of these frames are different from the corresponding portions of the respective reference frame. Thus, for these frames, only the differences are captured, compressed and stored. The differences between these frames are typically generated using motion vector estimation logic, as discussed below.

10 When an MPEG encoder receives a video file, the MPEG encoder generally first creates the I frames. The MPEG encoder may compress the I frame using an intraframe compression technique. The MPEG encoder divides respective frames into a grid of 16 x 16 pixel squares called macroblocks in order to perform motion estimation/compensation. Thus, for a respective target picture or frame, i.e., a frame being encoded, the encoder
15 searches for an exact, or near exact, match between the target picture macroblock and a block in a neighboring picture referred to as a search frame. For a target P frame the encoder searches in a prior I or P frame. For a target B frame, the encoder searches in a prior or subsequent I or P frame. When a match is found, the encoder transmits a vector movement code or motion vector. The vector movement code or motion vector only
20 includes information on the difference between the search frame and the respective target picture. The blocks in target pictures that have no change relative to the block in the reference picture or I frame are ignored. Thus the amount of data that is actually stored for these frames is significantly reduced.

 After motion vectors have been generated, the encoder then encodes the changes
25 using spatial redundancy. Thus, after finding the changes in location of the macroblocks, the MPEG algorithm further calculates and encodes the difference between corresponding macroblocks. Encoding the difference is accomplished through a math process referred to as the discrete cosine transform or DCT. This process divides the macroblock into four sub blocks, seeking out changes in color and brightness. Human perception is more
30 sensitive to brightness changes than color changes. Thus the MPEG algorithm devotes

more effort to reducing color data than brightness.

Therefore, MPEG compression is based on two types of redundancies in video sequences, these being spatial, which is the redundancy in an individual frame, and temporal, which is the redundancy between consecutive frames. Spatial compression is achieved by considering the frequency characteristics of a picture frame. Each frame is divided into non-overlapping blocks, and each block is transformed via the discrete cosine transform (DCT). After the transformed blocks are converted to the "DCT domain", each entry in the transformed block is quantized with respect to a set of quantization tables. The quantization step for each entry can vary, taking into account the sensitivity of the human visual system (HVS) to the frequency. Since the HVS is more sensitive to low frequencies, most of the high frequency entries are quantized to zero. In this step where the entries are quantized, information is lost and errors are introduced to the reconstructed image. Run length encoding is used to transmit the quantized values. To further enhance compression, the blocks are scanned in a zig-zag ordering that scans the lower frequency entries first, and the non-zero quantized values, along with the zero run lengths, are entropy encoded.

When an MPEG decoder receives an encoded stream, the MPEG decoder reverses the above operations. Thus the MPEG decoder performs inverse scanning to remove the zig zag ordering, inverse quantization to de-quantize the data, and the inverse DCT to convert the data from the frequency domain back to the pixel domain. The MPEG decoder also performs motion compensation using the transmitted motion vectors to re-create the temporally compressed frames.

When frames are received which are used as references for other frames, such as I or P frames, these frames are decoded and stored in memory. When a temporally compressed or encoded frame is received, such as a P or B frame, motion compensation is performed on the frame using the prior decoded I or P reference frames. The temporally compressed or encoded frame, referred to as a target frame, will include motion vectors which reference blocks in prior decoded I or P frames stored in the memory. The MPEG decoder examines the motion vector, determines the respective

reference block in the reference frame, and accesses the reference block pointed to by the motion vector from the memory.

A typical MPEG decoder includes motion compensation logic which includes local or on-chip memory. The MPEG decoder also includes an external memory which
5 stores prior decoded reference frames. The MPEG decoder accesses the reference frames or anchor frames stored in the external memory in order to reconstruct temporally compressed frames. The MPEG decoder also typically stores the frame being reconstructed in the external memory.

An MPEG decoder system also typically includes transport logic which operates
10 to demultiplex received data into a plurality of individual multimedia streams. An MPEG decoder system also generally includes a system controller which controls operations in the system and executes programs or applets.

Prior art MPEG video decoder systems have generally used a frame store memory for the MPEG decoder motion compensation logic which stores the reference frames or
15 anchor frames as well as the frame being reconstructed. Prior art MPEG video decoder systems have also generally included a separate memory for the transport and system controller functions. It has generally not been possible to combine these memories, due to size limitations. For example, current memory devices are fabricated on an 4 Mbit granularity. In prior art systems, the memory requirements for the transport and system
20 controller functions as well as the decoder motion compensation logic would exceed 16 Mbits of memory, thus requiring 20 or 24 Mbits of memory. This additional memory adds considerable cost to the system.

The amount of memory is a major cost item in the production of video decoders. Thus, it is desired to reduce the memory requirements of the decoder system as much as
25 possible to reduce its size and cost. Since practical memory devices are implemented using particular convenient discrete sizes, it is important to stay within a particular size if possible for commercial reasons. For example, it is desired to keep the memory requirements below a particular size of memory, such as 16 Mb, since otherwise a memory device of 20 or 24 Mb would have to be used, resulting in greater cost and
30 extraneous storage area. As mentioned above, it has heretofore not been possible to

combine the memory required for the transport and system controller functions with the memory required for the MPEG decoder logic due to the memory size requirements.

Therefore, a new video decoder system and method is desired which efficiently uses memory and combines the memory subsystem for reduced memory requirements
5 and hence reduced cost.

Summary of the Invention

The present invention comprises an MPEG decoder system and method for performing video decoding or decompression which includes a unified memory for multiple functions according to the present invention. The video decoding system includes transport logic, a system controller, and MPEG decoder logic. The video decoding system of the present invention includes a single unified memory which stores code and data for the transport logic, system controller and MPEG decoder functions. The single unified memory is preferably a 16 Mbit memory. The present invention thus requires only a single memory, and thus has reduced memory requirements compared to prior art designs.

The video decoding system includes transport logic which operates to demultiplex received data into a plurality of individual multimedia streams. The video decoding system also includes a system controller which controls operations in the system and executes programs or applets. The video decoding system further includes decoding logic, preferably MPEG decoder logic, which performs motion compensation between temporally compressed frames of a video sequence during video decoding or video decompression. The memory includes a plurality of memory portions, including a video frame portion for storing video frames, a system controller portion for storing code and data executable by the system controller, and a transport buffer for storing data used by the transport logic. The MPEG decoder logic preferably includes a memory controller which couples to the single unified memory. Each of the transport logic, system controller, and MPEG decoder logic accesses the single unified memory through the memory controller.

The video decoding system implements various frame memory saving schemes, such as compression or dynamic allocation, to reduce the required amount of frame store memory. Also, in one embodiment, the memory is not required to store reconstructed frame data during motion compensation, thus considerably reducing the required amount of memory for this function. Alternatively, the memory is only required to store a portion of the reconstructed frame data. These savings in memory allow portions of the memory to also be used for transport and system controller functions.

The present invention thus provides a video decoding system with reduced memory requirements.

Brief Description of the Drawings

A better understanding of the present invention can be obtained when the following detailed description of the preferred embodiment is considered in conjunction with the following drawings, in which:

5 Figures 1 illustrates a computer system which performs video decoding and which includes a motion compensation logic having a frame memory which stores reference block data according to the present invention;

Figure 2 is a block diagram illustrating the computer system of Figure 1;

10 Figure 3 is a block diagram illustrating an MPEG decoder system including a unified memory for MPEG transport, system controller, and decode functions according to the present invention;

Figure 4 is a block diagram illustrating the MPEG decoder logic in the system of Figure 3;

15 Figure 5 illustrates various frame memory saving schemes used in various embodiments of the invention;

Figures 6a and 6b illustrate a table listing the memory partitions under different display schemes;

Figure 7 illustrates the relationship of memory bandwidth vs. memory size in the NTSC decoding scheme;

20 Figure 8 illustrates the relationship of memory bandwidth vs. memory size in the PAL encoding scheme;

Figure 9 illustrates the memory partitions according to the preferred embodiment of the invention;

25 Figure 10 illustrates the estimated memory bandwidth distribution in the preferred embodiment of the invention;

Figure 11 illustrates the "worst case" relationship of processing power vs. memory size in the NTSC decoding scheme;

Figure 12 illustrates the clock domains in the system;

30 Figure 13 illustrates clock operating frequencies according to the preferred embodiment of the invention;

Figure 14 illustrates an example of the packet data interface between the transport controller and the source decoder; and

Figure 15 illustrates packet header formats used in the preferred embodiment.

Detailed Description of the Preferred Embodiment

Video Compression System

Referring now to Figure 1, a system for performing video decoding or
5 decompression and including a unified memory according to the present invention is shown. The video decoding system of the present invention includes a single unified memory which stores code and data for the transport, system controller and MPEG decoder functions. This simplifies the design and reduces the memory requirements in the system.

10 As shown, in one embodiment the video decoding or decompression system is comprised in a general purpose computer system 60. The video decoding system may comprise any of various types of systems, including a computer system, set-top box, television, or other device.

The computer system 60 is preferably coupled to a media storage unit 62 which
15 stores digital video files which are to be decompressed or decoded by the computer system 60. The media storage unit 62 may also store the resultant decoded or decompressed video file. In the preferred embodiment, the computer system 60 receives a compressed video file or bitstream and generates a normal uncompressed digital video file. In the present disclosure, the term "compressed video file" refers to a video file
20 which has been compressed according to any of various video compression algorithms which use motion estimation techniques, including the MPEG standard, among others, and the term "uncompressed digital video file" refers to a stream of decoded or uncompressed video.

As shown, the computer system 60 preferably includes a video decoder 74 which
25 performs video decoding or decompression operations. The video decoder 74 is preferably an MPEG decoder. The computer system 60 optionally may also include an MPEG encoder 76. The MPEG decoder 74 and MPEG encoder 76 are preferably adapter cards coupled to a bus in the computer system, but are shown external to the computer system 60 for illustrative purposes. The computer system 60 also includes software,

represented by floppy disks 72, which may perform portions of the video decompression or decoding operation and/or may perform other operations, as desired.

The computer system 60 preferably includes various standard components, including one or more processors, one or more buses, a hard drive and memory. Referring now to Figure 2, a block diagram illustrating the components comprised in the computer system of Figure 1 is shown. It is noted that Figure 2 is illustrative only, and other computer architectures may be used, as desired. As shown, the computer system includes at least one processor 80 coupled through chipset logic 82 to a system memory 84. The chipset 82 preferably includes a PCI (Peripheral Component Interconnect) bridge for interfacing to PCI bus 86, or another type of bus bridge for interfacing to another type of expansion bus. In Figure 2, MPEG decoder 74 and MPEG encoder 76 are shown connected to PCI bus 86. Various other components may be comprised in the computer system, such as video 88 and hard drive 90.

As mentioned above, in the preferred embodiment of Figure 1 the computer system 60 includes or is coupled to one or more digital storage or media storage devices. For example, in the embodiment of Figure 1, the computer system 60 couples to media storage unit 62 through cable 64. The media storage unit 62 preferably comprises a RAID (Redundant Array of Inexpensive Disks) disk array, or includes one or more CD-ROM drives and/or one or more Digital Video Disk (DVD) storage units, or other media, for storing digital video to be decompressed and/or for storing the resultant decoded video data. The computer system may also include one or more internal RAID arrays, CD-ROM drives and/or may couple to one or more separate Digital Video Disk (DVD) storage units. The computer system 60 also may connect to other types of digital or analog storage devices or media, as desired.

Alternatively, the compressed digital video file may be received from an external source, such as a remote storage device or remote computer system. In this embodiment, the computer system preferably includes an input device, such as an ATM (Asynchronous Transfer Mode) adapter card or an ISDN (Integrated Services Digital Network) terminal adapter, or other digital data receiver, for receiving the digital video file. The digital

video file may also be stored or received in analog format and converted to digital data, either externally to the computer system 60 or within the computer system 60.

As mentioned above, the MPEG decoder 74 in the computer system 60 performs video decoding or video decompression functions. As discussed further below, the video decoding system includes transport logic which operates to demultiplex received data into a plurality of individual multimedia streams. The video decoding system also includes a system controller which controls operations in the system and executes programs or applets comprised in the stream. The video decoding system further includes decoding logic, preferably MPEG decoder logic, which performs motion compensation between temporally compressed frames of a video sequence during video decoding or video decompression. The video decoding system of the present invention includes a single unified memory which stores code and data for the transport, system controller and MPEG decoder functions. This simplifies the design and reduces the memory requirements in the system. The MPEG decoder 74 thus performs functions with improved efficiency and reduced memory requirements according to the present invention.

It is noted that the system for decoding or decompressing video data may comprise two or more interconnected computers, as desired. The system for decoding or decompressing video data may also comprise other hardware, such as a set top box, either alone or used in conjunction with a general purpose programmable computer. It is noted that any of various types of systems may be used for decoding or decompressing video data according to the present invention, as desired.

Figure 3 - MPEG Decoder Block Diagram

Referring now to Figure 3, a block diagram illustrating an MPEG decoder system architecture according to one embodiment of the present invention is shown. As shown, the MPEG decoder system includes a channel receiver 202 for receiving a coded stream. As mentioned above, in the preferred embodiment, the coded stream is an MPEG encoded stream. The MPEG encoded stream may include interactive program content

comprised within this stream, as desired. The channel receiver 202 receives the coded stream and provides the coded stream to a transport and system controller block 204.

The transport and system controller block 204 includes transport logic 206 which operates to demultiplex the received MPEG encoded stream into a plurality of multimedia data streams. In other words, the encoded stream preferably includes a plurality of multiplexed encoded channels or multimedia data streams which are combined into a single stream, such as a broadcast signal provided from a broadcast network. The transport logic 206 in the transport and system controller block 204 operates to demultiplex this multiplexed stream into one or more programs, wherein each of the programs comprise individual multimedia data streams including video and/or audio components.

It is noted that the MPEG stream may comprise one of two types of streams including either a transport stream or a program stream. A transport stream comprises a 188 byte stream which includes error correction and which is designed for an error prone environment. A program stream, on the other hand, is designed for an error free environment and this does not include error correction capabilities.

The transport and system controller block 204 also includes a system controller 208 which monitors the MPEG system and is programmable to display audio/graphics on the screen and/or execute interactive applets or programs which are embedded in the MPEG stream. The system controller 208 also preferably controls operations in the MPEG decoder system. In the preferred embodiment, the system controller 208 comprises a MIPS RISC CPU which is programmed to perform system controller functions.

The transport and system controller block 204 couples through a memory controller 211 in MPEG decoder 224 to an external memory 212, also referred to as the single unified memory 212. The transport logic 206 and system controller logic 208 comprised in the transport and system controller block 204 utilize the external memory 212 to store and/or receive code and data. In the preferred embodiment, the external memory 212 is a 16 MB synchronous dynamic random access memory (SDRAM).

As shown, the transport and system controller block 204 couples to an MPEG decoder block 222. The MPEG decoder block 222 includes an MPEG audio visual decoder 224, as shown. The MPEG audio visual decoder 224 receives data from the transport and system controller block 204 and operates to perform MPEG decoding to
5 produce a decoded or decompressed signal. The visual component of the decompressed signal is output from the MPEG A/V decoder 224 and is provided to a video encoder 226. The video encoder 226 operates to convert the digital video stream into a format more appropriate for transmission or display, such as NTSC or PAL format. The video encoder logic 226 includes digital to analog (D/A) converters for converting the decoded digital
10 video stream into an analog stream. This analog video stream is then provided as an output of the system as shown.

The audio component of the decoded or decompressed MPEG stream is provided to an audio digital to analog converter (DAC) 228. The audio DAC 228 operates to perform digital to analog conversion on the digital audio signal output from the MPEG
15 A/V decoder 224. The resulting analog audio signals are provided as an output to the system as shown.

As shown, the external memory 212 is coupled to the MPEG A/V decoder 224. The MPEG A/V decoder 224 includes a memory controller 211 which controls access to the single unified memory 212. As noted above, each of the transport logic 206 and
20 system controller logic 208 comprised in the transport and system controller block 204 access the external memory 212 through the memory controller 211.

The MPEG A/V decoder 224 utilizes the external memory 212 in the MPEG decode process. Thus the MPEG A/V decoder 224 uses the same memory 212 as the transport and system controller blocks. As is well-known in the art, the MPEG A/V
25 decoder 224 uses the external memory 212 to store decoded reference frames or anchor frames which are used during motion compensation or reconstruction of temporally compressed frames. The MPEG A/V decoder 224 may also use the external memory 212 to store a portion or all of the reconstructed frames.

30 Reconstructed Frame Data Memory Saving Schemes

It is noted that reconstruction of a temporally compressed frame during MPEG decoding typically uses a full 16 MB of external memory. However, the MPEG decoder system 74 of the preferred embodiment uses one or more of various methods to reduce the amount of memory required for storing reconstructed frame data. For example, 5 current prior art video decoder implementations use at least one frame of memory to store the reconstructed B-picture prior to display. In other words, prior art decoders require that there be a full frame store into which to reconstruct the B frame or picture.

In one embodiment of the invention, the video decoder system 74 uses as little as 2.528 frame stores when there is no pulldown during B-frames. In this embodiment, the 10 system uses an improved method to reduce the required amount of memory, whereby the memory used to store the first field is used again for reconstruction as soon as that part of the picture has been displayed. This method reduces the amount of memory needed for B-frame reconstruction to about 0.528 frames. For more information on this method, please see U.S. Patent Application Serial No. 08/654,321 titled "Method and Apparatus for 15 Segmenting Memory to Reduce the Memory Required for Bidirectionally Predictive-Coded Frames" and filed May 27, 1996, which is hereby incorporated by reference in its entirety as though fully and completely set forth herein.

In another embodiment of the invention, the video decoder system 74 uses as little as 2.75 frames when there is pulldown. In this embodiment, a method is used to reduce 20 the memory required for decoding and displaying B frames during 3:2 pull-down. This method uses the fact that B frames are not used to predict other frames, so that once the B frame data is retrieved for display, it may be discarded. To enable re-use of memory, data from the top and bottom fields is separated into different segments of memory. Thus, once retrieval begins of the data in a segment, that segment becomes free for reconstruction. 25 However, this initial scheme is not completely sufficient for the top field of every other frame during 3:2 pull-down, since the top field must be somehow made available again for re-display. Rather than requiring additional memory to save the top field of every other frame, the top field is reconstructed again during the period when reconstruction is typically stalled. In this manner, the amount of memory required is reduced, and the field requiring 30 re-display for 3:2 pull-down is simply reconstructed again. For more information on this

method for reducing the required amount of memory when pull-down is being performed, please see U.S. Patent Application Serial No. 08/653,845 titled "Method and Apparatus for Reducing the Memory Required for Decoding Bidirectionally Predictive-Coded Frames During Pull-Down" and filed May 27, 1996, which is hereby incorporated by
5 reference in its entirety as though fully and completely set forth herein.

The above methods used to reduce memory requirements, which are disclosed in the above-referenced patent applications, are optimal, i.e., use the least possible memory, where the picture is decoded only once. In another embodiment, The MPEG decoder 74 includes frame reconstruction or decoder logic which operates to reconstruct a bi-
10 directionally encoded (B) frame without requiring storage of the frame being constructed in the external memory 112. In this embodiment, the MPEG decoder 74 operates to decode or reconstruct the frame twice, once during each field display period. This obviates the necessity of storing the reconstructed B frame data, thus reducing memory requirements.

15 In this embodiment, the MPEG decoder system includes a picture reconstruction unit, a picture display unit, a pointer register, and a temporary buffer (all not shown). The picture memory 212 includes separate buffers used for anchor pictures or reference frames (A1, A2) and a rate buffer which stores the temporally compressed frame, referred to as C. The pointer register stores the location of the first byte of the compressed picture,
20 which is stored in the rate buffer. According to this embodiment, the picture memory 212 is not required to store data from the reconstructed frame.

The picture reconstruction unit operates to decode or reconstruct the B frame twice, once each during a first field time and a second field time. The first field time substantially corresponds to the time when the first or top field of the picture is displayed,
25 and the second field time substantially corresponds to the time when the second or bottom field of the picture is displayed.

During the first field time, compressed picture data is read from the rate buffer into the picture reconstruction unit, where the picture is decoded. The top field data from the picture reconstruction unit is written to the temporary buffer, and the bottom field
30 data is discarded. After one slice of the picture has been decoded, the data in the

temporary buffer is retrieved by the picture display unit and is output for display. This process continues for the entire picture in order to display all of the first field. Thus, the entire picture is decoded or reconstructed, and only data from the top field is written to the temporary buffer for display.

5 During the second field time, the same compressed picture is again read from the rate buffer. The picture reconstruction unit again decodes the compressed picture. In the second field time, the picture reconstruction unit writes the bottom field data to the temporary buffer, and the top field data is discarded. After one slice of the picture has been decoded, the data in the temporary buffer is output by the picture display unit for
10 display. This process continues for the entire picture in order to display all of the second field.

 The reconstructed picture is never written to the memory during reconstruction of B-frames. It is also noted that the temporary buffer is about 32 times smaller than the external frame store required in the best implementation of prior art methods. This
15 allows the temporary buffer to be comprised on the same monolithic substrate as the decoder itself.

 Therefore, in this embodiment the video decoder system reconstructs the B-picture twice, once in each field time. This eliminates the storage requirement of the reconstructed B-frame entirely and thus allows this memory space to be used for transport
20 and system controller functions.

 In another embodiment, the MPEG decoder system of the preferred embodiment uses a dynamic segment allocation scheme and/or compression techniques which reduce the external memory requirement. These memory saving techniques are discussed further below.

25 Therefore, the video decoding system 74 includes transport logic 206 which operates to demultiplex received data into a plurality of individual multimedia streams. The video decoding system also includes a system controller 208 which controls operations in the system and executes programs or applets comprised in the stream. The video decoding system 74 further includes decoding logic 224, preferably MPEG decoder
30 logic, performs motion compensation between temporally compressed frames of a video

sequence during video decoding or video decompression. The video decoding system of the present invention includes a single unified memory which stores code and data for the transport, system controller and MPEG decoder functions. This simplifies the design and reduces the memory requirements in the system.

5 As discussed above, prior art MPEG decoder systems include different memory systems for the transport and system controller logic 204 and the MPEG decoder logic 224. These separate memories are required because of the separate bandwidth and processing requirements for each memory, as well as the memory size requirements of each block. According to the system and method of the present invention, the present
10 invention includes a single or unified memory which is used for each of the transport and system controller block 204 and the MPEG A/V decoder logic 224.

Figure 4 - MPEG Decoder Block Diagram

Referring now to Figure 4, a block diagram illustrating the MPEG A/V decoder
15 logic 224 in the MPEG decoder 74 which performs motion compensation according to the present invention is shown. As shown, the video decoder logic 224 receives an encoded or compressed digital video stream and outputs an uncompressed digital video stream. The compressed digital video stream is a bitstream of compressed video data which is used to present a video sequence, such as a television segment or movie, onto a
20 screen, such as a television or a computer system. In the preferred embodiment, the compressed digital video stream is compressed using the MPEG-2 compression algorithm, and the video decoder 74 is thus preferably an MPEG-2 decoder. Since the operation of MPEG decoders is well known in the art, details of their operation which are not necessary to the operation of the present invention are omitted for simplicity.

25 As shown in Figure 3, the decoder logic 224 comprises a Variable Length Decoding block 302 coupled to provide an output to an Inverse Scan block 304, which is coupled to provide an output to an Inverse Quantization block 306, which is coupled to provide an output to an Inverse DCT block 308, which is coupled to provide an output to a motion compensation block 310. The motion compensation block 310 provides an output
30 comprising decoded samples. A frame store memory 212 is coupled to the output of the

motion compensation block 310 to receive and store decoded frame data. The motion compensation block 310 is coupled to an output of the frame store memory 212 to receive reference block data from the frame store memory 212 during motion compensation.

As shown in Figure 3, the Variable Length Decoding block 302 receives coded data
5 and performs variable length decoding. As is well known, the MPEG standard provides that data is compressed for transmission using variable length codes. Thus the Variable Length Decoding block 302 decodes this data and produces an output, referred to as QFS[n]. The QFS[n] output of the Variable Length Decoding block 302 is provided to the Inverse Scan block 304. The Inverse Scan block 304 reverses the zig zag scan ordering of
10 the received data (is this right) and produces an output referred to as QF[v][u]. The output QF[v][u] is provided to the Inverse Quantization block 306. The Inverse Quantization block 306 performs inverse quantization or de-quantizes the data to produce de-quantized data, referred to as F[v][u]. The output F[v][u] of the Inverse Quantization block 306 is provided to the Inverse DCT block 308, which performs the inverse discrete cosine
15 transform to convert the data from the frequency domain back to the pixel domain. The inverse DCT block 308 produces an output referred to as f[y][x]. The output f[y][x] of the inverse DCT block 308 is provided to the motion compensation block 310.

The output f[y][x] from the inverse DCT block 308 comprises temporally encoded frames of pixel data. The motion compensation block 310 decompresses the temporally
20 compressed frames using motion compensation techniques. As described above, an MPEG encoded stream comprises I, P and B frames. P and B frames are temporally compressed relative to other frames. P frames are temporally compressed relative to prior I or P frames, and B frames are temporally compressed relative to prior or subsequent I or P frames. When a frame is temporally compressed, the frame is partitioned into macroblocks, referred
25 to as target blocks, and then the compression method searches in neighboring frames for blocks which are most similar to the block being encoded. When the best fit block is found, the respective target block is encoded by a motion vector which points to this best fit reference block in the reference frame. The difference between the block being encoded and the best fit block is also computed and transferred in the MPEG stream.

Output pixel values from the motion compensation block 310 are provided to a frame store memory 212. The frame store memory 212 is thus coupled to the motion compensation block 310 and stores one or more reference frames of video data. These reference frames of video data are used in performing motion compensation on temporally compressed frames, such as P and B frames. In general, an MPEG stream includes encoded reference frame data which is transmitted before temporally compressed data that depends on the prior transmitted reference frame data. Thus, incoming temporally encoded frame data, such as P and B frame data, comprises motion vectors which point to reference blocks in a prior transmitted reference frame of video data, which has been stored in the frame store memory 212. The motion compensation block 310 analyzes each motion vector from the incoming temporally compressed data and retrieves a reference block from the frame store memory 212 in response to each motion vector. The motion compensation block 310 includes a local memory or on-chip memory 116 which stores the retrieved reference block. The motion compensation block 110 then uses this retrieved reference block to decompress the temporally compressed data.

In the preferred embodiment, the frame store memory 212 is 1M x 16 SDRAM, such as Samsung KM416S1120AT-12, having an operating frequency of 81 MHz or 108 MHz and a burst size of 4 words. As discussed above, the frame store memory 112 is also used according to the present invention to store code and data for the transport logic 206 and the system controller logic 208.

Figure 5 - Memory Saving Schemes

Figure 5 illustrates various frame memory saving schemes used in various embodiments of the invention. As shown, in European systems which do not include a field repeat, dynamic memory segment allocation techniques are used to more efficiently use the memory space. In other words, memory segments or areas are dynamically allocated to minimize unused space. These dynamic memory segment allocation techniques range from a 40 segment technique ($\times/2.556$) to a 3.22 (3) segment technique ($\times/2.801$). As the memory segment size decreases, a larger amount of granularity is

provided, and the memory can be used in a more "detailed" or specific fashion. The dynamic allocation scheme operates to dynamically allocate segments of memory of different size to more efficiently use the available memory and correspondingly result in little or no un-used space.

5 In U.S. systems with field repeat, compression techniques are preferably used to reduce memory requirements. These compression techniques include a "compressed bitstream" technique and a "local compression" technique.

The compressed bitstream technique operates to store frame data in its received MPEG compressed format, instead of storing the frame data in a decoded or decompressed format. When this compressed data is read from memory, the compressed
10 memory is decoded or decompressed "on the fly". As shown, the compressed bitstream technique may involve storing only one of the anchor frames in a compressed format, storing only the B frames in a compressed format, or storing both the anchor and B frames in a compressed format.

15 The local compression technique comprises re-encoding the decoded or compressed bitstream, preferably using a standard compression standard such as DPCM or MPEG. Thus, once frames have been decoded or reconstructed, the frame data is re-encoded prior to storage in memory. As shown, the local compression may involve compressing one of the anchor frames only, the B frames only, or both the anchor and B
20 frames.

Figures 6a and 6b - Memory Partitions

Figures 6A and 6B illustrate a table listing the memory partitions under different memory reduction schemes. As shown, the table of FIG. 1 illustrates the memory
25 requirements for both the NTSC and PAL decoding schemes for a standard LSI L64005 part, a method which compresses the displayed anchor frame, a method which compresses both the anchor and the segment storing the B frame, a method which compresses only the B frame, and a method which compresses both the anchor and entire B frame. LSI part no. L64005 is a device produced by LSI Logic that has no memory
30 reduction for NTSC and has dynamic allocation for PAL.

As shown, in the NTSC format using LSI part No. L64005, the frame store memory requires 12,441,600 bits of memory for storing three full frames. The channel buffer requires 2,864,637 bits of memory for various functions. As shown in the table, these functions include the vbv (video buffer verifier) buffer, the video non-instantaneous
5 decode function, the video display sync function, the audio buffer, the audio-video latency difference function, the audio-display sync function, the video transport buffer, the audio transport buffer, and the jitter buffer (4 ms jitter at 15 Mbps). Each of the above functions collectively requires 2,864,637 bits for the channel buffer. The packet header overhead requires 20,000 bits of memory, the on-screen display (OSD) requires
10 675,840 bits of memory. This provides a subtotal for the software and data storage of 775,139 bits. The total required storage for the NTSC format is 16,777,216 bits of memory. As shown, the frame store and channel buffer collectively require 15,306,237 bits of memory.

As shown, the PAL decoding scheme using L64005 is similar. As shown the
15 PAL decoding scheme requires 12,718,080 bits of memory to store 2.556 frames of memory. The channel buffer's subtotal for the PAL decoding scheme requires 3,060,847 bits of memory. The packet header overhead for the pal scheme is also 20,000 bits, and the onscreen display requires 808,192 bits. The subtotal for software and data storage in the PAL decoding scheme is 170,097 bits. Thus, the PAL decoding scheme using
20 L64005 requires a total of 16,777,216 bits. As shown, for the PAL format, the frame store and channel buffer collectively require 15,778,927 bits of memory.

As shown, when the displayed anchor is compressed, the NTSC format requires 9,538,560 bits for the frame store, which is required to store the equivalent of 2.3 frames. The total for the frame store and channel buffer requirements is 14,208,205 bits, as well
25 as 1,873,171 bits for the software and data. For the PAL decoding scheme with a compressed display anchor, 11,197,440 bits are required for the frame store. The frame store and channel buffer collectively require 16,063,295 bits, and the software and data requirement is (114,271). Thus, there are 114,271 bits "over budget" over a 16Mbit target.

Where the anchor and the B segment are both compressed, for the NTSC decoding scheme, assuming 3.267 segments, the frame store is reduced to 8,778,240 bits and is required to store only 2.117 frames. Under this method, the frame store and channel buffer collectively require 13,447,885 bits of memory, and the subtotal for the software and data requirement is 2,633,491 bits of memory. In the PAL decoding scheme where the method compresses an anchor and segment B, assuming 40 segments, the frame store requires 8,985,600 bits and requires 1.806 frames to be stored. This method requires 13,851,455 bits to collectively store the frame store and channel buffer data, and the subtotal for software and data storage is 2,097,569 bits.

When the memory compresses only the B frame to optimize memory storage, in the NTSC format, the frame store required is 8,570,880 bits of memory and stores an equivalent of 2.067 frames. Under this method, the frame store and channel buffer require a total of 11,435,517 bits and a subtotal for software and data storage of 4,645,859 bits. In the PAL decoding scheme where the B frame only is compressed, the frame store requires 10,229,760 bits and thus stores 2.056 equivalent number of frames. In this method, the frames store and channel buffer collectively require 13,290,607 bits of memory, and the subtotal for software and data storage requires 2,658,417 bits of memory.

Where the system compresses both the anchor and the B frame to optimize memory, in the NTSC format, the frame store required is 5,667,840 bits of memory and stores an equivalent of 1.367 frames. Under this method, the frame store and channel buffer require a total of 10,337,485 bits and a subtotal for software and data storage of 5,743,891 bits. In the PAL decoding scheme where both the anchor frame and B frame are compressed, the frame store requires 6,497,280 bits and thus stores 1.306 equivalent number of frames. In this method, the frames store and channel buffer collectively require 11,363,135 bits of memory, and the subtotal for software and data storage requires 4,585,889 bits of memory.

Figure 7 - Memory Bandwidth vs. Memory Size in the NTSC Decoding Scheme

Figure 7 illustrates the relationship of memory bandwidth vs. memory size in the NTSC decoding scheme. The memory size on the x axis of the graph is the memory size required for the frame store memory and the channel buffer. As shown, as the memory size decreases from left to right, the required amount of memory and/or processing bandwidth increases. Thus, a greater amount of memory transfer and/or processing bandwidth is required as the memory size is reduced. Figure 7 illustrates four different plots for each memory size, where these plots comprise 100%, 96%, and 87%, and 72% of useable bandwidth. The various lines illustrated in the graph of FIG. 7 illustrate the change in bandwidth versus the change in memory size, i.e., the $\Delta\text{bandwidth} / \Delta\text{memory}$, which comprises the units bytes/second/bit. As shown, the optimum memory size in the NTSC format is 13,447,885 bits.

Figure 8 - Memory Bandwidth vs. Memory Size in the NTSC Decoding Scheme

Figure 8 illustrates the relationship of memory bandwidth vs. memory size in the PAL decoding scheme. As with Figure 7, the memory size on the x axis of the graph is the memory size required for the frame store memory and the channel buffer. As shown, as the memory size decreases from left to right, the required amount of memory and/or processing bandwidth increases. Thus, a greater amount of memory transfer and/or processing bandwidth is required as the memory size is reduced. Figure 8 also illustrates four different plots for each memory size, where these plots comprise 100%, 96%, and 87%, and 72% of useable bandwidth. The various lines illustrated in the graph of FIG. 8 illustrate the change in bandwidth versus the change in memory size, i.e., the $\Delta\text{bandwidth} / \Delta\text{memory}$, which comprises the units bytes/second/bit. As shown, the $\Delta\text{bandwidth} / \Delta\text{memory}$ peaks at 13,851,455 bits, which is the optimum memory size in the PAL format.

Figure 9 - Memory Partitions

Figure 9 illustrates the memory partitions of the external memory 212 for each of the NTSC and PAL encoding formats according to one embodiment of the invention. Figure 9 illustrates the number of bytes of memory size allocated for different purposes in

the unified memory 212, including number of bits for video frames, the vbv buffer, the video decode buffer, the video-display synch buffer, the audio buffer, the audio-video latency buffer, the audio-display synch buffer, the transport buffer, the jitter buffer, the PES header overhead memory, the OSD, and the system controller code and data storage. It is noted that Figure 9 illustrates the memory partition according to one embodiment of the invention, and it is noted that the memory 212 may be allocated differently, as desired. As shown, the memory size requirement are substantially comparable. In this example, the NTSC format uses 10,583,248 bytes for storing video frames, and the PAL format uses 10,790,608 bytes for storing video frames.

Figure 10 - Decoding Memory Bandwidth

Figure 10 illustrates the estimated memory bandwidth distribution in the preferred embodiment of the invention for the NTSC and PAL formats. Figure 10 illustrates the estimated memory bandwidth distribution using the memory partition embodiment of Figure 9. The estimated memory bandwidth distribution shown in Figure 10 presumes a 16 X 1 MB SDRAM running at 100 MHz, wherein bandwidth is available at 200 MB per second. This memory bandwidth distribution also presumes a requirement of 20 Mbytes per second for code and data executed by the system controller 208 in the transport and system controller block 204. As noted above, the system controller 208 is preferably a MIPS RISC CPU. As shown, the NTSC scheme requires 160.19 MB per second bandwidth, whereas the PAL decoding scheme requires 157.18 MB per second of bandwidth. The bandwidth requirements for each of the NTSC and PAL formats are substantially comparable with the exception that the NTSC format requires a greater amount of memory bandwidth for the channel in/out function than does the PAL format.

Figure 11 - Processing Power vs. Memory Size (NTSC)

Figure 11 illustrates the "worst case" relationship of processing power vs. memory size in the NTSC decoding scheme. In Figure 11, the lines represent available cycles per macroblock for a decoder operating at 27 to 216 MHz. The bars represent the required cycles per macroblock reconstructed for 1 to 4 cycle/coefficient throughput. For

example, a 100 MHz decoder can operate with 13,447,885 memory points at 1 and 2-cycle/coefficient throughput only (not the slow 4-cycle/coefficient). However, as shown, the processing power tends to increase as the memory decreases in size from 13,447,885 bytes to 11,435,517 bytes. The 11,435,517 and 19,337,485 memory points require a large amount of processing power, and thus even 216 MHz processing speed is not sufficient with 2-cycle/coefficient throughput.

Figures 12 and 13 - Clock Domains

Figure 12 illustrates the clock domains in the system, i.e., the various possible clock rates for the external memory 212 according to one embodiment of the invention. The video decoder system in the preferred embodiment includes a source decoder which operates at 27 Megahertz. The source decoder clock frequency of 27 Megahertz is required according to modern video encoding schemes. However, current memory operating frequencies are not designed for video applications, i.e., are not designed to operate at multiples of 27 MHz. As shown, the memory 212 operates near multiples of this source decoder frequency such as 50 MHz or 100 MHz.

Figure 13 illustrates clock operating frequencies according to the preferred embodiment of the invention. In this embodiment, the external memory 212 is SDRAM or other suitable memory operating at 108 MHz, or a higher multiple. As shown, the transport and system controller block 204 preferably operates at either 54 MHz or 108 MHz. The source decoder 224 preferably also operates at 54 MHz or 108 MHz. Thus, as shown in FIG. 13, in the preferred embodiment the memory and hardware elements operate at multiples of the 27 MHz required clock frequency, i.e., either 54 Megahertz or 108 Megahertz.

Figure 14 - Packet Data Interface

Figure 14 illustrates an example of the packet data interface between the transport and system controller block 204 and the source decoder 224. As shown, the transport and system controller block 204 and the source decoder 224 communicate 16 bit transmission data, referred to as TD[15:0], in a bi-directional manner. The transmission data signals

TD[15:0] comprise a data bus for transmitting data between the transport and system control logic 204 and the source decoder 224. The transport and system controller block 204 provides a transmission data output enable (TDOE) signal which is provided as an input to the source decoder 224. The transport and system controller block 204 also provides a new packet word (NPW) signal as an input to the source decoder 224. The source decoder 224 provides two outputs to the transport and system controller block 204, these being a data chain hold (DCH) signal, which is a wait cycle request, and a TRDY (transmission ready) signal which indicates that the logic is ready for a new packet.

10 Figure 15 - Packet Header Formats

Figure 15 illustrates packet header formats used in the preferred embodiment. As shown, different packet header values are used to indicate a reset, a general data read, a general data write, a video stream write, and an audio stream write. The general data read and general data write packets each include fields for word count and address.

15 Conclusion

Therefore, the present invention comprises a video decoder system and method which includes a single unified memory for MPEG transport, decode, and system controller functions. This reduces the required amount of memory, thus simplifying system design and reducing system cost.

Although the system and method of the present invention has been described in connection with the described embodiments, it is not intended to be limited to the specific form set forth herein, but on the contrary, it is intended to cover such alternatives, modifications, and equivalents, as can be reasonably included within the spirit and scope of the invention as defined by the appended claims.

Claims

Sub A' > 1

2 An MPEG decoder system which includes a single memory for use by
transport, decode and system controller functions, comprising:

3 (a channel receiver) for receiving an MPEG encoded stream;

4 transport logic coupled to the channel receiver which demultiplexes one or more
5 multimedia data streams from the encoded stream;

6 a system controller coupled to the transport logic which controls operations within
7 the MPEG decoder system;

8 an MPEG decoder coupled to receive one or more multimedia data streams output
9 from the transport logic, wherein the MPEG decoder logic operates to perform MPEG
10 decoding on the multimedia data streams; and

11 a memory coupled to the MPEG decoder, wherein the memory is used by the
12 MPEG decoder during MPEG decoding operations, wherein the memory stores code and
13 data useable by the system controller which enables the system controller to perform
14 control functions within the MPEG decoder system, wherein the external memory is used
15 by the transport logic for demultiplexing operations;

16 wherein the MPEG decoder is operable to access the memory during MPEG
17 decoding operations;

18 wherein the transport logic is operable to access the memory to store and retrieve
19 data during demultiplexing operations; and

20 wherein the system controller is operable to access the memory to retrieve code
21 and data during system control functions.

22 2. The MPEG decoder system of claim 1, wherein the MPEG decoder
23 includes a memory controller coupled to the memory;

24 wherein the transport logic is coupled to the memory controller and is operable to
25 access the memory through the memory controller; and

26 wherein the system controller is coupled to the memory controller and is operable
27 to access the memory through the memory controller.

28

1 3. The MPEG decoder system of claim 2, wherein the memory controller is
2 operable to store compressed data in the memory to reduce memory storage requirements.

3 4. The MPEG decoder system of claim 2, wherein the memory controller is
4 operable to dynamically allocate segments of memory space in the memory to optimize
5 memory use.

5 5. The MPEG decoder system of claim 1, wherein the memory stores anchor
frame data during reconstruction of temporally compressed frames.

6 6. The MPEG decoder system of claim 1, wherein said memory has a
7 memory size which does not exceed 16 Mbit.

8 7. The MPEG decoder system of claim 1, wherein said memory includes a
9 plurality of memory portions, wherein said memory includes a video frame portion for
10 storing video frames, a system controller portion for storing code and data executable by
11 the system controller, and a transport buffer portion for storing data used by the transport
12 logic.

13

14 8. The MPEG decoder system of claim 7, wherein said memory further
15 includes a video decode buffer portion for storing decoded video data, a video display
16 sync buffer, and an on-screen display buffer.

17

18 9. The MPEG decoder system of claim 8, wherein said memory further
19 includes one or more audio buffers for storing audio data.

20

21 10. A method for performing video decoding in an MPEG decoder system
22 which includes a single memory for use by transport, decode and system controller
23 functions, the comprising:

24 receiving an MPEG encoded stream;

1 demultiplexing one or more multimedia data streams from the encoded stream,
2 wherein said demultiplexing one or more multimedia data streams from the encoded
3 stream operates using a first unified memory;
4 performing MPEG decoding on the multimedia data streams, wherein said
5 performing MPEG decoding operates using said first unified memory; and
6 a system controller controlling operations within the MPEG decoder system,
7 wherein said controlling operations accesses code and data from said first unified
8 memory;
9 wherein said demultiplexing one or more multimedia data streams, said
10 performing MPEG decoding, and said controlling operations each use said first unified
11 memory.

12
13 11. The method of claim 10,
14 wherein said demultiplexing one or more multimedia data streams from the
15 encoded stream includes accessing multimedia data stream data from said first unified
16 memory;
17 wherein said performing MPEG decoding on the multimedia data streams
18 includes accessing video frame data from said first unified memory; and
19 wherein said controlling operations includes accessing code and data from said
20 first unified memory.

21
22 *Sub A* 3 12. The method of claim 10, wherein the MPEG decoder system includes a
23 memory controller coupled to the first unified memory;
24 wherein said accessing multimedia data stream data from said first unified
25 memory comprises accessing said multimedia data stream data through the memory
26 controller;
27 wherein said accessing video frame data from said first unified memory comprises
28 accessing said video frame data through the memory controller; and
29 wherein said accessing code and data from said first unified memory comprises
30 accessing said code and data through the memory controller.

1 13. The method of claim 10, wherein the MPEG decoder system includes a
2 memory controller coupled to the first unified memory, the method further comprising:
3 the memory controller storing compressed data in the first unified memory to
4 reduce memory storage requirements.

5 14. The method of claim 10, wherein the MPEG decoder system includes a
6 memory controller coupled to the first unified memory, the method further comprising:
7 the memory controller dynamically allocating segments of memory space in the
8 first unified memory to optimize memory use.

9
10 15. The method of claim 10, wherein said first unified memory has a memory
11 size which does not exceed 16 Mbit.

12 *Sub A⁴* 16. A video decoder system which includes a single memory for use by
13 transport, decode and system controller functions, comprising:
14 a channel receiver for receiving an encoded video stream;
15 transport logic coupled to the channel receiver which demultiplexes one or more
16 multimedia data streams from the encoded stream;
17 a system controller coupled to the transport logic which controls operations within
18 the video decoder system;
19 a video decoder coupled to receive one or more multimedia data streams output
20 from the transport logic, wherein the video decoder logic operates to perform video
21 decoding on the multimedia data streams; and
22 a memory coupled to the video decoder, wherein the memory is used by the video
23 decoder during video decoding operations, wherein the memory stores code and data
24 useable by the system controller which enables the system controller to perform control
25 functions within the video decoder system, wherein the external memory is used by the
26 transport logic for demultiplexing operations;

1 wherein the video decoder is operable to access the memory during video
2 decoding operations;

3 wherein the transport logic is operable to access the memory to store and retrieve
4 data during demultiplexing operations; and

5 wherein the system controller is operable to access the memory to retrieve code
6 and data during system control functions.

7 17. The video decoder system of claim 16, wherein the video decoder includes
8 a memory controller coupled to the memory;

9 wherein the transport logic is coupled to the memory controller and is operable to
10 access the memory through the memory controller; and

11 wherein the system controller is coupled to the memory controller and is operable
12 to access the memory through the memory controller.

13 18. The video decoder system of claim 17, wherein the memory controller is
14 operable to store compressed data in the memory to reduce memory storage requirements.

15 19. The video decoder system of claim 17, wherein the memory controller is
16 operable to dynamically allocate segments of memory space in the memory to optimize
17 memory use.

20 20. The video decoder system of claim 16, wherein said memory has a
memory size which does not exceed 16 Mbit.

18

19

20

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Abstract of the Disclosure

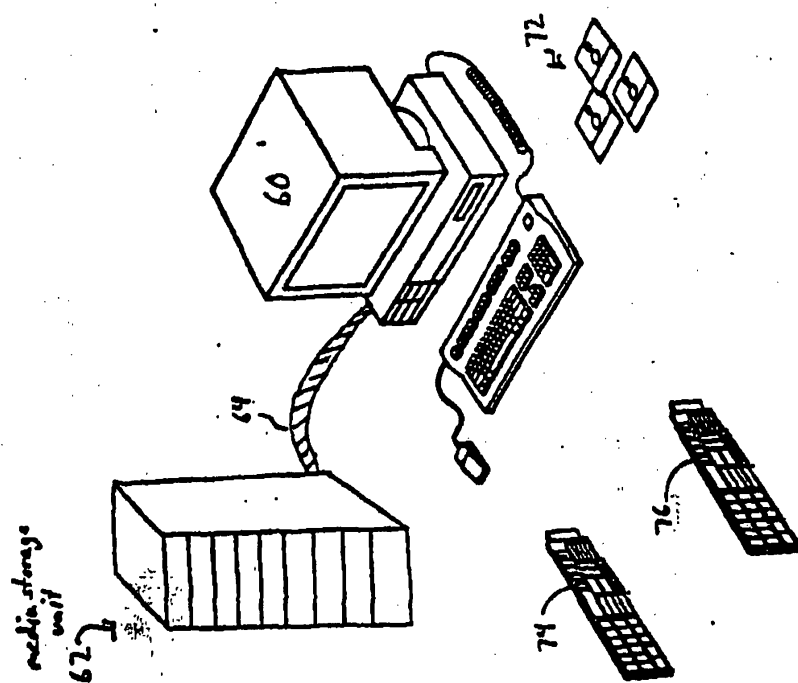
5 An MPEG decoder system and method for performing video decoding or decompression which includes a unified memory for multiple functions according to the present invention. The video decoding system includes transport logic, a system controller, and MPEG decoder logic. The video decoding system of the present invention includes a single unified memory which stores code and data for the transport, system controller and MPEG decoder functions. The single unified memory is preferably a 16 Mbit memory. The MPEG decoder logic includes a memory controller which couples to
10 the single unified memory, and each of the transport logic, system controller and MPEG decoder logic access the single unified memory through the memory controller. The video decoding system implements various frame memory saving schemes, such as compression or dynamic allocation, to more efficiently use the memory. In one embodiment, the memory is not required to store reconstructed frame data during B-frame reconstruction, thus considerably reducing the required amount of memory for this
15 function. Alternatively, the memory is only required to store a portion of the reconstructed frame data. In addition, these savings in memory allow portions of the memory to also be used for transport and system controller functions. The present invention thus provides a video decoding system with reduced memory requirements.

20

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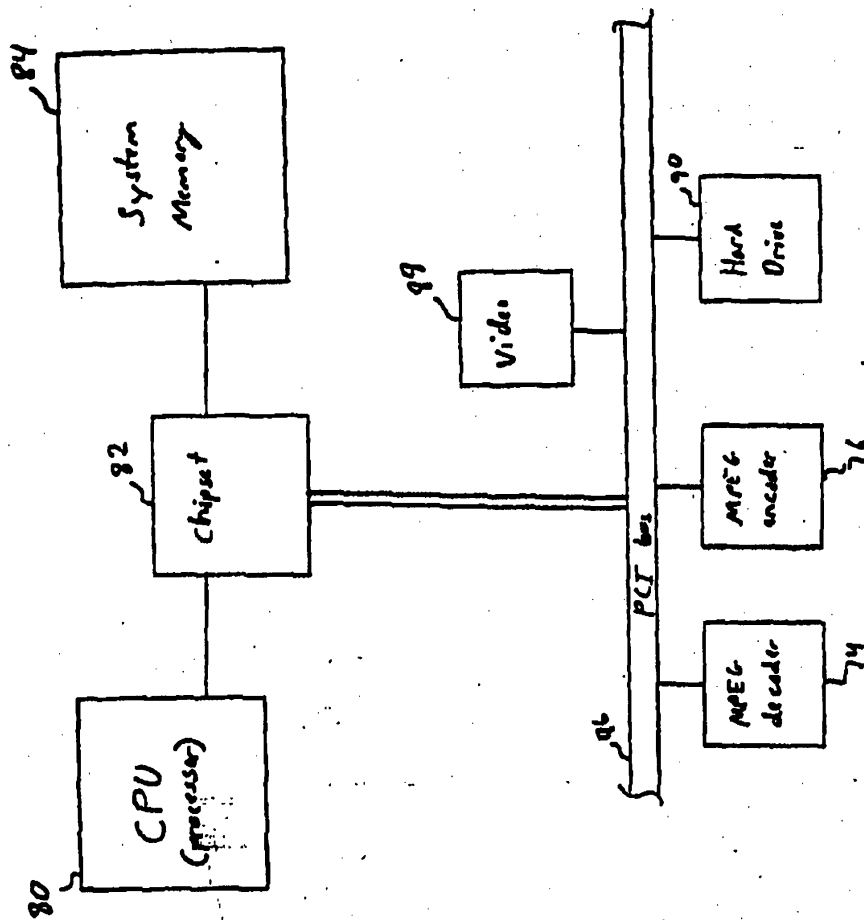


Figure 2

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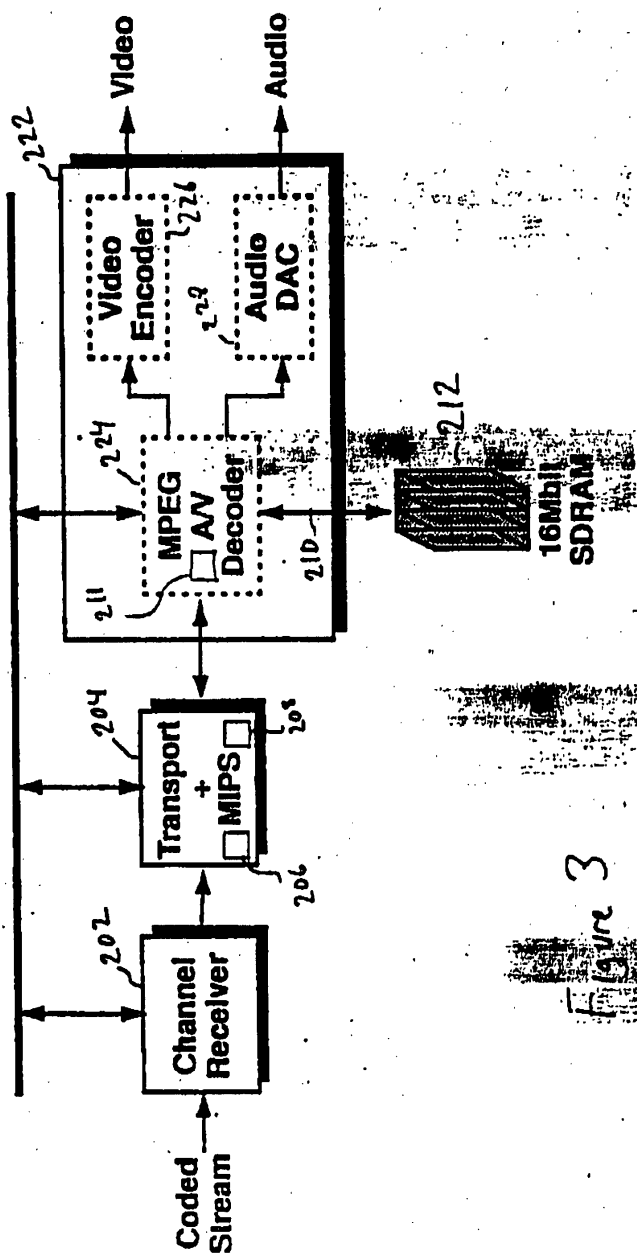


Figure 3

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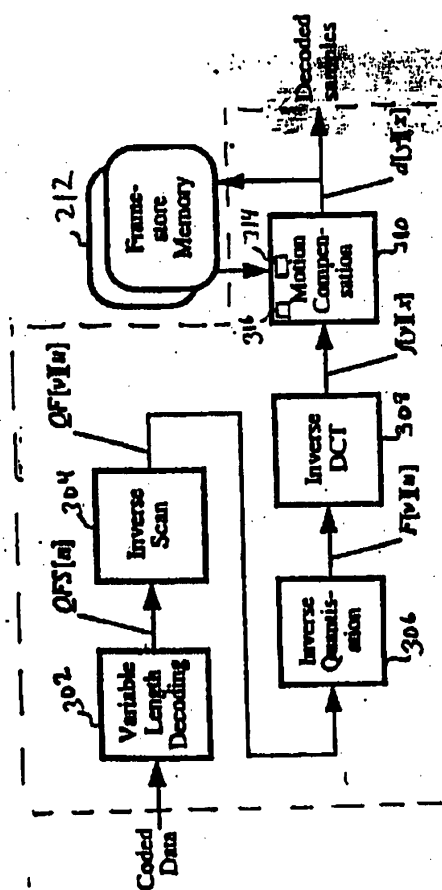
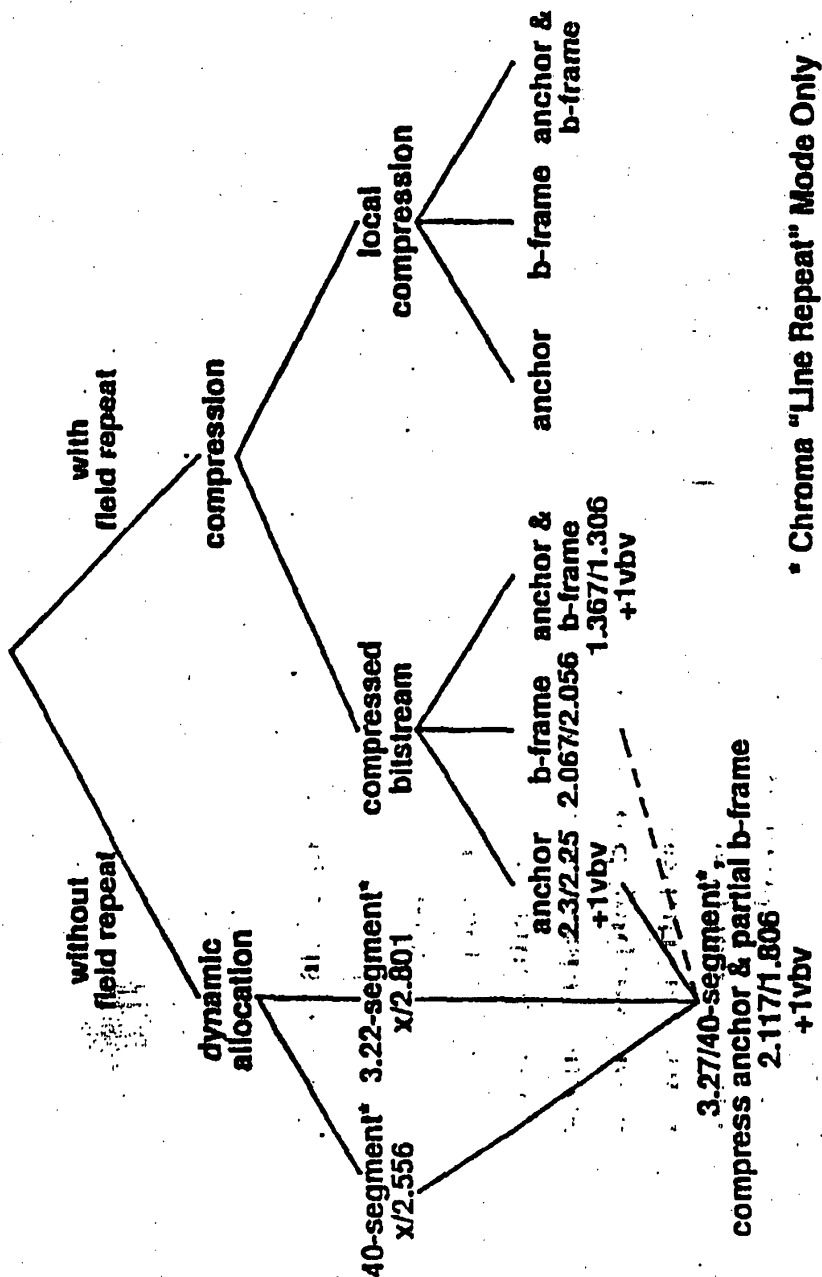


Figure 4

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FIG. 5.



* Chroma "Line Repeat" Mode Only

08/748269

FIG. 6A

Table 1 MPEG Decoder: Memory Partition

	L64005		Compress Displayed Anchor	
	NTSC	PAL	NTSC	PAL
frame store (number of frames)	12,441,888 (3,000)	12,718,880 (2,556)	9,538,880 (2,300)	11,197,440 (2,250)
vbv buffer	1,805,008	1,805,008	3,610,016	3,610,016
video non-instantaneous decode	430,785	520,575		
video-display sync	500,000	600,000		
audio buffer	28,672	28,672		
audio-video latency difference	19,200	23,040		
audio-display sync	12,800	15,360		
video transport buffer	4,096	4,096		
audio transport buffer	4,096	4,096		
4ms jitter at 15Mbps	60,000	60,000		
sub-total for channel buffer	2,864,537	3,060,847	4,669,645	4,865,655
packet header overhead	20,000	20,000		
OSD	675,840	808,192		
sub-total for software data	775,139	170,097	1,673,171	(114,271)
Grand Total	15,777,216	16,777,216		
frame store + channel buffer	15,308,237	15,778,927	14,208,205	18,063,295

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FIG. 6B

MPEG Decoder: Memory Partition

Table 1

Compress Anchor & Segment B		Compress B-Frame		Compress Anchor & B-Frame	
NTSC: 3.267 segments	PAL: 40 segments	NTSC	PAL	NTSC	PAL
8,778,240 (2.117)	8,985,600 (1.806)	8,570,880 (2.067)	10,229,760 (2.056)	5,867,840 (1.367)	6,497,280 (1.306)
3,610,016	3,610,016			3,610,016	3,610,016
4,889,645	4,885,855			4,889,645	4,885,855
2,633,491	2,097,589	4,845,859	5,858,417	5,743,891	4,585,889
13,447,885	13,851,455	11,435,517	13,290,807	10,337,485	11,369,135

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Fig. 7 Memory Bandwidth vs Memory Size (Frame & Channel)
NTSC

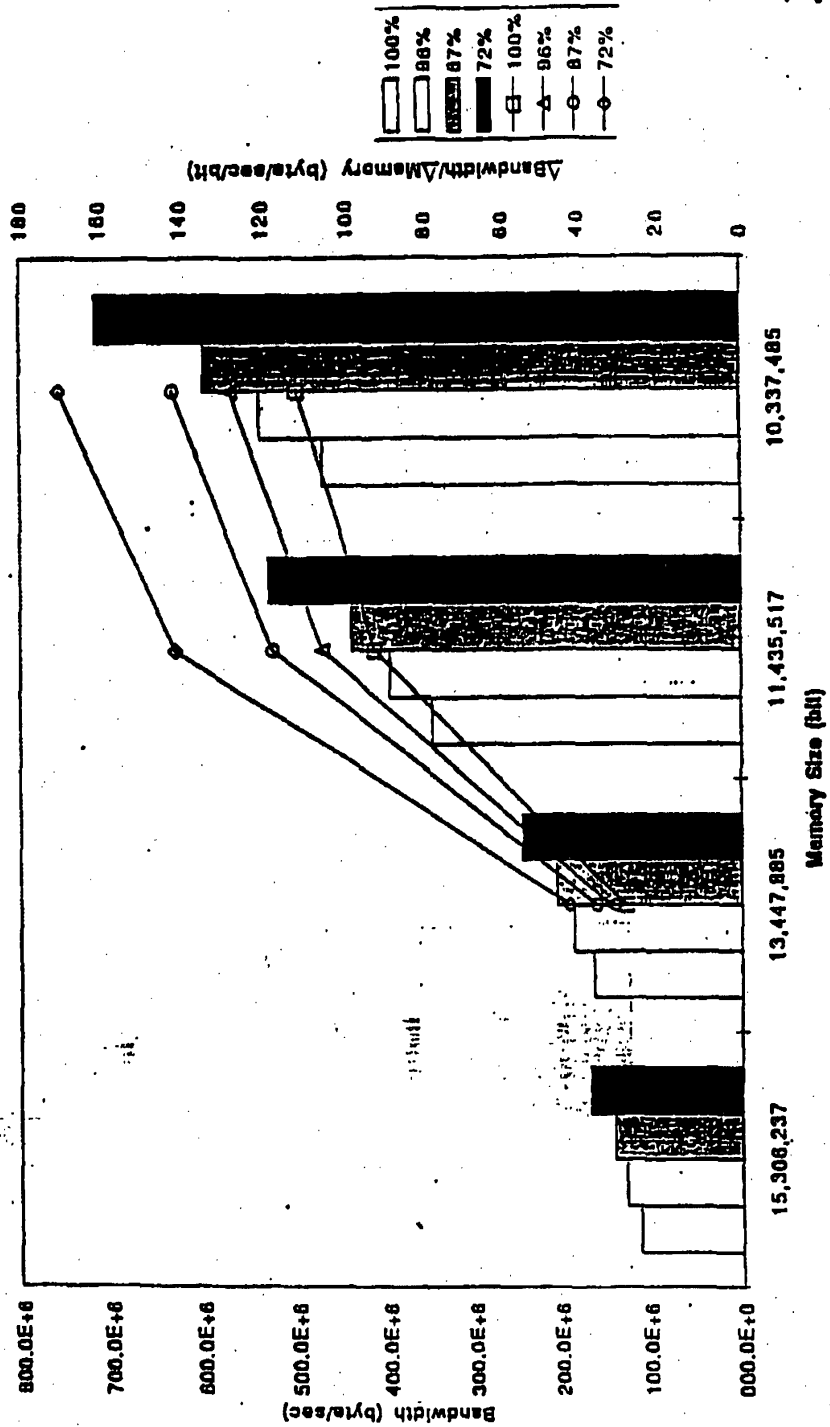


Fig. 8
Memory Bandwidth vs Memory Size (Frame & Channel)
PAL

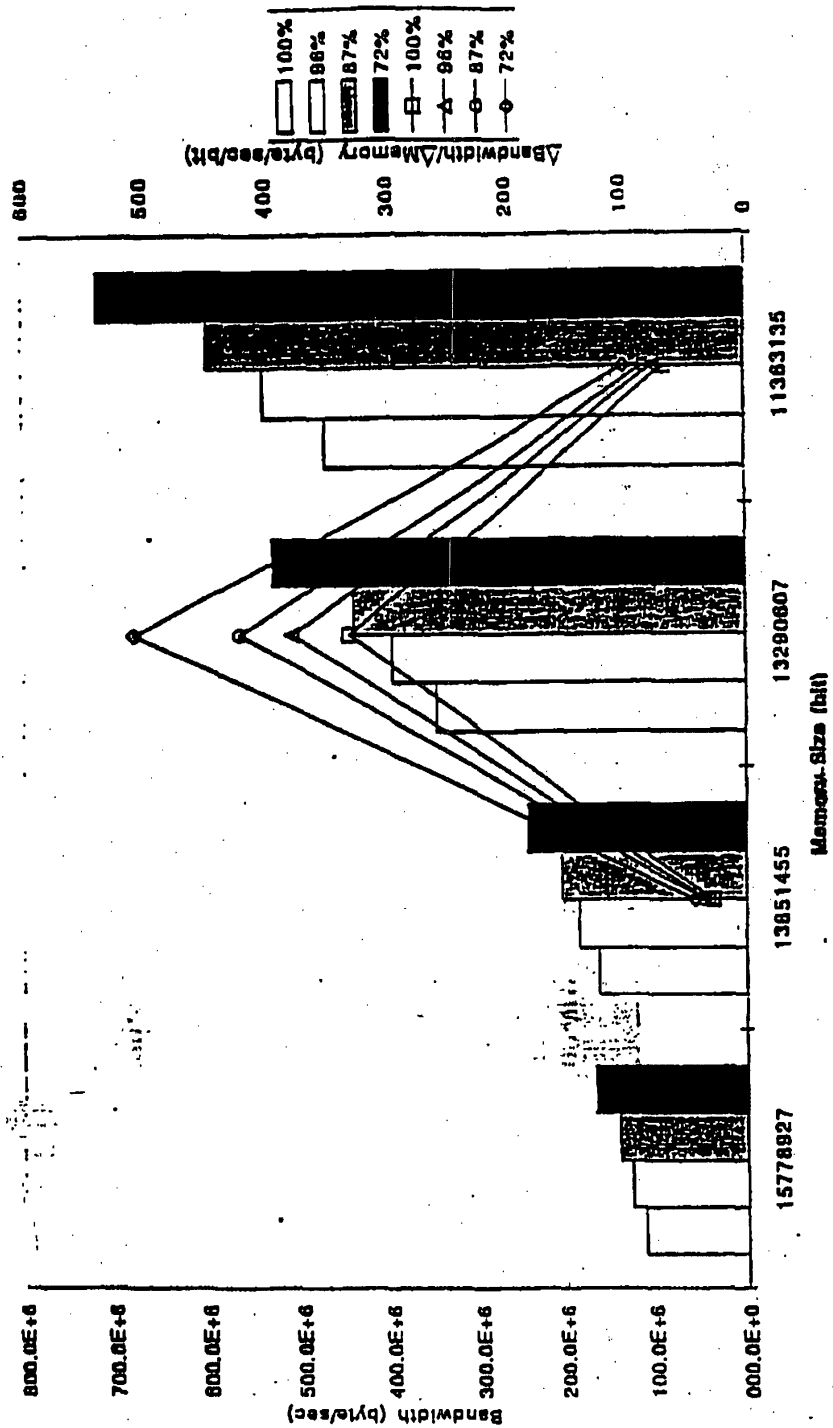


FIG. 9

	bit	
	NTSC	PAL
Video Frames (incl. compressed)	10,583,248	10,790,608
VBV Buffer	1,805,008	1,805,008
Video Decode Buffer	430,765	520,575
Video-Display Sync Buffer	500,000	600,000
Audio Buffer	28,672	28,672
Audio-Video Latency Buffer	19,200	23,040
Audio-Display Sync Buffer	12,800	15,360
Transport Buffer	8,192	8,192
Jitter Buffer (4ms)	60,000	60,000
PES Header Overhead	20,000	20,000
OSD	675,840	808,192
MIPS Code and Data	2,633,491	2,097,569

FIG. 10

	Bandwidth (Mbyte/sec)	
	NTSC	PAL
Channel In/Out	18.82	15.98
Motion Compensation	72.70	72.59
Store	38.29	38.23
Display & OSD	30.38	30.38
TOTAL	160.19	157.18

- With 16x1M SDRAM running at 100MHz, Bandwidth Available is 200Mbyte/sec
- Expecting 20Mbyte/sec for MIPS Code and Data

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Fig. 11 Processing Power vs Memory (Frame & Channel) Size
NTSC

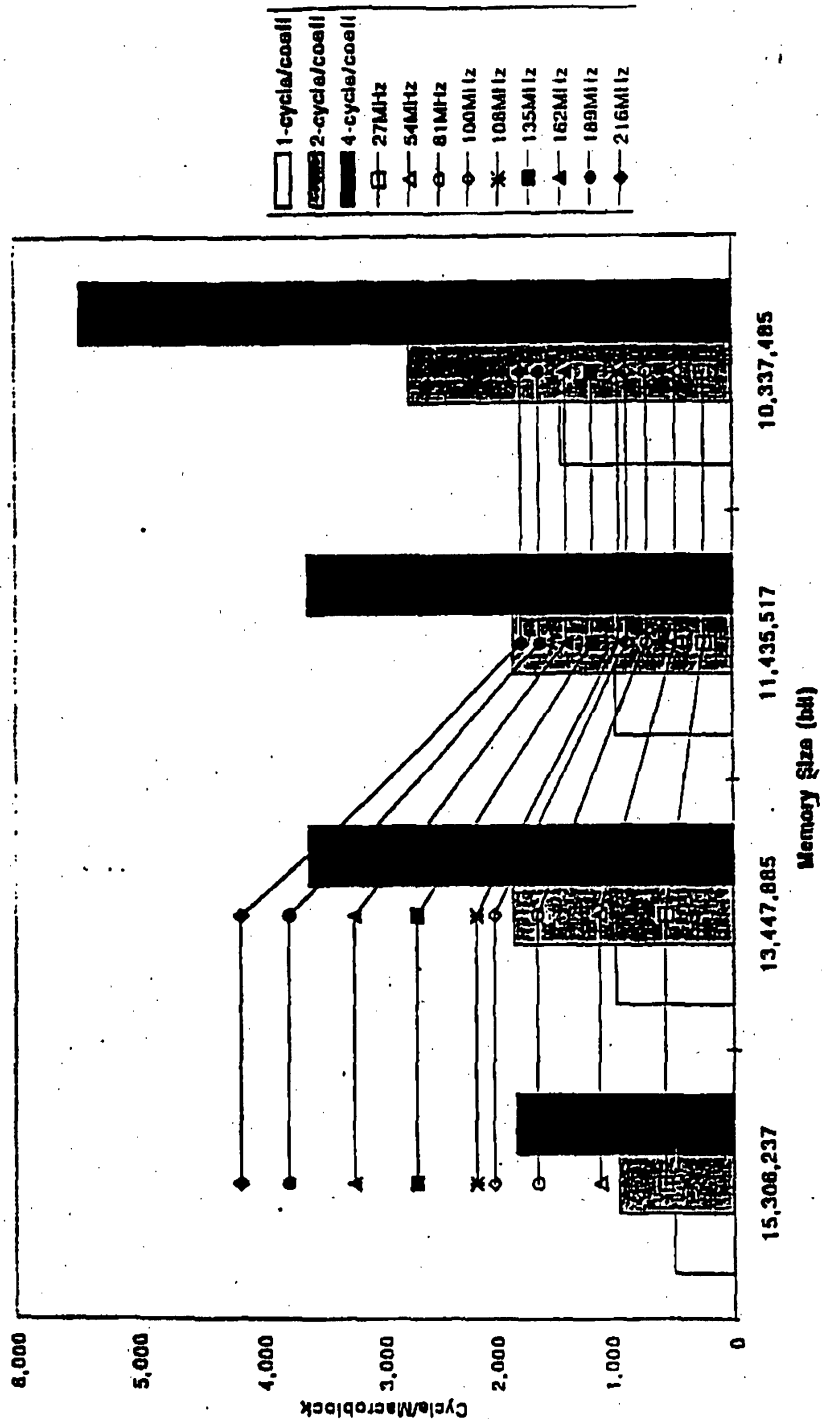


FIG. 12

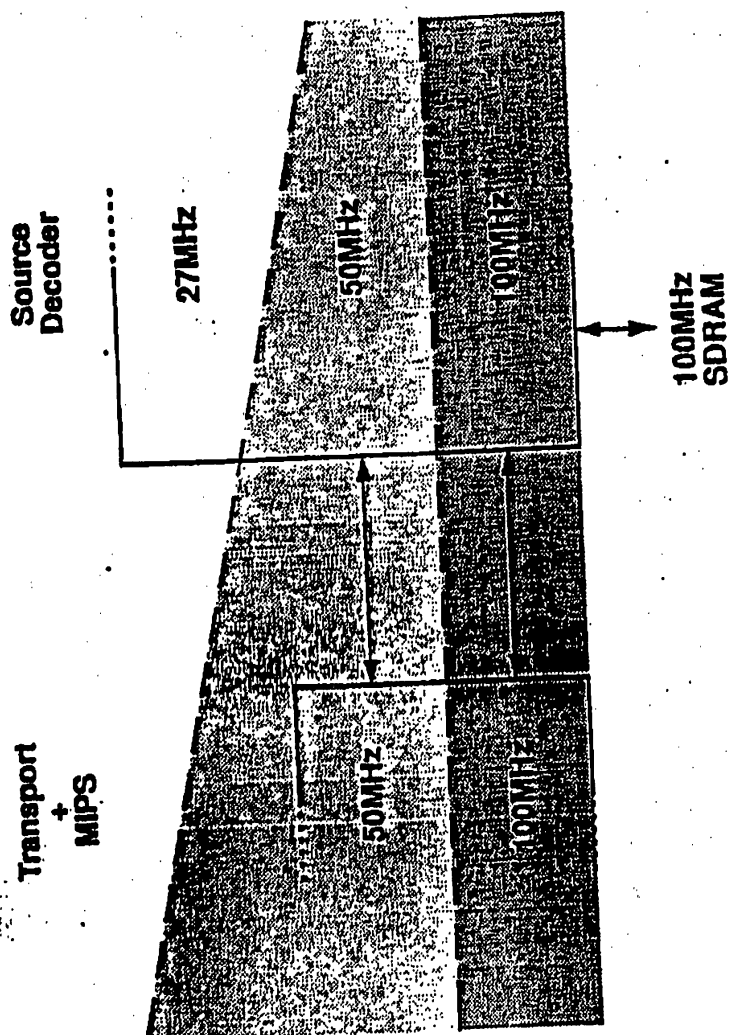
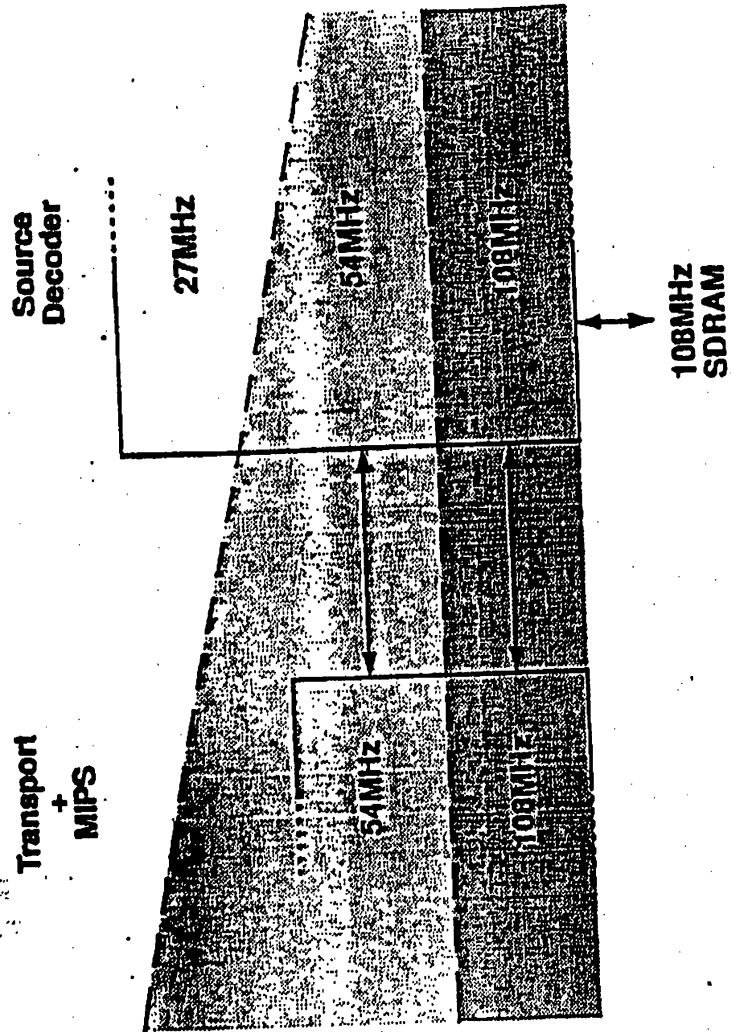
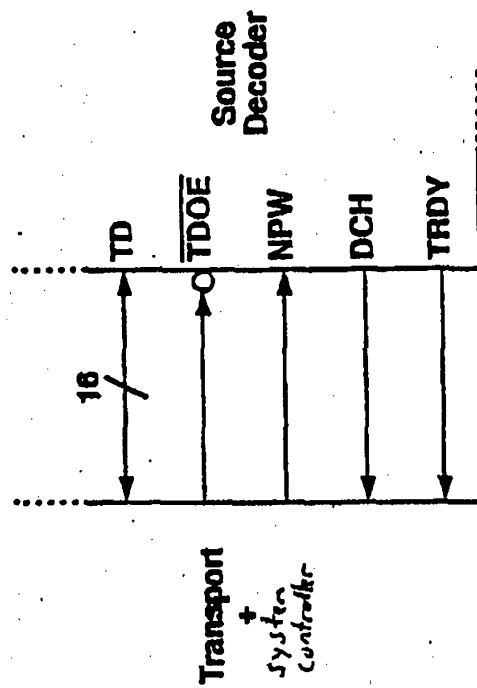


FIG. 13



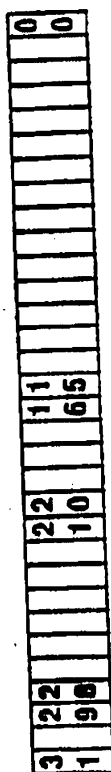
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FIG. 14



Signal	Description	Type
TD[15:0]	Transmission Data	Bidirectional
TDOE	Transmission Data Output Enable (active low)	Input
NPW	New Packet Word (reset if TD[15:13]=000)	Input
DCH	Data Chain Hold (i.e. wait cycle request)	Output
TRDY	Transmission Ready (for new packet)	Output

Fig. 15



Reset (to Idle):

000000

General Data Read:

001	word count*	address
-----	-------------	---------

General Data Write:

0	1	0	word count*	address
---	---	---	-------------	---------

Video Stream Write:

101	
-----	--

Audio Stream Write:

110	
-----	--

* 256 words if word count = 0

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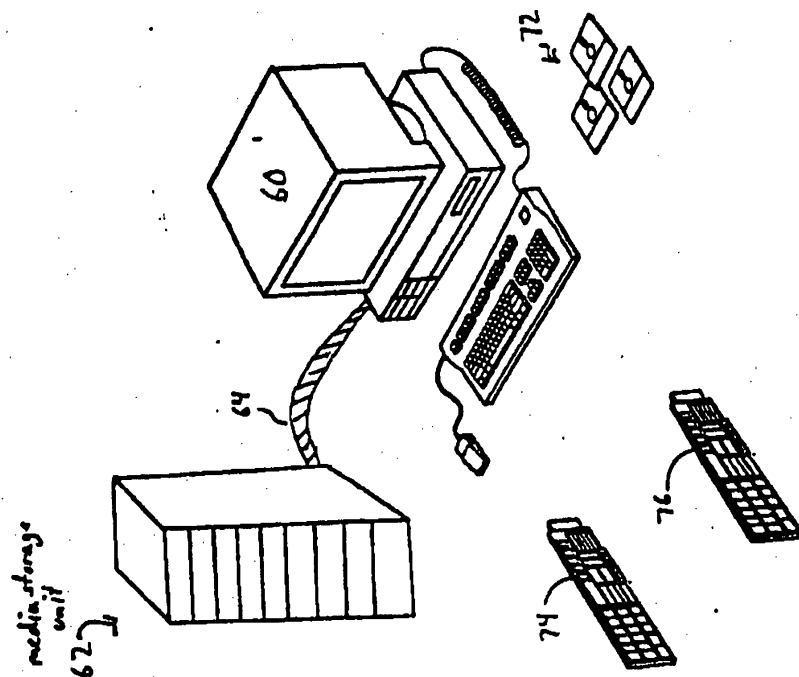


Figure 1

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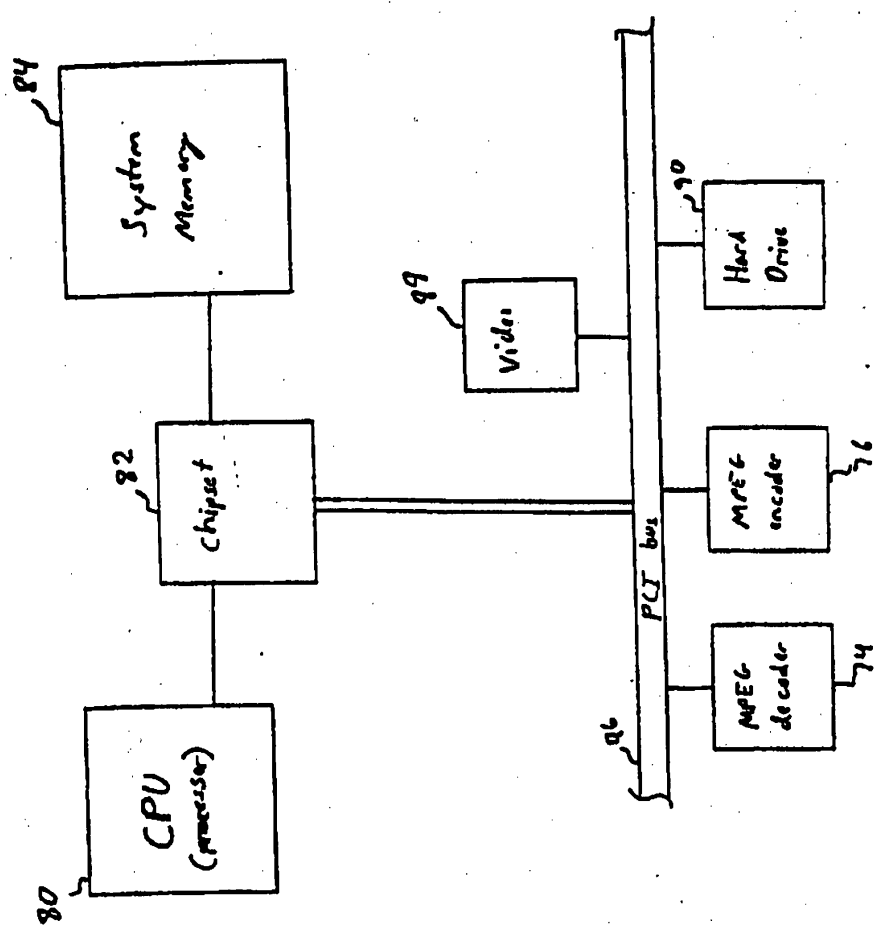


Figure 2

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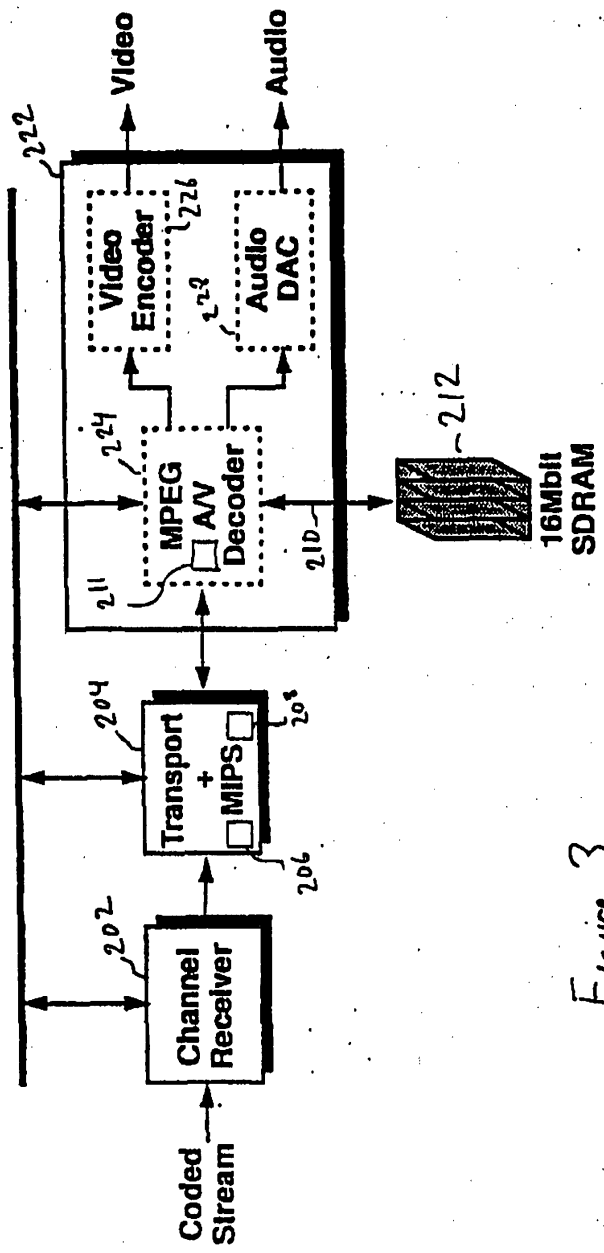


Figure 3

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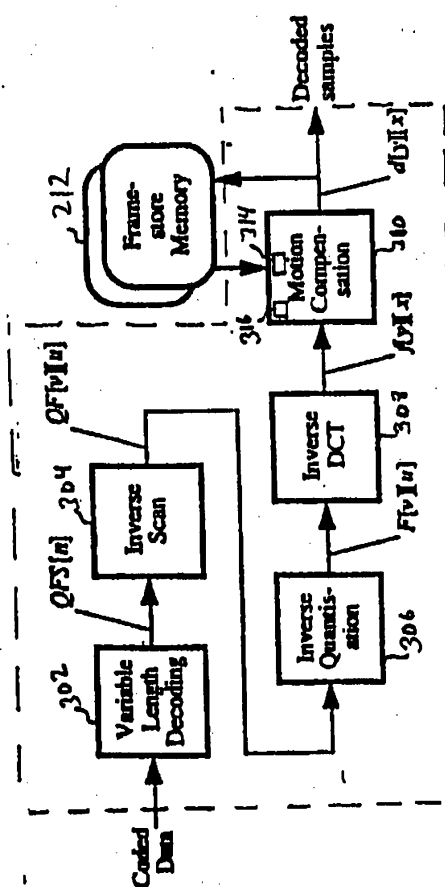
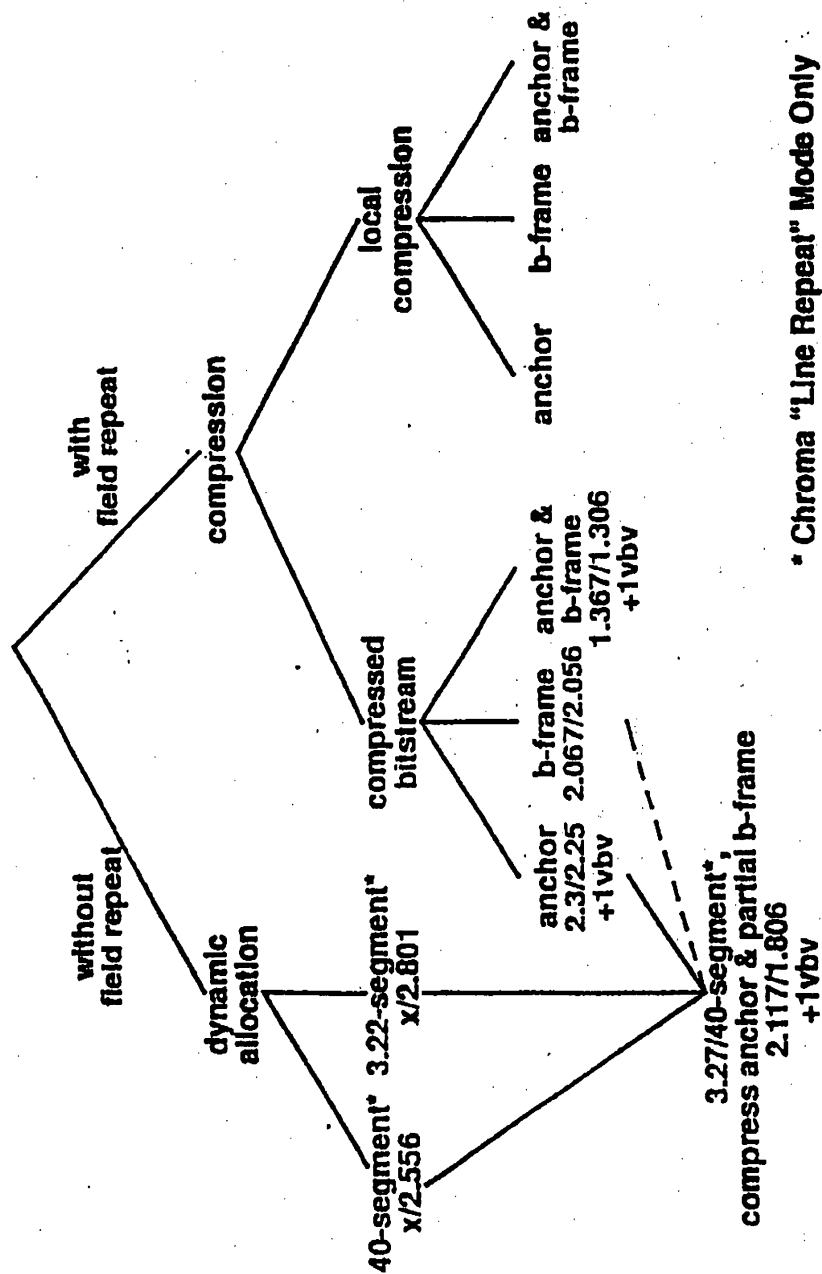


Figure 4

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FIG. 5



* Chroma "Line Repeat" Mode Only

FIG. 6A

Table 1 MPEG Decoder: Memory Partition

	L84005		Compress Displayed Audio	
	NTSC	PAL	NTSC	PAL
frame store (number of frames)	12,441,600 (3,000)	12,718,080 (2,556)	9,538,560 (2,300)	11,197,440 (2,250)
vbv buffer	1,805,008	1,805,008	3,610,016	3,610,016
video non-instantaneous decode	430,765	520,575		
video-display sync	500,000	600,000		
audio buffer	28,672	28,672		
audio-video latency difference	19,200	23,040		
audio-display sync	12,800	15,360		
video transport buffer	4,096	4,096		
audio transport buffer	4,096	4,096		
4ms filter at 15Mbps	60,000	60,000		
sub-total for channel buffer	2,864,637	3,060,847	4,669,645	4,865,855
packet header overhead	20,000	20,000		
OSD	675,840	808,192		
sub-total for software & data	775,139	170,097	1,873,171	(114,271)
Grand Total	16,777,216	16,777,216		
frame store + channel buffer	15,306,237	15,778,927	14,208,205	16,063,295

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FIG. 6B

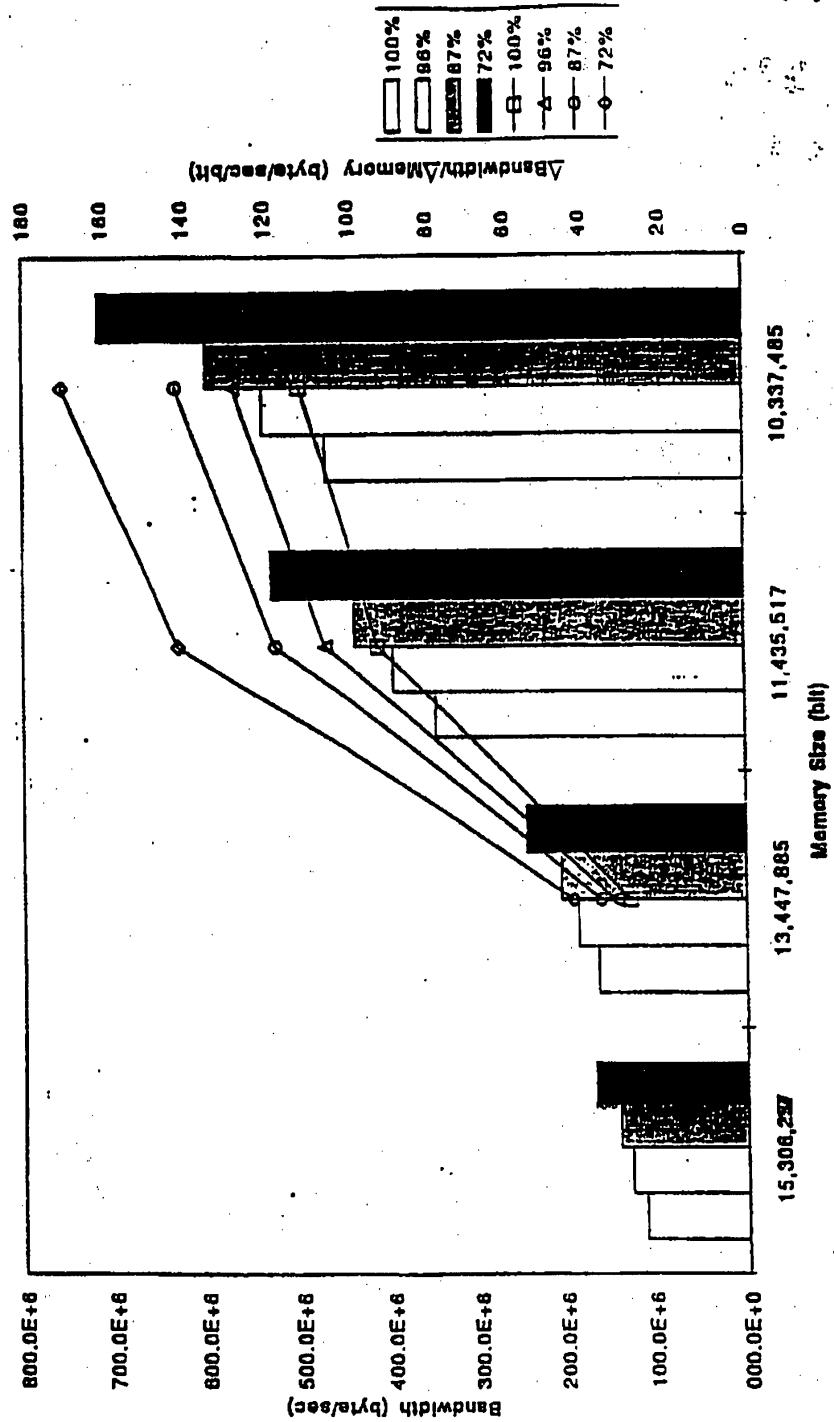
Table 1 MPEG Decoder: Memory Partition

Compress Anchor & Segment B		Compress B-Frame		Compress Anchor & B-Frame	
NTSC: 3.267 segments	PAL: 40 segments	NTSC	PAL	NTSC	PAL
8,778,240	8,985,600	8,570,880	10,229,760	5,667,840	6,497,280
(2.117)	(1.806)	(2.067)	(2.056)	(1.367)	(1.306)
3,610,016	3,610,016			3,610,016	3,610,016
4,669,645	4,865,855			4,869,645	4,865,855
2,633,491	2,097,569	4,645,859	2,659,417	5,743,891	4,585,889
13,447,885	13,861,455	11,435,517	13,290,607	10,337,485	11,383,135

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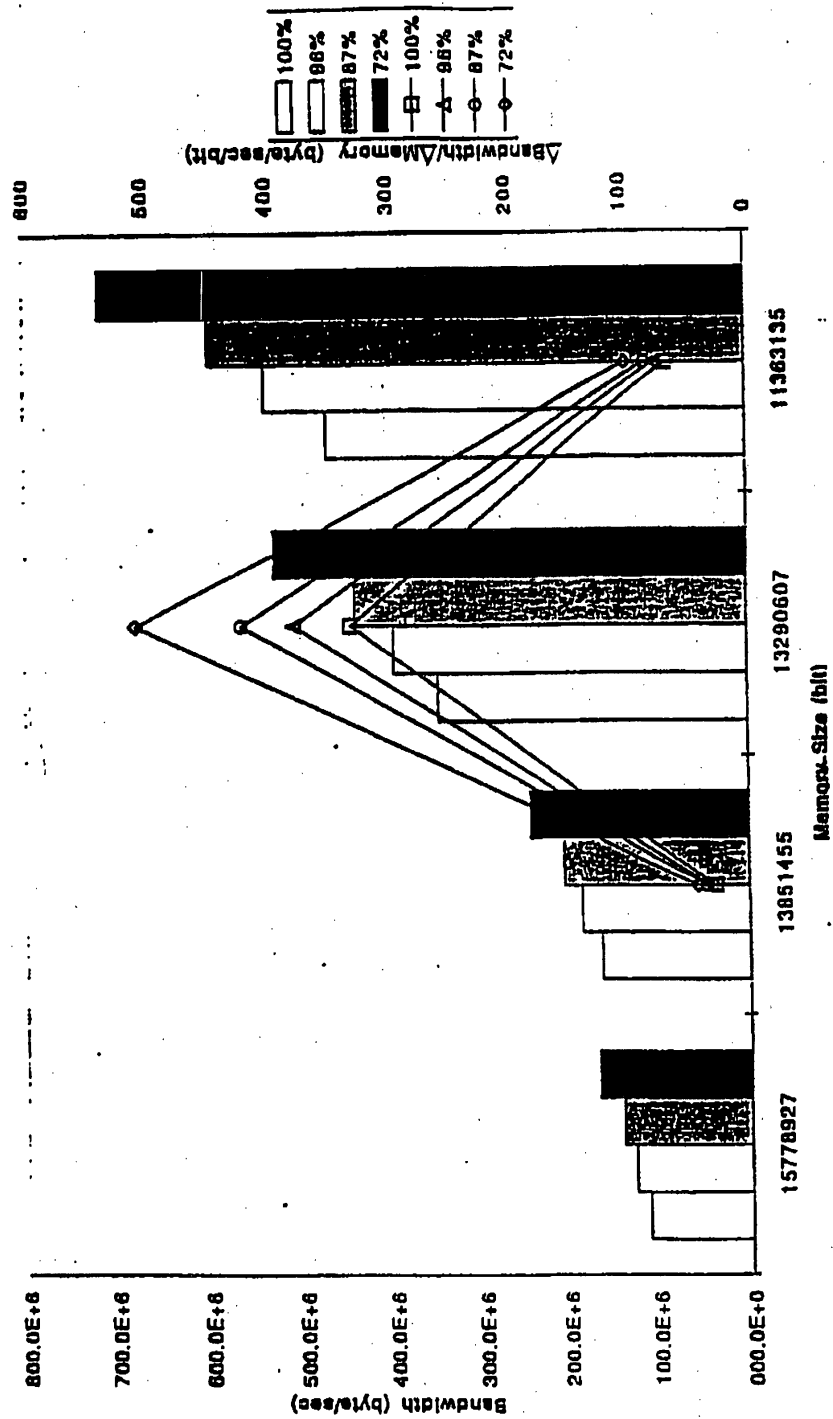
Fig. 7 Memory Bandwidth vs Memory Size (Frame & Channel)
NTSC



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Fig. 8 Memory Bandwidth vs Memory Size (Frame & Channel)
PAL



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FIG. 9

	bit	
	NTSC	PAL
Video Frames (incl. compressed)	10,583,248	10,790,608
VBV Buffer	1,805,008	1,805,008
Video Decode Buffer	430,765	520,575
Video-Display Sync Buffer	500,000	600,000
Audio Buffer	28,672	28,672
Audio-Video Latency Buffer	19,200	23,040
Audio-Display Sync Buffer	12,800	15,360
Transport Buffer	8,192	8,192
Jitter Buffer (4ms)	60,000	60,000
PES Header Overhead	20,000	20,000
OSD	675,840	808,192
MIPS Code and Data	2,633,491	2,097,569

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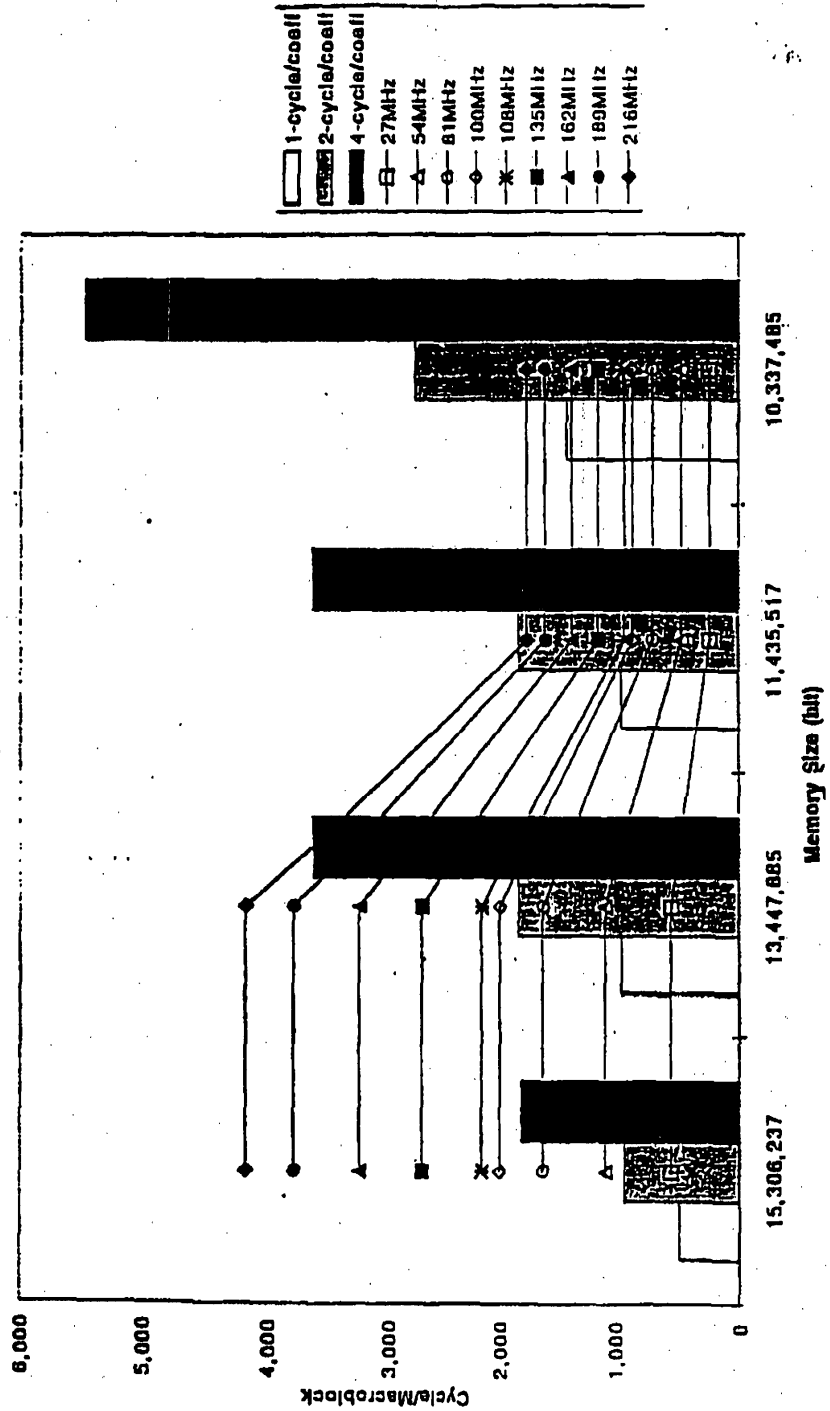
FIG. 10

	Bandwidth (Mbyte/sec)	
	NTSC	PAL
Channel In/Out	18.82	15.98
Motion Compensation	72.70	72.59
Store	38.29	38.23
Display & OSD	30.38	30.38
TOTAL	160.19	157.18

- With 16x1M SDRAM running at 100MHz, Bandwidth Available is 200Mbyte/sec
- Expecting 20Mbyte/sec for MIPS Code and Data

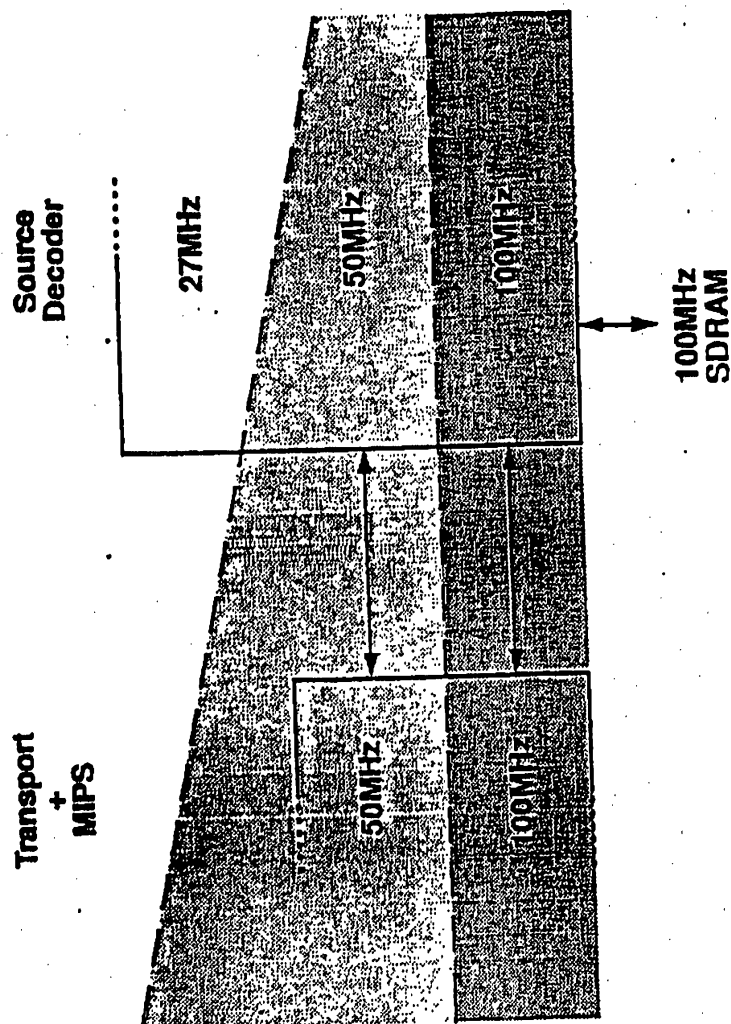
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Fig. 11 Processing Power vs Memory (Frame & Channel) Size
NTSC



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FIG. 12



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FIG. 13

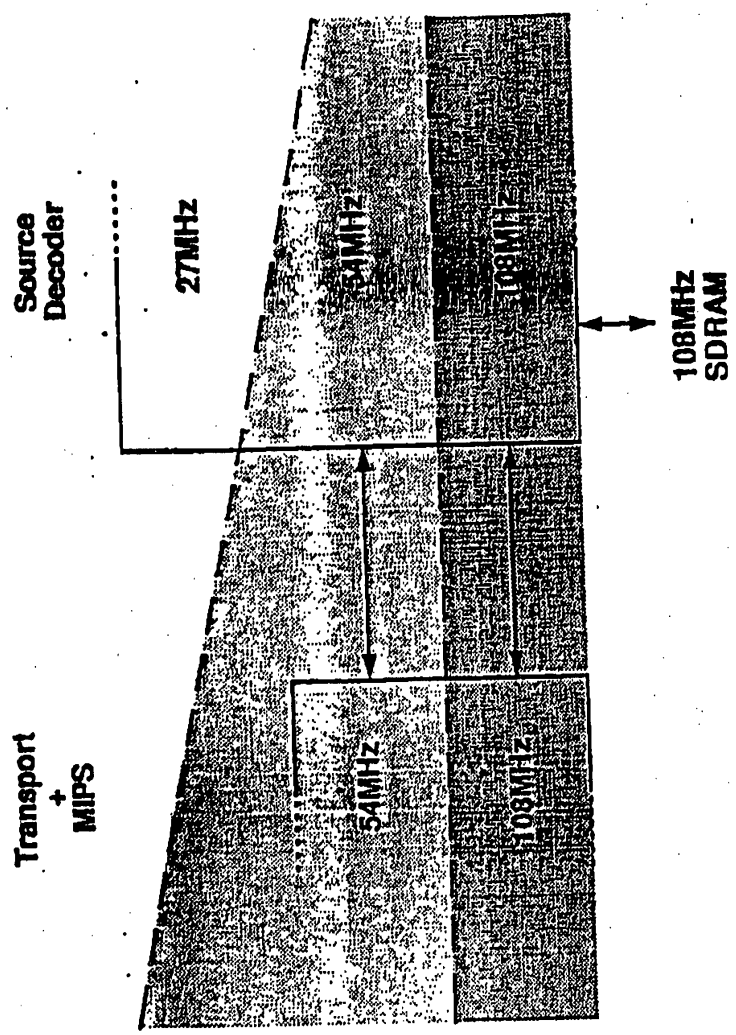
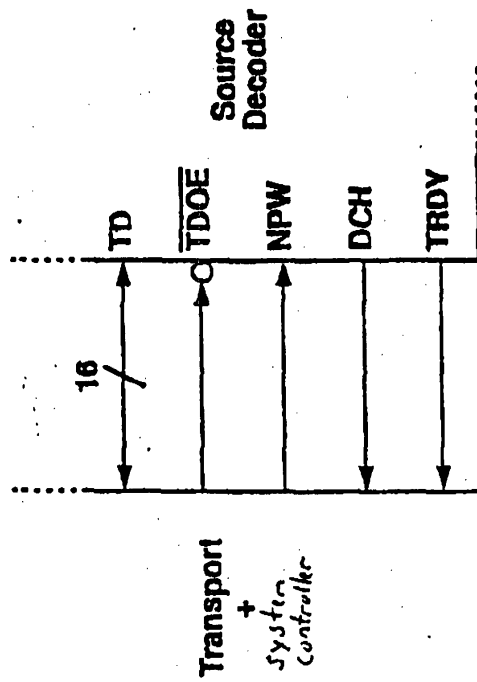


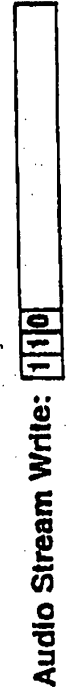
FIG. 14



Signal	Description	Type
TD[15:0]	Transmission Data	Bidirectional
$\overline{\text{TDOE}}$	Transmission Data Output Enable (active low)	Input
NPW	New Packet Word (reset if TD[15:13]=000)	Input
DCH	Data Chain Hold (i.e. wait cycle request)	Output
TRDY	Transmission Ready (for new packet)	Output

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* 256 words if word count = 0

PATENT
5201-01600
P-2892

DECLARATION AND POWER OF ATTORNEY

As a below named inventor, I hereby declare that:

My residence, post office and citizenship are as stated below next to my name.

I believe I am the original, first and sole inventor (if only one name is listed below) or the below named inventors believe they are the original, first and joint inventors (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled "MPEG Decoder System and Method Having a Unified Memory for Transport, Decode and System Controller Functions," the specification of which:

 X is attached hereto.
_____ was filed on _____ as Application Serial No. _____
and was amended on _____ (if applicable)

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose to the Patent and Trademark Office all information known to me to be material to patentability of the subject matter claimed in this application, as "materiality" is defined in Title 37, Code of Federal Regulations, §1.56.

I hereby claim foreign priority benefits under Title 35, United States Code, §119 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

PRIOR FOREIGN APPLICATION(S)			Priority Claimed
N/A			Yes/No
(Number)	(Country)	(Date Filed)	
N/A			Yes/No
(Number)	(Country)	(Date Filed)	

I hereby claim the benefit under Title 35, United States Code, §120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, §112, I acknowledge the duty to disclose all information known to me to be material to the patentability of the subject matter claimed in this application, as "materiality" is defined in Title 37, Code of Federal Regulations, §1.56, which become available between the filing date of the prior application and the national or PCT international filing date of this application:

N/A		
(Application Serial No.)	(Filing Date)	(Status)

I hereby declare that all statements made of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

8

The Assignee hereby revokes any previous Powers of Attorney and appoints Kevin P. McAndrews, Reg. No. 34,496, David G. Pursel, Reg. No. 28,659 and Franklyn C. Weiss, Reg. No. 41 each said attorneys being employed by LSI Logic Corporation; and Kevin L. Daffer, Reg. No. 34,146, B. Noel Kivlin, Reg. No. 33,929, Jeff C. Hood, Reg. No. 35,198, Eric B. Meyertons, Reg. No. 34,876 and David A. Rose, Reg. No. 26,223, each said attorneys being members or associates of the firm of Conley, Rose & Tayon, P.C., as attorney or agent for so long as they remain with such company or firm, with full power of substitution and revocation, to prosecute the application, to make alterations and amendments therein, to transact all business in the Patent and Trademark Office in connection therewith, and to receive the Letters Patent.

Please direct all communications as follows:

Jeffrey C. Hood
Conley, Rose & Tayon/P.C.
P.O. Box 3267
Houston, Texas 77253-3267
Ph: (312) 703-1246

1-00

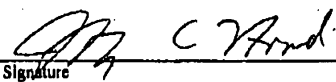
Inventor's Full Name: Kwok Kit Chau
(First) (Initial) (Last)

Inventor's Signature: [Signature] Date: 11/11/96

Country of Residence: USA Citizenship: USA

Post Office and Residence Address: 1721 Hawkins Drive, Los Altos, CA 94024 CA
(Include number, street name, city, state and zip code)

(1)

FORM DTO-1595 1-30-92 01-22-1997		U.S. DEPARTMENT OF COMMERCE Patent and Trademark Office	
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1. Name of conveying party(ies): Kwok Kit Chau Additional name(s) of conveying party(ies) attached? <input type="checkbox"/> Yes <input type="checkbox"/> No		2. Name and address of receiving party(ies): 08/748269 Name: LSI Logic Corporation Internal Address: _____ Street Address: 1551 McCarthy Boulevard City Milpitas State CA 95035 Additional name(s) & address(es) attached? <input type="checkbox"/> Yes <input type="checkbox"/> No	
3. Nature of Conveyance: <input checked="" type="checkbox"/> Assignment <input type="checkbox"/> Merger <input type="checkbox"/> Security Agreement <input type="checkbox"/> Change of Name <input type="checkbox"/> Other _____ Execution Date: November 11, 1996		4. Application number(s) or patent number(s): If this document is being filed together with a new application, the execution date of this application is: November 13, 1996 A. Patent Application No.(s) B. Patent No.(s) Additional numbers attached? <input type="checkbox"/> Yes <input checked="" type="checkbox"/> No	
5. Name and address of party to whom correspondence concerning document should be mailed: Name: Jeffrey C. Hood Internal Address: Conley, Ross & Tayon, P.C. Street Address: P.O. Box 3267 City Houston State TX ZIP 77253-3267		6. Total number of applications and patents involved: 1 7. Total fee (37 CFR 3.41): \$ 40.00 <input checked="" type="checkbox"/> Enclosed <input type="checkbox"/> Authorized to be charged to deposit account 8. Deposit account number: (Attach a duplicate copy of this page if paying by deposit account)	
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9. Statement and Signature. To the best of my knowledge and belief, the foregoing information is true and correct and any attached copy is a true copy of the original document.			
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		11/13/96 Date	
Total number of pages comprising cover sheet: 2			
OMB No. 0651-011 (exp. 4/94)			

P-2892

08, 748269
PATENT
5201-01600

ASSIGNMENT

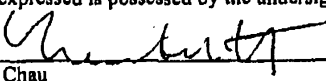
For Good And Valuable Consideration, the receipt and sufficiency of which is hereby acknowledged, we the undersigned, Kwok Kit Chau do hereby sell, assign and transfer to LSI LOGIC CORPORATION, a corporation of Delaware, having a place of business at 1551 McCarthy Boulevard, Milpitas, California 95035, ("Assignee"), its successors, assigns, and legal representatives, the entire right, title and interest for the United States and all foreign countries, in and to any and all inventions and improvements which are disclosed in the application for United States Letters Patent,

- (X) which has been executed by the undersigned concurrently herewith,
() which was filed on _____, 19__ and assigned Serial No. _____

and is entitled "MPEG Decoder System and Method Having a Unified Memory for Transport, Decode and System Controller Functions," and in and to said application and all divisional, continuing, substitute, renewal, reissue and all other applications for Letters Patent which have been or shall be filed in the United States and all foreign countries on any of said improvements; and in and to all original and reissued patents which have been or shall be issued in the United States and all foreign countries on said improvements; and in and to all rights of priority resulting from the filing of said United States application; and

Agree that said Assignee may apply for and receive Letters Patent for said improvements in its own name; and that, when requested, without charge to, but at the expense of, said Assignee, its successors, assigns and legal representatives, to carry out in good faith the intent and purpose of this Assignment, the undersigned will execute all divisional, continuing, substitute, renewal, reissue, and all other patent applications on any and all said improvements; execute all rightful oaths, assignments, powers of attorney and other papers; communicate to said Assignee, its successors, assigns, and representatives, all facts known to the undersigned relating to said improvements and the history thereof; and generally do everything possible which said Assignee, its successors, assigns or representatives shall consider desirable for aiding in securing and maintaining proper patent protection for said improvements and for vesting title to said improvements and all applications to patents and all patents on said improvements, in said Assignee, its successors, assigns and legal representatives; and

Covenant with said Assignee, its successors, assigns and legal representatives that no assignment, grant mortgage, license, or other agreement affecting the rights and property herein conveyed has been made to others by the undersigned, and that full right to convey the same as herein expressed is possessed by the undersigned.

Name:  Date: 11/11/96
Kwok Kit Chau

Witness Signature: _____ Date: _____

Printed Name (Witness): _____



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:
Kwok K. Chau

Serial No. 08/748,269

Filed: November 13, 1996

For: MPEG Decoder System and
Method Having a Unified Memory
For Transport Decode and System
Controller Functions

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§

Att'y. Dkt. No.: 5201-01600

I hereby certify that this correspondence is being deposited
with the U.S. Postal Service at First Class Mail in an
envelope addressed to: Assistant Commissioner for Patents,
Washington, D.C. 20231, on the date below:
9/15/97 Date Signature

INFORMATION DISCLOSURE STATEMENT

Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

Applicant requests consideration of ☐ the references listed on the attached Form PTO-1449 and/or ☒ the additional information identified below in paragraph 3. A copy of each reference listed on the Form PTO-1449 is enclosed.

1. This Information Disclosure Statement is submitted:

- a. ☒ within 3 months of the filing date of the above identified application, or within 3 months of entry into National stage prosecution of an International application, or before the mailing date of the first Office Action on the merits, and thus no certification and/or fee is required.
- b. ☐ after the events of above paragraph 1a and prior to the mailing date of a final Office Action or Notice of Allowance, and thus:
- ☐ the certification of paragraph 2 below is provided, or

- ☐ a fee of \$230.00 is enclosed.
- c. ☐ after the mailing date of a final Office Action or a Notice of Allowance and prior to payment of the issue fee, and thus:
- ☐ the certification of paragraph 2 below is provided, and
- ☐ a Petition and fee of \$130.00 are enclosed.
2. It is hereby certified:
- ☐ that each item of information contained in this Information Disclosure Statement was cited in a communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the Statement, or
- ☐ that no item of information contained in the Information Disclosure Statement was cited in a communication from a foreign patent office in a counterpart foreign application or, to the knowledge of the person signing the certification after making reasonable inquiry, was known to any individual designated in § 1.56 (c) more than three months prior to the filing of the Statement.
3. ☒ Consideration of the following additional information (including any co-pending or abandoned U.S. applications, prior uses and/or sales, etc.) is requested:
- U.S. Patent Application Serial No. 08/772,442 (5201-01700)
- U.S. Patent Application Serial No. 08/667,100 (5201-02700)
4. For each non-English language reference listed on the attached Form PTO-1449:
- ☐ reference is made to an English language translation submitted herewith, and/or
- ☐ reference is made to a foreign patent office search report (in the English language) submitted herewith, and/or
- ☐ reference is made to an English language translation of a foreign patent office search report submitted herewith, and/or
- ☐ reference is made to the concise explanation contained in the specification of the present application at page(s) _____, and/or
- ☐ reference is made to the concise explanation set forth below:
5. ☐ Applicant also offers the following comments for the Examiner's consideration:
6. ☐ Also enclosed is a copy of a foreign search report citing these references.

7. ☐ The listed documents were brought to the attention of the Applicant(s) after payment of the issue fee in the captioned case. The documents were cited in a communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this Information Disclosure Statement. Applicant(s) request this Information Disclosure Statement and attached Form PTO-1449 be placed in the file of the captioned application.
8. ☐ Applicant(s) requests that the Information Disclosure Statement and attached Form PTO-1449 and references, which are being filed before the grant of the patent and pursuant to 37 C.F.R. § 1.98(i), be placed in the file of the captioned application.

If any required fees are missing, the Commissioner is authorized to charge said fees to Conley, Rose & Tayon, P.C. Deposit Account No. 03-2769/5201-01600/JCH. A duplicate copy of this sheet is enclosed.

Respectfully submitted,



Jeffrey C. Hood
Reg. No. 35,198
Attorney for Applicant(s)

CONLEY, ROSE & TAYON, P.C.
P. O. Box 3267
Houston, Texas 77253-3267
(512) 476-1400

Date: 9/15/97

K:\V\ai01600\ai016.ids.pto.jch.doc

File History Content Report

The following content is missing from the original file history record obtained from the United States Patent and Trademark Office. No additional information is available.

Document Title: List of References cited by applicant and considered by examiner

Document Date: 1997-09-18

Page(s): All

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UNITED STATES DEPARTMENT OF COMMERCE
Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231

SERIAL NUMBER	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
0874181257	11/13/98	CHAU	5701-01649
JERREY C. HOOD COBLEY ROSE & TAYON P.O. BOX 1167 HOUSTON, TX 77253-3267			1941/0511
EXAMINER			
ART UNIT			PAPER NUMBER
2772			3
DATE MAILED:			05/11/98

This is a communication from the examiner in charge of your application.
COMMISSIONER OF PATENTS AND TRADEMARKS

☒ This application has been examined ☐ Responsive to communication filed on _____ ☐ This action is made final.

A shortened statutory period for response to this action is set to expire 3 month(s), _____ days from the date of this letter.
Failure to respond within the period for response will cause the application to become abandoned. 35 U.S.C. 133

Part I THE FOLLOWING ATTACHMENT(S) ARE PART OF THIS ACTION:

- | | |
|---|--|
| 1. <input type="checkbox"/> Notice of References Cited by Examiner, PTO-892. | 2. <input checked="" type="checkbox"/> Notice of Draftsman's Patent Drawing Review, PTO-848. |
| 3. <input type="checkbox"/> Notice of Art Cited by Applicant, PTO-1448. | 4. <input type="checkbox"/> Notice of Informal Patent Application, PTO-152. |
| 5. <input type="checkbox"/> Information on How to Effect Drawing Changes, PTO-1474. | 6. <input type="checkbox"/> _____ |

Part II SUMMARY OF ACTION

1. ☒ Claims 1-20 are pending in the application.
Of the above, claims none are withdrawn from consideration.
2. ☐ Claims _____ have been cancelled.
3. ☒ Claims 1-11 & 13-20 are allowed.
4. ☒ Claims 12 are rejected.
5. ☐ Claims _____ are objected to.
6. ☐ Claims _____ are subject to restriction or election requirement.
7. ☒ This application has been filed with informal drawings under 37 C.F.R. 1.85 which are acceptable for examination purposes.
8. ☐ Formal drawings are required in response to this Office action.
9. ☐ The corrected or substitute drawings have been received on _____. Under 37 C.F.R. 1.84 these drawings are ☐ acceptable; ☐ not acceptable (see explanation or Notice of Draftsman's Patent Drawing Review, PTO-848).
10. ☐ The proposed additional or substitute sheet(s) of drawings, filed on _____, has (have) been ☐ approved by the examiner; ☐ disapproved by the examiner (see explanation).
11. ☐ The proposed drawing correction, filed _____, has been ☐ approved; ☐ disapproved (see explanation).
12. ☐ Acknowledgement is made of the claim for priority under 35 U.S.C. 119. The certified copy has ☐ been received ☐ not been received ☐ been filed in parent application, serial no. _____; filed on _____.
13. ☐ Since this application appears to be in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under Ex parte Quayle, 1935 C.D. 11; 453 O.G. 213.
14. ☐ Other

EXAMINER'S ACTION

PTOL-326 (Rev. 2/93)

Serial Number: 08/748,269

-2-

Art Unit: 2772

Part III DETAILED ACTION

Drawings

1. This application has been filed with informal drawings which are acceptable for examination purposes only. Formal drawings will be required when the application is allowed.

Specification

2. The disclosure is objected to because of the following informalities:

The Applicant is respectfully requested to provide the U.S. Patent Application Serial Numbers and their updated status as listed at page 1 of the present application.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

3. Claims 12 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

As per claim 12, the terms "said accessing multimedia data stream data" (lines 3-4), "said accessing video frame data" (lines 6-7) lack clear antecedent basis.

Serial Number: 08/748,269

-3-

Art Unit: 2772

Conclusion

4. Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D.C. 20231

or faxed to:

(703) 308-9051, (for formal communications intended for entry)

Or:

(703) 305-9724 (for informal or draft communications, please label "PROPOSED"

or "DRAFT")

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington.

VA., Sixth Floor (Receptionist).

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Cliff N. Vo whose telephone number is (703) 305-9594. He can normally be reached Monday-Friday and alternate Monday from 8:00am-5:30pm.

If attempts to reach the examiner are unsuccessful, the examiner's supervisor, Heather Herndon, can be reached at (703) 305-9701. The fax phone number for this Group is (703) 305-9724.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (703) 305-3800.

Cliff N. Vo

Cliff N. Vo
May 4, 1998

Attachment 3

BEST COPY

The drawings submitted with this application were declared informal by the applicant. Accordingly they have not been reviewed by a draftsperson at this time. When formal drawings are submitted, the draftsperson will perform a review.

Direct any inquiries concerning drawing review to the Drawing Review Branch (703) 305-8404.




G.P. 2772
#4/A
6-16-98
MJC

Application. No:	08/748,269
Filed:	November 13, 1996
Inventor(s):	Kwok Kit Chau
Title:	MPEG Decoder System and Method Having a Unified Memory for Transport, Decode and System Controller Functions
Examiner:	Cliff N. Vo
Group/Art Unit:	2772 /

Atty. Dkt. No: 5201-01600

I hereby certify that this correspondence is being deposited with the United States Postal Service as First Class Mail in an envelope addressed to Assistant Commissioner for Patents, Washington, DC 20231, on the date indicated below.

6/3/88 Date  Signature

AMENDMENT

**Assistant Commissioner for Patents
Washington, D.C. 20231**

Dear Sir:

In response to the Office Action mailed May 11, 1998, please amend the application as follows:

IN THE SPECIFICATION:

At page 1 line 13, please delete "27" and insert --28-- therefor.

At page 1 line 17, please delete "27" and insert --28-- therefor.

At page 1 line 19, please delete the blank line and insert --08/689,300-- therefor.

At page 1 line 19, please delete "System and Method" and insert --Method and Apparatus-- therefor.

At page 1 line 20, please delete "7" and insert --8-- therefor.

RECEIVED
98 JUN 11 AM 7:23
GROUP 2700

IN THE CLAIMS:

Please amend the claims as follows:

1. (Amended) An MPEG decoder system which includes a single memory for use by transport, decode and system controller functions, comprising:

a channel receiver for receiving an MPEG encoded stream;

transport logic coupled to the channel receiver which demultiplexes one or more multimedia data streams from the encoded stream;

a system controller coupled to the transport logic which controls operations within the MPEG decoder system;

A¹ an MPEG decoder coupled to receive one or more multimedia data streams output from the transport logic, wherein the MPEG decoder [logic] operates to perform MPEG decoding on the multimedia data streams; and

a memory coupled to the MPEG decoder, wherein the memory is used by the MPEG decoder during MPEG decoding operations, wherein the memory stores code and data useable by the system controller which enables the system controller to perform control functions within the MPEG decoder system, wherein the [external] memory is used by the transport logic for demultiplexing operations;

wherein the MPEG decoder is operable to access the memory during MPEG decoding operations;

wherein the transport logic is operable to access the memory to store and retrieve data during demultiplexing operations; and

wherein the system controller is operable to access the memory to retrieve code and data during system control functions.

2
A 10. (Amended) A method for performing video decoding in an MPEG decoder system which includes a single memory for use by transport, decode and system controller functions, the method comprising:

receiving an MPEG encoded stream;

demultiplexing one or more multimedia data streams from the encoded stream, wherein said demultiplexing one or more multimedia data streams from the encoded stream operates using a first unified memory;

2 performing MPEG decoding on the multimedia data streams, wherein said performing MPEG decoding operates using said first unified memory; and

A a system controller controlling operations within the MPEG decoder system, wherein said controlling operations accesses code and data from said first unified memory;

wherein said demultiplexing one or more multimedia data streams, said performing MPEG decoding, and said controlling operations each use said first unified memory.

12. (Amended) The method of claim [10] 11, wherein the MPEG decoder system includes a memory controller coupled to the first unified memory;

3 wherein said accessing multimedia data stream data from said first unified memory comprises accessing said multimedia data stream data through the memory controller;

A wherein said accessing video frame data from said first unified memory comprises accessing said video frame data through the memory controller; and

wherein said accessing code and data from said first unified memory comprises accessing said code and data through the memory controller.

16. (Amended) A video decoder system which includes a single memory for use by transport, decode and system controller functions, comprising:

4 a channel receiver for receiving an encoded video stream;

A transport logic coupled to the channel receiver which demultiplexes one or more multimedia data streams from the encoded stream;

a system controller coupled to the transport logic which controls operations within the video decoder system;

a video decoder coupled to receive one or more multimedia data streams output from the transport logic, wherein the video decoder [logic] operates to perform video decoding on the multimedia data streams; and

4
A a memory coupled to the video decoder, wherein the memory is used by the video decoder during video decoding operations, wherein the memory stores code and data useable by the system controller which enables the system controller to perform control functions within the video decoder system, wherein the [external] memory is used by the transport logic for demultiplexing operations;

wherein the video decoder is operable to access the memory during video decoding operations;

wherein the transport logic is operable to access the memory to store and retrieve data during demultiplexing operations; and

wherein the system controller is operable to access the memory to retrieve code and data during system control functions.

REMARKS

Applicant is in receipt of the Office Action mailed 5/11/98. Claims 1 - 11 and 13 - 20 were allowed. Claim 12 was rejected for an antecedent basis problem.

Applicant has amended the specification to update the status of the patent applications incorporated by reference. Also, Applicant has amended claim 12 to correct the antecedent basis problem. Applicant has also amended certain of the claims to correct typographical errors.

In view of the above amendments, Applicant submits that all claims are allowable.

If any fees are inadvertently omitted or overpaid, the Commissioner is authorized to charge or refund said fees to Conley, Rose, & Tayon, P.C. Deposit Account No. 03-2769/5201-01600/JCH.

Respectfully submitted,



Jeffrey C. Hood
Reg. No. 35,198
ATTORNEY FOR APPLICANT(S)

Conley, Rose & Tayon, P.C.
P.O. Box 398
Austin, TX 78767-0398
Phone: (512) 476-1400

Date 6/3/98

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Transaction Date: 1998-09-02
Date of Invention: JSPTO Patent
Application: (PAIR) system
records: www.uspto.gov



UNITED STATES DEPARTMENT OF COMMERCE
Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231

SERIAL NUMBER	FILING DATE	FIRST NAMED APPLICANT	ATTORNEY DOCKET NO.
---------------	-------------	-----------------------	---------------------

JOSEPH A. TAYLOR
JOSEPH ROBERT A. TAYLOR
1000 1000
WASHINGTON, D.C. 20000-4207

LN111/8902

EXAMINER

ART UNIT PAPER NUMBER

5

DATE MAILED:

NOTICE OF ALLOWABILITY

PART I

- ☒ This communication is responsive to 6/8/98
- ☒ All the claims being allowable. PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice Of Allowance And Issue Fee Due or other appropriate communication will be sent in due course.
- ☒ The allowed claims are 1-20
- ☐ The drawings filed on _____ are acceptable.
- ☐ Acknowledgment is made of the claim for priority under 35 U.S.C. 119. The certified copy has ☐ been received. ☐ not been received. ☐ been filed in parent application Serial No. _____, filed on _____
- ☐ Note the attached Examiner's Amendment.
- ☐ Note the attached Examiner Interview Summary Record, PTOL-413.
- ☐ Note the attached Examiner's Statement of Reasons for Allowance.
- ☒ Note the attached NOTICE OF REFERENCES CITED, PTO-892.
- ☐ Note the attached INFORMATION DISCLOSURE CITATION, PTO-1449.

PART II

A SHORTENED STATUTORY PERIOD FOR RESPONSE to comply with the requirements noted below is set to EXPIRE THREE MONTHS FROM THE "DATE MAILED" indicated on this form. Failure to timely comply will result in the ABANDONMENT of this application. Extensions of time may be obtained under the provisions of 37 CFR 1.136(a).

- ☐ Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL APPLICATION, PTO-152, which discloses that the oath or declaration is deficient. A SUBSTITUTE OATH OR DECLARATION IS REQUIRED.
- ☒ APPLICANT MUST MAKE THE DRAWING CHANGES INDICATED BELOW IN THE MANNER SET FORTH ON THE REVERSE SIDE OF THIS PAPER.
 - ☒ Drawing Informalities are indicated on the NOTICE RE PATENT DRAWINGS, PTO-948, attached hereto to Paper No. 3. CORRECTION IS REQUIRED.
 - ☐ The proposed drawing correction filed on _____ has been approved by the examiner. CORRECTION IS REQUIRED.
 - ☐ Approved drawing corrections are described by the examiner in the attached EXAMINER'S AMENDMENT. CORRECTION IS REQUIRED.
 - ☒ Formal drawings are now REQUIRED.

Any response to this letter should include in the upper right hand corner, the following information from the NOTICE OF ALLOWANCE AND ISSUE FEE DUE: ISSUE BATCH NUMBER, DATE OF THE NOTICE OF ALLOWANCE, AND SERIAL NUMBER.

Attachments:

- Examiner's Amendment
- Examiner Interview Summary Record, PTOL-413
- Reasons for Allowance
- ☒ Notice of References Cited, PTO-892
- Information Disclosure Citation, PTO-1449

- Notice of Informal Application, PTO-152
- Notice re Patent Drawings, PTO-948
- Listing of Bonded Draftsman
- Other

Phu K. Nguyen

PHU K. NGUYEN
PRIMARY EXAMINER
GROUP 2400

Notice of References Cited				Application No. 08/746,269		Applicant(s) CHAU	
				Examiner CLIFF VO		Group Art Unit 2772	
U.S. PATENT DOCUMENTS							
*	DOCUMENT NO.	DATE	NAME			CLASS	SUBCLASS
*A	5,692,213	10/16/95	GOLDBERG et al.			345	302
*B	5,675,511	12/21/95	PRASAD et al.			345	302
*C	5,767,846	10/10/95	NAKAMURA et al.			345	302
D							
E							
F							
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I							
J							
K							
L							
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FOREIGN PATENT DOCUMENTS							
*	DOCUMENT NO.	DATE	COUNTRY	NAME		CLASS	SUBCLASS
N							
O							
P							
Q							
R							
S							
T							
NON-PATENT DOCUMENTS							
*	DOCUMENT (Including Author, Title, Source, and Pertinent Pages)					DATE	
U							
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W							
X							

* A copy of this reference is not being furnished with this Office action.
(See Manual of Patent Examining Procedure, Section 707.05(a).)



UNITED STATES DEPARTMENT OF COMMERCE
Patent and Trademark Office

NOTICE OF ALLOWANCE AND ISSUE FEE DUE

LN41/0902

JEFFREY C HOOD
CONLEY ROSE & TAYLOR
P O BOX 3267
HOUSTON TX 77253-3267

APPLICATION NO.	FILING DATE	TOTAL CLAIMS	EXAMINER AND GROUP ART UNIT	DATE MAILED
08/748,269	11/13/96	020	VO, C	2772 09/02/98
First Named Applicant	CHAU, KWOK K.			

TITLE OF INVENTION MPEG DECODER SYSTEM AND METHOD HAVING A UNIFIED MEMORY FOR TRANSPORT DECODE AND SYSTEM CONTROLLER FUNCTIONS

ATTY'S DOCKET NO.	CLASS-SUBCLASS	BATCH NO.	APPLN. TYPE	SMALL ENTITY	FEE DUE	DATE DUE
2 52/11-01600	045-002.000	163	UTILITY	NO	\$1320.00	12/02/98

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED.

THE ISSUE FEE MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED.

HOW TO RESPOND TO THIS NOTICE:

I. Review the SMALL ENTITY status shown above.

If the SMALL ENTITY is shown as YES, verify your current SMALL ENTITY status:

- A. If the status is changed, pay twice the amount of the FEE DUE shown above and notify the Patent and Trademark Office of the change in status, or
- B. If the status is the same, pay the FEE DUE shown above.

If the SMALL ENTITY is shown as NO:

- A. Pay FEE DUE shown above, or
- B. File verified statement of Small Entity Status before, or with, payment of 1/2 the FEE DUE shown above.

II. Part B-Issue Fee Transmittal should be completed and returned to the Patent and Trademark Office (PTO) with your ISSUE FEE. Even if the ISSUE FEE has already been paid by charge to deposit account, Part B Issue Fee Transmittal should be completed and returned. If you are charging the ISSUE FEE to your deposit account, section "4b" of Part B-Issue Fee Transmittal should be completed and an extra copy of the form should be submitted.

III. All communications regarding this application must give application number and batch number. Please direct all communications prior to issuance to Box ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

PATENT AND TRADEMARK OFFICE COPY

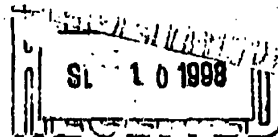
PTOL-85 (REV. 10-90) Approved for use through 06/30/99. (0851-0033)

U.S. GPO. 1998-437-638/0023

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PTO-B-ISSUE FEE TRANSMITTAL

Complete and mail this form, together with applicable fees, to: Assistant Commissioner for Patents, Washington, D.C. 20231



MAILING INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE. Blocks 1 through 4 should be completed where appropriate. All further correspondence including the Issue Fee Receipt, the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Legibly mark-up with any corrections or use Block 1)

ATTORNEY IN FEE
JEFFREY ROSE & TAYLOR
1000 AVENUE
SUITE 200
FARMINGTON, CT 06030-3817

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Publishing Division

OCT 26 1998

11

Note: The certificate of mailing below can only be used for domestic mailings of the Issue Fee Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing.

Certificate of Mailing

I hereby certify that this Issue Fee Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Box Issue Fee address above on the date indicated below.

MARIA KOVACS

(Depositor's name)

Maria Kovacs

(Signature)

OCT 21 1998

(Date)

APPLICATION NO.	FILING DATE	TOTAL CLAIMS	EXAMINER AND GROUP ART UNIT	DATE MAILED
01/01/98	11/1/98	200	VEL	11/1/98
First Named Applicant	KOVACS, MARIA			

TITLE OF INVENTION: DATA REDUCTION SYSTEM AND METHOD HAVING LIMITED MEMORY FOR TRANSPORT OF DATA AND SYSTEM CONTROL FUNCTIONS

ATTY'S DOCKET NO.	CLASS-SUBCLASS	BATCH NO.	APPLN. TYPE	SMALL ENTITY	FEE DUE	DATE DUE
P-2892	43-002.000	150	UTILITY	NO	\$30.00	12/31/98

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.383). Use of PTO form(s) and Customer Number are recommended, but not required.

☒ Change of correspondence address (or Change of Correspondence Address form PTO/8B/122) attached.

☐ "Fee Address" indication (or "Fee Address" indication form PTO/8B/47) attached.

2. For printing on the patent front page, list (1) the names of up to 3 registered patent attorneys or agents OR, alternatively, (2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 3 registered patent attorneys or agents. If no name is listed, no name will be printed.

1. Conley, Rose & Tayon

2. Jeffrey C. Hood

3.

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type) PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. Inclusion of assignee data is only appropriate when an assignment has been previously submitted to the PTO or is being submitted under separate cover. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE LSI Logic Corporation

(B) RESIDENCE: (CITY & STATE OR COUNTRY) Milpitas, CA

Please check the appropriate assignee category indicated below (will not be printed on the patent)

☐ Individual ☒ corporation or other private group entity ☐ government

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☒ Issue Fee

☒ Advance Order - # of Copies 10 (ten)

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(Authorized Signature)

Sandeep Jaggi

Reg. 43.331

(Date)

Oct. 21, '98

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Transaction

1998-10-26

Date of

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Application

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USPTO 001

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APPLICATION**

Application Number	08/748,289
Filing Date	November-13, 1998
First Named Inventor	Kwok Kit Chau
Group Art Unit	2772
Examiner Name	P. Vo
Attorney Docket Number	6201-01800 / P-2892

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☐ Practitioners at Customer NumberPlace Customer
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OR

☒ Practitioner(s) named below:

Name	Registration Number
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RALPH VESLI	33,807
WAYNE BAILEY	34,289
DAVID LUCENTE	36,202
BRUCE HOPENFELD	39,714
SANDEEP JAGGI	43,331

as my/our attorney(s) or agent(s) to prosecute the application identified above, and to transact all business in the Patent and Trademark Office connected therewith.

Please change the correspondence address for the above-identified application to:

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☒ Firm or
Individual Name

LSI LOGIC CORPORATION

Address 1551 McCarthy Blvd., MS: D-106

Address Patent Law Department

City MILPITAS State CA ZIP 95035

Country USA

Telephone 408-433-8708 Fax 408-433-7770

I am the:

☐ Applicant☒ Assignee of Record of the entire interest

Certificate under 37 CFR 3.73(b) is enclosed

SIGNATURE of Applicant or Assignee of Record

Name	DAVID G. PURSEL
Signature	
Date	10/14/98

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Transaction Date: 1998-10-26
Date into USPTO Patent
Application and records (PAIR) system
records www.uspto.gov

OKC 4100 #67
IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

Kwok Kit Chau

Serial No.: 08/748,269

Group Art Unit: 2772

Filed: November 13, 1996

Examiner: Vo, P.

For: MPEG Decoder System And
Method Having A Unified Memory
For Transport Decode And System
Controller Functions

Atty Docket: 5201-01600 / P-2892

I hereby certify that this correspondence is being deposited with the U.S. Postal
Service as First Class Mail in an envelope addressed to: Assistant Commissioner
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Maria Kovacs

October 21, 1998
Date

Maria Kovacs
Signature

SUBMISSION OF FORMAL DRAWINGS PURSUANT TO 37 C.F.R. §1.85

Official Draftsman

Assistant Commissioner of Patents
Washington, D.C. 20231

Sir:

Applicant hereby substitutes the enclosed formal drawings for those presently in the above referenced
application.

Respectfully submitted,

LSI Logic Corporation
1551 McCarthy Blvd., MS D-106
Milpitas, CA 95035
408/954-4923

Date: Oct. 21, 1998

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Publication Division
OCT 26 1998
Sandeep Jaggi

Reg. No. 43,331

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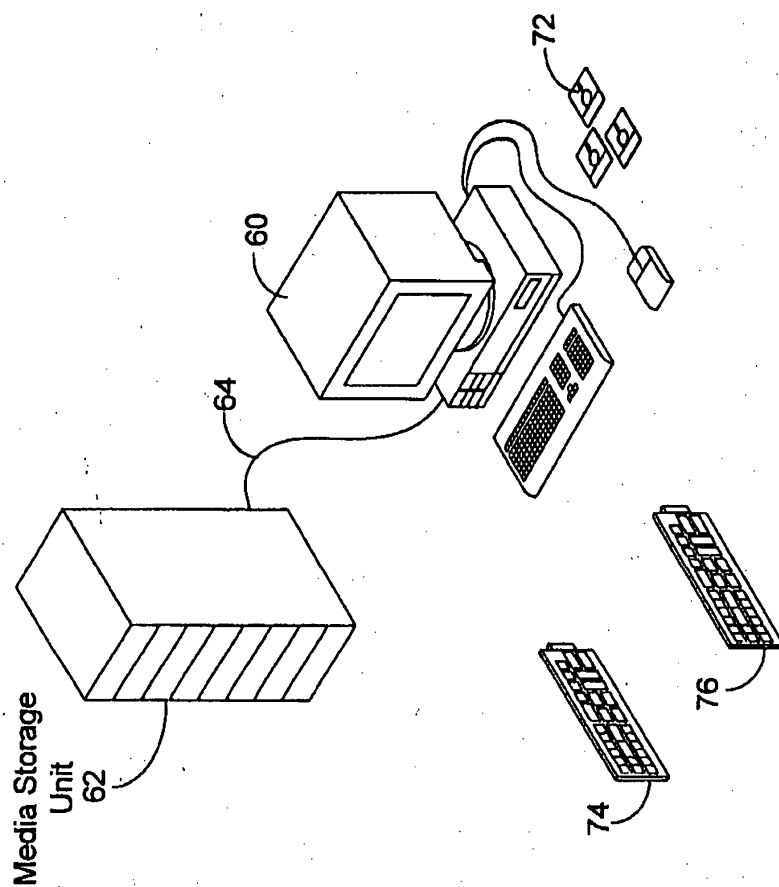


FIG. 1

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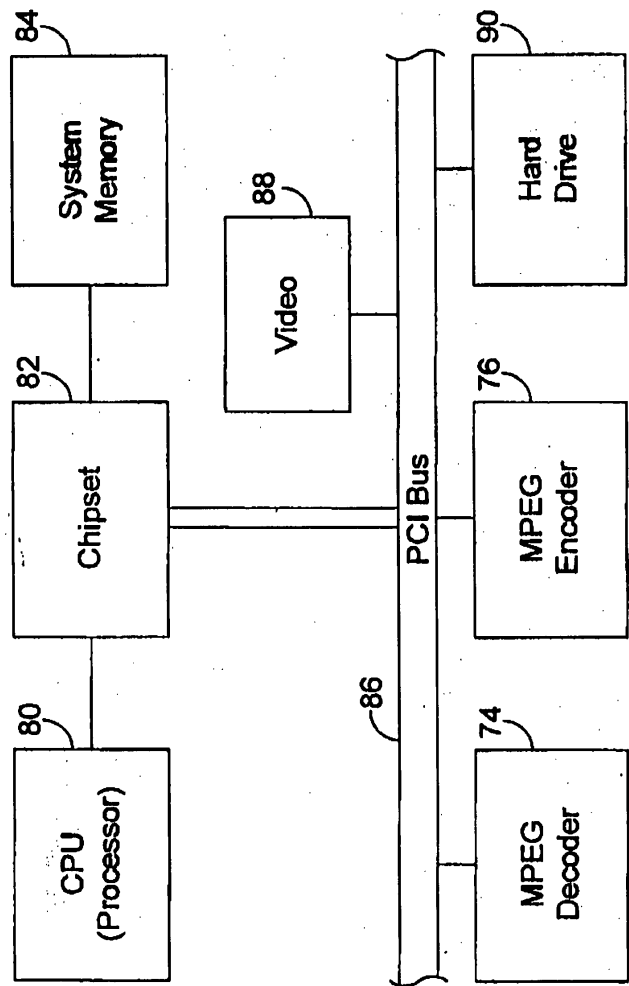


FIG. 2

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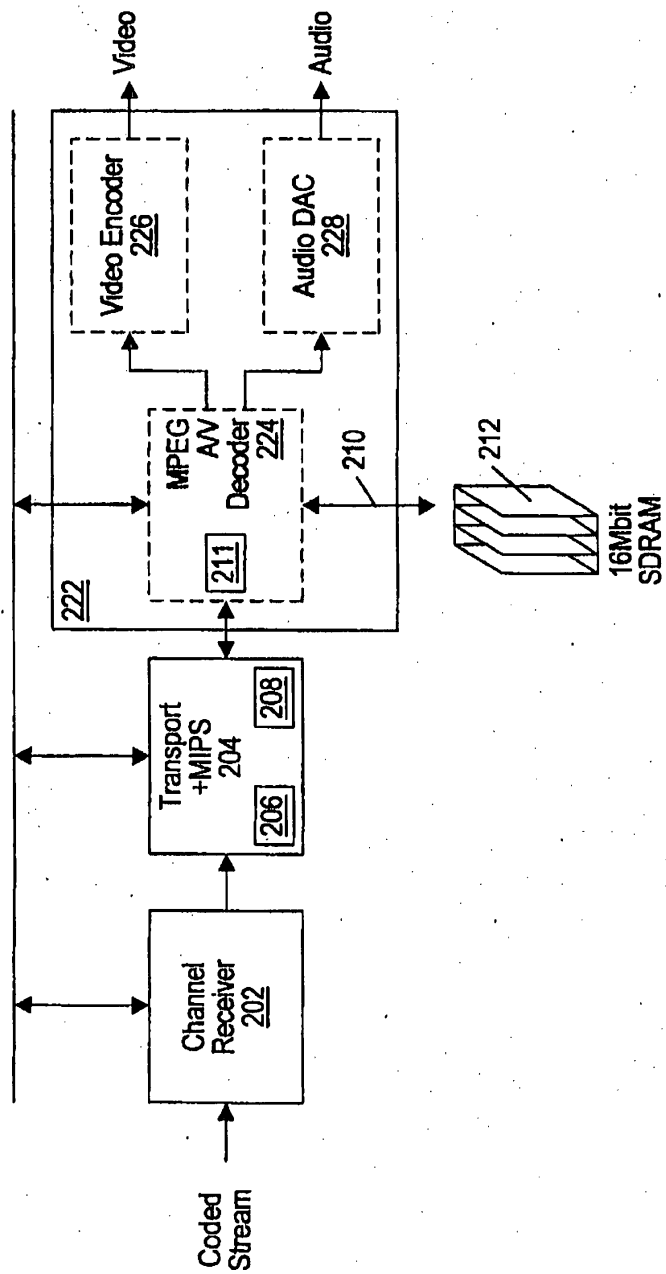


FIG. 3

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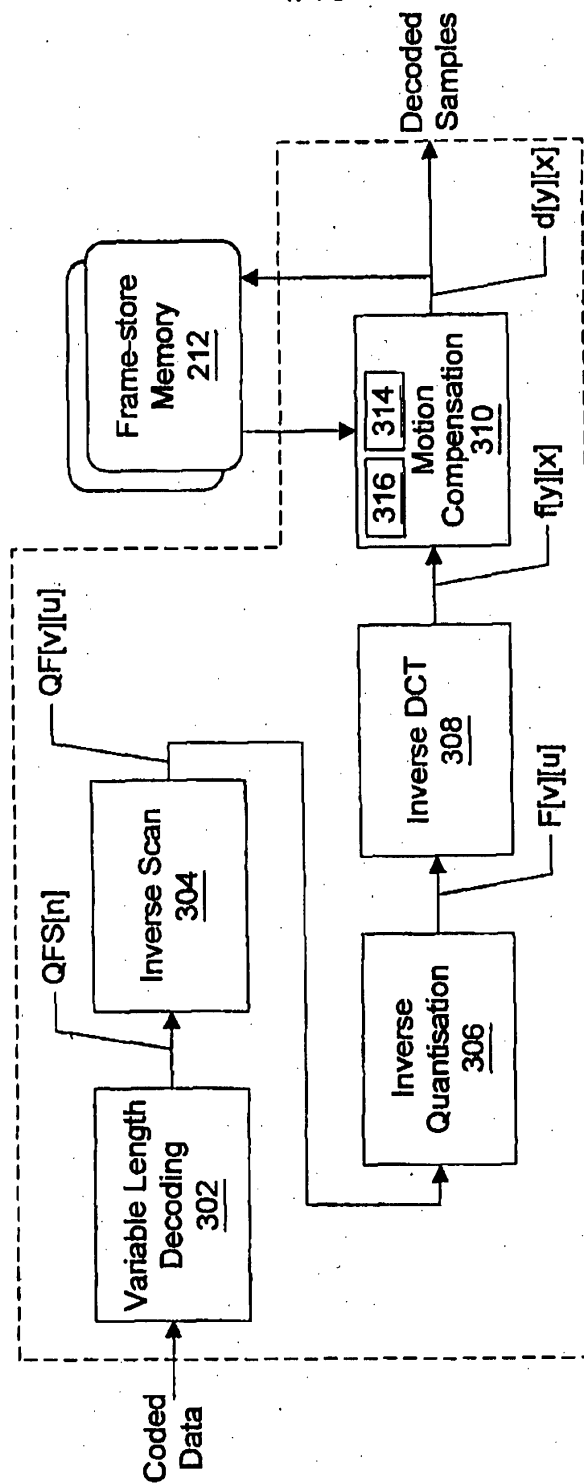


FIG. 4

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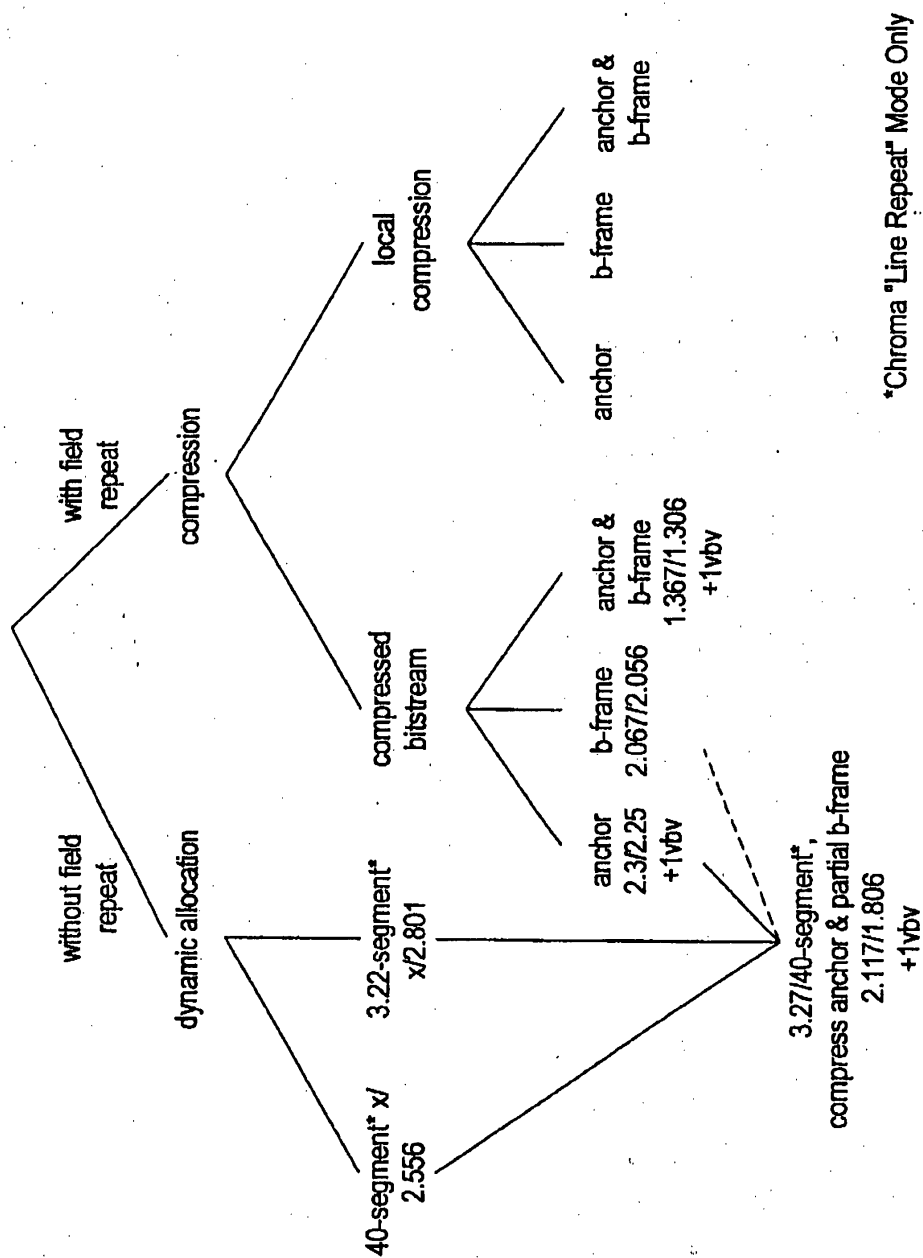


FIG. 5

***Chroma "Line Repeat" Mode Only**

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6/16

Table 1
MPEG Decoder: Memory Partition

	L64005		Compress Displayed Anchor	
	NTSC	PAL	NTSC	PAL
frame store (number of frames)	12,441,600 (3,000)	12,718,080 (2,556)	9,538,560 (2,300)	11,197,440 (2,250)
vbv buffer	1,805,008	1,805,008	3,610,016	3,610,016
video non-instantaneous decode	430,765	520,575		
video-display sync	500,000	600,000		
audio buffer	28,672	28,672		
audio-video latency difference	19,200	23,040		
audio-display sync	12,800	15,360		
video transport buffer	4,096	4,096		
audio transport buffer	4,096	4,096		
4ms jitter at 15Mbps	60,000	60,000		
sub-total for channel buffer	2,864,637	3,060,847	4,669,645	4,865,855
packet header overhead	20,000	20,000		
OSD	675,840	808,192		
sub-total for software & data	775,139	170,097		
Grand Total	16,777,216	16,777,216	1,873,171	(114,271)
frame store + channel buffer	15,306,237	15,778,927	14,208,205	16,063,295

FIG. 6A

APPROVED	O.G. FIG	
BY	CLASS	SUBCLASS
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Table 1
MPEG Decoder: Memory Partition

Compress Anchor & Segment B		Compress B-Frame		Compress Anchor & B-Frame	
NTSC: 3.267 segments 8,778,240 (2.117)	PAL: 40 segments 8,985,600 (1.806)	NTSC 8,570,880 (2.067)	PAL 10,229,760 (2.056)	NTSC 5,667,840 (1.367)	PAL 6,497,280 (1.306)
3,610,016	3,610,016			3,610,016	3,610,016
4,669,645	4,865,855			4,669,645	4,865,855
2,633,491	2,097,569	4,645,859	2,658,417	5,743,891	4,585,889
13,447,885	13,851,455	11,435,517	13,290,607	10,337,485	11,363,135

FIG. 6B

APPROVED	O.G. FIG	
BY	CLASS	SUBCLASS
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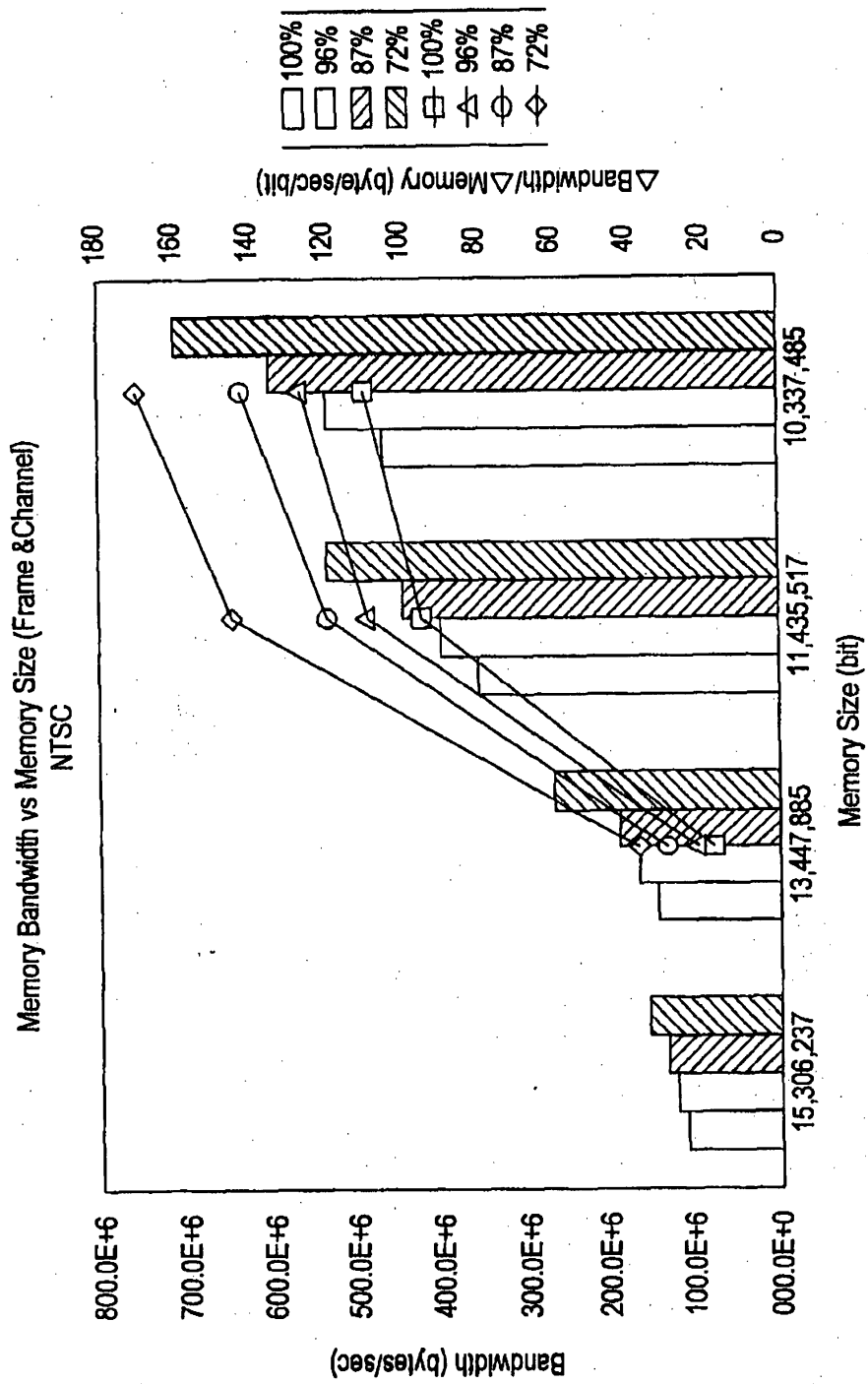


FIG. 7

APPROVED	O.G. FIG	
BY	CLASS	SUBCLASS
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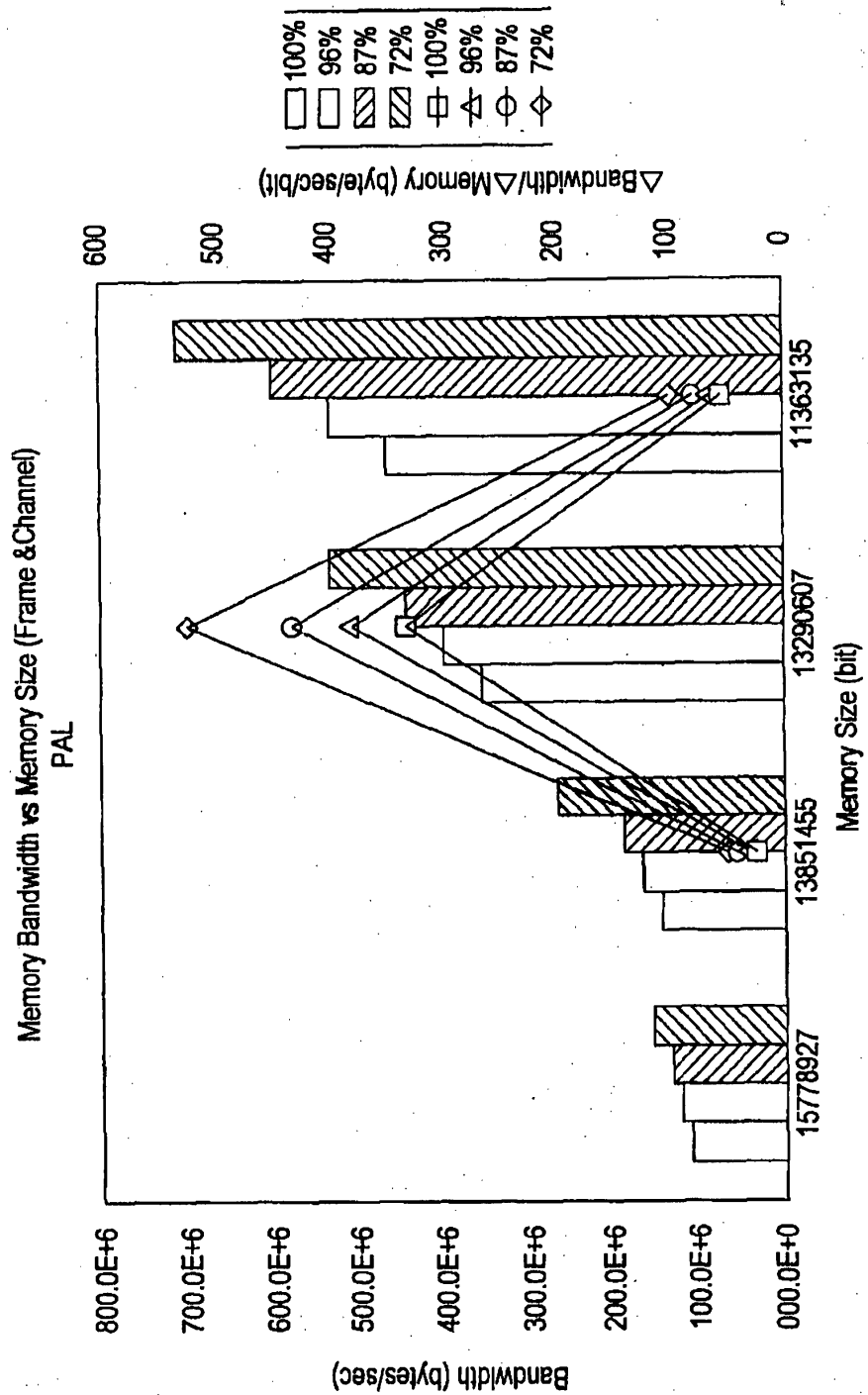


FIG. 8

APPROVED	O.G. FIG.	
BY	CLASS	SUBCLASS
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	bit	
	NTSC	PAL
Video Frames (incl. compressed)	10,583,248	10,790,608
VBV Buffer	1,805,008	1,805,008
Video Decode Buffer	430,765	520,575
Video-Display Sync Buffer	500,000	600,000
Audio Buffer	28,672	28,672
Audio-Video Latency Buffer	19,200	23,040
Audio-Display Sync Buffer	12,800	15,360
Transport Buffer	8,192	8,192
Jitter Buffer (4ms)	60,000	60,000
PES Header Overhead	20,000	20,000
OSD	675,840	808,192
MIPS Code and Data	2,633,491	2,097,569

FIG. 9

APPROVED	O.G. FIG.	
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	Bandwidth (Mbyte/sec)	
	NTSC	PAL
Channel In/Out	18.82	15.98
Motion Compensation	72.70	72.59
Store	38.29	38.23
Display & OSD	30.38	30.38
TOTAL	160.19	157.18

- With 16x1M SDRAM running at 100 MHz, Bandwidth Available is 200Mbyte/sec
- Expecting 20Mbyte/sec for MIPS Code and Data

FIG. 10

APPROVED	O.G. FIG.	
BY	CLASS	SUBCLASS
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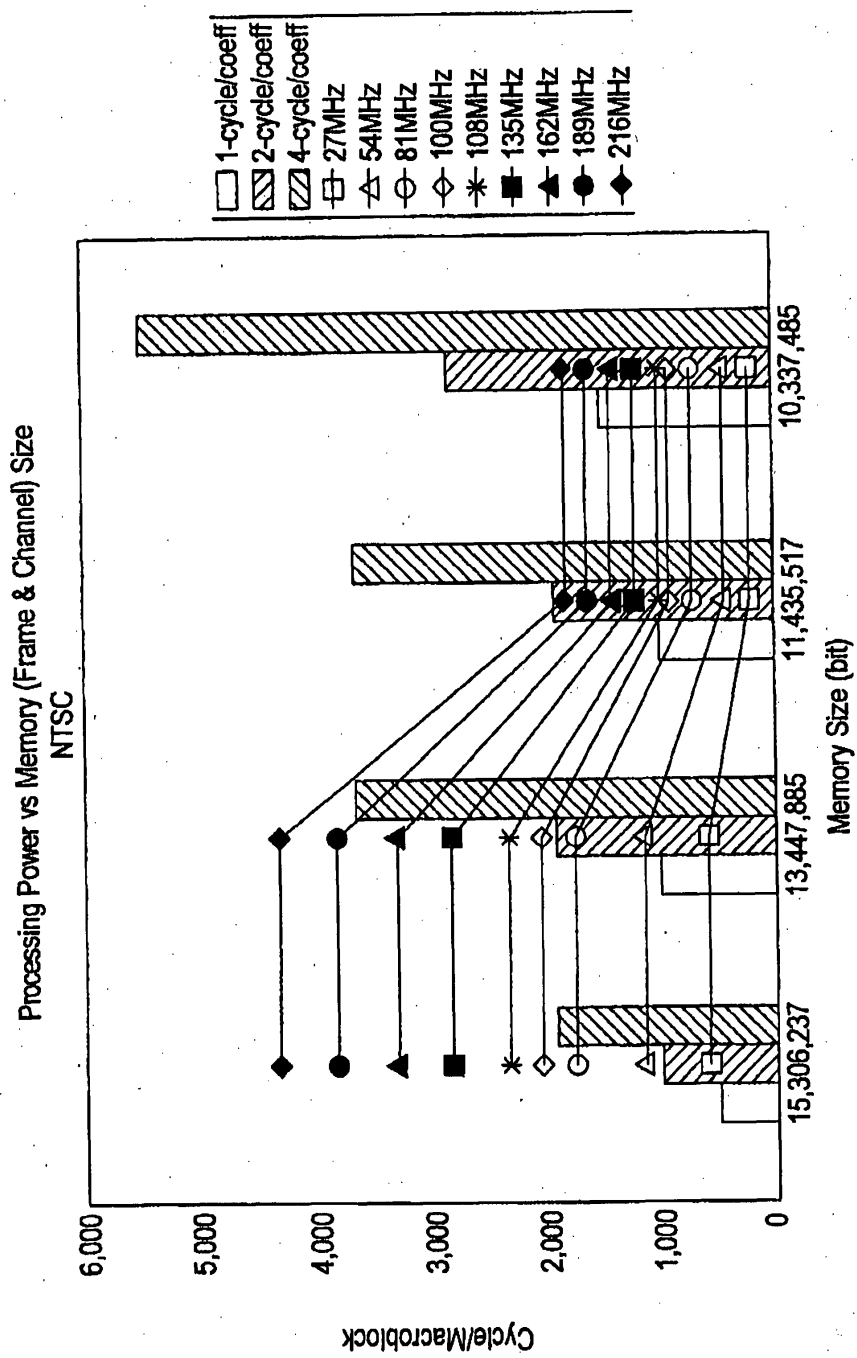


FIG. 11

APPROVED	O.G. FIG.	
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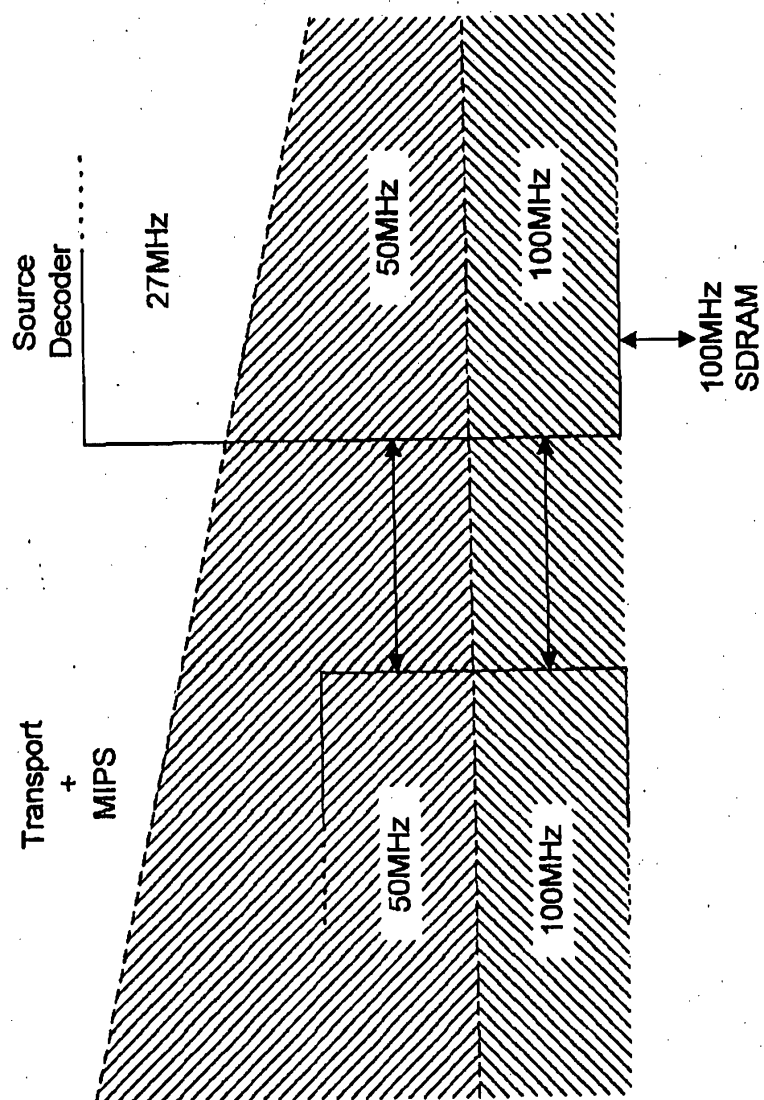


FIG. 12

APPROVED	O.G. FIG.	
BY	CLASS	SUBCLASS
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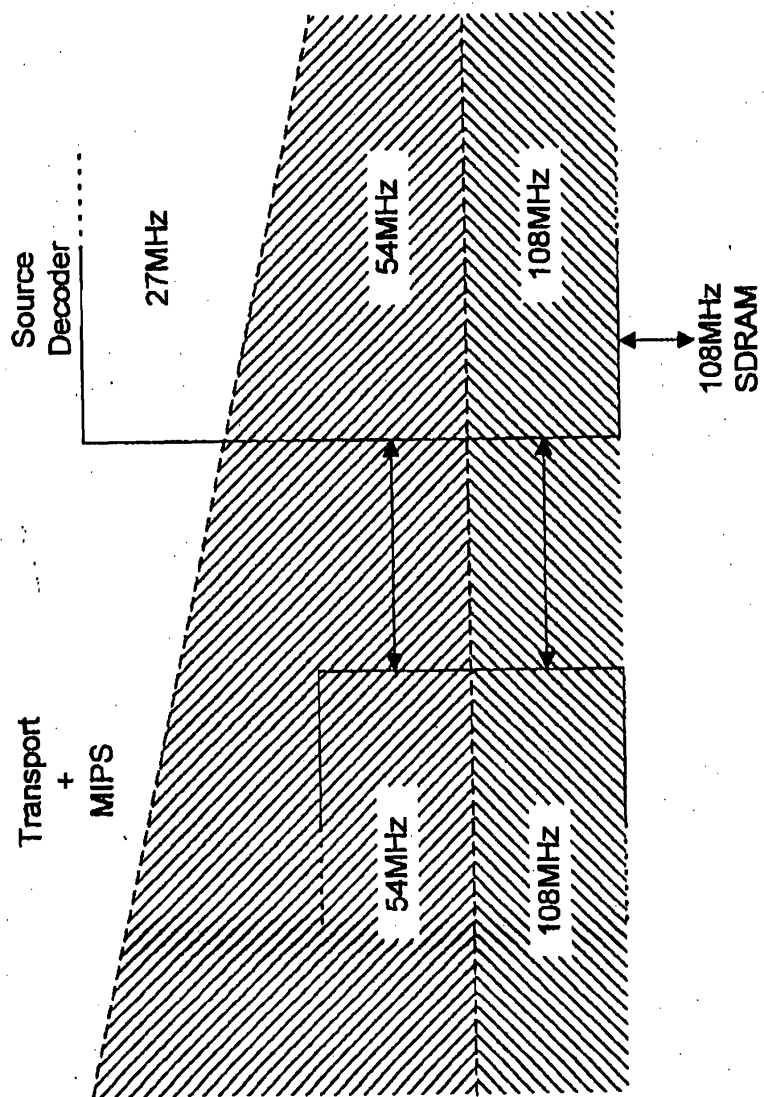
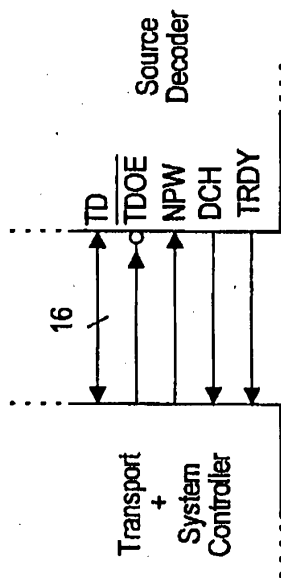


FIG. 13

APPROVED	O.G. FIG.	
BY	CLASS	SUBCLASS
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Signal	Description	Type
TD[15:0]	Transmission Data	Bidirectional
TDOE	Transmission Data Output Enable (active low)	Input
NPW	New Packet Word (reset if TD[15:13]=000)	Input
DCH	Data Chain Hold (i.e. wait cycle request)	Output
TRDY	Transmission Ready (for new packet)	Output

FIG. 14

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08/748269

11/13/96

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5201-01600

EXAMINER

JEFFREY C HOOD
CONLEY ROSE & TAYON
P O BOX 3267
HOUSTON TX 77253-3267

VIA RT UNITIFF N PAPER NUMBER

DATE MAILED 11/25/98

11/25/98

This is in response to the Power of Attorney filed

- ☐ 1. The Power of Attorney to you in this application has been ^{10/26/98}revoked by the applicant. Future correspondence will be mailed to the new address of record. 37 CFR 1.33.
- ☒ 2. The Power of Attorney to you in this application has been revoked by the assignee who has intervened as provided by 37 CFR 3.71. Future correspondence will be mailed to the new address of record. (37 CFR 1.33).
- ☐ 3. The withdrawal as attorney in this application has been accepted. Future correspondence will be mailed to the new address of record. 37 CFR 1.33.

Robert E. Jones
This is a communication from the
Patent and Trademark Office

- ☒ 4. The Power of Attorney in this application is accepted. Correspondence in this application will be mailed to the below-noted address as provided by 37 CFR 1.33.
- ☐ 5. The Power of Attorney in this application is not accepted for the reason(s) checked below:
- ☐ a. The Power of Attorney is from an assignee and the Certificate required by 37 CFR 3.73 (b) has not been received.
 - ☐ b. The person signing for the assignee has omitted their empowerment to sign on behalf of the assignee.
 - ☐ c. The inventor(s) is without authority to appoint attorneys since the assignee has intervened as provided by 37 CFR 3.71.
 - ☐ d. The signature of _____, a co-inventor in this application, has been omitted. The Power of Attorney will be entered upon receipt of confirmation signed by said co-inventor.
 - ☐ e. The person(s) appointed in the Power of Attorney is not registered to practice before the U. S. Patent & Trademark Office.
 - ☐ f. The revocation is not signed by the applicant, the assignee of the entire interest, or one particular principal attorney having the authority to revoke.

LSI LOGIC CORPORATION
1551 MCCARTHY BLVD., MS: D-106
PATENT LAW DEPARTMENT
MILPITAS CA 95035

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Transaction: Date 1999-02-02
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Application: never (PAIR) system
ecomp: www.uspto.gov

PTO UTILITY GRANT

Paper Number 10

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United
States
of
America



The Commissioner of Patents and Trademarks

Has received an application for a patent for a new and useful invention. The title and description of the invention are enclosed. The requirements of law have been complied with, and it has been determined that a patent on the invention shall be granted under the law.

Therefore, this

United States Patent

Grants to the person(s) having title to this patent the right to exclude others from making, using, offering for sale, or selling the invention throughout the United States of America or importing the invention into the United States of America for the term set forth below, subject to the payment of maintenance fees as provided by law.

If this application was filed prior to June 8, 1995, the term of this patent is the longer of seventeen years from the date of grant of this patent or twenty years from the earliest effective U.S. filing date of the application, subject to any statutory extension.

If this application was filed on or after June 8, 1995, the term of this patent is twenty years from the U.S. filing date, subject to an statutory extension. If the application contains a specific reference to an earlier filed application or applications under 35 U.S.C. 120, 121 or 365(c), the term of the patent is twenty years from the date on which the earliest application was filed, subject to any statutory extension.

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Commissioner of Patents and Trademarks

Margaret V. Turner
Attorney

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