Pentium® and Pentium Pro Processors and Related Products

Pentium® Pro Processor

Pentium® Processor

OverDrive® Processor

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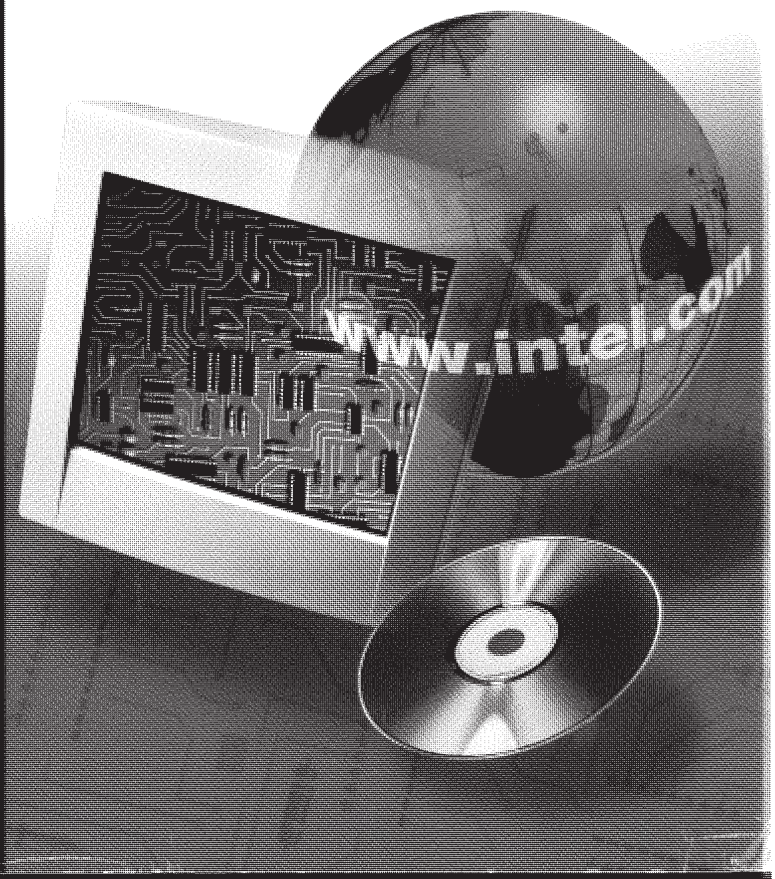
Peripheral Components



intel®

Pentium® and Pentium Pro Processors and Related Products

In 1993, Intel introduced the Pentium® Processor, the fifth generation processor based on the Intel Architecture. The Pentium processor is fully code-compatible with previous members of the Intel Architecture family of microprocessors, thus preserving the value of user's software investments. Up to 3-1/2 times faster than the IntelDX2™ 66MHz processor, the Pentium processor extends the Intel processor performance continuum while maintaining full compatibility with existing software. The Pentium processor utilizes advanced design techniques, superscalar technology and enhanced floating-point to speed up today's applications and enable tomorrow's emerging technologies. The family is designed for mainstream desktops and powerful mobiles.

In November of 1995, Intel introduced the Pentium Pro processor, Intel's next generation of performance for high-end desktops, workstations and servers. The family is easily scalable up to four microprocessors in a multiprocessor system. The Pentium Pro processor delivers more performance than previous generation processors through an innovation called Dynamic Execution. This is the next step beyond superscalar architecture. Dynamic Execution makes possible the advanced 3D visualization and interactive capabilities required by high-end commercial and technical applications. The Pentium Pro processor includes advanced data integrity, reliability, and serviceability features for mission critical applications.

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THE PENTIUM® FAMILY-A TECHNICAL OVERVIEW

Intel's Pentium® processor family combines the performance traditionally associated with minicomputers and workstations with the flexibility and compatibility that characterize the personal computer platform. Designed to meet the needs of today's and tomorrow's sophisticated software applications, the Pentium processor extends the range of Intel's microprocessor architecture to new heights, blurring previous distinctions between hardware platforms and creating an entirely new realm of possibilities for notebook computers, desktop PCs, and servers.

This article begins by presenting an overview of the Pentium processor. It then details the key technological features that enable the Intel solution to meet the market's evolving requirements for high performance, continued software compatibility, and advanced functionality.

THE WORLD'S BEST PERFORMANCE FOR ALL PC SOFTWARE

The Pentium processor family includes the highest performing members of Intel's family of microprocessors.

Pentium® Processor 75/90/100/120/133 Core Frequency	External Bus Interface	iCOMP® Index
133 MHz	66 MHz	1110
120 MHz	60 MHz	1000
100 MHz	66/50 MHz	815
90 MHz	60 MHz	735
75 MHz	50 MHz	610

While incorporating new features and improvements made possible by advances in semiconductor technology, the Pentium processor is fully software compatible with previous members of the Intel microprocessor family-thereby preserving the value of users' software investments. The Pentium processor meets the demands of computing in a number of areas: advanced operating systems, such as DOS*, Windows*, OS/2*, and UNIX*; computing-intensive graphics applications, such as 3-D modeling, computer-aided design/engineering (CAD/CAE), large scale financial analysis, high-throughput client/server, handwriting, and voice recognition; network applications; virtual reality; electronic mail that combines many of the above areas; and new applications yet to be developed.

The Pentium processor family was designed using an advanced process technology and has features that are less than a micron (one-millionth of a meter) in size. The Pentium processor (510\60, 567\66) was developed utilizing 5V, 0.8 micron technology, while the Pentium processor (610\75, 735\90, 815\100. 1000\120, 1110\133) was designed using 3.3V, 0.6 micron and 3.3V, 0.35 micron technology.

The increasingly improved Pentium processor family brings the users CPUs with higher frequencies, while the system bus frequencies range from 50 MHz to 66 MHz, allowing cost effective system designs.

THE PENTIUM® PROCESSOR: TECHNICAL INNOVATIONS

A number of innovative product features contribute to the Pentium processor's unique combination of high performance, compatibility, data integrity and upgradability. These include:

- Superscalar Architecture
- Separate 8K Code and Data Caches
- Writeback MESI Protocol in the Data Cache
- Dynamic Branch Prediction
- Pipelined Floating-point Unit
- Improved Instruction Execution Time
- 64-Bit Data Bus
- Bus Cycle Pipelining
- Address Parity
- Internal Parity Checking
- Functional Redundancy Checking
- Execution Tracing
- Performance Monitoring

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- IEEE 1149.1 Boundary Scan
- System Management Mode
- Virtual Mode Extensions
- Upgradable With a Future Pentium OverDrive® Processor
- Multiprocessor Support

In addition to the features listed above, the Pentium processor 75/90/100/120/133 offers the following enhancements over the Pentium processor 60/66

- Dual Processing Support
- SL Power Management Features
- Fractional Bus Operation
- On-chip Local APIC Device

Superscalar Architecture

The Pentium processor's superscalar architecture enables the processor to achieve superior performance by executing more than one instruction per clock cycle. The term "superscalar" refers to a microprocessor architecture that contains more than one execution unit. These execution units, or piplines are where the CPU processes the data and instructions that are fed to it by the rest of the system.

The Pentium processor's superscalar implementation represents a natural progression from previous generations of processors in the 32-bit Intel architecture. The Intel486™ processor for instance, is able to execute many instructions in one clock cycle, while previous generations of Intel microprocessors require multiple clock cycles to execute a single instruction.

The ability to execute multiple instructions per clock cycle is due to the fact that the Pentium processor has two pipelines that can execute two instructions simultaneously. The Pentium processor's dual pipelines execute integer instructions in five stages: *prefetch, decode1, decode2, execute* and *writeback*. This permits several instructions to be in various stages of execution, thus increasing processing performance.

The Pentium processor also uses hardwired instructions to replace many of the microcoded instructions used in previous microprocessor generations. Hardwired instructions are simple and commonly used, and can be executed by the processor's hardware without requiring microcode.

This improves performance without affecting compatibility. In the case of more complex instructions, the Pentium processor's enhanced microcode further boosts performance by employing both dual integer pipelines to execute instructions.

Separate 8K Code and Data Caches

Pentium processors include separated code and data caches integrated on-chip to meet performance goals. On-chip caches increase performance by acting as temporary storage places for commonly-used instructions and data, replacing the need to go off-chip to the system's main memory to fetch information. The separate caches reduce bus conflicts and are available more often when they are needed.

The Pentium processor's code and data caches each contain 8 Kbytes of information and both are organized as two-way set associative caches-meaning that they save time by searching only pre-specified 32-byte segments rather than the entire cache. Each cache has a dedicated Translation Lookaside Buffer (TLB) to translate linear addresses to physical addresses.

The Pentium processor's data cache is configurable to be "writeback" or "write through" on a line-by-line basis and follows the MESI (Modified, Exclusive, Shared, Invalid) protocol. The "writeback" method transfers data to the cache without going out to main memory. Data is written to main memory only when it is removed from the cache. In contrast, the "write through" method transfer data to the external memory each time the processor writes data to the cache. The "writeback" technique increases performance by reducing bus utilization and preventing unnecessary bottlenecks in the system.

To ensure that data in the cache and in main memory are consistent, the data cache implements the MESI protocol during reads and writes. This is especially important in a multiprocessor environment.

Dynamic Branch Prediction

Branch prediction is an advanced computing technique that boosts performance by keeping the execution pipelines full. It is accomplished by predetermining the most likely set of instructions to be executed.

To understand the concept better, consider a typical application program. After each pass through a software loop, the program performs a conditional test to determine whether to return to the beginning of the loop or to exit and continue on to the next execution step. These two paths are called branches. Dynamic branch prediction forecasts which branch the software will require, based on the assumption that the previous taken branch will be used again. Pentium processors make prediction by using a Branch Target Buffer (BTB). Pentium processors also implement two prefetch buffers, one to prefetch code in a linear fashion and the other to prefetch code according to the addresses in the BTB. As a result, the needed code is always prefetched before it is required for execution. In addition, the Pentium processors support more sophisticated algorithms by using two level branch prediction.

Pipe-lined Floating-Point Unit

The 32-bit compute-intensive software applications require a high degree of floating-point processing power to handle mathematical calculations. As the floating-point requirements of personal computer software have steadily increased, advances in microprocessor technology have been introduced to satisfy these needs. The Intel486 DX processor, for example, was the first Intel microprocessor to integrate math coprocessing functions on-chip; previous-generation Intel processors used off-chip math coprocessors when floating-point calculations were required.

The Pentium processor family takes math computational ability to the next performance level by using an enhanced on-chip floating-point unit that incorporates sophisticated eight-stage pipeline and hardwired functions. A three-stage floating-point instruction pipeline is appended to the integer pipelines. Most floating-point instructions begin execution in one of the integer pipelines, then move on to the floating-point pipeline. In addition, common floating-point functions, such as, add, multiply and divide, are hardwired for faster execution.

Enhanced 64-Bit Data Bus

The data bus is the highway that carries information between the processor and the memory subsystem. Because of its external 64-bit data bus, the Pentium processor can transfer data to and from memory at rates up to 528 Mbytes/second, a more than five-fold increase over the peak transfer rate of the 66 MHz Intel DX2™ microprocessor (105 Mbytes/second). This wider data bus facilitates high-speed processing by maintaining the flow of instructions and data to the processor's superscalar execution unit.

In addition to having a wider data bus, the Pentium processor implements bus cycle pipelining to increase bus bandwidth. Bus cycle pipelining allows a second cycle to start before the first one is completed. This gives the memory subsystem more time to decode the address, which allows slower and less-expensive memory components to be used, resulting in a lower overall system cost. Burst reads and writes, parity on address and data, and a simple cycle identification all contribute to providing greater bandwidth and improved system reliability.

The Pentium processor also has two write buffers, one corresponding to each pipeline, to enhance the performance of consecutive writes to memory. Write buffers improve performance by allowing the processor to proceed with the next pair of instructions, even though one of the current instructions needs to write to memory while the bus is busy.

Data Integrity and Error Detection Features

Protecting important data and ensuring its integrity has become increasingly important as mission-critical applications continue to proliferate. To ensure the Pentium processors' reliability, Intel ran millions of simulations and tests. In addition, designers have added significant data integrity and error detection capability. Data parity checking is supported on byte-by-byte basis. Address parity checking, and internal parity checking features have been added along with a new exception, the machine check exception.

Internal error detection places parity bits on the internal code and data caches, translation look aside buffers, microcode, and branch target buffer. This feature helps to detect errors in a manner that remains transparent to both the user and the system.

Furthermore, the Pentium processors have implemented functional redundancy checking to provide maximum error detection of the processor and the interface to the processor. When functional redundancy checking is used, two Pentium processors act as "master" and "checker" respectively. The "checker" is used to