UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE PATENT TRIAL AND APPEAL BOARD

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SAMSUNG ELECTRONICS CO., LTD. and
SAMSUNG ELECTRONICS AMERICA, INC.,
Petitioner,

v.

PARTHENON UNITED MEMORY ARCHITECTURE LLC,
Patent Owner.

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Case IPR2015-01946
Patent 5,960,464

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Before MICHAEL R. ZECHER, JAMES B. ARPIN, and
MATTHEW R. CLEMENTS, *Administrative Patent Judges*.

CLEMENTS, *Administrative Patent Judge*.

DECISION
Institution of *Inter Partes* Review
35 U.S.C. § 314(a) and 37 C.F.R. § 42.108

I. INTRODUCTION

Petitioner, Samsung Electronics Company, Limited and Samsung Electronics America, Incorporated (collectively "Petitioner"), filed a Petition requesting an *inter partes* review of claims 1–4, 7–13, 16–24, 32–36, and 40 ("the challenged claims") of U.S. Patent No. 5,960,464 (Ex. 1001, "the '464 patent"). Paper 2 ("Pet."). Parthenon Unified Memory Architecture Limited Liability Corporation ("Patent Owner") filed a Preliminary Response. Paper 6 ("Prelim. Resp.").

Under 35 U.S.C. § 314(a), an *inter partes* review may not be instituted unless the information presented in the Petition shows "there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition." Taking into account the arguments presented in Patent Owner's Preliminary Response, we conclude that the information presented in the Petition establishes that there is a reasonable likelihood that Petitioner would prevail in challenging claims 1–4, 7–13, 16–24, 32–36, and 40 of the '464 patent as unpatentable under 35 U.S.C. §§ 102(e) and 103(a). Pursuant to § 314, we hereby institute an *inter partes* review as to the challenged claims of the '464 patent.

A. Related Matters

The '464 patent is involved in the following district court cases: (1) *Parthenon Unified Memory Architecture LLC v. Huawei Technologies Co.*, No. 2:14-cv-00687-JRG-RSP (E.D. Tex.); (2) *Parthenon Unified Memory Architecture LLC v. Motorola Mobility, Inc.*, No. 2:14-cv-00689-JRG-RSP (E.D. Tex.); (3) *Parthenon Unified Memory Architecture LLC v. HTC Corp.*, No. 2:14-cv-00690-RSP (E.D. Tex.); (4) *Parthenon Unified Memory*

Architecture LLC v. LG Electronics, Inc., No. 2:14-cv-00691-JRG-RSP (E.D. Tex.); (5) *Parthenon Unified Memory Architecture LLC v. Samsung Electronics Co.*, No. 2:14-cv-00902-JRG-RSP (E.D. Tex.); (6) *Parthenon Unified Memory Architecture LLC v. Qualcomm Inc.*, No. 2:14-cv-00930-JRG-RSP (E.D. Tex.); (7) *Parthenon Unified Memory Architecture LLC v. ZTE Corp.*, No. 2:15-cv-00225-JRG-RSP (E.D. Tex.); and (8) *Parthenon Unified Memory Architecture LLC v. Apple Inc.*, No. 2:15-cv-00621-JRG-RSP (E.D. Tex.). Pet. 1–2; Paper 5, 2. Also, U.S. Patent No. 5,812,789 is involved in *STMicroelectronics, Inc. v. Motorola, Inc.*, No. 4:03-cv-00276-LED (E.D. Tex.). Pet. 2.

In addition to this Petition, Petitioner filed other petitions challenging the patentability of claims in the following patents owned by Patent Owner: (1) U.S. Patent No. 7,321,368 B2 (Case IPR2015-01500); (2) U.S. Patent No. 7,777,753 B2 (Case IPR2015-01501); (3) U.S. Patent No. 7,542,045 B2 (Case IPR2015-01502); (4) U.S. Patent No. 8,054,315 B2 (Case IPR2015-01494); (5) U.S. Patent No. 8,681,164 B2 (Case IPR2015-01503); and (6) U.S. Patent No. 5,812,789 (Case IPR2015-01944). *Id.*

B. The '464 Patent

The '464 patent, titled "Memory Sharing Architecture for a Decoding in a Computer System," issued September 28, 1998, from U.S. Patent Application No. 08/701,890, filed on August 23, 1996. Ex. 1001, at [54], [45], [21], [22]. Because the application that led to the '484 patent was filed August 23, 1996, the '464 patent is set to expire on August 23, 2016.

The '464 patent generally relates to "a memory management system that can be used with applications requiring a large contiguous block of

memory, such as video decompression techniques (e.g., [Motion Picture Expert Group 2 (MPEG 2)] decoding)." *Id.* at Abstract. Existing MPEG 2 decompression chip sets could be expensive because they required two (2) megabytes of dynamic random-access memory. *Id.* at 2:18–24. As a result, it was desirable to employ the main memory of the computer. *Id.* However, because typical operating systems allocate memory in four (4)-kilobyte blocks, it was difficult to obtain two (2)-megabytes of contiguous memory. *Id.* at 2:51–63. To address these and other problems, the disclosed memory management module requests and employs approximately 500, four (4)-kilobyte pages of the main memory, some of which are in noncontiguous blocks of pages, to construct a single contiguous two (2)-megabyte block of memory. *Id.* at 3:8–15.

Figure 2 of the '464 patent is reproduced below.
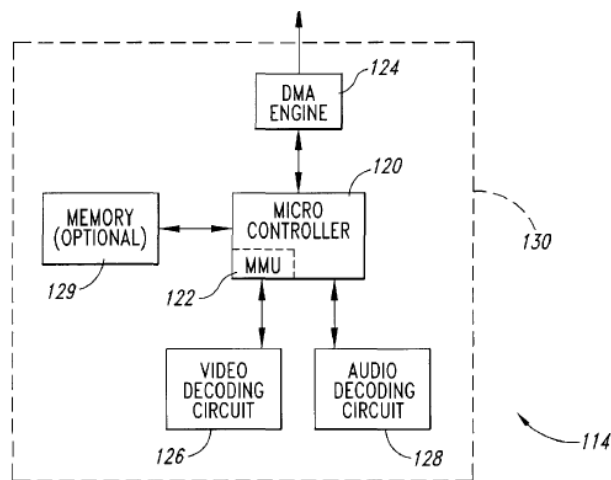
Fig. 2

Figure 2 is a block diagram of MPEG 2 decoder 114. *Id.* at 4:1–2, 4:42–43. MPEG 2 decoder 114 includes direct memory access (DMA) engine 124, video decoding circuit 126, and audio decoding circuit 128, each of which is

conventional. *Id.* at 4:51–54, 5:3–7. MPEG 2 decoder 114 further includes microcontroller 120, which, in turn, includes memory management unit 122. *Id.* at 4:43–46. Microcontroller 120 directly accesses main memory 106 through DMA engine 124. *Id.* at 4:46–54. Microcontroller 120 performs memory sharing routine 200 (illustrated in the flowchart of Figure 4) to request a two (2)-megabyte portion of main memory 106. *Id.* at 6:63–66. If two (2)-megabytes of contiguous memory is not available, microcontroller 120 can request two, one (1)-megabyte blocks. *Id.* at 7:16–27. If two, one (1)-megabyte blocks of contiguous memory are not available, microcontroller 120 can request four (4), 500-kilobyte blocks. *Id.* In a worst-case scenario, microcontroller 120 can request 500, four (4)-kilobyte blocks of memory. *Id.* at 7:56–63. "[M]icrocontroller 120 programs or creates a lookup table to translate or map the 500 pages to a contiguous string of memory locations beginning at a set address and increasing contiguously therefrom to an address 2 megabytes later" (*id.* at 7:46–50) using conventional lookup table techniques (*id.* at 8:30–35).

C. Illustrative Claim

Of the challenged claims, claims 1, 10, 19, and 32 are independent. Claims 2–4 and 7–9 depend from independent claim 1. Claims 11–13 and 16–18 depend from independent claim 10. Claims 20–24 depend from independent claim 19. Claims 33–36 and 40 depend from independent claim 32. Independent claim 1 is illustrative of the challenged claims and is reproduced below:

> 1.   In a computer system having a main memory, a storage device having encoded data stored therein and a

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