

United States Patent [19]

Thomas et al.

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[54] **BUS STRUCTURE FOR OVERLAPPED DATA TRANSFER**

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[73] Assignee: Gould Inc., Ft. Lauderdale, Fla.

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[51] Int. Cl.⁵ G06F 13/40

[52] U.S. Cl. 364/200; 364/240; 364/240.2; 364/242.92

[58] Field of Search ... 364/200 MS File, 900 MS File

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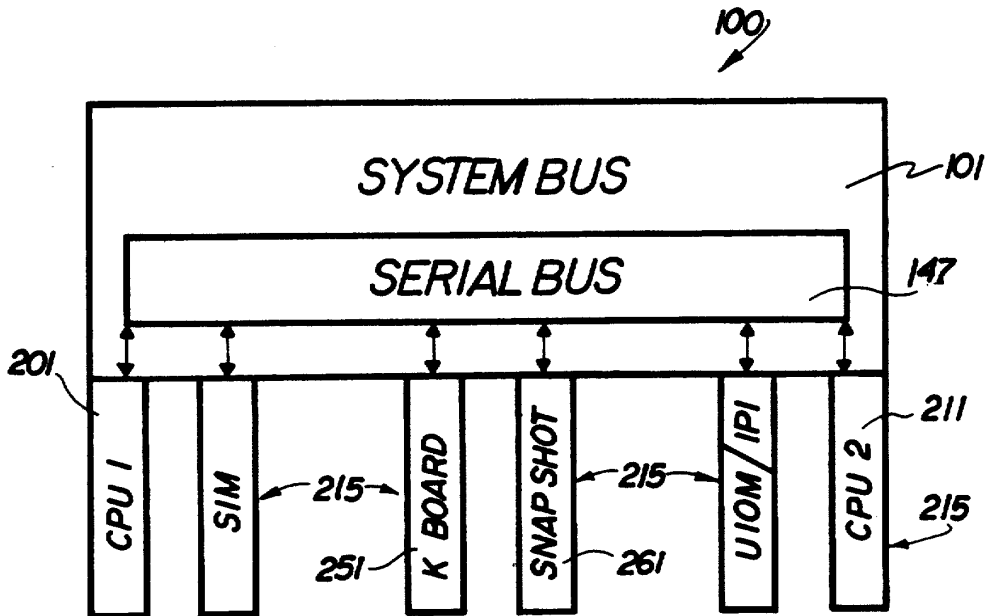
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Attorney, Agent, or Firm—Fleit, Jacobson, Cohn, Price, Holman & Stern

[57] **ABSTRACT**

An improved system bus structure for versatile use in various digital computer architecture configurations, particularly those of mini-supercomputers, and, designed to support high speed, high reliability, parallel processing of bi-directional signal transfers in a multi-processor and multiple central processor unit (CPU) communication environment as between system bus units or devices. The system bus structure may be sized for a compact encasement and may carry as many as 129 simultaneous signals to and from various units connected to it. The system bus structure includes enabling structure for a centralized arbitration system, a centralized clock and synchronized transfer system, a centralized transfer monitor, a centralized parity error assessor and signalling system including transfer termination, and, a memory/inter-system inhibit system.

11 Claims, 34 Drawing Sheets



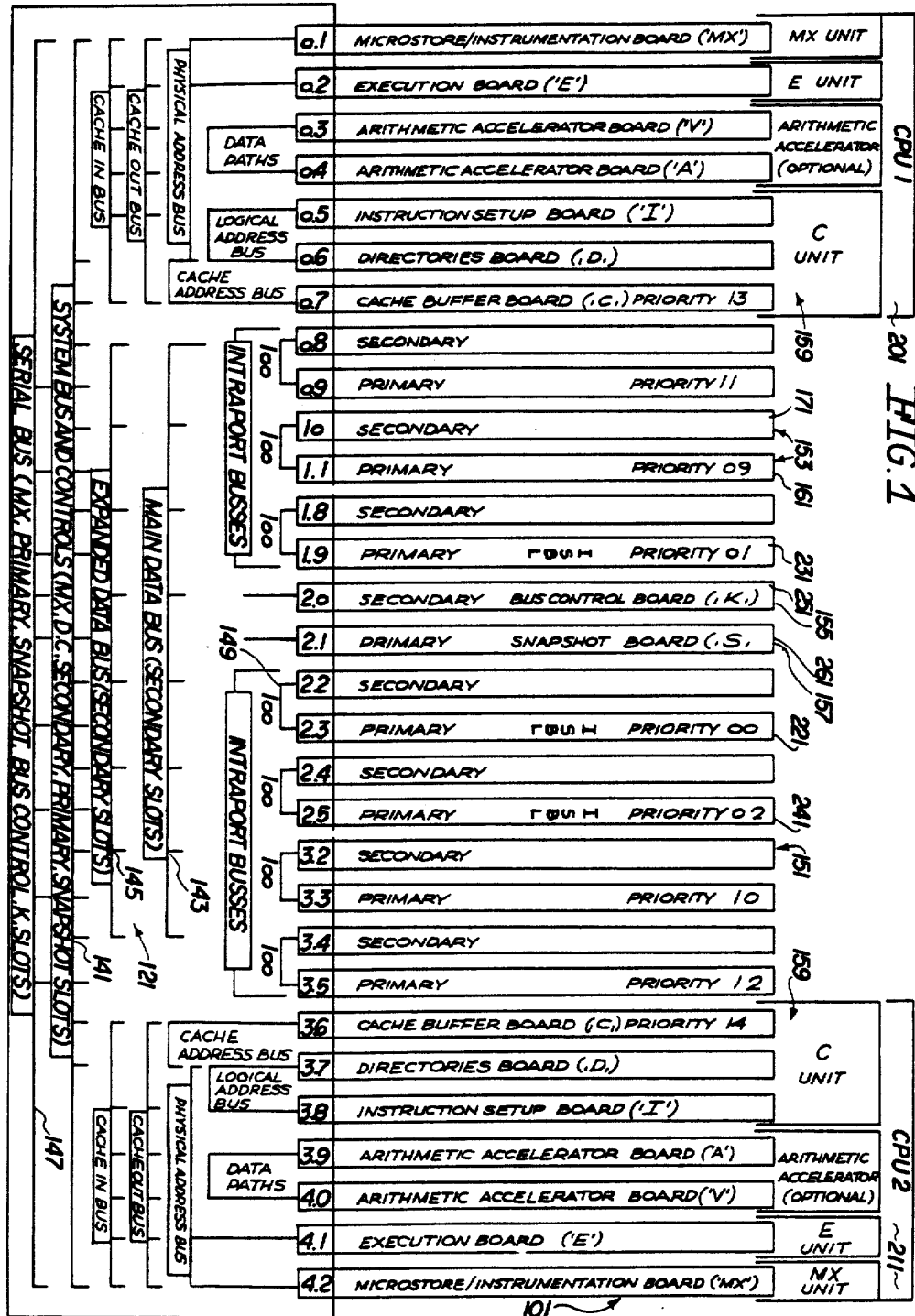


FIG. 1

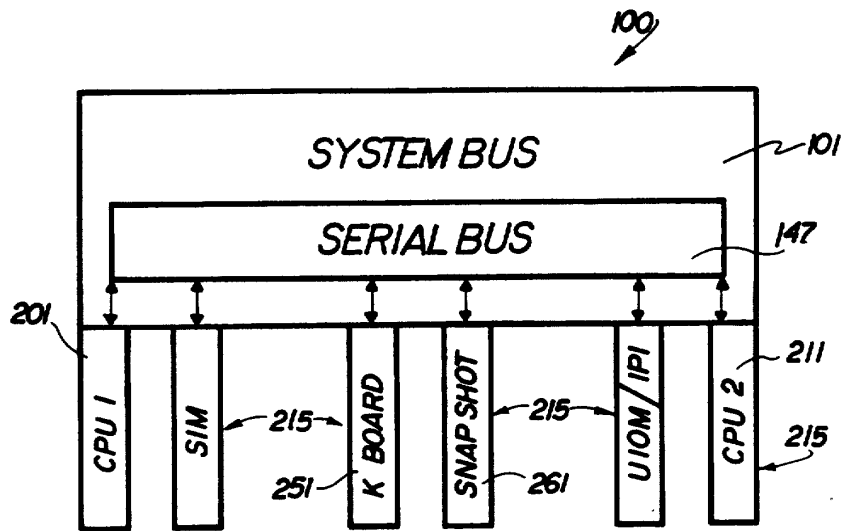


FIG. 2

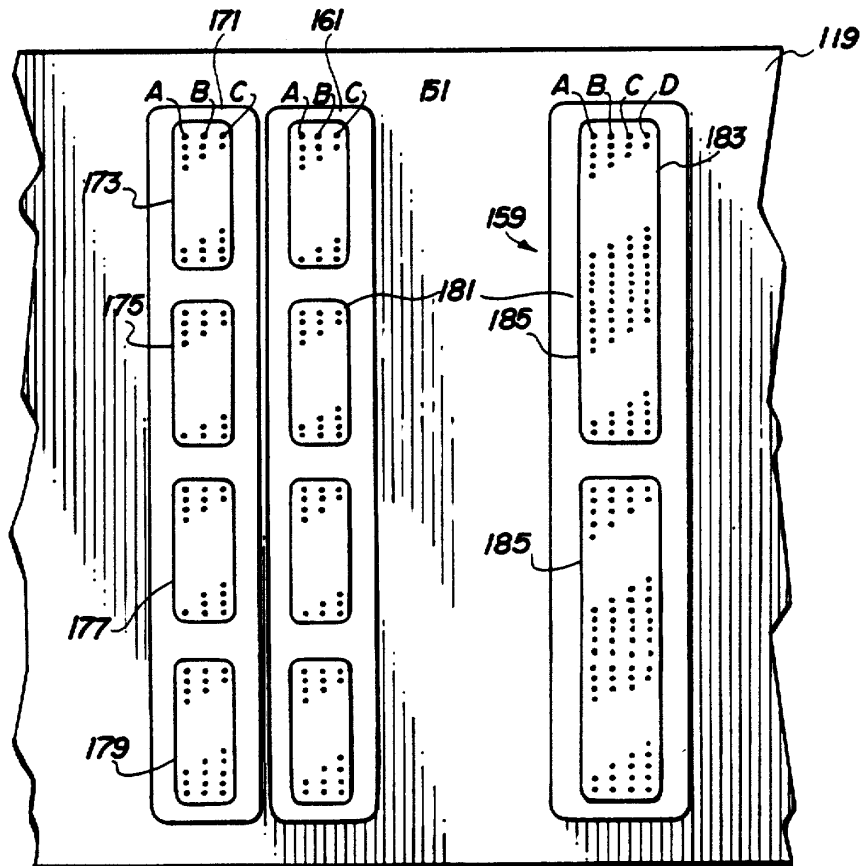


FIG. 3

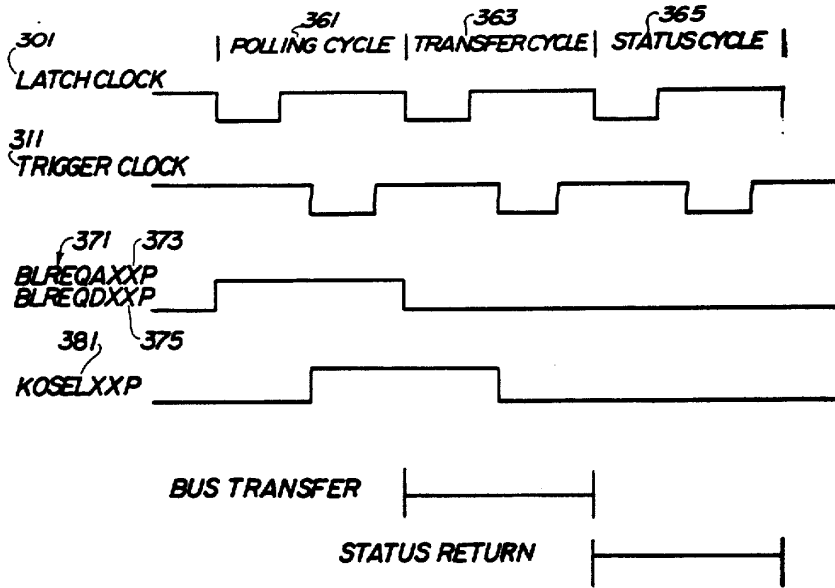


FIG. 4

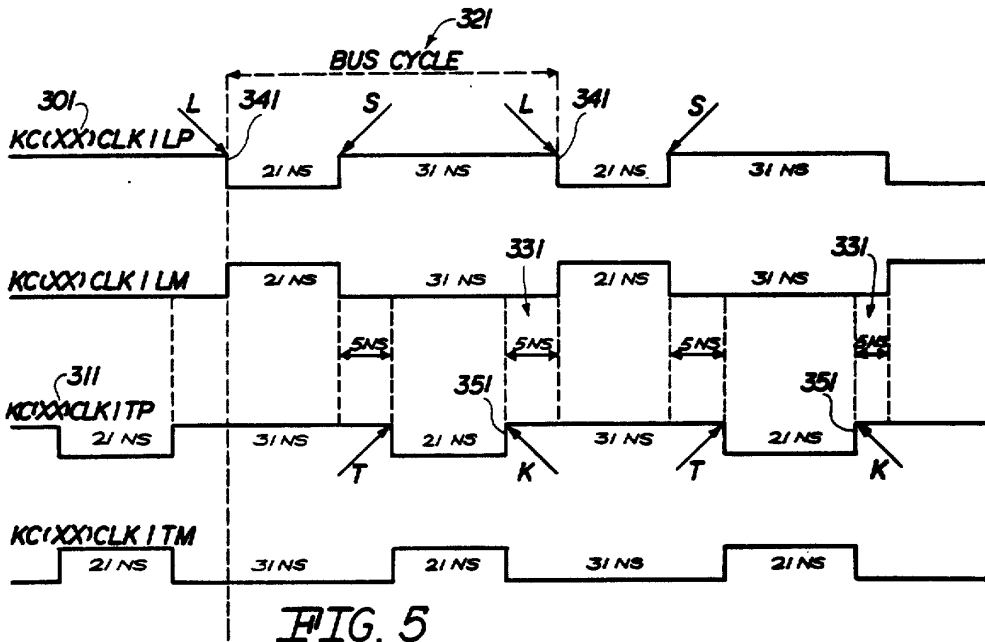


FIG. 5

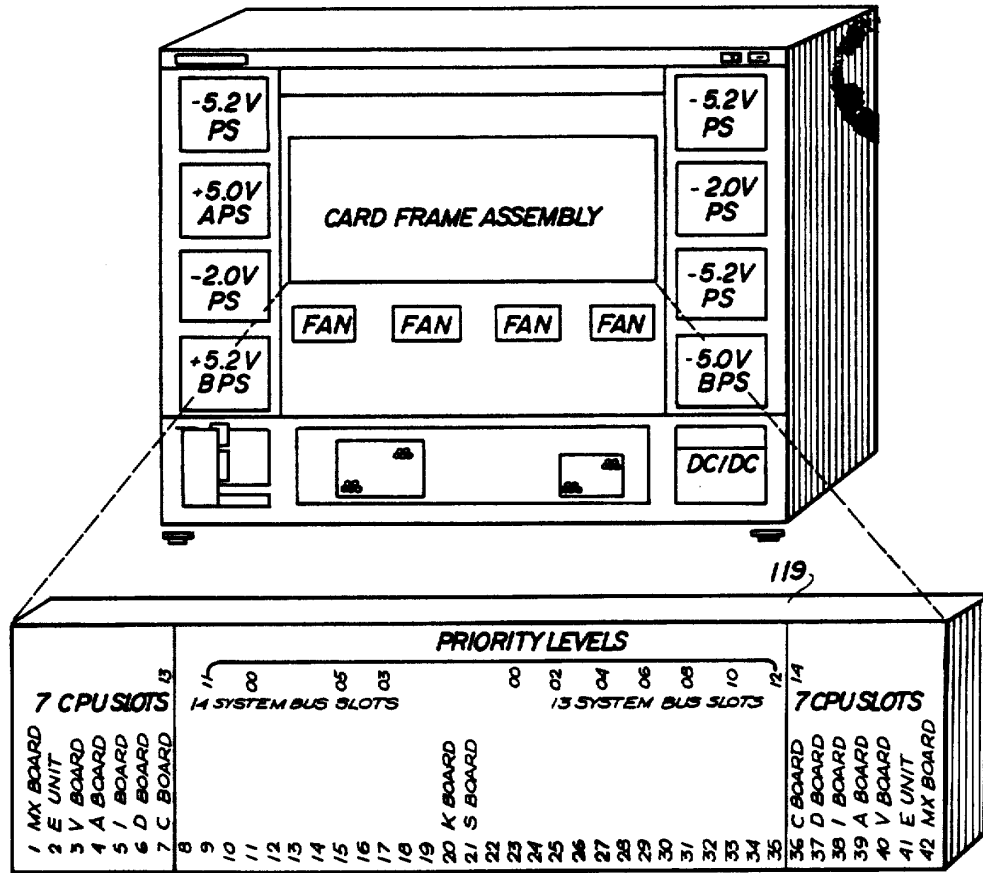


FIG. 6

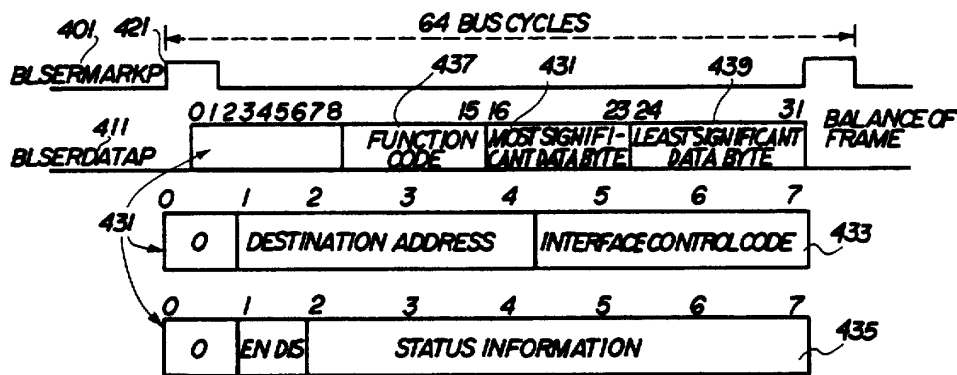


FIG. 7

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