ROBERT P. COLWELL

3594 NW BRONSON CREST LOOP
PORTLAND, OR 97229
503-629-9638
BOB COLWELL@GMAIL COM

PROFESSIONAL EXPERIENCE

- **Director**, Microsystems Technology Office, DARPA Arlington VA 2012-2014
- **Deputy Director**, Microsystems Technology Office, DARPA 2011-2012

  Led office of 17 program managers, budget ~$600M/yr, funding research on computer systems, nanophotonics, bioengineering, radar, comms, lasers, IR imaging, and much more.
- **Consultant**, Portland, OR 2001-2011, 2014 - present

  General computer HW/SW consulting to industry and academia

- Named an **Intel Fellow** (27 Fellows in Intel's employee population of ~80,000) in 1997; winner of 2005 **Eckert-Mauchly Award**, highest award in field of computer architecture, for "outstanding achievements in the design and implementation of industry-changing microarchitectures, and for significant contributions to the RISC/CISC architecture debate"; elected to **IEEE Fellow** and the **National Academy of Engineering** in 2006 (the highest recognition in field of engineering) for "contributions to turning novel computer architecture concepts into viable, cutting-edge commercial processors." Inducted into the **American Academy of Arts and Sciences**, 2012. Winner of **IEEE Bob Rau Award**, 2015.
- **Chief IA-32 Architect**, Intel Corporation, Hillsboro OR, 1992-2001

  Lead IA32 architect, responsible for all of Intel's x86 Pentium CPU architecture efforts (direct management included 40 – 110 people): Pentium Pro, Pentium II, III, 4; Initiated and led Intel's Pentium 4 CPU development

- **Senior CPU Architect**, Intel Corporation, Hillsboro OR, 1990-1992

  One of three senior architects responsible for conceiving Intel's P6 microarchitecture, the core of the company's Pentium II, Pentium III, Celeron, Xeon, and Centrino families

- **Hardware Architect**, Multiflow Computer, New Haven, CT 1985-1990

  One of seven hardware engineers who created the world's first VLIW (very long instruction word) scientific supercomputer under direction of Josh Fisher

- **Hardware Engineer** (part-time) Perq Systems, Pittsburgh PA, 1980 - 1984

  Hardware design engineer working on graphics display hardware for first generation bit-slice-based engineering workstations

- **Member of Technical Staff**, Bell Telephone Laboratories, Holmdel, NJ, 1977-1980

  Hardware design engineer working on 8 and 32-bit microprocessors

EDUCATION

- **PhD in Computer Engineering**, Carnegie-Mellon University, 1985
- **MSEE** in Computer Engineering, Carnegie-Mellon University, 1978
- **BSEE** in Electrical Engineering, University of Pittsburgh, 1977

PUBLICATIONS

Wrote foreword to "Weaving High Performance Multi-Core Processor Fabric: Essential Insights to the Intel Quickpath Architecture", Maddox, Singh, Safranek, Intel Press 2009

National Research Council, The Future of Computing Performance: Game Over or Next Level?, Washington, D.C.: The National Academies Press, 2010.

VLIW: The Unlikeliest Architecture, IEEE Solid State Circuits News, 2009

Wrote intro to DE Shaw's article on the Anton molecular folding engine in CACM, July 2008

Contributed parameterized chapter 2 problem sets to Hennessy & Patterson's "Computer Architecture: A Quantitative Approach, 4th Edition" 2006

The Pentium Chronicles, IEEE/Wiley, December 2005

IEEE Computer Magazine, 48 columns for "At Random" column 2002-2005

Wrote foreword to Josh Fisher's book "Embedded Computing: A VLIW Approach to Architecture, Compilers and Tools", Morgan-Kaufman 2005

We May Need A New Box, IEEE Computer March 2004

Superscalar Processor Design, P6 chapter, Shen & Lipasti, McGraw-Hill 2003

Embedded Everywhere, National Academy of Science, October 2001

Intel's College Hiring Methods and Recent Results, Microelectronics Systems Education Conference, Robert Colwell, Gary Brown, Frank See, July 1999

Microprocessor, Wiley & Son Technical Encyclopedia, 1999

Challenges and Trends in Processor Design, roundtable discussion in IEEE Computer, January 1998

A 0.6um BiCMOS Processor with Dynamic Execution, Robert P. Colwell, Randy L. Steck, 1995 IEEE International Solid State Circuits Conference, pp. 176-177 (won best paper award)

Latent Design Faults in the Development of Multiflow's TRACE/200, 22nd Annual International Symposium on Fault-Tolerant Computing, Boston MA, July 1992

Architecture and Implementation of a VLIW Supercomputer, Robert P. Colwell, W. Eric Hall, Chandra S. Joshi, David B. Papworth, Paul K. Rodman, James E. Tornes, Proceedings of Supercomputing '90, New York, November 1990

A VLIW Architecture for a Trace Scheduling Compiler, Robert P. Colwell, Robert P. Nix, John J. O'Donnell, David B. Papworth, Paul K. Rodman, IEEE Trans. on Comp., V. 37, N. 8, Aug.1988

A VLIW Architecture for a Trace Scheduling Compiler, Robert P. Colwell, Robert P. Nix, John J. O'Donnell, David B. Papworth, Paul K. Rodman, Proceedings of the 2nd Int'l Conf. on Architectural Support for Programming Languages and Operating Systems, Oct. 1987, Palo Alto CA

Fast Object-Oriented Procedure Calls: Lessons From the Intel 432, Edward F. Gehringer, Robert P. Colwell, ISCA 13, June 1986, pp. 92-101

The Performance Effects of Architectural Complexity in the Intel 432, Robert P. Colwell, Edward F. Gehringer, E. Douglas Jensen, ACM Transactions on Computer Systems, Aug. 1988, V. 6, N. 3

A Display Architecture for Driving Two Different Bitmapped Displays from One Frame Buffer, Robert P. Colwell, 1st Int'l Conference on Computer Workstations, San Jose CA, November 1985

Computers, Complexity, and Controversy, R.P. Colwell, C.Y. Hitchcock III, E.D. Jensen, H.M. Brinkley Sprunt, C.P. Kollar, IEEE Computer, September, 1985, pp. 8-19

The Performance Effects of Function Migration and Architectural Complexity in Object-Oriented Systems, Robert P. Colwell, PhD thesis, Carnegie-Mellon University, Pittsburgh, PA, August 1985

Peering Through The RISC/CISC Fog: An Outline Of Research, Computer Architecture News, Vol. 11, No. 1, March 1983 pp. 44-50

A Perspective on the Processor Complexity Controversy, Proceedings of the International Conference on Computer Design, 1983, pp. 613-616

LECTURES AND INVITED TALKS

P6: Myths and Pipelined Realities, MP Forum '95 in Santa Clara

Evolution of Slot 1 and Slot 2, MP Forum '97 in Santa Clara

Micro '30 keynote speaker, 1997, San Jose

HPCA2 keynote speaker, Santa Clara, 1996

Talks on computing futures at CMU and Oregon Graduate Institute, Intel's Design Test and Technology Conference 1997-1998 (best presentation DTTC), invited keynote DTTC '04

LCPC (Languages and Compilers for Parallel Computing) keynote speaker, San Jose 1996

Intel Research Forum invited speaker, Hillsboro '96, Santa Clara '99

Intel Distinguished Lecture Series talks on the Pentium Pro at BYU, MIT, UCB, Stanford, CMU, Illinois, Wisconsin, Univ of Washington, OGI, UCLA

Distinguished Lectures: UC Davis May 2003; Carnegie-Mellon Univ Nov. 2003; USC April 2004

Microprocessor Report dinner speaker on Pentium Pro, March '95

Neural Networks for Computing Conference, Snowbird Utah, April 1994

IEEE Winter VLSI Workshop 1995

DARPA Winter PI conference, Pasadena CA, January 1994

International Applications Conference, San Diego CA, June 1994

Nature's Paradigm and the Challenge of Validation, Intel Validation Summit 1998, invited talk

Validation Lessons From Elsewhere, Intel Validation Summit 1999, invited talk

ISCA keynote, Anchorage Alaska, June 2002

ECE380 Seminar invited talk, Stanford Univ. February 2004

Invited speaker, Technology Management Lecture Series, PSU May 2004

Invited speaker, CSE Division Wide Seminar, University of Michigan, January 2005

Invited keynote speaker, IEEE Int'l Symp. on Async Circuits and Systems, NYC, March 2005

Invited speaker, IEEE Management Series, Portland OR, April 2005

Eckert-Mauchly Award acceptance speech, ISCA, Madison Wisconsin, June 2005

Invited keynote, International Multiconference on Computer Science and Computer Engineering, Las Vegas NV, June 2005

Invited speaker: Google, Sun Labs, Portland State University 2005

Invited speaker: Cadence, Carnegie-Mellon Univ. CS, Univ. of Rochester, Walla Walla College 2006

Invited keynote, PICMET, Portland Oregon, August 2005

Distinguished lecture, Univ. of Utah, March 2006

Invited speaker: Computer Science Symposium, St. Petersburg, Russia 2006

Invited speaker, IEEE-CS 60th anniversary meeting, Santiago Chile, San Diego CA 2006

Invited speaker, National Academies "Distinguished Voices" lecture series, April 2007, Irvine CA

Invited speaker, FCRC "Future Of Computer Architecture 2007", June, San Diego CA

Invited keynote speaker, ASAP 2007 conference, July, Montreal Canada 2007

Invited speaker, UC Irvine, "How To Be a Successful Engineer", Feb. 2008

Invited speaker, US Naval Workshop on Ship Design, Williamsburg, VA May 2008

Invited speaker, DARPA DSRC summer session, Santa Cruz CA July 2008

Distinguished Hopeman Lecture, Grove City College, April 2009

Many invited talks as DARPA MTO spokesperson on the end of Moore's Law 2011-2014

Invited speaker, Microsoft Research 20th Anniversary Symposium, Sept. 2011

Invited speaker, Computer Science and Telecommunications Board (CSTB), Sept. 2011

Invited speaker, Secretary of Defense Corporate Fellows, July 2012, 2013

Invited speaker after-dinner talk, Salishan Conference on High Performance Computing, April 2013

Invited speaker, Industrial Physics Forum, Baltimore MD, March 2013

Invited speaker, Computing Community Consortium (CCC), Pgh PA, March 2013

Invited speaker, National Defense University College, Wash. DC, May 2013

Invited speaker, Design Automation Conference, Austin TX, June 2013

Invited keynote, Hot Chips Conference, Stanford, August 2013

Invited speaker, Gov't Forum on Moore's Law, Wash. DC, November 2013

Invited talks at UT Austin, seminar & computer architecture lecture, November 2013

Invited speaker, Rebooting Computing, Wash. DC, December 2013

Invited speaker, Dartmouth College, January 2014

Invited speaker, MIT Annual Research Conference (MARC), January 2014

Invited speaker, Virginia Tech Univ., February 2014

Invited speaker, Univ. of Rochester, March 2014

Invited speaker, IEEE Technology Time Machine conf, October 2014

Invited speaker, DARPA HAPTIX kickoff meeting, Arlington VA, Nov. 2014

Invited speaker, CSTB Continuing Innovation in IT workshop, Washington DC, Mar. 2015

Invited keynote, Stanford SystemX "Headlights" Workshop, April 2015

Invited keynote, Berkeley Energy Efficient Electronics Systems Symposium, Oct. 2015

Invited speaker, University of Washington, Nov. 2015

PANEL SESSIONS

DAC '91 panel session panelist; DAC '92 CAD tools workshop instructor

ICCD '91 moderator/organizer of panel session, San Jose CA

ICCAD-94, panel session panelist, November 1994, San Jose CA

Micro 26 '93, moderator/organizer of panel session, Portland OR

ISCA workshop talk, Santa Margerita Ligure, Italy 1995, panelist Phila. PA 1996

PAID 97 Workshop talk on "accidental performance decisions" with Dave Papworth

FPGA panel session panelist, November 1996, Monterey CA

ASPLOS-VII panel session panelist, October 1998, San Jose CA

DOCKET ALARM

Explore Litigation Insights

Docket Alarm provides insights to develop a more informed litigation strategy and the peace of mind of knowing you're on top of things.

Real-Time Litigation Alerts

Keep your litigation team up-to-date with **real-time alerts** and advanced team management tools built for the enterprise, all while greatly reducing PACER spend.

Our comprehensive service means we can handle Federal, State, and Administrative courts across the country.

Advanced Docket Research

With over 230 million records, Docket Alarm's cloud-native docket research platform finds what other services can't. Coverage includes Federal, State, plus PTAB, TTAB, ITC and NLRB decisions, all in one place.

Identify arguments that have been successful in the past with full text, pinpoint searching. Link to case law cited within any court document via Fastcase.

Analytics At Your Fingertips

Learn what happened the last time a particular judge, opposing counsel or company faced cases similar to yours.

Advanced out-of-the-box PTAB and TTAB analytics are always at your fingertips.

API

Docket Alarm offers a powerful API (application programming interface) to developers that want to integrate case filings into their apps.

LAW FIRMS
Build custom dashboards for your attorneys and clients with live data direct from the court.

Automate many repetitive legal tasks like conflict checks, document management, and marketing.

FINANCIAL INSTITUTIONS
Litigation and bankruptcy checks for companies and debtors.

E-DISCOVERY AND LEGAL VENDORS
Sync your system to PACER to automate legal marketing.