



[54] **MESSAGING PERIPHERAL WITH SECURE MESSAGE DATA FUNCTION**

[75] Inventors: **William J. Macko**, West Palm Beach; **Greg Cannon**, Delray Beach, both of Fla.

[73] Assignee: **Motorola, Inc.**, Schaumburg, Ill.

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[52] U.S. Cl. **340/825.44**; 340/825.27; 340/825.34

[58] Field of Search 340/825.44, 825.34, 340/825.31, 825.27, 311.1; 379/59

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Primary Examiner—Donald J. Yusko

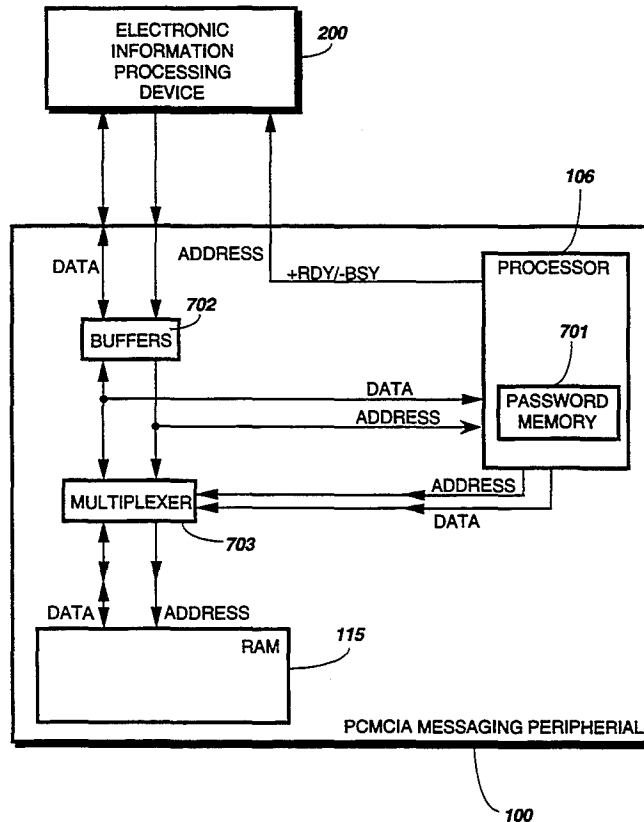
Assistant Examiner—Mark H. Rinehart

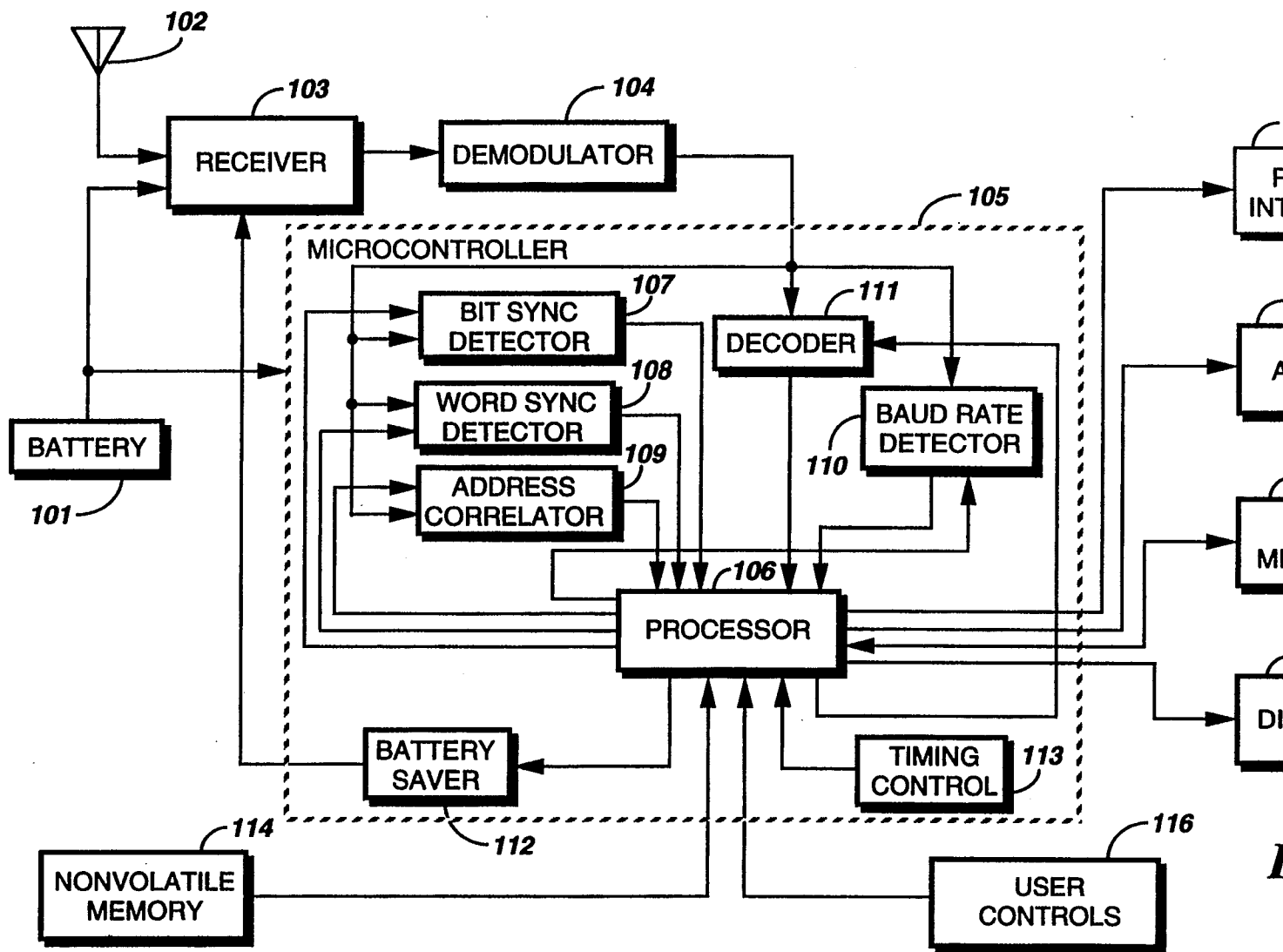
Attorney, Agent, or Firm—Gregg E. Rasor

[57] **ABSTRACT**

A messaging peripheral (100) includes a processor (106) for executing a microcode program that controls operation of the messaging peripheral (100), and a PCMCIA memory only interface (119) that allows communication of communication of at least one message and a user selectable password between an electronic information processing device (200) and the messaging peripheral (100). The PCMCIA memory only interface couples to a secure memory access interface that is controlled by the processor (106). The secure memory access interface (703) allows the electronic information processing device (200) to access the at least one message when a memory protection mode is selected and the processor (106) receives a user entered password and performs a correlation between the user entered password and the user selectable password.

18 Claims, 8 Drawing Sheets





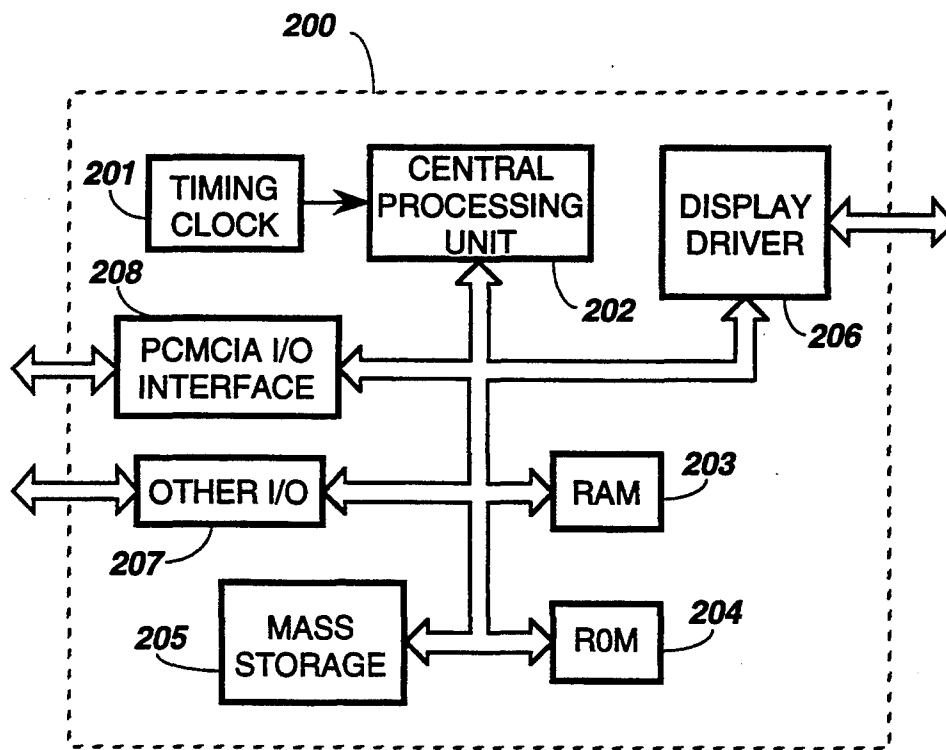


FIG. 2

Pin	Signal	I/O	Function	+/-
1	GND		Ground	
2	D3	I/O	Data bit 3	
3	D4	I/O	Data bit 4	
4	D5	I/O	Data bit 5	
5	D6	I/O	Data bit 6	
6	D7	I/O	Data bit 7	
7	CE1	I	Card enable	-
8	A10	I	Address bit 10	
9	OE	I	Output enable	-
10	A11	I	Address bit 11	
11	A9	I	Address bit 9	
12	A8	I	Address bit 8	
13	A13	I	Address bit 13	
14	A14	I	Address bit 14	
15	WE/PGM	I	Write enable	-
16	RDY/BSY	O	Ready/Busy	+/-
17	Vcc		Power Supply	
18	Vpp1		Programming and Peripheral Supply	
19	A16	I	Address bit 16	
20	A15	I	Address bit 15	
21	A12	I	Address bit 12	
22	A7	I	Address bit 7	
23	A6	I	Address bit 6	
24	A5	I	Address bit 5	
25	A4	I	Address bit 4	
26	A3	I	Address bit 3	
27	A2	I	Address bit 2	
28	A1	I	Address bit 1	
29	A0	I	Address bit 0	
30	D0	I/O	Data bit 0	
31	D1	I/O	Data bit 1	
32	D2	I/O	Data bit 2	
33	WP	O	Write protect	-
34	GND		Ground	

FIG 3

Pin	Signal	I/O	Function	+/-
35	GND		Ground	
36	CD1	O	Card Detect	-
37	D11	I/O	Data bit 11	
38	D12	I/O	Data bit 12	
39	D13	I/O	Data bit 13	
40	D14	I/O	Data bit 14	
41	D15	I/O	Data bit 15	
42	CE2	I	Card enable	-
43	RFSH	I	Refresh	
44	RFU		Reserved	
45	RFU		Reserved	
46	A17	I	Address bit 17	
47	A18	I	Address bit 18	
48	A19	I	Address bit 19	
49	A20	I	Address bit 20	
50	A21	I	Address bit 21	
51	Vcc		Power Supply	
52	Vpp2		Programming and Peripheral Supply 2	
53	A22	I	Address bit 22	
54	A23	I	Address bit 23	
55	A24	I	Address bit 24	
56	A25	I	Address bit 25	
57	RFU		Reserved	
58	RESET	I	Card Reset	+
59	WAIT	O	Extend bus cycle	-
60	RFU		Reserved	-
61	REG	I	Register select	-
62	BVD2	O	Battery voltage detect 2	
63	BVD1	O	Battery voltage detect 1	
64	D8	I/O	Data bit 8	
65	D9	I/O	Data bit 9	
66	D10	I/O	Data bit 10	
67	CD2	O	Card detect	-
68	GND		Ground	

FIG. 4

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