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Paper 42
Entered: April 21, 2016

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

HUGHES NETWORK SYSTEMS, LLC and
HUGHES COMMUNICATIONS, INC.,
Petitioner,

v.

CALIFORNIA INSTITUTE OF TECHNOLOGY,
Patent Owner.

Case IPR2015-00059
Patent 7,916,781 B2

Before KALYAN K. DESHPANDE, GLENN J. PERRY, and
TREVOR M. JEFFERSON, *Administrative Patent Judges*.

PERRY, *Administrative Patent Judge.*

FINAL WRITTEN DECISION
Inter Partes Review
35 U.S.C. § 318(a) and 37 C.F.R. § 42.73

I. INTRODUCTION

A. Procedural History

Hughes Network Systems, LLC and Hughes Communications, Inc.[1] (collectively "Petitioner" or "Hughes") filed a Petition requesting an *inter partes* review of claims 1–7, 13–16, and 19 of U.S. Patent No. 7,916,781 B2 (Ex. 1005, "the '781 Patent"). Paper 4 ("Pet.").[2] California Institute of Technology ("Patent Owner" or "CIT") timely filed a Preliminary Response. Paper 13 ("Prelim. Resp."). We instituted trial as to claims 1 and 2 of the '781 Patent as being anticipated by Divsalar[3] and did not authorize trial as to the other grounds of unpatentability alleged in the Petition. Paper 18 ("Dec."). Following institution of trial, Patent Owner filed its formal response. Paper 24 ("PO Resp."). Petitioner replied. Paper 29 ("Pet. Reply"). Patent Owner moved to "strike" and to "exclude" various Petitioner exhibits. Paper 32 ("Mot."). Petitioner opposed. Paper 35 ("Mot. Opp."). We heard oral argument on February 10, 2016. Paper 39 ("Tr.").

B. Related Proceedings

Petitioner states that the '781 Patent is involved in a pending lawsuit titled *California Institute of Technology v. Hughes Communications, Inc.*, No. 13-CV-07245 (C.D. Cal.). Pet. 1 (citing Ex. 1015). In that lawsuit the following patents are asserted: (i) U.S. Patent No. 7,116,710; (ii) U.S. Patent No. 7,421,032; (iii) U.S. Patent No. 7,916,781; and (iv) U.S. Patent

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[1] EchoStar Corporation is named in the Petition as the parent of Hughes Satellite Systems Corporation, which is the parent of Hughes Communications, Inc. Pet. 1.

[2] "Pet." refers to the corrected Petition filed October 30, 2014 (Paper 4).

[3] Dariush Divsalar, et al., *Coding Theorems for "Turbo-Like" Codes*, THIRTY-SIXTH ANNUAL ALLERTON CONFERENCE ON COMMUNICATION, CONTROL, AND COMPUTING 201–209 (1998) (Ex. 1011, "Divsalar").

No. 8,284,833. Petitioner has filed additional Petitions for *inter partes* review challenging other patents of the patent family. Pet. 1.

C. The '781 Patent

1. Background and Context

Error correcting codes are used to communicate information across a noisy communication channel. They enable recovery of a transmitted message that may have become distorted by noise on the communication channel. To error correction encode a message for transmission, its bits are parsed into groups of message bits that are "encoded" into "codewords" that include additional redundant information.[4] Thus, the encoded codewords have more information than the original message had prior to encoding. The codewords are transmitted over the communication channel and are received at another location, where the codewords are "decoded" into the original message. No single coding scheme is optimal for all communication channels. There are design tradeoffs between the use of complex codes, which permit better error correction, and less complex codes, which are easier to decode. This has led to the development of many different encoding/decoding schemes. The '781 Patent describes one such scheme.

2. Disclosed Invention

The '781 Patent describes the serial concatenation of interleaved convolutional codes forming turbo-like codes. Ex. 1005, Title. It explains some of the prior art with reference to its Figure 1, reproduced below.

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[4] For example, message bits "10011" may be encoded into a codeword "100111" by adding a "parity" bit "1" to the original message.

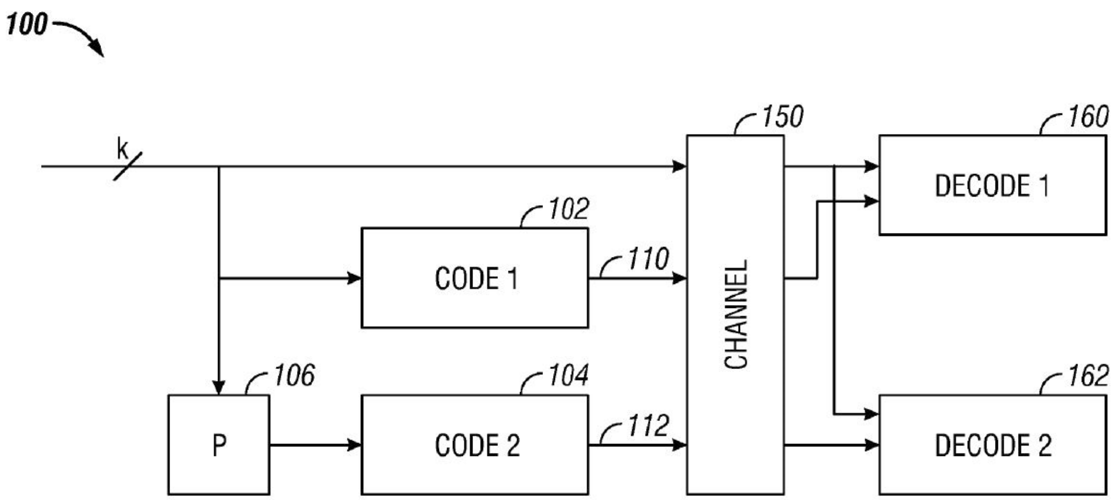

FIG. 1
(Prior Art)

Figure 1 is a schematic diagram of a prior "turbo code" system. Ex. 1005, 2:20–21. The '781 Patent specification describes Figure 1 as follows:

> A block of k information bits is input directly to a first coder 102. A k bit interleaver 106 also receives the k bits and interleaves them prior to applying them to a second coder 104. The second coder produces an output that has more bits than its input, that is, it is a coder with rate that is less than 1. The coders 102, 104 are typically recursive convolutional coders.
>
> Three different items are sent over the channel 150: the original k bits, first encoded bits 110, and second encoded bits 112. At the decoding end, two decoders are used: a first constituent decoder 160 and a second constituent decoder 162. Each receives both the original k bits, and one of the encoded portions 110, 112. Each decoder sends likelihood estimates of the decoded bits to the other decoders. The estimates are used to decode the uncoded information bits as corrupted by the noisy channel.

Ex. 1005, 1:44–60.

A coder 200, according to a first embodiment of the invention, is described with respect to Figure 2, reproduced below.

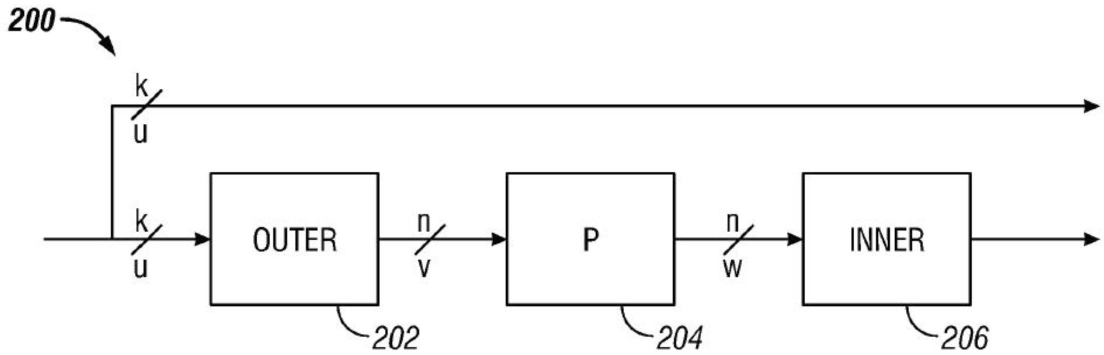

FIG. 2

Figure 2 of the ’781 Patent is a schematic diagram of coder 200.

> The coder 200 may include an outer coder 202, an interleaver 204, and inner coder 206. . . . The outer coder 202 receives the uncoded data [that] may be partitioned into blocks of fixed size, [e.g.] k bits. The outer coder may be an (n,k) binary linear block coder, where n>k. The coder accepts as input a block u of k data bits and produces an output block v of n data bits. The mathematical relationship between u and v is $v=T_0u$, where T_0 is an nxk matrix, and the rate[5] of the coder is k/n.
>
> The rate of the coder may be irregular, that is, the value of T_0 is not constant, and may differ for sub-blocks of bits in the data block. In an embodiment, the outer coder 202 is a repeater that repeats the k bits in a block a number of times q to produce a block with n bits, where n=qk. Since the repeater has an irregular output, different bits in the block may be repeated a different number of times. For example, a fraction of the bits in the block may be repeated two times, a fraction of bits may be repeated three times, and the remainder of bits may be repeated four times. These fractions define a degree sequence or degree profile, of the code.
>
> The inner coder 206 may be a linear rate-1 coder, which means that the n-bit output block x can be written as $x=T_Iw$, where T_I is a nonsingular n x n matrix. The inner coder 210 can have a

[5] We understand that the “rate” of an encoder refers to the ratio of the number of input bits to the number of resulting encoded output bits related to those input bits.

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