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Ikehashi et al.

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(54) **SEMICONDUCTOR MEMORY DEVICE WITH TEST MODE**

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(51) **Int. Cl.**[7] **G11C 16/06**
(52) **U.S. Cl.** **365/185.22**; 365/185.09; 365/189.12; 365/200
(58) **Field of Search** 365/200, 201, 365/230.03, 230.06, 221, 189.02, 189.05, 189.12, 185.22, 185.19, 185.09; 714/710, 711, 718, 42

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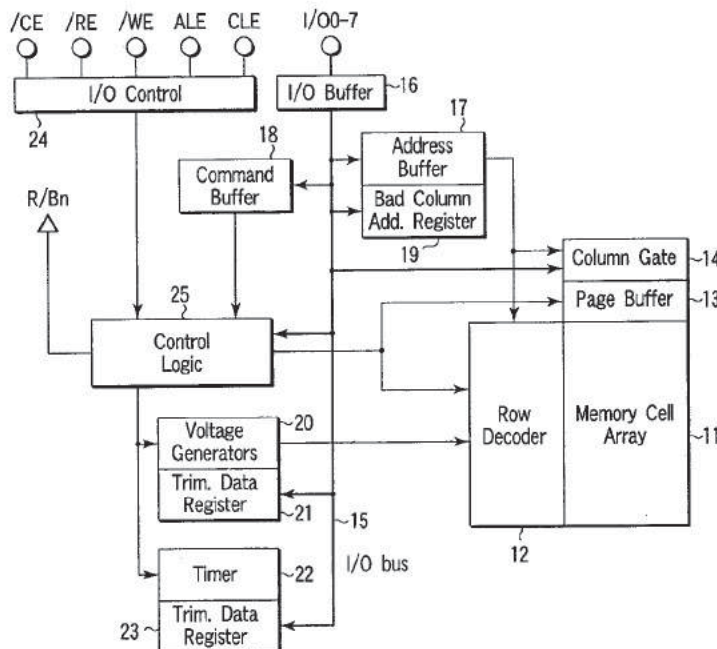* cited by examiner

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(57) **ABSTRACT**

In a method of testing a nonvolatile semiconductor memory integrated on a semiconductor chip comprising a memory cell array, a first register that stores an address of a defective region in the memory cell array, a plurality of internal voltage generator circuits, and a second register, the second register storing a trimming value for setting an internal voltage value generated by each of the internal voltage generator circuits, the testing method carries out resetting the address of the defective region stored in the first register and the trimming value stored in the second register, and setting the address of the defective region stored in the first register and the trimming value stored in the second register to a value according to a property of each of the semiconductor chips, wherein the testing is carried out without turning a power supply off after the power supply has been turned on.

7 Claims, 23 Drawing Sheets

/CE   /RE   /WE   ALE   CLE   I/O0-7

I/O Control   ~24

I/O Buffer   ~16

17

Command Buffer   18

Address Buffer

Bad Column Add. Register

19

R/Bn

Column Gate   ~14

Page Buffer   ~13

25

Control Logic

Voltage Generators   ~20

Trim. Data Register   ~21

~15

Row Decoder

Memory Cell Array   ~11

12

Timer   ~22

Trim. Data Register

23 ~

I/O bus

FIG. 1

BL   BL   BL

11

WL0
WL1
WL2

B0

WL14
WL15

WL15
WL14

B1

WL1
WL0

WL15
WL14

B2

WL1
WL0

WL0
WL1

Bn

WL14
WL15

FIG.2

Wafer Test Sequence

```
┌─────────────────────────────┐
│          DC Test            │
└─────────────────────────────┘
              │
              ▼
┌─────────────────────────────┐
│        Default Reset        │
└─────────────────────────────┘
              │
              ▼
┌─────────────────────────────┐
│   Timer & Voltage Trimming  │
└─────────────────────────────┘
              │
              ▼
┌─────────────────────────────┐
│   Bad Col. Detect & Repair  │
└─────────────────────────────┘
              │
              ▼
┌─────────────────────────────┐
│      Good Block Search      │
└─────────────────────────────┘
              │
              ▼
┌─────────────────────────────┐
│      Vpgm Initial Value     │
│          Trimming           │
└─────────────────────────────┘
              │
              ▼
┌─────────────────────────────┐
│      Bad Block Detection    │
└─────────────────────────────┘
              │
              ▼
┌─────────────────────────────┐
│          Option Set         │
└─────────────────────────────┘
              │
              ▼
┌─────────────────────────────┐
│       ROM-fuse Program      │
└─────────────────────────────┘
              │
              ▼
┌─────────────────────────────┐
│        Power Off, On        │
│ Verification of Register State │
└─────────────────────────────┘
```
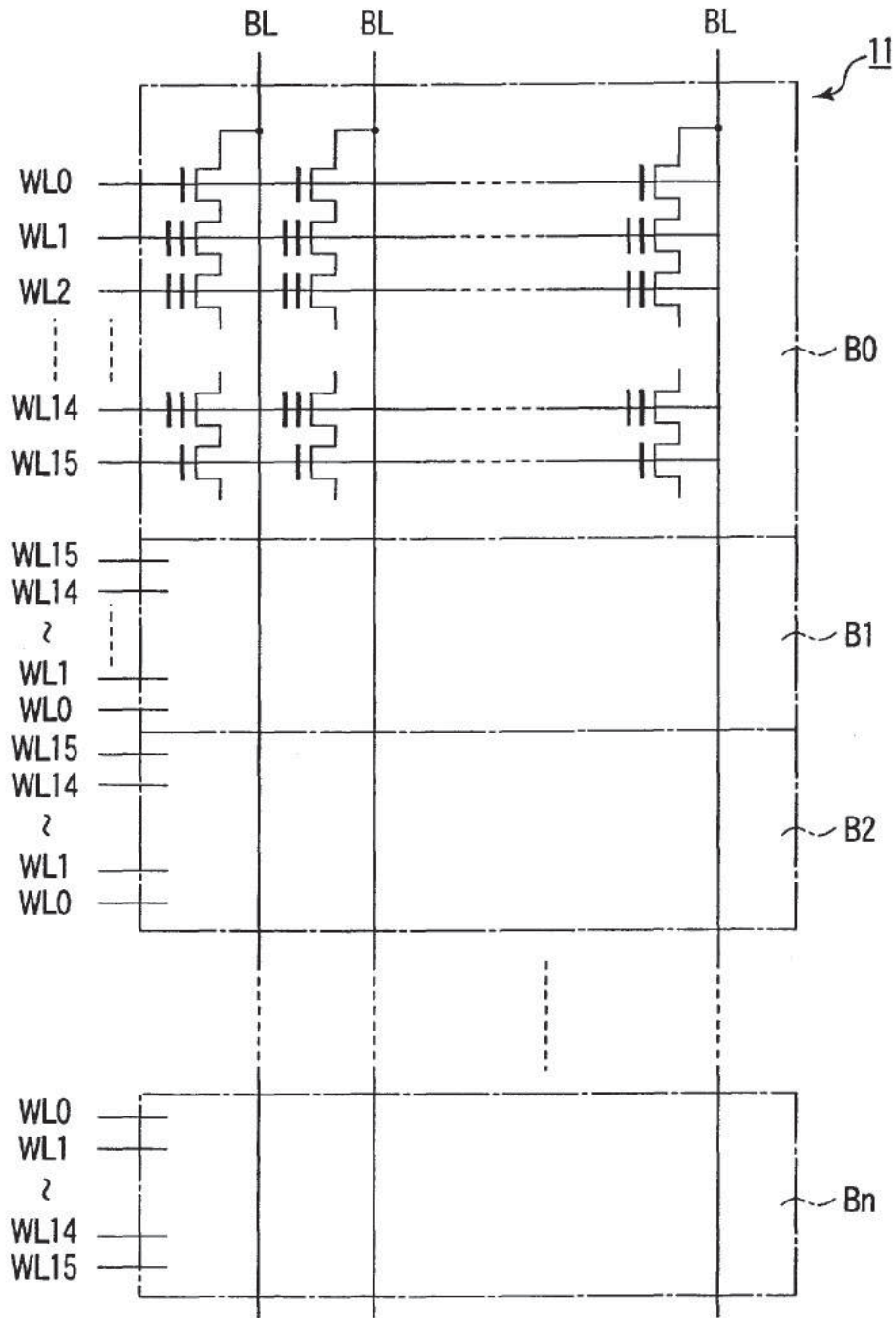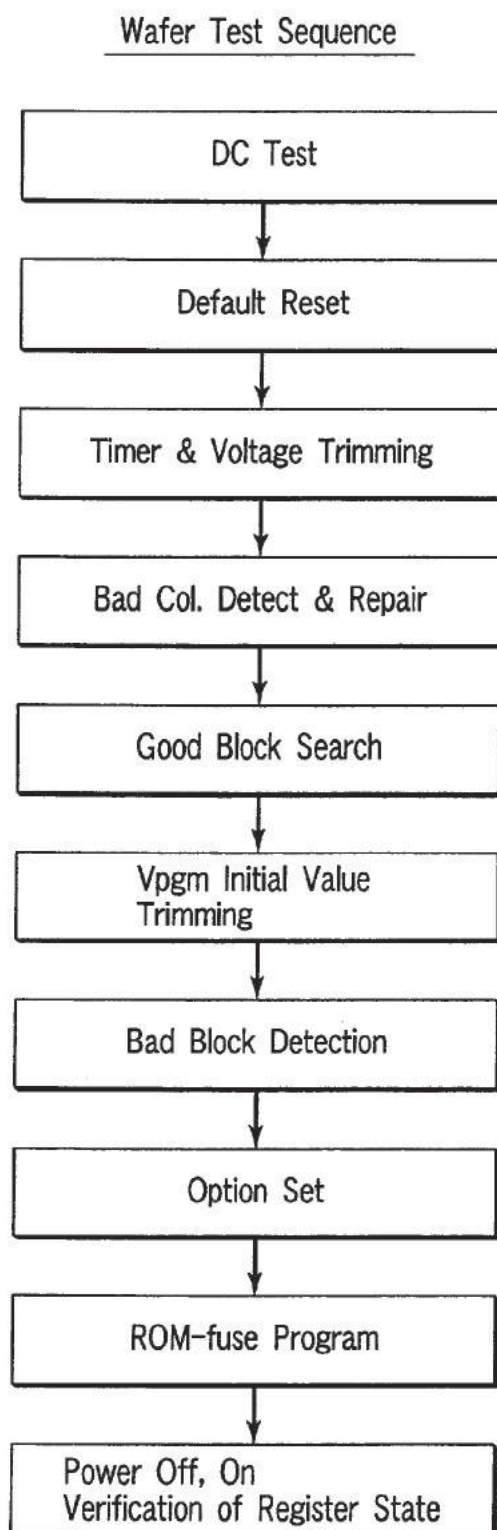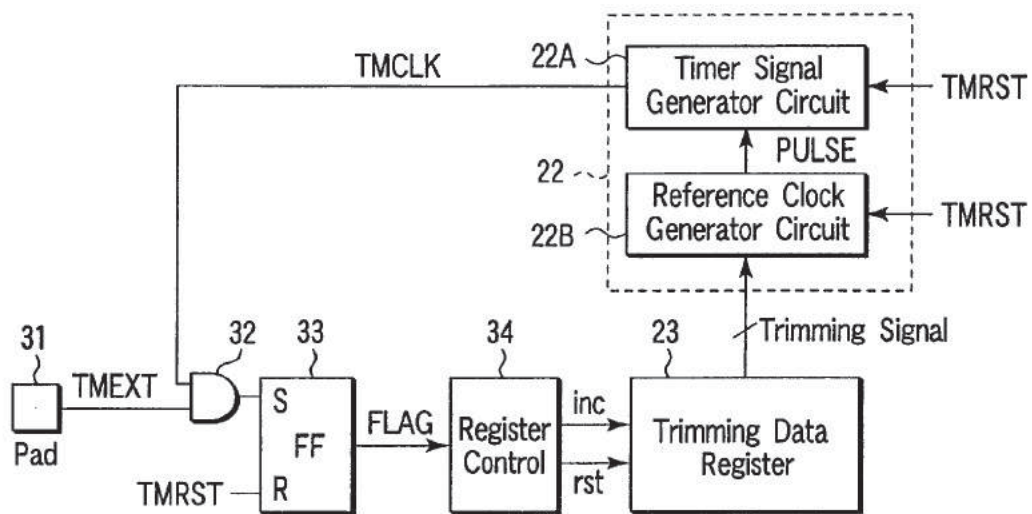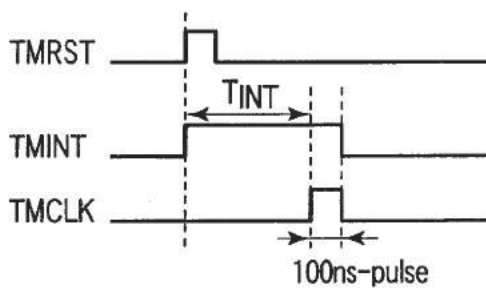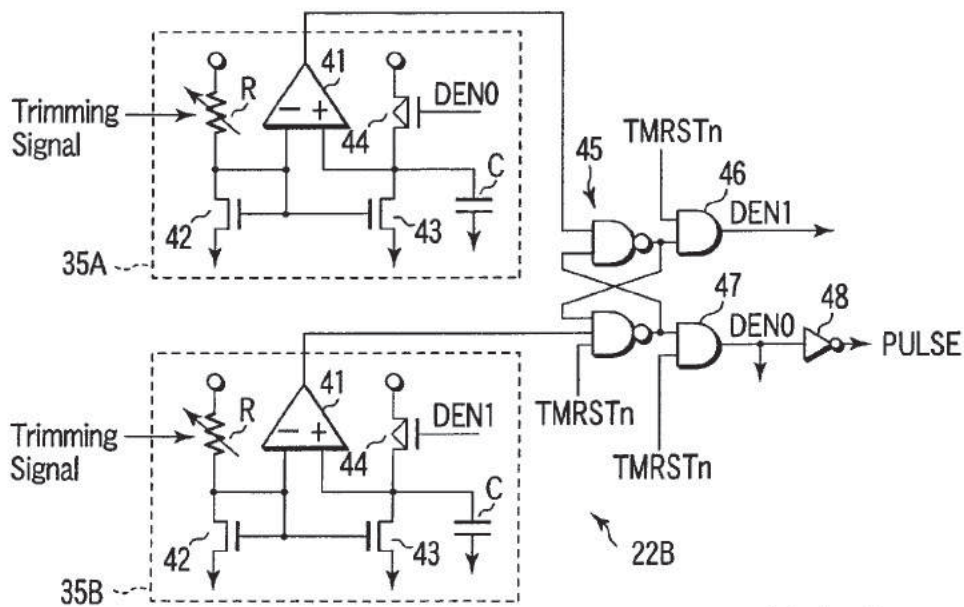
FIG. 3

FIG. 4

FIG. 5

FIG. 6

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