(12) **United States Patent**

Tanaka et al.

(10) Patent No.: **US 7,000,160 B2**

(45) Date of Patent: **Feb. 14, 2006**

(54) **SEMICONDUCTOR INTEGRATED CIRCUIT AND A METHOD OF TESTING THE SAME**

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(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 659 days.

(21) Appl. No.: **10/083,399**

(22) Filed: **Feb. 27, 2002**

(65) **Prior Publication Data**

US 2002/0153917 A1 Oct. 24, 2002

(30) **Foreign Application Priority Data**

Apr. 24, 2001 (JP) 2001-125275

(51) **Int. Cl.**
G01R 31/28 (2006.01)

(52) **U.S. Cl.** **714/724**; 324/765

(58) **Field of Classification Search** 714/724, 714/819; 324/765, 771
See application file for complete search history.

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(57) **ABSTRACT**

A semiconductor integrated circuit (LSI) in which control information for determining a voltage or a width of a pulse produced itself can easily be set in parallel with other LSIs, and set information can be corrected easily. From an external evaluation device, a voltage of an expected value is supplied in overlapping manner to a plurality of LSIs each having a CPU and a flash memory. Each LSI incorporates a comparison circuit comparing an expected voltage value and a boosted voltage generated in itself. The CPU refers to a comparison result and optimizes control data in a data register for changing a boosted voltage. The CPU controls the comparison circuit and the data register and performs trimming in a self-completion manner, thereby making, trimming on a plurality of LSIs easily in a parallel manner and a total test time reduced.
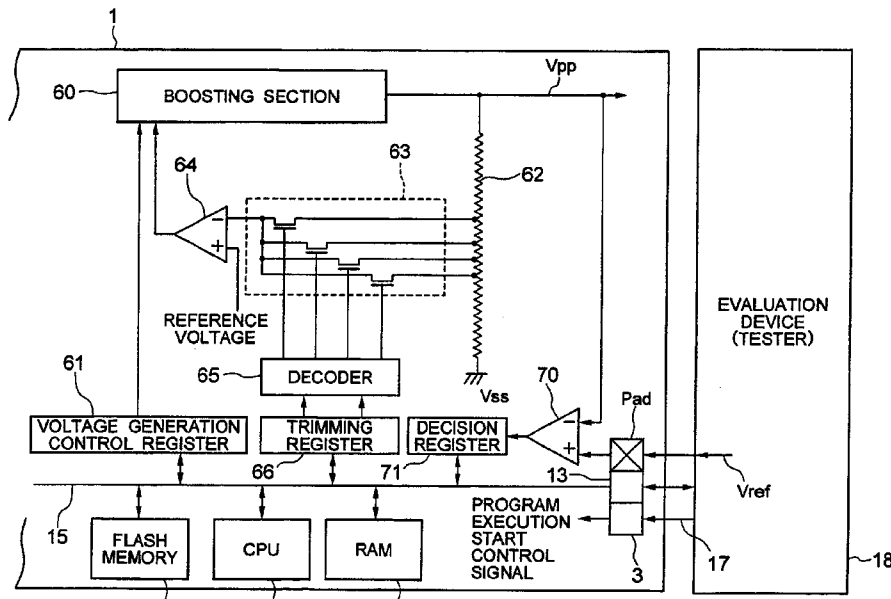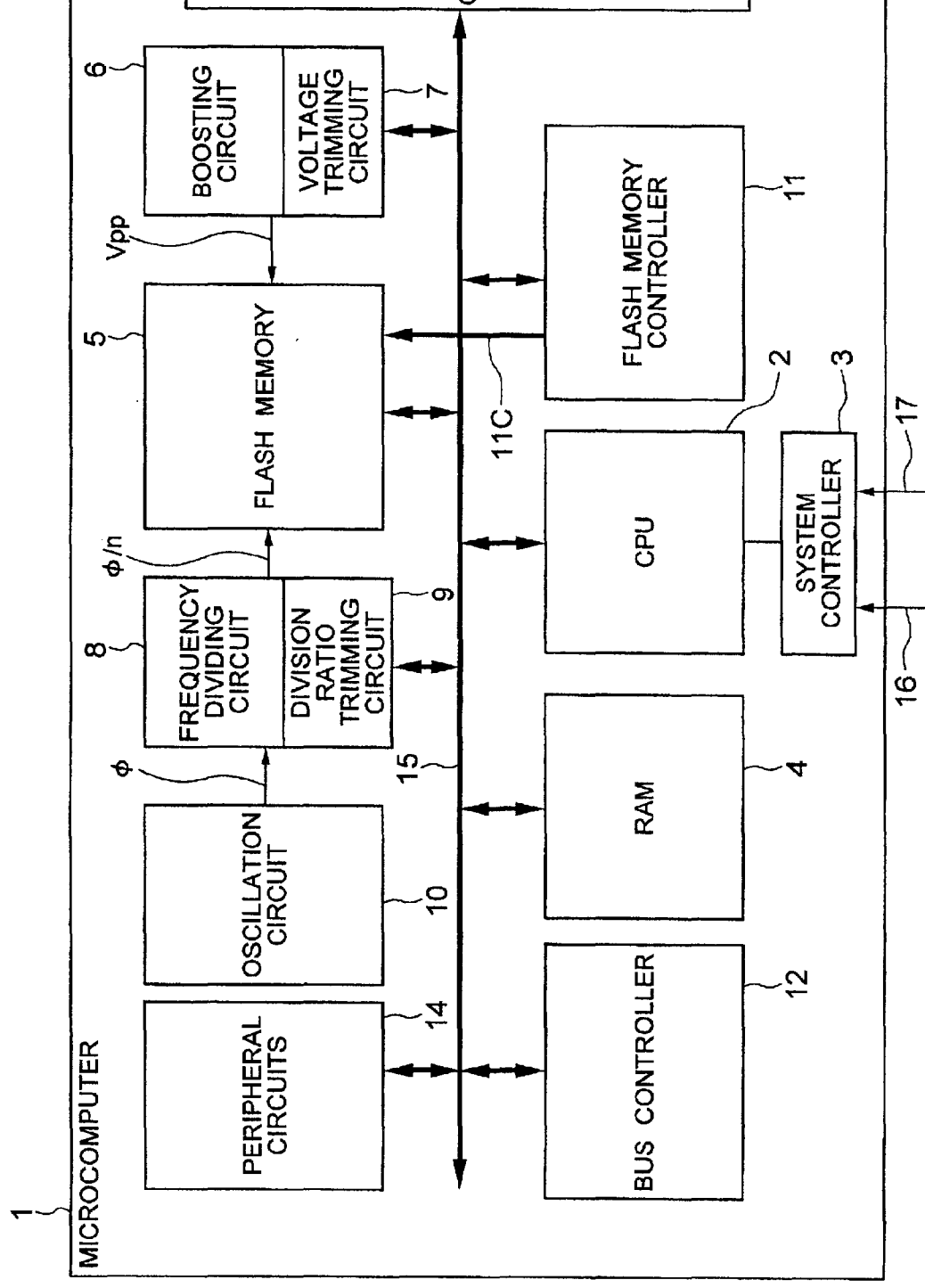
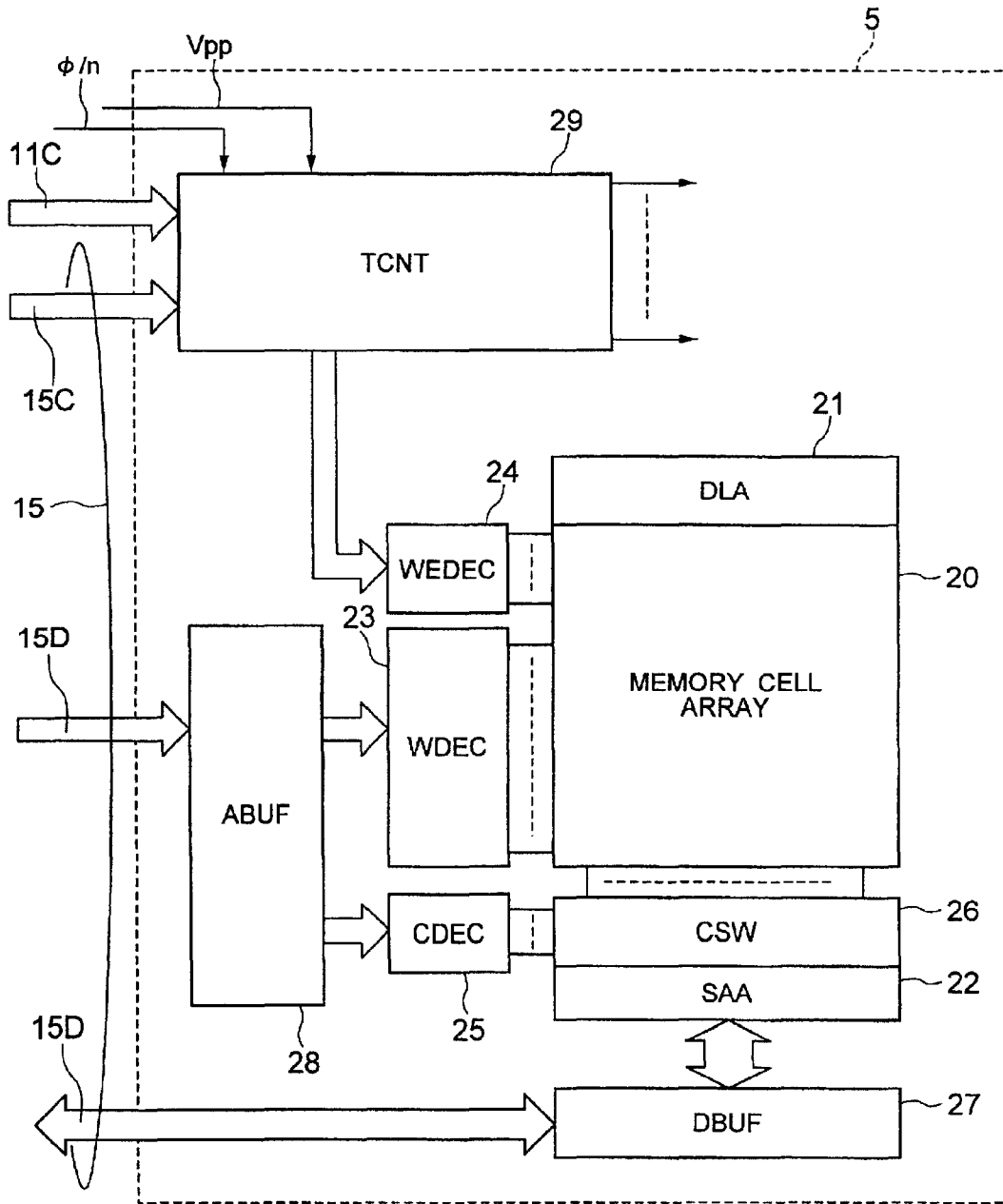**23 Claims, 29 Drawing Sheets**

FIG. 1

MICROCOMPUTER — 1

BOOSTING CIRCUIT — 6

VOLTAGE TRIMMING CIRCUIT — 7

FLASH MEMORY CONTROLLER — 11

FLASH MEMORY — 5

Vpp

11C

CPU — 2

SYSTEM CONTROLLER — 3

17

16

FREQUENCY DIVIDING CIRCUIT — 8

DIVISION RATIO TRIMMING CIRCUIT — 9

φ/n

15

RAM — 4

OSCILLATION CIRCUIT — 10

φ

PERIPHERAL CIRCUITS — 14

BUS CONTROLLER — 12

FIG. 2

FIG. 3

H' 00002008

REPAIR AND
TRIMMING MAT ～ Rmat

H' 00002000

～ Tmat

BOOT MAT

H' 00000000

H' XXXXXXXX
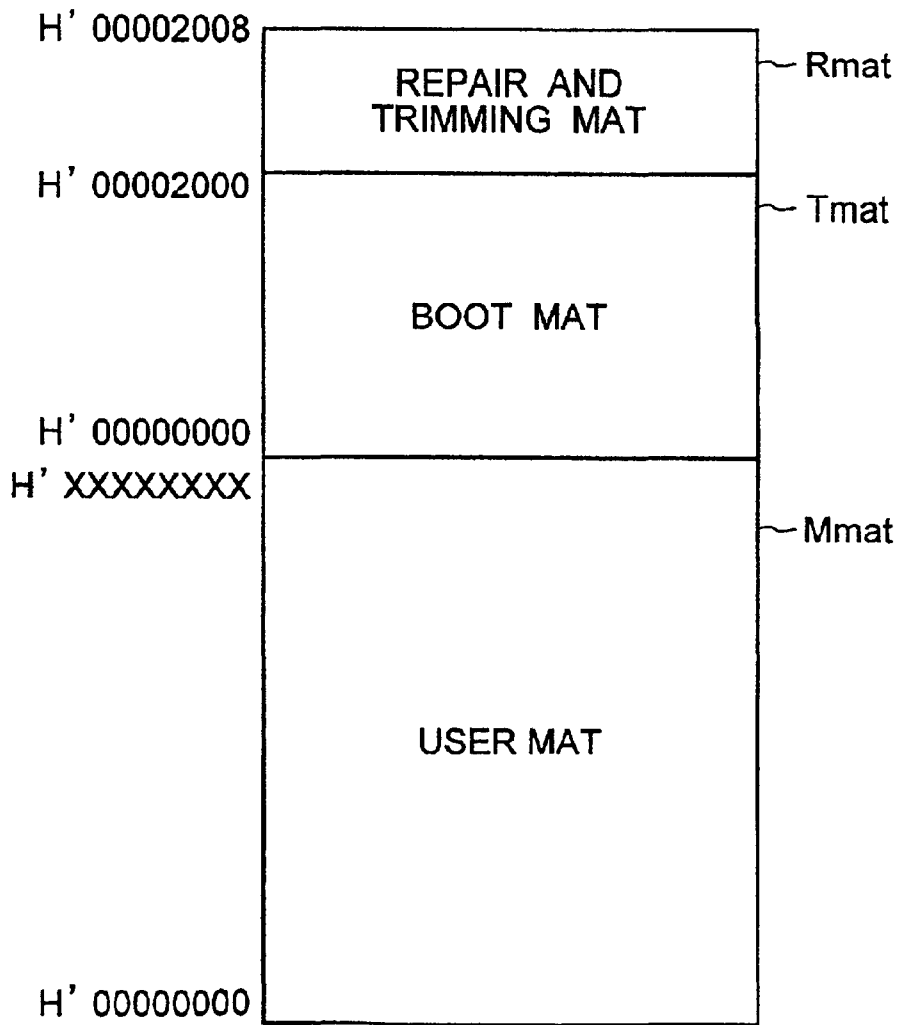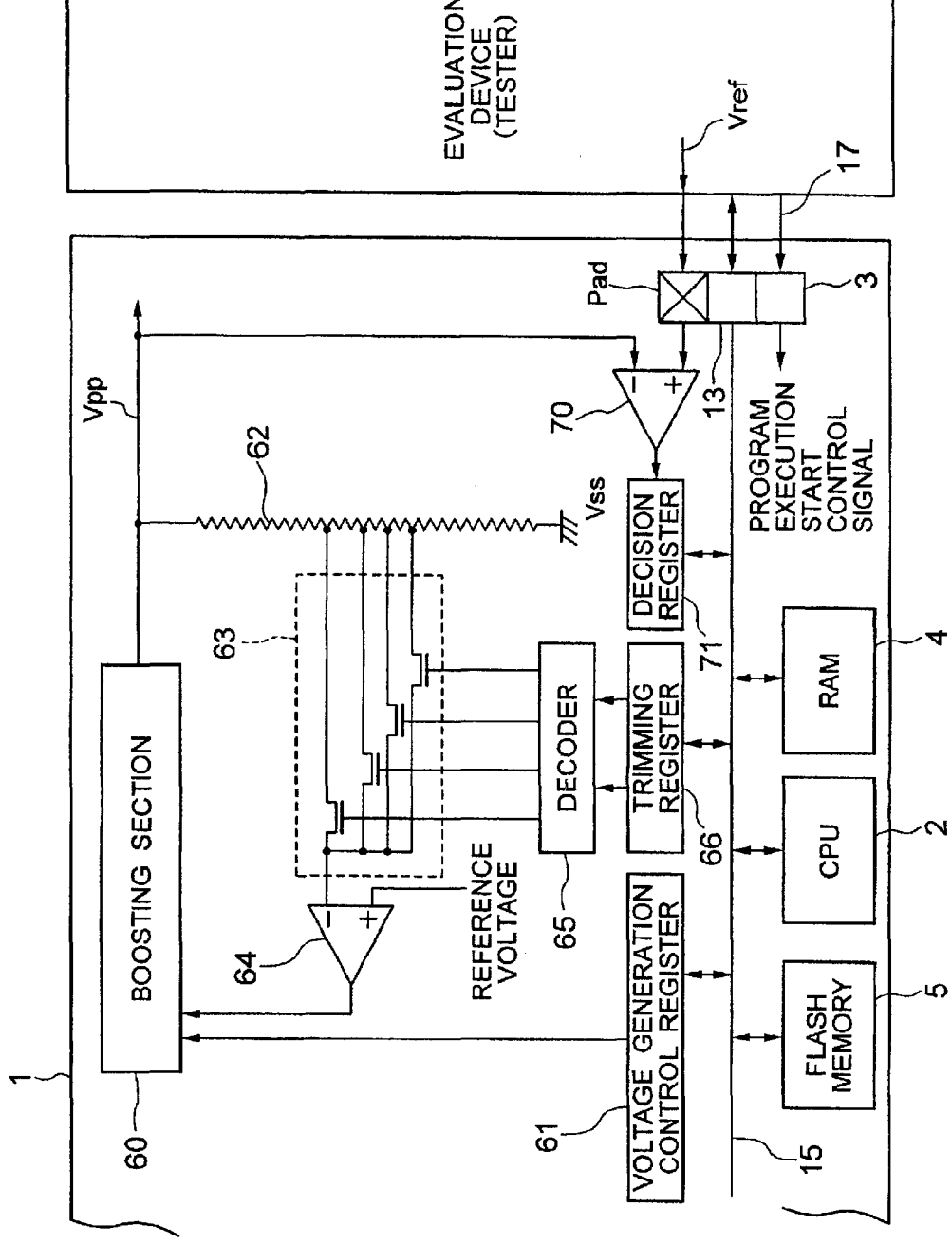
～ Mmat

USER MAT

H' 00000000

FIG. 4

DOCKET ALARM

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