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Hartmann et al.

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(54) **METHOD AND APPARATUS FOR INTERNALLY TRIMMING OUTPUT DRIVERS AND TERMINATIONS IN SEMICONDUCTOR DEVICES**

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G06F 11/00 (2006.01)
G11C 5/00 (2006.01)

(52) **U.S. Cl.** **714/30**; 365/189.09

(58) **Field of Classification Search** 714/30, 714/32, 721; 365/189.09
See application file for complete search history.

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(57) **ABSTRACT**

To trim interface devices on semiconductor devices, such as trimmable output drivers and terminations, a measurement current produced in the test apparatus is impressed onto the interface device, and a measurement voltage produced by the measurement current in the interface device is detected by a trimming unit provided within the semiconductor device and is trimmed using control elements and trimming registers controlled by the trimming unit. To this end, the trimming unit ascertains trimming information which is stored in nonvolatile fashion in a memory unit in the semiconductor device and is loaded into the trimming registers in the semiconductor device whenever the semiconductor device is started up.

20 Claims, 3 Drawing Sheets

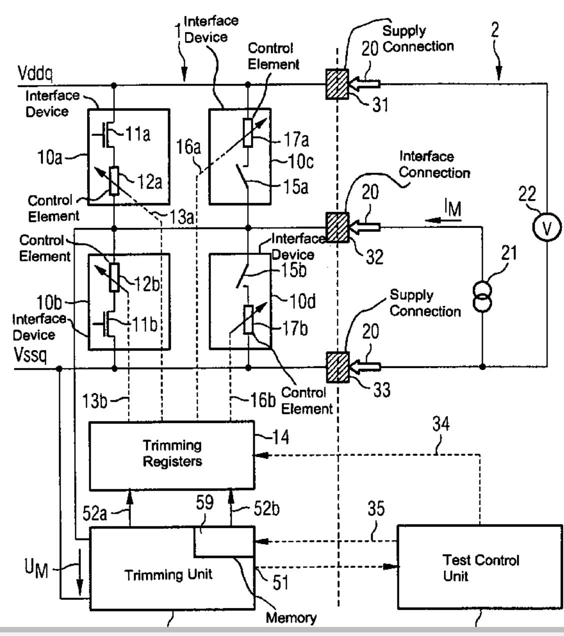


FIG 1
PRIOR ART

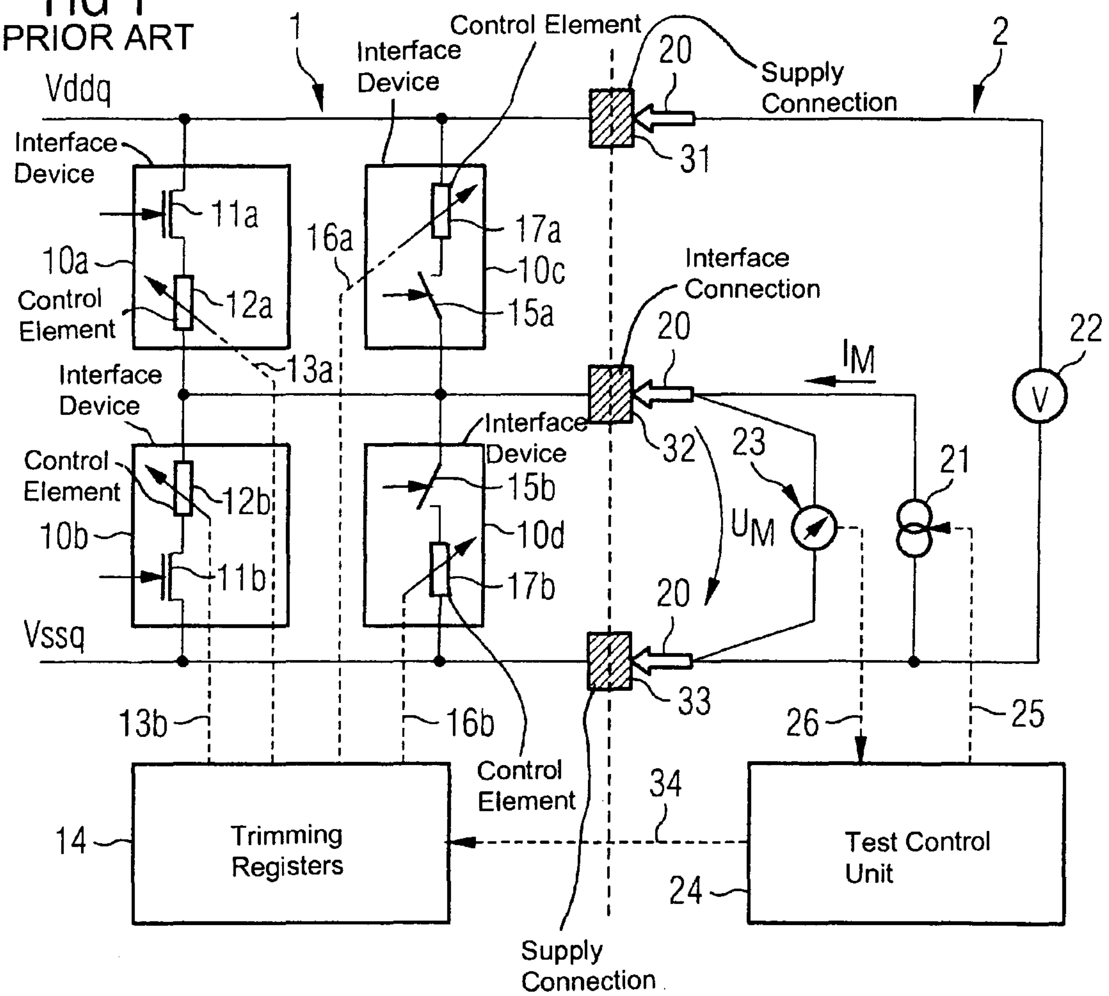


FIG 2
PRIOR ART

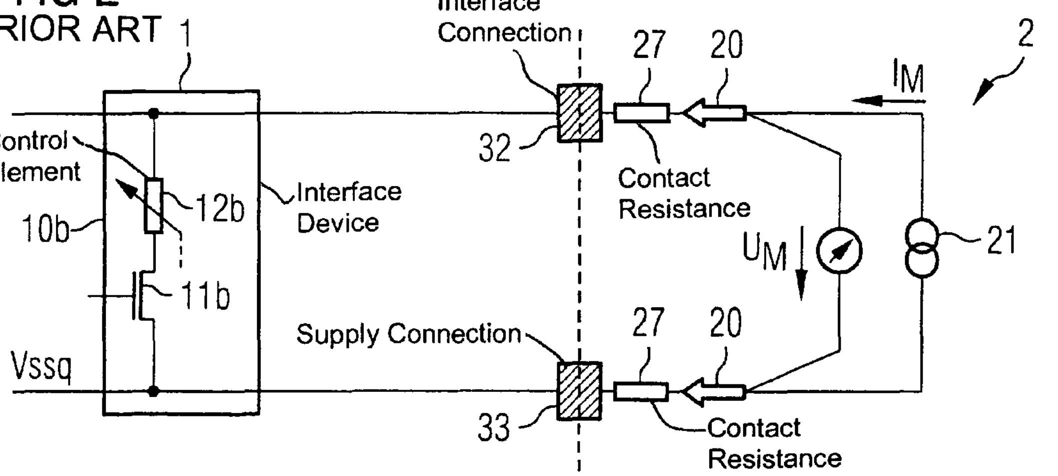
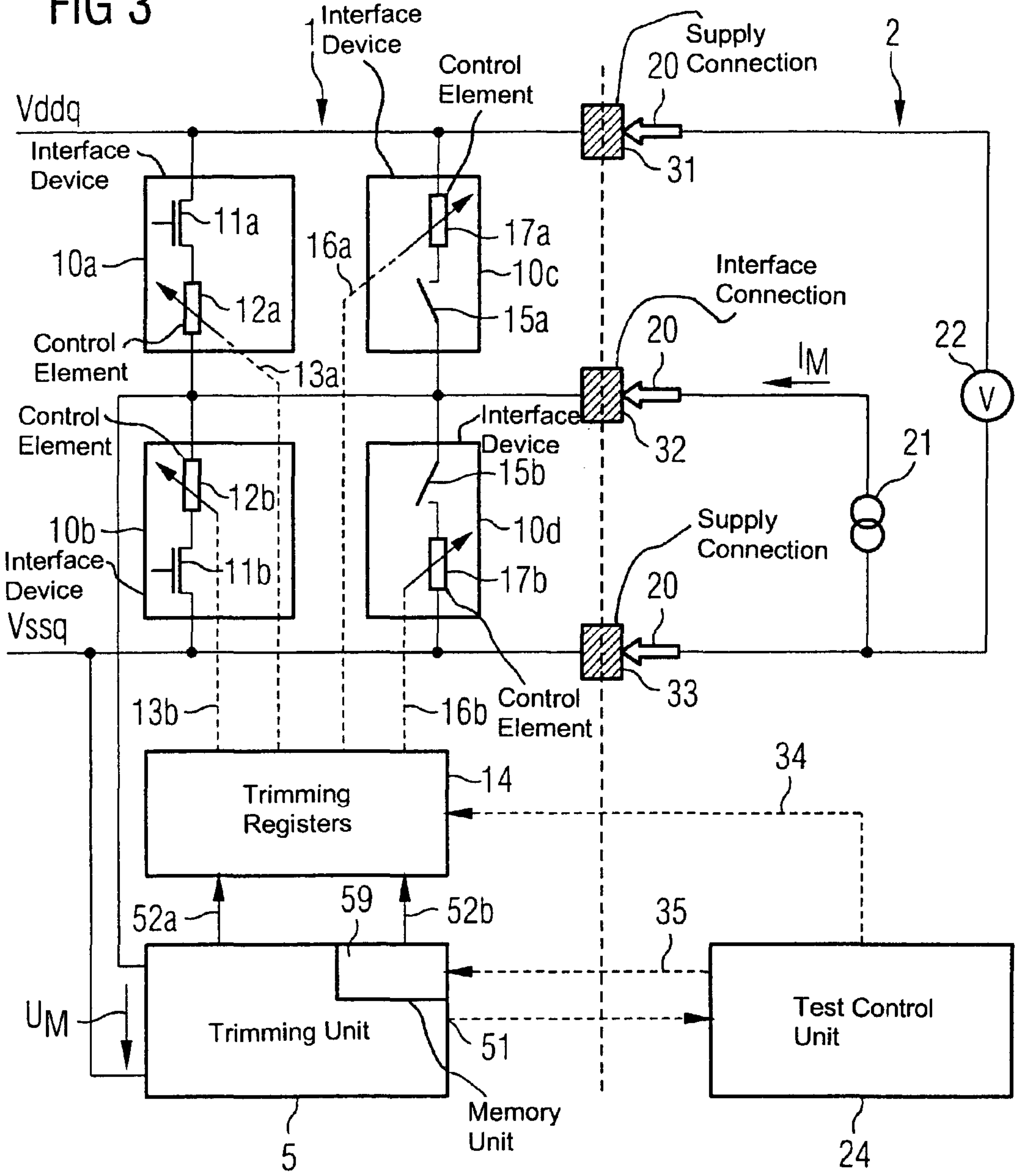
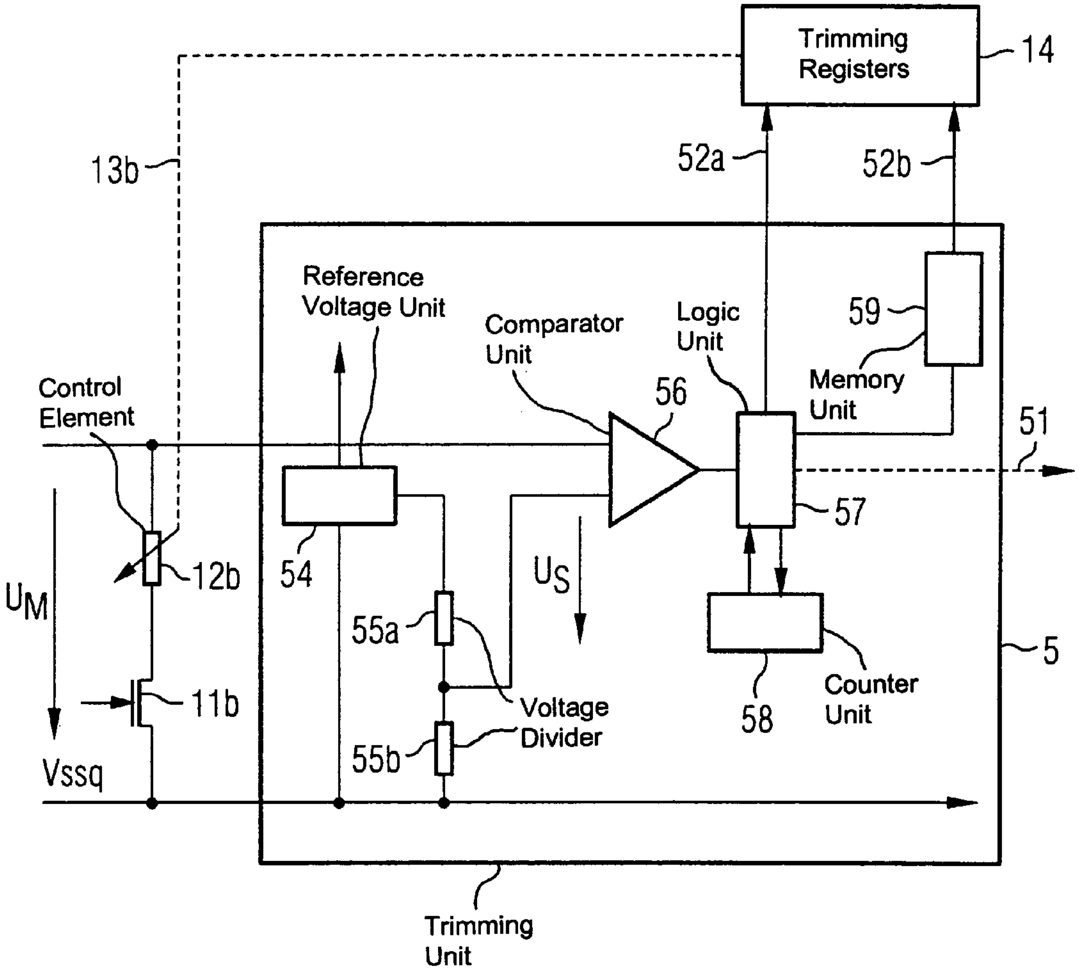


FIG 3



Interface Device
1
Control Element
Supply Connection
20
2
Vddq
Interface Device
11a
10a
12a
16a
17a
10c
15a
31
Control Element
13a
Interface Connection
20
22
IM
V
32
Control Element
Interface Device
15b
12b
21
10b
10d
Supply Connection
Interface Device
11b
17b
20
Vssq
33
13b
16b
Control Element
Trimming Registers
14
34
52a
59
52b
35
UM
Trimming Unit
51
Test Control Unit
Memory Unit
5
24

FIG 4


Trimming
Registers
14
13b
52a
52b
Reference
Voltage Unit
Comparator
Unit
Logic
Unit
59
Memory
Unit
Control
Element
56
51
57
12b
54
U_S
U_M
55a
11b
Voltage
Divider
Counter
Unit
58
5
Vssq
55b
Trimming
Unit

METHOD AND APPARATUS FOR INTERNALLY TRIMMING OUTPUT DRIVERS AND TERMINATIONS IN SEMICONDUCTOR DEVICES

BACKGROUND OF THE INVENTION

Field of the Invention

The invention relates to a method for trimming interface devices on semiconductor devices using a test apparatus having at least one current source. Each of the interface devices has a settable control element.

In data bus systems, data signals are transmitted between a plurality of semiconductor devices on data lines combined to form a common data bus. The power of the data bus system is characterized, inter alia, by a data transmission rate at which data are interchanged between the semiconductor devices within the data bus system.

An example of a data bus system with a high data transmission rate is the DDR (double data rate) II memory system for computer systems, such as PCs, workstations and servers. In this case, a system board for the DDR memory system is provided with slots for memory modules in the form of plug sockets, and these slots are fitted with a variable number of memory modules on the basis of the desired size of the main memory. The memory modules are normally in the form of DIMMs (dual inline memory modules) whose mechanical and electrical interfaces for the system board are subject to industrial standards. The memory modules hold DDRII-DRAMs (double data rate II-dynamic random access memories) as semiconductor memory devices. For DDRII memory systems, typical data transmission rates that are obtained to and from the DDRII-DRAMs are 333 Mbits per second and per data signal (Mbit/s/pin).

As data transmission rates increase on the data bus, the semiconductor devices effecting access for the purpose of writing to the data bus or reading from the data bus demand narrower tolerances for the interface parameters in order to maintain the integrity of the data signals transmitted to the data bus.

A first such interface parameter is the impedance of the output drivers (OCD-off chip driver), which a semiconductor device uses to effect a write access to the data bus, or to output data signals to the data bus. The impedance of an output driver influences the rise and fall times when there is a signal level change in the data signal driven by the output driver, and hence influences a signal delay in the data signal. A maximum skew in the signal delays of all of the output drivers in a semiconductor device or in all of the semiconductor devices in a data bus system limits a maximum data transmission rate. The smaller the maximum skew in this case, the higher the data transmission rates that can be implemented.

Another interface parameter is formed by terminations, which terminate the data bus locally in the semiconductor device in order to prevent reflections (ODT-on die termination). As the precision of the termination increases, interference signals arising at the location of the termination are attenuated to an increasing extent and a higher maximum data transmission rate is made possible in the data bus system.

The interface parameters of semiconductor devices are subject to production variations and vary both from semiconductor device to semiconductor device and within a

variations over time during the operation of the semiconductor device. In this case, the variations over time result, by way of example, from any temperature dependency of the interface parameters or the latter's dependency on an operating voltage for the semiconductor device.

For operation in data bus systems with a high data transmission rate, provision is therefore made for the semiconductor device's interface parameters to be trimmed at least once before or during the initial startup of the semiconductor device or repeatedly during the operation of the semiconductor device. The trimming is performed by control elements in the respective interface devices. The control elements are in the form of switchable impedances whose respective value can be programmed on the basis of a register value in a trimming register (EMRS-extended mode register set).

For ordinary DDRII memory systems, it is normally not possible to trim the interface parameters of DDRII-DRAMs in a target system, since the DDRII-DRAMs cannot be addressed individually within the data bus system. However, selective addressing of individual DDRII-DRAMs is a necessary prerequisite for trimming the interface parameters.

For DDRII-DRAMs, it is therefore necessary to perform trimming in the course of testing the DDRII-DRAMs outside a target system on test apparatuses that are normally designed for conventional, untrimmable DRAMs or DDRII-DRAMs.

A DDRII-DRAM, which has interface devices to be trimmed, is trimmed on a conventional test apparatus by connecting a test output on the test apparatus to an interface connection on the semiconductor device. The test output is connected within the test apparatus to a first DC unit, operated as a current source, and to a further, second DC unit, operated as a voltmeter. As their control element, the interface devices have respective programmable resistors that each have the lowest possible value at the start of the trimming. The current source is used to impress a measurement current onto the interface device. A measurement voltage produced by the measurement current is compared in the test apparatus with a nominal voltage. While the measurement voltage is below the nominal voltage, the register value in the test piece's trimming register is incremented in stages, and the resultant newly obtained measurement voltage is respectively compared with the nominal voltage again. If the measurement voltage is above the nominal voltage, then the register value corresponding thereto is detected and is stored in a suitable manner for further use.

A drawback of this method is, in particular, the relatively low throughput of test pieces, which results from the limited number of DC units suitable for precise output and/or measurement of currents and voltages within test apparatuses designed for conventional DRAMs. Since equipping the test apparatuses with a large number of precise DC units, if at all possible, results in high costs, and testing conventional, untrimmable DRAMs does not require a large number of DC units, the number of the DC units is normally limited in relation to other system resources in the test apparatus.

Another drawback is the time required for evaluating measurement and trimming data, since the test apparatuses designed for digitally operating semiconductor devices normally have only limited resources available for determining,

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