

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD. and
SAMSUNG ELECTRONICS AMERICA, INC.,
Petitioner,

v.

IMAGE PROCESSING TECHNOLOGIES LLC,
Patent Owner.

Case IPR2017-00336
Patent 6,959,293 B2

Before JONI Y. CHANG, MICHAEL R. ZECHER, and
JESSICA C. KAISER, *Administrative Patent Judges*.

CHANG, *Administrative Patent Judge*.

DECISION

Granting Institution of *Inter Partes* Review
35 U.S.C. § 314(a) and 37 C.F.R. § 42.108

I. INTRODUCTION

Samsung Electronics Co., Ltd. and Samsung Electronics America, Inc. (collectively, “Petitioner”) filed a Petition requesting an *inter partes* review of claims 1, 18, 19, 22, and 29 (“the challenged claims”) of U.S. Patent No. 6,959,293 B2 (Ex. 1001, “the ’293 patent”). Paper 2 (“Pet.”). Image Processing Technologies LLC (“Patent Owner”) filed a Preliminary Response. Paper 6 (“Prelim. Resp.”).

Under 35 U.S.C. § 314(a), an *inter partes* review may not be instituted unless the information presented in the petition “shows that there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition.” For the reasons that follow, we determine that Petitioner has established a reasonable likelihood that it would prevail with respect to claim 22, but not with respect to claims 1, 18, 19, and 29. We hereby institute an *inter partes* review only as to claim 22 of the ’293 patent.

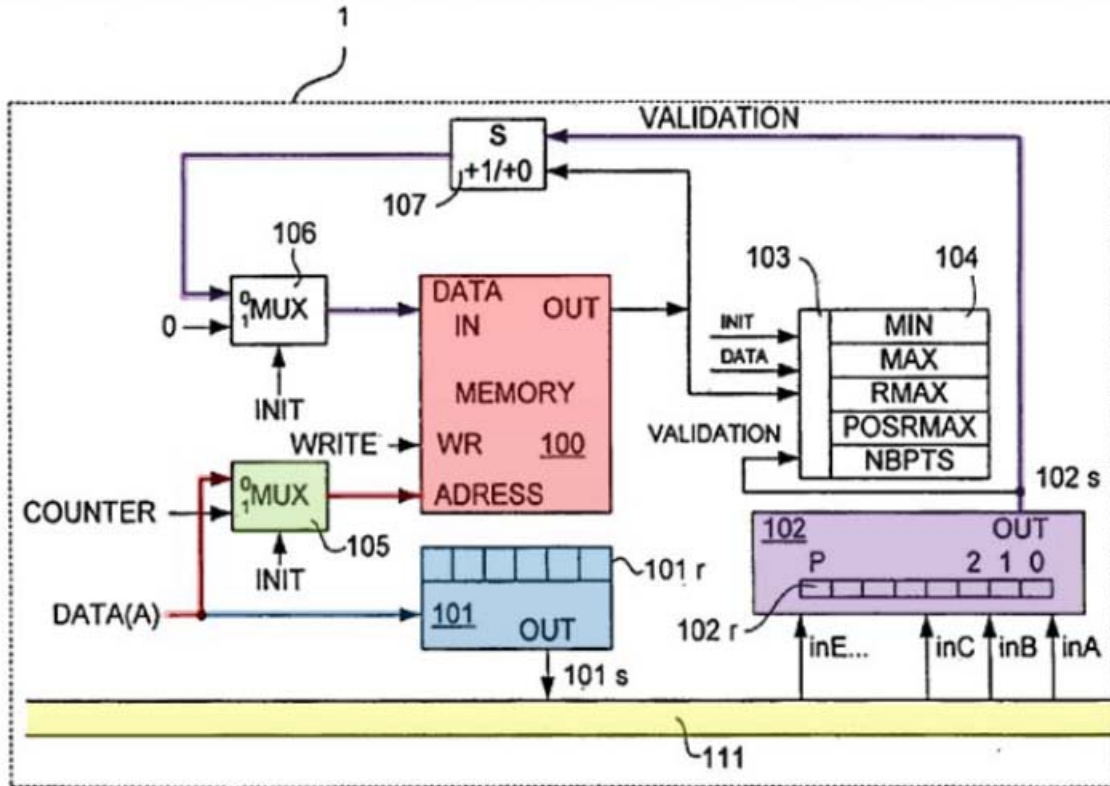
A. Related Matters

The parties indicate that the ’293 patent is involved in *Image Processing Techs., LLC v. Samsung Elecs. Co.*, Case No. 2:16-cv-00505-JRG (E.D. Tex.) and other proceedings. Pet. 2; Paper 4, 2.

B. The ’293 Patent

The ’293 patent describes a visual perception device, particularly a device for processing image signals using self-adapting histogram calculation units. Ex. 1001, 1:6–10. Figure 3 of the ’293 patent illustrates a

passive histogram calculation unit, and is reproduced below with highlighting added by Petitioner (Pet. 5).

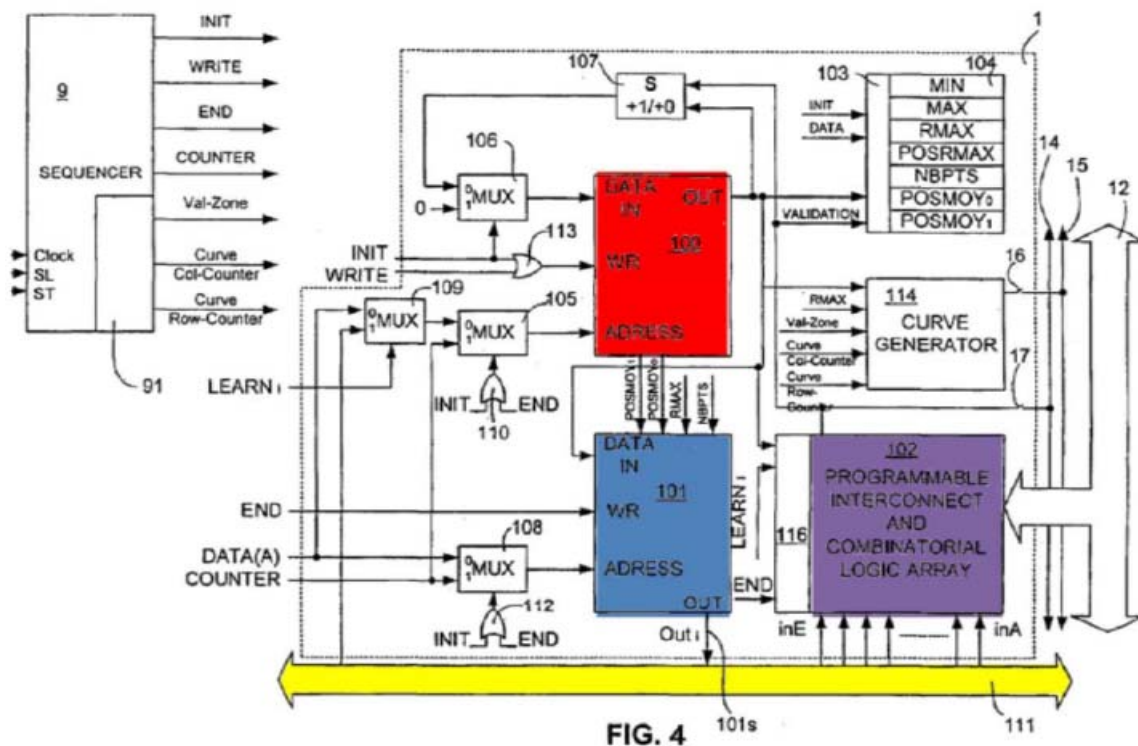


As shown in highlighted Figure 3 above, histogram calculation unit 1 includes analysis memory 100 (highlighted in red), address multiplexer 105 (highlighted in green), data input multiplexer 106, incrementation unit 107, classifier 101 (highlighted in blue), time coincidences unit 102 (highlighted in purple), and test unit 103, which is connected to analysis output registers 104. Ex. 1001, 8:37–43, 9:51–54. Output of classifier 101 is connected to bus 111 (highlighted in yellow). *Id.* at 9:36.

Analysis output registers 104 receive and store statistical information prepared on the basis of the values of parameter A of signal DATA(A) for each frame. *Id.* at 9:51–57. In particular, after processing a complete frame,

statistical information representative of this frame is produced and stored in analysis output registers 104. *Id.* at 10:1–14. This statistical information includes minimum values (MIN) and maximum values (MAX) of the histogram, the number of points (NBPTS) of the histogram, the position (POSRMAX) of the maximum of the histogram, and the number of points (RMAX) at the maximum of the histogram. *Id.* These features are determined in parallel with the formation of the histogram by test unit 103.

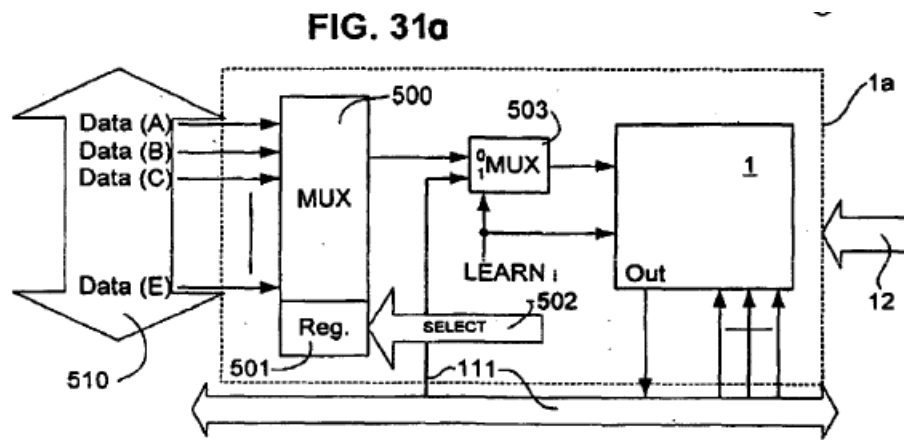
Figure 4 of the '293 patent illustrates a self-adapting histogram calculation unit with anticipation and learning functionalities, and is reproduced below with highlighting added by Patent Owner (Prelim. Resp. 7).



According to the '293 patent, in the self-adapting embodiment illustrated in Figure 4, the content of the memory of classifier 101 is updated

automatically. Ex. 1001, 11:14–29. To implement the self-adapting function (i.e., real-time updating of classifier 101), classifier 101 has an addressable memory whose writing is controlled by signal END, which is generated by sequencer 9. *Id.* Histogram calculation unit 1 also includes selection circuit 110 (e.g., an “OR” gate), receiving as its input signals INIT and END and whose output is connected to the selection input of address multiplexer 105. *Id.*

Figure 31a of the '293 patent illustrates a polyvalent histogram calculation unit that can be programmed to process more than one parameter, and is reproduced below (*id.* at 21:18–36).



As shown in Figure 31a above, polyvalent histogram calculation unit 1a comprises histogram calculation unit 1, input multiplexer 500, associated register 501, and learning multiplexer 503. *Id.* In this embodiment, it is possible to use a single histogram calculation unit to process any of parameters Data (A) – Data (E), which are addressed by bus 510 in relation to SELECT command 502. *Id.* at 20:58–66. Additionally, polyvalent histogram calculation units can be operated in a matrix. *Id.* at 21:37–42.

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