Trials@uspto.gov
571.272.7822

Paper No. 16
Entered: July 5, 2017

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

APPLE INC.,
Petitioner,

v.

CALIFORNIA INSTITUTE OF TECHNOLOGY,
Patent Owner.

Case IPR2017-00423
Patent 7,916,781 B2

Before KEN B. BARRETT, TREVOR M. JEFFERSON, and
JOHN A. HUDALLA, *Administrative Patent Judges*.

HUDALLA, *Administrative Patent Judge*.

DECISION
Institution of *Inter Partes* Review
35 U.S.C. § 314(a) and 37 C.F.R. § 42.108

Petitioner, Apple, Inc. ("Apple"), filed a Petition (Paper 5, "Pet.") requesting an *inter partes* review of claims 13–22 of U.S. Patent No. 7,916,781 B2 (Ex. 1101, "the '781 patent") pursuant to 35 U.S.C. §§ 311–319. Apple proffered a Declaration of James A. Davis, Ph.D. (Ex. 1104) with its Petition. Patent Owner, California Institute of Technology ("Caltech"), filed a Preliminary Response (Paper 14, "Prelim. Resp.") to the Petition.

Under 35 U.S.C. § 314(a), the Director may not authorize an *inter partes* review unless the information in the petition and preliminary response "shows that there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition." For the reasons that follow, we institute an *inter partes* review as to claims 13–16, 18, and 22 of the '781 patent on certain grounds of unpatentability presented.

I. BACKGROUND

A. Related Proceedings

The parties identify the following district court cases related to the '781 patent (Pet. 1; Paper 7, 1):

Cal. Inst. of Tech. v. Broadcom Ltd., No. 2:16-cv-03714 (C.D. Cal. filed May 26, 2016);[1]

Cal. Inst. of Tech. v. Hughes Commc'ns, Inc., No. 2:15-cv-01108 (C.D. Cal. filed Feb. 17, 2015); and

Cal. Inst. of Tech. v. Hughes Commc'ns, Inc., 2:13-cv-07245 (C.D. Cal. filed Oct. 1, 2013).

The parties also identify co-pending Case IPR2017-00297, in which Apple has filed a petition for *inter partes* review of claims 3–12 and 19–21 of the '781 patent. Pet. 2 n.1; Paper 7, 1. In addition, the '781 patent was previously subject to an *inter partes* review in Case IPR2015-00059 ("059 IPR"). Pet. 19; Ex. 1111; Paper 7, 1. In the Final Written Decision from the 059 IPR, which Apple filed as Exhibit 1111 in this proceeding, the

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[1] Apple is a defendant in this case. *See* Pet. 1.

Board determined that claims 1 and 2 of the ’781 patent are unpatentable as anticipated by the Divsalar reference, which is one of the asserted references in this case. *See* Ex. 1111, 43.

Apple additionally states that patents in the priority chain of the ’781 patent were challenged in Cases IPR2015-00068, IPR2015-00067, IPR2015-00060, IPR2015-00061, and IPR2015-00081. Pet. 1. We additionally identify the following cases between the parties: Cases IPR2017-00210, IPR2017-00211, IPR2017-00219, IPR2017-00700, IPR2017-00701, IPR2017-00702, IPR2017-00703, and IPR2017-00728.

B. The ’781 patent

The ’781 patent describes the serial concatenation of interleaved convolutional codes forming turbo-like codes. Ex. 1101, Title. It explains some of the prior art with reference to its Figure 1, reproduced below.

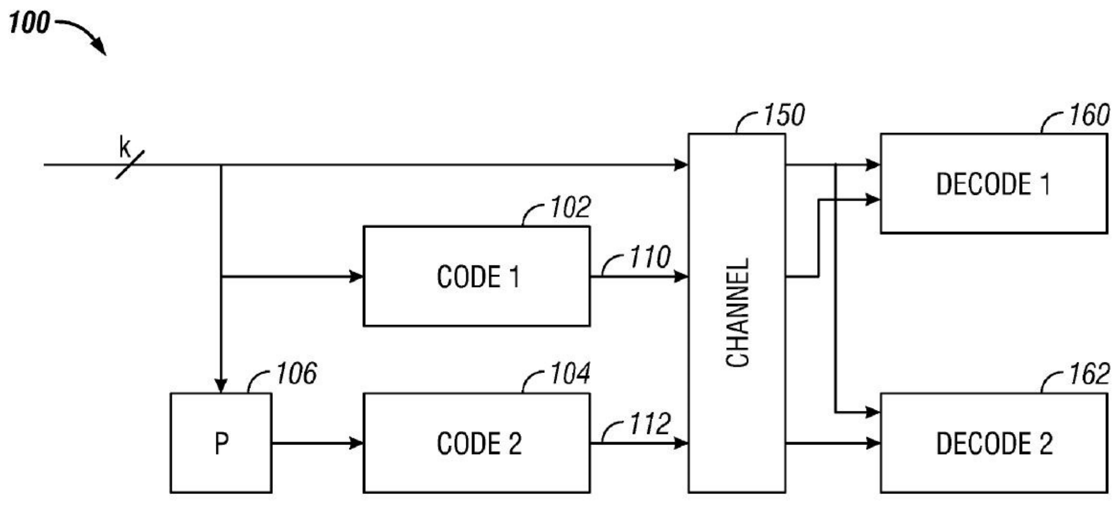

FIG. 1
(Prior Art)

Figure 1 is a schematic diagram of a prior “turbo code” system. *Id.* at 2:20–21. The ’781 patent specification describes Figure 1 as follows:

> A block of k information bits is input directly to a first coder 102. A k bit interleaver 106 also receives the k bits and interleaves them prior to applying them to a second coder 104. The second coder produces an output that has more bits than its input, that is, it is a coder with rate that is less than 1. The coders 102, 104 are typically recursive convolutional coders.
>
> Three different items are sent over the channel 150: the original k bits, first encoded bits 110, and second encoded bits 112. At the decoding end, two decoders are used: a first constituent decoder 160 and a second constituent decoder 162. Each receives both the original k bits, and one of the encoded portions 110, 112. Each decoder sends likelihood estimates of the decoded bits to the other decoders. The estimates are used to decode the uncoded information bits as corrupted by the noisy channel.

Id. at 1:44–60.

A coder 200, according to a first embodiment of the invention, is described with respect to Figure 2, reproduced below.

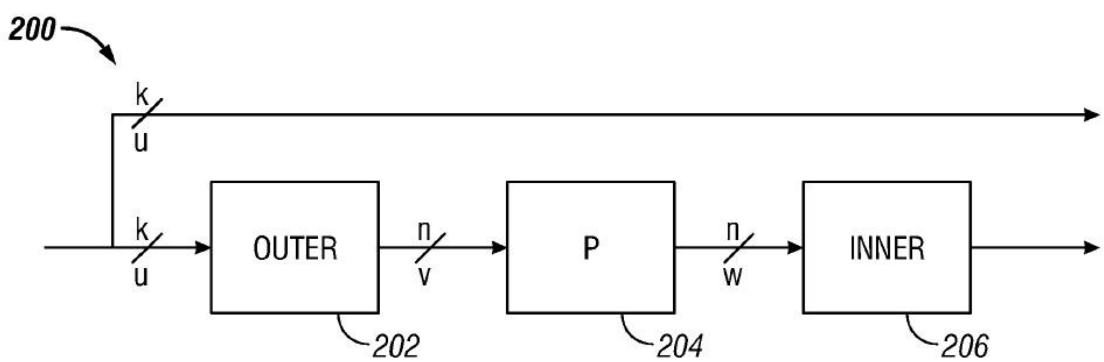

FIG. 2

Figure 2 of the ’781 patent is a schematic diagram of coder 200.

> The coder 200 may include an outer coder 202, an interleaver 204, and inner coder 206. . . . The outer coder 202 receives the uncoded data [that] may be partitioned into blocks of fixed size, [e.g.] k bits. The outer coder may be an (n,k) binary linear block coder, where n>k. The coder accepts as input a block u of k data bits and produces an output block v of n data bits.

> The mathematical relationship between u and v is $v=T_0u$, where T_0 is an n×k matrix, and the rate[2] of the coder is k/n.
>
> The rate of the coder may be irregular, that is, the value of T_0 is not constant, and may differ for sub-blocks of bits in the data block. In an embodiment, the outer coder 202 is a repeater that repeats the k bits in a block a number of times q to produce a block with n bits, where n=qk. Since the repeater has an irregular output, different bits in the block may be repeated a different number of times. For example, a fraction of the bits in the block may be repeated two times, a fraction of bits may be repeated three times, and the remainder of bits may be repeated four times. These fractions define a degree sequence or degree profile, of the code.
>
> The inner coder 206 may be a linear rate-1 coder, which means that the n-bit output block x can be written as $x=T_Iw$, where T_I is a nonsingular n×n matrix. The inner coder 210 can have a rate that is close to 1, e.g., within 50%, more preferably 10% and perhaps even more preferably within 1% of 1.

Id. at 2:40–3:2 (footnote added). Codes characterized by a regular repeat of message bits into a resulting codeword are referred to as "regular repeat," whereas codes characterized by irregular repeat of message bits into a resulting codeword are referred to as "irregular repeat." The second ("inner") encoder 206 performs an "accumulate" function. Thus, the two step encoding process illustrated in Figure 2, including a first encoding ("outer encoding") followed by a second encoding ("inner encoding"), results in either a "regular repeat accumulate" ("RRA") code or an "irregular repeat accumulate" ("IRA") code, depending upon whether the repetition in the first encoding is regular or irregular.

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[2] We understand that the "rate" of an encoder refers to the ratio of the number of input bits to the number of resulting encoded output bits related to those input bits.

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