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# United States Patent [19]

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Schoenborn

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- [54] ANISOTROPIC POLYSILICON ETCHING PROCESS
- [75] Inventor: Philippe Schoenborn, San Jose, Calif.
- [73] Assignee: LSI Logic Corporation, Milpitas, Calif.
- [21] Appl. No.: 632,461
- [22] Filed: Dec. 20, 1990
- [51] Int. Cl.<sup>5</sup> ..... H01L 21/00
- [52] U.S. Cl. .... 156/643; 156/646; 156/657; 156/662
- [58] Field of Search ..... 656/657, 662, 643, 646

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Primary Examiner—Thi Dang

Attorney, Agent, or Firm—Gerald E. Linden; Michael D. Rostoker

### [57] ABSTRACT

An anisotropic polysilicon etching process in Cl<sub>2</sub>/HBr/He is disclosed. The use of HBr allows etching to occur under high poly:oxide selectivity conditions (e.g., above 40:1) that would otherwise produce lateral etching of the poly under the photoresist mask (isotropy). The selectivity of poly:resist is also increased (e.g., above 4:1). Poly sidewall passivation is enhanced without relying on resist redeposition. Gate oxide loss is also minimized, and anisotropy is realized with increased overetch (e.g., 60%). Exemplary process settings are: 1) 250 mTorr, 190 Watts, 0.5 cm gap, 100 sccm Cl<sub>2</sub>, 50 sccm HBr and 40 sccm He; and 2) 270 mTorr, 200 Watts, 0.5 cm gap, 80 sccm Cl<sub>2</sub>, 55 sccm HBr and 45 sccm He.

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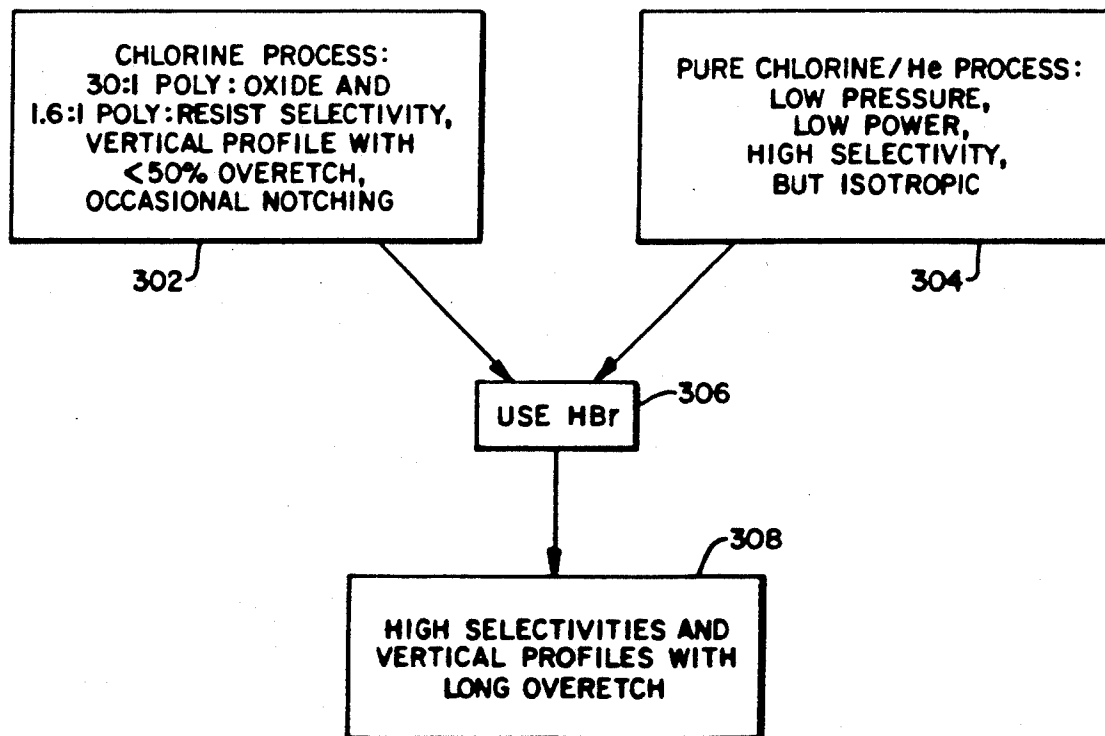
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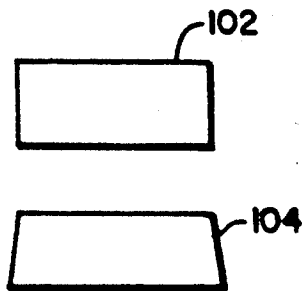
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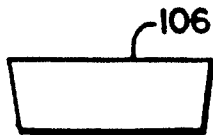
19 Claims, 16 Drawing Sheets





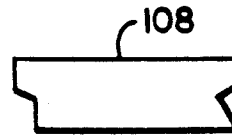
ACCEPTABLE

FIG. 1A



RE-ENTRANT OR  
NEGATIVE, NOT  
ACCEPTABLE

FIG. 1B



NOTCHED  
NOT ACCEPTABLE

FIG. 1C

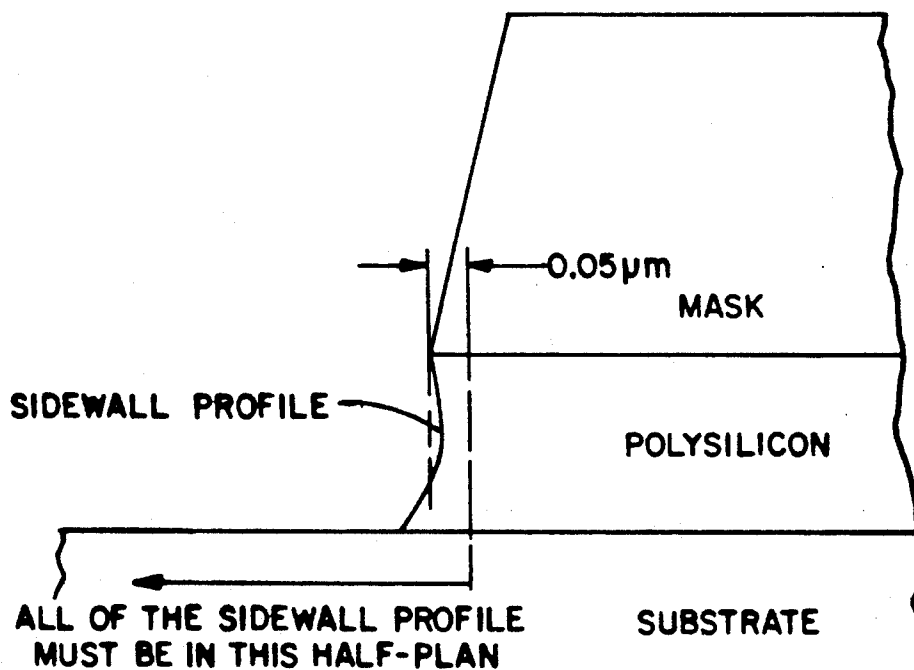


FIG. 1D

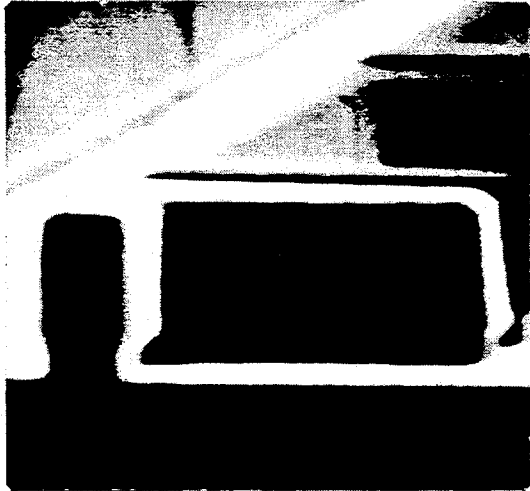


FIG. 2A

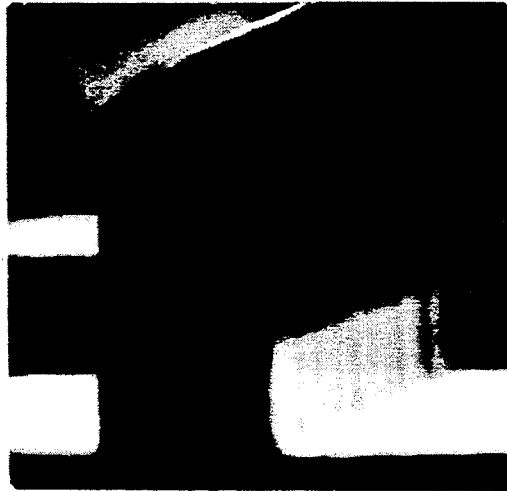


FIG. 2B

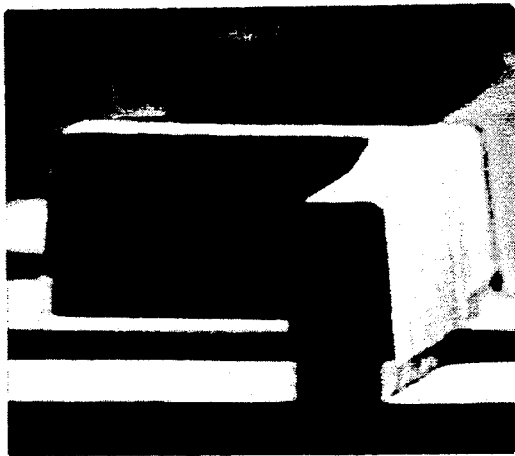


FIG. 4

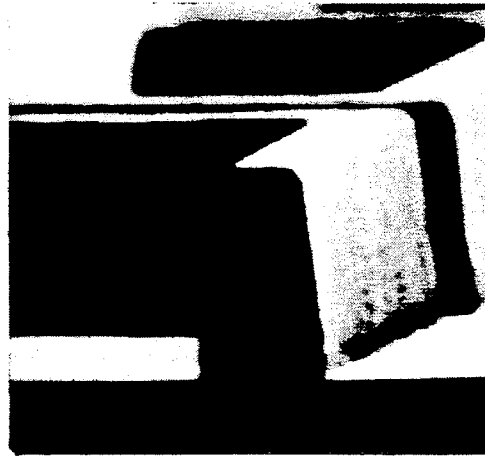


FIG. 5

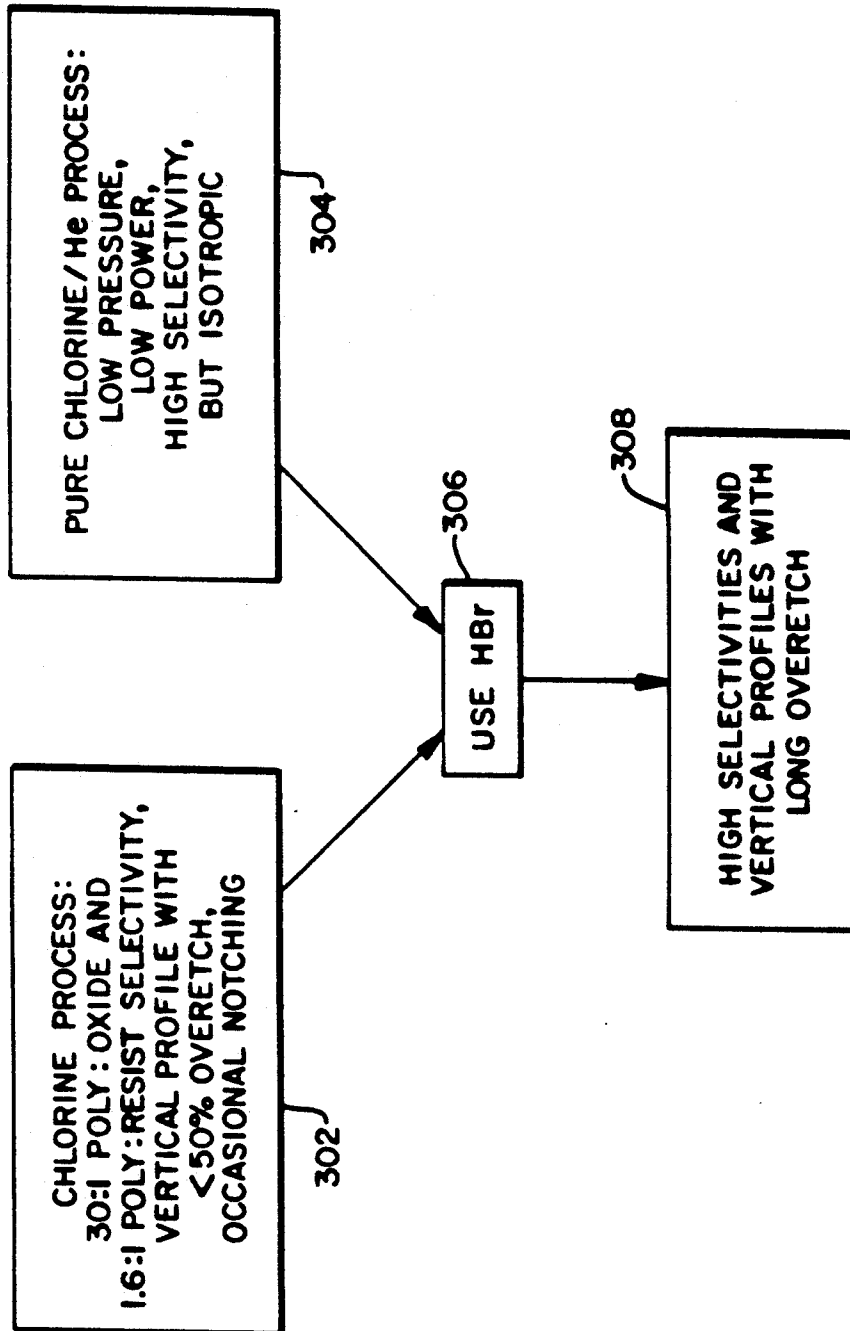
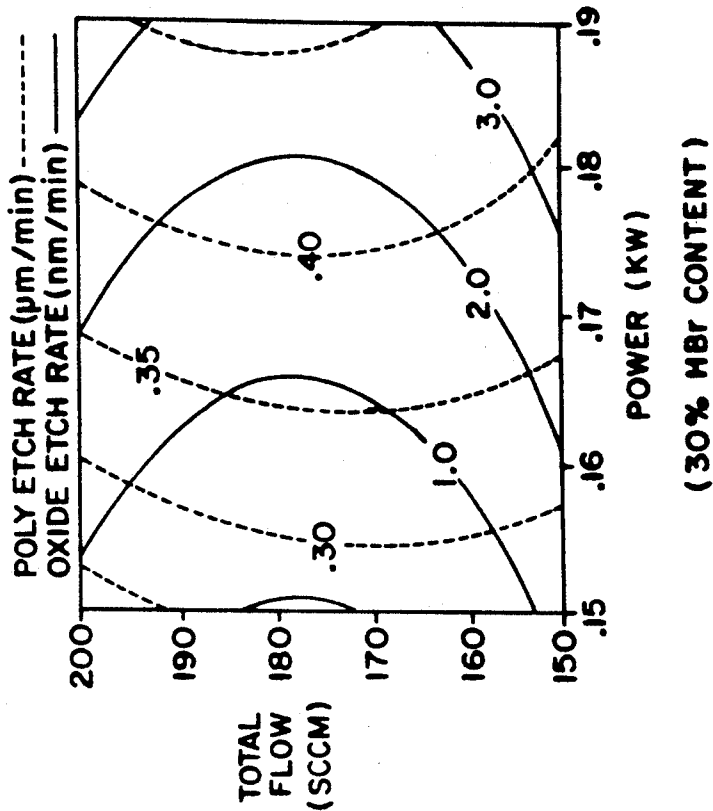
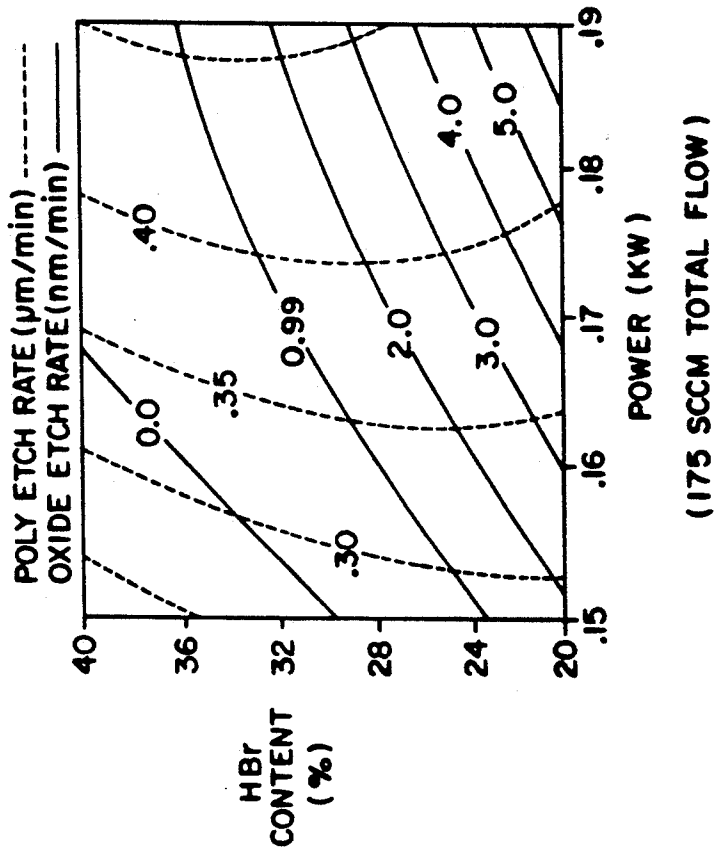


FIG. 3



**FIG. 6B**



**FIG. 6A**

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