

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

INTEL CORPORATION, GLOBALFOUNDRIES U.S., INC.,
and MICRON TECHNOLOGY, INC.
Petitioner,

v.

DANIEL L. FLAMM,
Patent Owner.

Case IPR2017-00282
Patent RE40,264 E

Before CHRISTOPHER L. CRUMBLEY, JO-ANNE M. KOKOSKI, and
KIMBERLY McGRAW, *Administrative Patent Judges*.

McGRAW, *Administrative Patent Judge*.

DECISION

Institution of *Inter Partes* Review
35 U.S.C. § 314(a) and 37 C.F.R. § 42.108

I. INTRODUCTION

Intel Corporation, GLOBALFOUNDRIES U.S., Inc., and Micron Technology, Inc. (collectively, “Petitioner”), filed a Petition requesting an *inter partes* review of claims 56–63, 70, and 71 (“the challenged claims”) of U.S. Patent No. RE40,264 E (Ex. 1001, “the ’264 patent”). Paper 2 (“Pet.”). Daniel L. Flamm (“Patent Owner”), filed a Preliminary Response. Paper 8 (“Prelim. Resp.”).

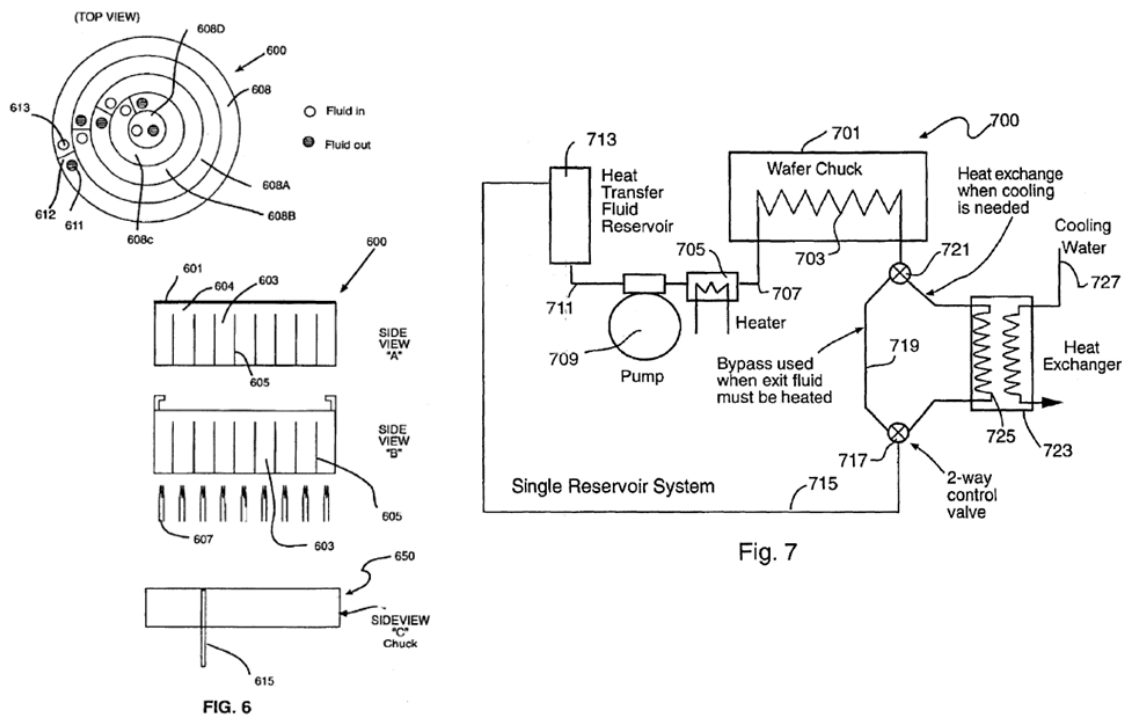
Under 35 U.S.C. § 314(a), an *inter partes* review may not be instituted unless the information presented in the Petition shows “there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition.” Taking into account the arguments presented in Patent Owner’s Preliminary Response, we conclude that the information presented in the Petition establishes that there is a reasonable likelihood that Petitioner would prevail in challenging claims 56–63, 70, and 71 as unpatentable under 35 U.S.C. § 103(a). Pursuant to § 314, we hereby institute an *inter partes* review as to these claims of the ’264 patent

A. Related Matters

Petitioner reports that Patent Owner has asserted the ’264 patent against Petitioner and other defendants in five proceedings in the Northern District of California: Case Nos. 5:16-cv-01578-BLF, 5:16-cv-1579-BLF, 5:16-cv-1580-BLF, 5:16-cv-1581-BLF, and 5:16-cv-02252-BLF. Pet. 2. The parties also state that Lam Research Corporation filed a declaratory judgment action against Patent Owner on the ’264 patent (N.D. Cal. Case No. 5:15-cv-01277-BLF) and filed seven IPR petitions on the ’264 patent: IPR2015-01759; IPR2015-01764; IPR2015-01766; IPR2015-01768; IPR2016-00468; IPR2016-00469; and IPR2016-00470. Pet. 2; Prelim.

Figure 1 depicts a substrate (product 28, such as a wafer to be etched) on a substrate holder (product support chuck or pedestal 18) in a chamber (chamber 12 of plasma etch apparatus 10). *Id.* at 3:24–25, 3:32–33, 3:40–41.

Figures 6 and 7, reproduced below, depict a temperature-controlled substrate holder and temperature control systems.



Figures 6 and 7 depict temperature-controlled fluid flowing through substrate holder (600, 701), guided by baffles 605, where “[t]he fluid [is] used to heat or cool the upper surface of the substrate holder.” Ex. 1001, 14:28–63, 16:5–67. Figure 6 also depicts heating elements 607 underneath the substrate holder, where “[t]he heating elements can selectively heat one or more zones in a desirable manner.” *Id.* at 15:10–26. Referring to Figure 7, the operation of the temperature control system is described as follows:

The desired fluid temperature is determined by comparing the desired wafer or wafer chuck set point temperature to a measured wafer or wafer chuck temperature The heat exchanger, fluid flow rate, coolant-side fluid temperature, heater power, chuck, etc. should be designed using conventional means to permit the heater to bring the fluid to a setpoint temperature and bring the temperature of the chuck and wafer to predetermined temperatures within specified time intervals and within specified uniformity limits.

Id. at 16:36–39, 16:50–67.

An example of a semiconductor substrate to be patterned is shown in Figure 9, reproduced below.

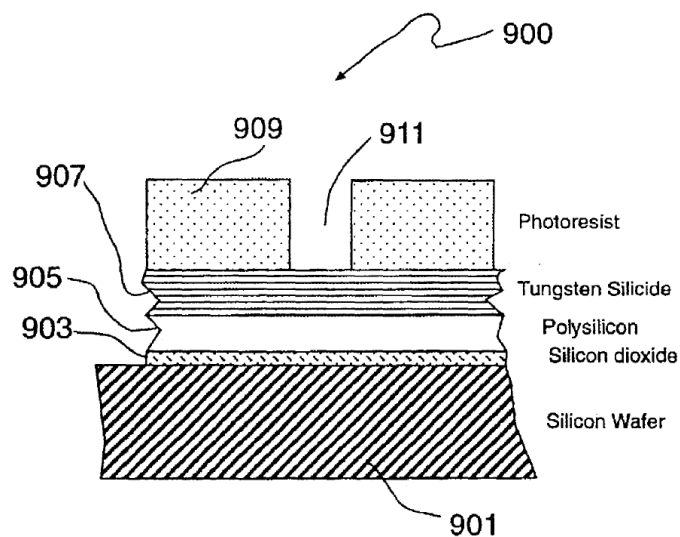


Figure 9 depicts substrate 901 having a stack of layers including oxide layer 903, polysilicon layer 905, tungsten silicide layer 907, and photoresist masking layer 909 with opening 911, from the treatment method shown in Figure 10, reproduced below. *Id.* at 17:58–18:57.

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