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Paper 8
Entered: September 23, 2014

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

KINETIC TECHNOLOGIES, INC.,
Petitioner,

v.

SKYWORKS SOLUTIONS, INC.,
Patent Owner.

Case IPR2014-00529
Patent 7,921,320 B2

Before GLENN J. PERRY, SCOTT A. DANIELS, and BARRY L. GROSSMAN, *Administrative Patent Judges.*

GROSSMAN, *Administrative Patent Judge*.

DECISION
Denying Institution of *Inter Partes* Review
37 C.F.R. § 42.108

I. INTRODUCTION

Kinetic Technologies, Inc. ("Petitioner") filed a Petition requesting *inter partes* review of claims 13–24 and 37–47 of U.S. Patent No. 7,921,320 B2 (Ex. 1001, "the '320 patent"). Paper 1 ("Pet."). Skyworks Solutions, Inc., ("Patent Owner"), filed a Preliminary Response. Paper 6 ("Prelim. Resp."). We have jurisdiction under 35 U.S.C. § 314.

We determine that the information presented does not show that there is a reasonable likelihood that Petitioner would prevail in establishing the unpatentability of any of claims 13–24 and 37–47. Accordingly, we deny the Petition and do not institute an *inter partes* review of the '320 patent.

A. Related Proceedings

Petitioner informs us of the following related matters.

The '320 Patent is at issue in *Skyworks Solutions, Inc. v. Kinetic Technologies, Inc.*, Case No. 1:13-cv-10655 (N.D. Cal.), filed March 20, 2013; and *Skyworks Solutions, Inc. v. Kinetic Technologies, Inc.*, Case No. 3:14-cv-00010 (N.D. Cal.), filed January 2, 2014.

The '320 Patent is a continuation of U.S. Application 10/144,333, now U.S. Patent No. 7,127,631, which is the subject of Reexamination Control No. 95/000,501. U.S. Patent No. 7,127,631 is at issue in *Advanced Analogic Technologies, Inc. v. Kinetic Technologies, Inc.*, Case No. 3:09-cv-01360 (N.D. Cal.), filed March 2, 2009.

U.S. Application 14/028,365, filed September 16, 2013, claims priority to the '320 Patent.

Petitioner filed a second petition (IPR2014-00530) requesting *inter partes* review of claims 13–22 and 37–45[1] of the '320 patent on grounds different from the grounds asserted in this case.

We also are aware that U.S. Patent No. 8,539,275 B2, a continuation of Application No. 11/582,927, now the '320 Patent, is the subject of a petition to institute an *inter partes* review (IPR2014-00690).

B. The '320 Patent

The '320 patent, titled "Single Wire Serial Interface," relates generally to control interfaces for integrated circuits ("ICs") and other devices. Ex. 1001, col. 1, ll. 14–15. The device disclosed in the '320 patent provides a single wire serial interface that may be used to control stand-alone power ICs and other devices. *Id.* at col. 1, ll. 62–64. When so used, an IC is configured to include a sensing circuit, a counter, and a ROM or similar decoder. *Id.* at col. 1, ll. 64–66.

The '320 patent describes that stand-alone power systems for power integrated circuits often are constrained by package size and cost, and where most of the available pins in such stand-alone power applications are used for power load, there are few pins in the interface left to accommodate power control functions. *Id*. at col. 1, ll. 34–43. The '320 patent states that ideally in such applications, minimal pins, or a single pin "interface would be able to accommodate a wide variety of control needs and be scalable to many levels of complexity." *Id*. at col. 1, ll. 52–58.

Figure 2 of the '320 patent, reproduced below, illustrates integrated circuit 200, which has a single wire serial interface. *Id.* at col. 2, ll. 59–60. According to the '320 patent, to use a single wire serial protocol compatible devices must provide a single wire serial interface. *Id.* at col. 3, ll. 57–60. Figure

[1] The second petition does not include a request to review claims 23, 24, 46, and 47, which are challenged in this proceeding.

2 shows a block diagram of an IC configured to provide a single wire serial interface. *Id.*

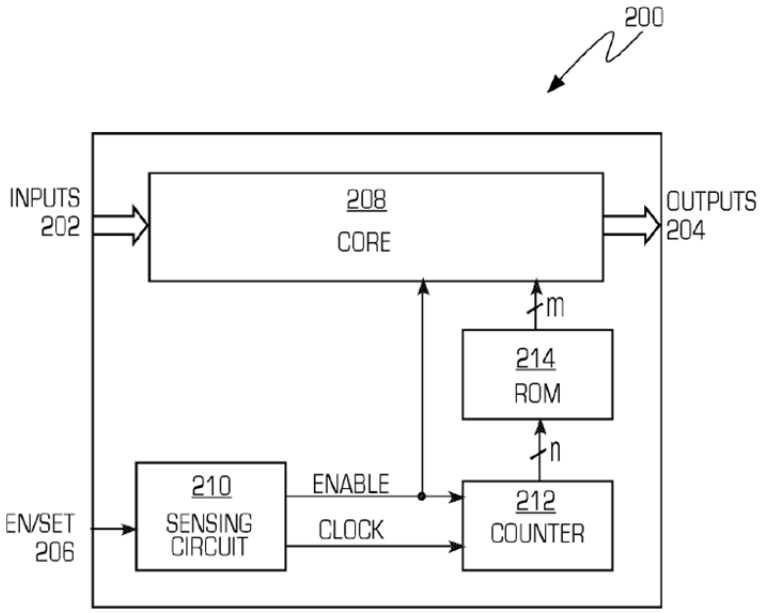

FIG. 2

As depicted in Figure 2 of the '320 patent, integrated circuit 200 has one or more inputs 202, and one or more outputs 204, as well as EN/SET signal input 206. EN/SET input 206 is connected to sensing circuit 210, which, as discussed further below, determines the voltage state, i.e. high, low, or toggling, of the EN/SET signal. *Id.* at col. 3, l. 60–col. 4, l. 1.

Figure 1 of the '320 patent illustrates three waveform types defining EN/SET signal. The first of these is a toggling waveform, where the EN/SET signal is composed of a series of clock pulses. The second waveform is where the EN/SET signal has a constant high value. The third waveform is where the EN/SET signal has a constant low value. Ex. 1001, col. 3, ll. 27–34.

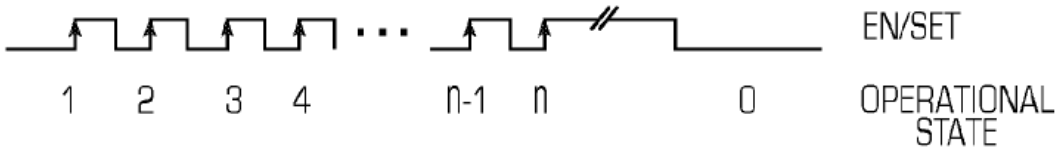

FIG. 1

The toggling waveform causes compatible devices to select particular operational states. The total number of clock pulses (or rising edges) determines the particular operational state that will be selected (i.e., four clock pulses selects the fourth operational state and so on. *Id.* at col. 3, ll. 35–39. The constant high waveform causes compatible devices to maintain their previously selected operational states. *Id.* at col. 3, ll. 43–44. The constant low waveform causes compatible devices to power off (or otherwise adopt a predefined configuration) after a pre-defined timeout period has elapsed. *Id.* at col. 3, ll. 47–49.

Sensing circuit 210 determines the waveform type of the EN/SET signal and produces two output signals, Clock signal and Enable signal, to send to counter 212. *Id*. at col. 4, ll. 1–3. The '320 patent states that:

> a rising transition of the EN/SET signal causes sensing circuit 210 to assert the Enable signal. Sensing circuit 210 holds the Enable signal high until the EN/SET signal transitions to a logical low state and remains in the low state until the predetermined timeout period has elapsed.

Id. at col. 4, ll. 10–15. In other words, the Enable signal is a gate signal for the Clock signal; as long as the Enable signal is high, the Clock signal is forwarded by sensing circuit 210 to counter 212. *Id*. at col. 4, ll. 15–18. In this case, counter 212 counts the transitions, i.e., waveform pulses, forwarded by sensing circuit 210 (e.g. 1, 2, 3, 4. . . n), to determine a counter n-bit output. *Id*. at col. 4, ll. 22-23. Counter 212 resets to 0 "when sensing circuit transitions the Enable signal to a low value." *Id*. at col. 4, ll. 21–25.

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