JEDEC STANDARD

CONFIGURATIONS FOR SOLID STATE MEMORIES

JESD21-C

JEDEC Standard No. 21-C Release 4

(Revision of JESD 21-B

November 1993

ELECTRONIC INDUSTRIES ASSOCIATION

ENGINEERING DEPARTMENT

Jedec 0007680

jx0056-001

KINGSTON 1007

CONFIGURATIONS FOR SOLID STATE MEMORIES

Formulated under the cognizance of Committees JC–42.1, PLD devices, JC–42.3, volatile memories, JC–42.4, non–volatile memories, and JC–42.5, memory modules and cards, and approved by the JEDEC Council.

Standard 21–C Revision Log.

Release 1, August 1990

Release 2, September 1991

Release 3, November 1992

Release 4, November 1993

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jx0056-002

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2 TERMS AND DEFINITIONS

This section contains listings and definitions of a number of terms that are needed for a clear understanding of the standards as presented. Most of these terms have been developed within the semiconductor memory industry and are not covered by JEDEC Standard 100. They are, however, not in conflict with this standard which contains all JEDEC approved definitions.

The following pin names and functional descriptions apply uniformly to all devices covered by this standard. Where a pin has a dual-function, and those functions are invoked at substantially different times, the names and symbols for the functions are separated by a slash (/)(e.g., VPP/G\). Where a pin has multiple functions which are used interspersed at essentially the same time, the slash is omitted(e.g., DQ). Where multiple pins have a similar function, a number symbolized as (n) is appended to the symbol. Where the pin function has an inverted logic sense, that is, the function is true or invoked for a low signal, the overbar or reverse slash (\) is appended to the symbol. Where alternative functions are allowed by the standard, the allowed functions are listed separated by commas. Where common usage has resulted in two terms being used interchangeably, both are listed but the deprecated term is enclosed in parentheses.

Following the list of PIN definitions, there are a series of other terms and definitions that are required for a clear understanding of the individual device standards.

Standard 21-B introduces a family of pin names and functional descriptions that are applicable to the MPDRAM devices. Because of their newness, they are included in a separate section of the standard for ease of access.

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2.1 Conventional Device Pin Names

2.1.1 – A, PORT A
In dual port memory devices, the two ports are designated port A & port B. The letter A or B is appended as a suffix to any pin that is specific to one or the other of the ports.

2.1.2 – A(n), ADDRESS INPUTS
Those inputs that select (address) a particular cell or set of cells within a memory array for presentation on the device outputs. The integer (n) serves to differentiate the address inputs, one from another.

2.1.3 – ADQ(n), ADDRESS DATA INPUT/OUTPUT
The pins that are multiplexed three ways to serve as address input, data input, and data output pins.

2.1.4 – AL, $\overline{AL}$, ADDRESS LATCH ENABLE
An input that when true, allows the input address to be entered into a register, and when false, causes the address state previously entered to be latched.

2.1.5 – B, PORT B
In dual port memory devices, the two ports are designated port A & port B. The letter A or B is appended as a suffix to any pin that is specific to one or the other of the ports.

2.1.6 – BA, BANK ADDRESS
In a RAM that has multiple banks in its architecture, the BANK ADDRESS is used, at any instant of time, ti select any one of the available banks.

2.1.7 – BG, BG, BYTE MODE ENABLE
An input that when true, causes a word wide device to operate in the byte mode and to present the high or low byte on a pre–defined data pin set. Truth tables will be provided to define the details of the operation.

2.1.8 – BS, BLOCK SELECT
A group of input signals that enable individual bit blocks of the data interface.

2.1.9 – BY, BY, BUSY
The output that, on some devices, signifies that some internal asynchronous operation is still in process, and that the device is not available for normal functions. This signal is normally implemented so that multiple devices can be OR–tied.

2.1.10 – C, OUTPUT CLOCK
The input, on some devices that contain an output data register, that causes the data to be set into the register.

2.1.11 – CA, COLUMN ADDRESS
In an address multiplexed DRAM, the address field that is captured by the COLUMN ENABLE clock CE\.

2.1.12 – CE, $\overline{CE}$,($\overline{CAS}$), COLUMN ENABLE
An enable signal that on some dynamic RAMs actuates only the column oriented internal circuits and the data input/output circuits. Most devices normally require the RE\ signal to be present for the CE\ signal to be effective. In some newer designs, however, special sequences of the RE\ and CE\ signals are used to actuate certain special device control functions.

2.1.13 – CK, $\overline{CK}$, INPUT AND OUTPUT CLOCK
An input that controls the activation of both input and output circuitry, normally storage registers or latches.

2.1.14 – CKE, CLOCK ENABLE
In certain synchronous memory devices, a logic level input that enables the clock input and allows it to fulfill its defined function.

2.1.15 – CL, Clear
An input that, when true, causes all cells in the memory array to be cleared to their zero state.

2.1.16 – D(n), DATA INPUT
Those inputs whose state represents the value of data that is to be written into the selected address on a write cycle of an alterable memory device.

2.1.17 – DC, DIAGNOSTIC CLOCK
The input that, on some devices, invokes and controls any built–in diagnostic test features.

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2.1.18 – DQ(n), DATA INPUT/OUTPUT
The pins that serve as data output(s) when in the read mode and as data input(s) when in the write mode. When the device is not selected or enabled, the output(s) are in a floating state. On a devices having both serial and parallel access ports, these pins provide access to the parallel RAM port data channels. The suffix (n) is a numeric value indicating the number assignment of a particular pin with numbering starting at 0. In some situations the letters U or L are used to indicate that the pins are assigned to the upper or lower byte of a 2 byte data interface. In devices where the standard supports an optional 9th bit that may be used as a parity bit, the suffix P may be used in lieu of a numeric value.

2.1.19 – E, $\overline{E}$, CHIP ENABLE
The input that, when true, permits active operation including the input and/or output of data, and when false, prevents active operation and causes the memory to be in a reduced power standby mode with the outputs floating.

2.1.20 – F, $\overline{F}$, REFRESH
An input that, when true, causes the device to enter a data refresh mode.

2.1.21 – G, $\overline{G}$, OUTPUT ENABLE
The input that, when false, disables the outputs and causes them to go to an inactive state, but that does not effect the writing function. When disabled, the inactive state is floating (Z), for MOS and TTL devices and low (L), for ECL devices.

2.1.22 – GS, $\overline{GS}$, SYNCHRONOUS OUTPUT ENABLE
An output enable input that must be set in by a synchronizing clock signal, K (q.v.).

2.1.23 – $\overline{I}$, INITIALIZE INPUT
A control input that provides a preassigned Manufacturer or User defined code to be set into the data register. If the input is all "0", it can be called "clear", and if all "1", then "preset".

2.1.24 – ID(n), IDENTIFICATION
A group of output terminals, nominally used to convey information about the configuration or other attributes of the device when plugged into a system. The function of these outputs are similar to those of the PD(n) terminals but they often have different electrical interface chatacteristics.

2.1.25 – I/O, INPUT/OUTPUT
A generic term for otherwise undefined signal pins which can have either an input and/or an output function. This term is not used as a specific pin name, only as a generic indicatior of the nature of the function of the pin.

2.1.26 – $\overline{IS}$, INITIALIZE INPUT (SYNCHRONOUS)
A control input that provides a preassigned Manufacturer or User defined code to be presented to the data register for subsequent setting by a clock input. If the input is all "0", it can be called "clear", and if all "1", then "preset".

2.1.27 – K, INPUT CLOCK
The input that, on devices that contain input buffer registers, causes the address on the A(n), the data on the D(n) pins and/or certain control inputs to be set into the register.

2.1.28 – L, LATCH ENABLE or LOWER BYTE
An input that, on devices containing a latch register, causes the data to be latched into the register. When L is used in conjunction with a data or control term it signifies that the combined term applies to the lower byte of a two byte data interface device (e.g. $\overline{LW}$).

2.1.29 – $\overline{LB}$, LOWER BYTE ENABLE
An input, on wordwide devices, that, when true, enables the lower byte data input/outputs, pins DQ0 through DQ7.

2.1.30 – $\overline{LW}$, LOWER BYTE WRITE ENABLE
An input, on wordwide devices, that when true causes the data present on the lower byte input/output, terminals DQ0 through DQ7, to be written into the addressed cells of the device.

2.1.31 – M(n), M, MODE SELECT, MASK
Input signals that when true select an alternative mode of operation for the device. The alternative modes available must be defined in the applicable device standard. When M is used in conjuction with other symbols to create a new pin name, it signifies that the pin function is either MASK or MODE related.

2.1.32 – MA, MATCH
An output signal that when true indicates that there has been a match (logic compare equal) between data stored in the memory and data presented on a set of input pins as defined in the individual device standard.

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2.1.33 – NC, NO CONNECTION
A pin to which no internal electrical connection is present or allowed to the chip.

2.1.34 – NE, NE, NON–VOLATILE ENABLE
The input, on a NVRAM, that enables the non–volatile functions ST\ & RC\ as determined by the states of S\,E\,G\, and W\.

2.1.35 – NF, NO FUNCTION
An input that is electrically connected to the device but for which the signal has no function in the device operation.

2.1.36 – NP, NO PIN
A pin position on a package where the pin has been purposely been left blank or removed after assembly. No physical pin is allowed in this position.

2.1.37 – NU, NOT USABLE
A device pin to which there may or may not be an internal connection but to which no external connections are allowed.

2.1.38 – OP, OPTIONAL
The designation for pins on which the manufacturer has the freedom to supply a specialized function not previously defined in the standard, and still have his part meet the requirements of the standard.

2.1.39 – P, P, PROGRAM or PROGRAM ENABLE, PARITY
The input on a non–volatile memory device that, when true, causes the data present on the D or DQ pins to be written into the addressed cell(s) of the device. The letter P may also be used as a suffix for data pins where an optional 9th bit, that may be used for parity, is allowed by the standard (e.g. DQP)

2.1.40 – PD(n), PRESENCE DETECT
A group of output pins, normally used on modules or cards, whose state is used to convey information about the capacity, speed, configuration, or other attributes of the device when plugged into a system.

2.1.41 – PR, PR, PAGE RESET
The input on a page select memory that, when true, unconditionally causes the page select address register to be reset to zero and the corresponding page to be selected.

2.1.42 – PS, PS, PAGE SELECT
The input on a page select memory that, when true, causes one of the pages of memory to be selected as identified by the inputs on the DQ pins (as defined in the appropriate function table) and for this page address to be stored in an internal register.

2.1.43 – Q(n), DATA OUTPUT
The outputs whose state represents the data read from the selected cells. When the device is not selected or enabled, the outputs are usually in a floating (Z, high impedance) state.

2.1.44 – RA, ROW ADDRESS
In an address multiplexed DRAM, the address field that is captured by the ROW ENABLE clock, RE\.

2.1.45 – RC, RC, RECALL
The input on a NVRAM, that transfers the non–volatile data into the RAM array.

2.1.46 – RE, RE, (RAS)ROW ENABLE
A chip enable signal that, on certain dynamic RAMs, actuates only row oriented internal circuitry.

2.1.47 – RFU, RESERVED FOR FUTURE USE
A terminal whose function is not currently defined, but which is intended to be defined in some future enhancement of this Standard. This terminal should not be used (either internally or externally) until it has been further defined.

2.1.48 – RSVD, RESERVED
In a family of standards where some devices in the family are subsets of others, terminals that are defined in some devices but not used in others. To allow for upgradeability, the unused terminals are "RESERVED" to prevent their being used. NC has often been used in similar situations.

2.1.49 – RY, READY
The output that, on some devices, signifies that no internal asynchronous operations are still in process, and that the device is available for normal functions. This signal is normally implemented so that multiple devices can be OR–tied. This signal is the inverse of BY (RY=BY\)

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2.1.50 – S(n), $\overline{S(n)}$, CHIP SELECT
The input(s) that, when any one is false, causes the device to be disabled without any significant change in the power consumption. When deselected, the outputs go to the inactive state (floating (Z) for MOS and TTL devices and low (L) for ECL devices), and the device becomes insensitive to a write command.

2.1.51 – ST, $\overline{ST}$, STORE
The input, on a NVRAM, that initiates the non–volatile data storage of the entire RAM array.

2.1.52 – Sxx, SYNCHRONOUS FUNCTION
On a synchronous memory device, any input terms that are synchronous with a clock should start with the letter S. For example: $\overline{SG}$ = Synchronous Output Enable, $\overline{SW}$ = Synchronous Write Enable.

2.1.53 – $\overline{TF}$, TEST FUNCTION
The input, on a MEMORY that, when true, causes built in on–chip test logic to be actuated and for the part to go into its test mode of operation.

2.1.54 – U, UPPER BYTE
When U is used in conjunction with a data or control term it signifies that the combined term applies to the lower byte of a two byte data interface device (e.g. $\overline{UW}$).

2.1.55 – $\overline{UB}$, UPPER BYTE ENABLE
An input that, on wordwide devices, when true, enables the upper byte data input/outputs, pins DQ8 through DQ15.

2.1.56 – $\overline{UW}$, UPPER BYTE WRITE ENABLE
An input, on wordwide devices, that, when true, causes the data present on the upper byte input/output, terminals DQ8 through DQ15, to be written into the addressed cells of the device.

2.1.57 – W, $\overline{W}$, WRITE ENABLE
The input that, when true, causes the data present on the D or the DQ pin(s) to be written into the address cell(s) of the device

2.2 MULTIPORT DRAM Pin Names

The following pin names apply primarily to specialized function pins for MPDRAM. In some situations, the names may also be applicable to other types of memories.

2.2.1 – DSF, SPECIAL FUNCTION ENABLE
The input on a device, having both serial and parallel access ports, that when true, actuates certain special operational functions.

2.2.2 – QSY, TRANSFER ACKNOWLEDGE
The output on a device having both serial and parallel access ports which signifies that a transfer of data from the parallel to the serial port, in certain special transfer cycles, has been completed.

2.2.3 – SC, SERIAL CLOCK
An input, on devices having a serial data access port, that actuates the serial transfer of data, either in or out.

2.2.4 – SDQ(n) or SQ(n), SERIAL DATA INPUT/OUTPUT
The pins, on a device having a serial data access port, that serve as serial data output(s) when in the read mode and as serial data inputs(s) when in the write mode. When the device or the serial port is not selected or enabled, the output(s) are in a floating (Z) state. Not all devices have implemented the write function from the serial port; so in that case, an alternative name for this pin is SQ(n).

2.2.5 – $\overline{SE}$, SERIAL PORT ENABLE
The input that, when true, actuates the device's serial access circuitry.

2.2.6 – SG, SERIAL PORT OUTPUT ENABLE
The input that, when true, actuates the device's serial data output circuitry.

2.2.7 – TRG, DATA TRANSFER/OUTPUT ENABLE
The input on a device having both serial and parallel access ports that, depending on the state of one or more of the other control lines of the device, either enables an internal data transfer between the serial and parallel port circuitry, or enables the data outputs of the parallel port.

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2.3 Power Pin Names

The following symbols are used to designate the power pins in a memory device. When only a single pin is provided for a given supply, the pin name is used without suffix. When multiple pins are used, a suffix may be used to designate specific pins. A numeric suffix is used to indicate the preferred order of implementation when optional redundant pins are allowed. An alphabetic suffix is used to indicate pins which have a specific power circuit or loop connection. The use of a common suffix for different supplies indicates that those pins connect to a common power loop.

2.3.1 VBB, SUBSTRATE POWER VOLTAGE

A bias voltage that maintains the substrate at a potential which is negative with respect to GND or VSS in an NMOS part.

2.3.2 VCC, LOGIC POWER VOLTAGE

The most positive potential of the two logic power supply pins. This is used for the memory device power voltage when it uses the same voltage as the logic devices in the system. VCC is also commonly used to designate the ground reference power supply voltage for ECL interface devices.

2.3.3 VDD, DRAIN POWER VOLTAGE

The primary power voltage on MOS devices that require a potential that is different from the normal system logic voltage. This is used interchangeably with VCC on devices that use the system logic voltage.

2.3.4 VEE, EMITTER POWER VOLTAGE

For ECL interface devices, the primary and most negative power supply terminal.

2.3.5 VHH, SPECIAL FUNCTION ENABLE VOLTAGE

A special high voltage logic level (super voltage) that enables special on-chip functions.

2.3.6 VPP, PROGRAMMING POWER VOLTAGE

A special high voltage supply that supplies the potential and energy for altering the state of certain non-volatile memory arrays. On some devices the presence of VPP also acts as a PROGRAM ENABLE signal (see P).

2.3.7 VSS, (GND), GROUND REFERENCE or SOURCE POWER VOLTAGE

The ground reference voltage for NMOS, CMOS, and TTL devices, commonly the reference pin for all other device pins. VSS is normally the system ground and the symbol is often used interchangeably with GND.

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2.6.14 DOUBLE BUFFERED READ TRANSFER, (DRT)

A read transfer in an array that contains two full SAM data registers which are used alternately. Each one is loaded while the contents of the other is being transferred to the SDQ(n) port. The selection of the two SAM registers is automatic.

2.6.15 RAM WRITE WITH NEW MASK, (RWNM)

A RAM write cycle in which the data bits that are to be written are controlled by a write mask which is supplied at the beginning of the write cycle on the DQ(n) terminals. A high mask bit normally enables the write function for that bit. A low mask bit leaves the data unaltered.

2.6.16 RAM WRITE WITH OLD MASK, (RWOM)

A RAM write cycle in which the data bits that are to be written are controlled by a write mask register which was loaded in a previous "load write mask" cycle. A high mask bit normally enables the write function for that bit. A low mask bit leaves the data unaltered.

2.6.17 RAM READ/WRITE, NO MASK, (RR), (RW)

A normal RAM read or write access cycle with no SAM or special RAM features or functions actuated.

2.6.18 BLOCK WRITE, NO MASK, (BW)

A RAM write cycle in which four (4) bits are written into each bit plane as defined by the contents of the color register. The four (4) bits are those locations controlled by the two LSB of the column address.

2.6.19 BLOCK WRITE WITH NEW MASK, (BWNM)

A Block Write cycle in which the data written is also controlled by the write mask supplied on the DQ(n) terminals in that cycle.

2.6.20 BLOCK WRITE WITH OLD MASK, (BWOM)

A Block Write cycle in which the data written is controlled by the contents of the write mask register which was previously loaded in a "Load Write Mask" cycle.

2.6.21 LOAD WRITE MASK REGISTER, (LWR)

A non-memory cycle in which the write mask register is loaded with a new value for use in subsequent masked write cycles.

2.6.22 LOAD COLOR REGISTER, (LCR)

A non-memory cycle in which the color register is loaded with a new value for use in subsequent special cycles which utilize its contents.

2.6.23 READ WRITE MASK REGISTER, (RWR)

A non-memory cycle in which the contents of the "Write Mask Register" are interrogated with the results placed on the RAM data terminals, DQ(n).

2.6.24 READ COLOR REGISTER, (RCR)

A non-memory cycle in which the contents of the "Color Register" are interrogated with the results placed on the RAM data terminals, DQ(n).

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2.7 Package–Related Terms

A series of package–related terms have been used in the Standard and are included in the glossary. The recently published JEDEC Standard JESD30, "Descriptive Designation System for Semiconductor–Device Packages" has obsoleted many of the package designations previously used. As new standaeds are published in Std. No. 21–C, the JESD30 approved term will be used or referenced. Commonly used industry package terms will be included in this section, but the reader is refered to JESD30 for definitions of the approved terms.

2.7.1 – CC, Leadless or Leaded Chip Carrier
A family of device packages that can be square (SCC) or rectangular (RCC) depending on the application.

2.7.2 – DIP, Dual–In–line Package
A device package configuration that has two parallel rows of pins that are spaced nominally 0.3", 0.4", or 0.6" apart with the pins on 0.1" centers.

2.7.3 – LCC, Lateral Chip Carrier
A family of device packages that can be square (SCC) or rectangular (RCC) depending on the application and can be with or without leads.

2.7.4 – PLDCC, Plastic Leaded Chip Carrier
A chip–carrier package that has a molded plastic body and J formed leads (see CC, 2.7.1). The often used term "PLCC" is ambiguous and is deprecated in favor of this term.

2.7.5 – PP, Pin Pitch
The nominal center to center distance between adjacent pins or terminals along the side of an IC package.

2.7.6 – QFP, Quad Flat Pack
A flat pack package that has leads on all four sides (see SFP).

2.7.7 – RCC, Rectangular Chip Carrier
See LCC, par 2.7.3.

2.7.8 – SCC, Square Chip Carrier
See LCC, par. 2.7.3.

2.7.9 – SFP, Square Flat Pack
A square package body of uniform thickness with flexible, flat leads exiting, on 0.050 " centers, peripherally from the center plane of the four package sides.

2.7.10 – SIMM, Single–In–line–Memory–Module
A multichip module in which the body has a SIP form and is made up primarily of memory devices. (see SIP/SIMM and ZIP/SIMM).

2.7.11 – SIP, Single–in–line Package
A rectangular package with the leads along one side, normally one of the long sides.

2.7.12 – SIP/SIMM, SIP/SIMM Module
A multichip memory module in which the body has a SIP form, and the pins are formed into an in–line configuration.

2.7.13 – SOG, (SOP), Small Outline, Gull Wing Lead
A surface mount package that conforms to the "small outline" concept and which has the leads formed into a "gull wing" configuration.

2.7.14 – SOJ, Small Outline J Lead
A surface mount package that conforms to the "small outline" concept and which has the leads formed into a "J" configuration.

2.7.15 – TSOP, Types I and II, TSOP1, TSOP2
These are small outline packages with gull wing lead formation and whose thickness is substantially less than the standard SOG package. TSOP1 has the leads on the end or short edges of the package while TSOP2 has the leads on the sides or long edges of the package. The lead pitch is often finer than that commonly used in the standard SOG package.

2.7.16 – ZIP, Zig–Zag In–line Package
A package whose body resembles that of a DIP, except that the external leads are all along one edge of the package. The leads emerge on 0.050" centers and are formed alternately into two rows of pins that are separated by 0.100" with the individual leads on 0.100" centers along the rows. The package is mounted standing on one edge.

2.7.17 – ZIP/SIMM, ZIP/SIMM Module
A multichip memory module in which the body has a SIP form but the leads have been formed into a ZIP foot–print.

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3.4.1.1 – 4K BY 8 EPROM IN DIP, TYPE A

CAPACITY—4K WORDS OF 8 BITS, TYPE A
PACKAGE—24 PIN DIP, 0.6" WIDE
PIN ASSIGNMENT—Fig. 3.4.1–1

3.4.1.2 – 4K AND 8K BY 8 EPROM IN DIP,

CAPACITY—4K, 8K WORDS OF 8 BITS,
PACKAGE—24 PIN DIP, 0.6" WIDE
PIN ASSIGNMENT—Fig. 3.4.1–1

3.4.1.3 – 8K TO 64K BY 8 EPROM FAMILY IN DIP,

CAPACITY—8K, 16K, 32K, 64K WORDS OF 8 BITS,
PACKAGE—28 PIN DIP, 0.6" WIDE
PIN ASSIGNMENT—Fig. 3.4.1–2

3.4.1.4 – 2K TO 512K BY 8 EPROM FAMILY IN RCC

CAPACITY—2K, 4K, 8K, 16K, 32K, 64K, 128K, 256K, & 512K WORDS OF 8 BITS
PACKAGE—32 PAD (PIN) RCC, 0.450" BY 0.550"
PIN ASSIGNMENT—Fig. 3.4.1–3

3.4.1.5 – 32K TO 512K BY 8 EPROM FAMILY IN SOJ,

CAPACITY—32K, 64K, 128K, 256K, 512K WORDS OF 8 BITS,
PACKAGE—28 OR 32 PIN SOJ, 0.4" WIDE OR NOT DEFINED
PIN ASSIGNMENT—Fig. 3.4.1–4

3.4.1.6 – 128K TO 1M BY 8 EPROM FAMILY IN DIP,

CAPACITY—128K, 256K, 512K, 1M WORDS OF 8 BITS,
PACKAGE—32 PIN DIP, 0.6" WIDE
PIN ASSIGNMENT—Fig. 3.4.1–5

3.4.1.7 – 64K TO 512K BY 9 EPROM FAMILY IN DIP,

CAPACITY—64K, 128K, 256K, 512K WORDS OF 9 BITS,
PACKAGE—32 PIN DIP, 0.6" WIDE
PIN ASSIGNMENT—Fig. 3.4.1–6

3.4.1.8 – 2 TO 64 X 16K BY 8 PAGE SELECT EPROM FAMILY IN DIP,

CAPACITY—32K, 64K, 128K, 256K, 512K, 1M WORDS OF 8 BITS,
—2, 4, 8, 16, 32, 64 PAGES OF 16K WORDS OF 8 BITS,
LOGIC FEATURES—Selectable pages of 16K words
PACKAGE—28 PIN DIP, 0.6" WIDE
PIN ASSIGNMENT—Fig. 3.4.1–7

This device contains multiple pages of 16K words which can be selected and the address for which is stored in an internal register.

3.4.1.9 – 128K TO 512K BY 8 EPROM FAMILY IN TSOP–1,

CAPACITY—128K, 256K, 512K WORDS OF 8 BITS,
PACKAGE—32 PIN TSOP–1, 8 mm X 20 mm. PP=0.5 mm
PIN ASSIGNMENT—Fig. 3.4.1–8

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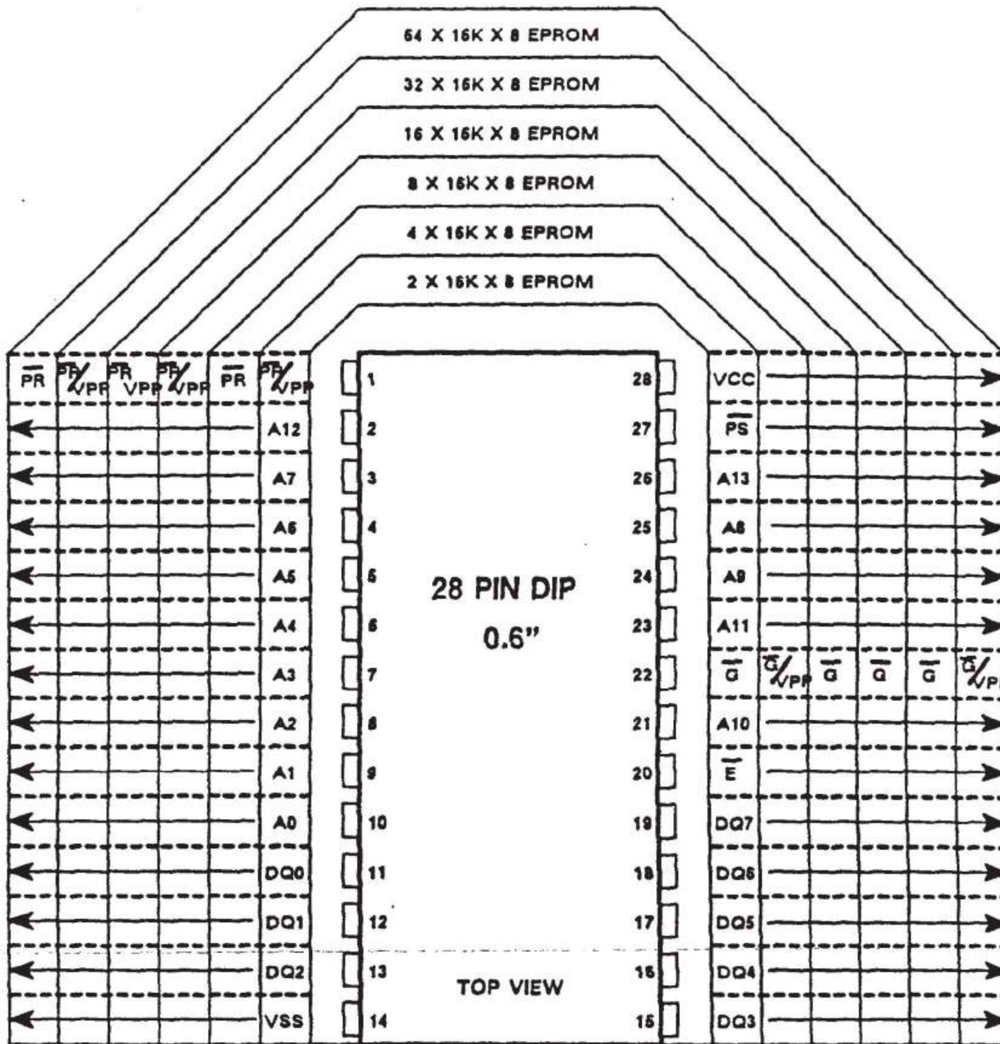

FUNCTION TABLE

MODE \ PIN	$\overline{PS}$	$\overline{PR}$	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0
ASYN. RESET (PAGE 0)	H	L	X	X	X	X	X	X
PAGE 0	L	H	L	L	L	L	L	L
PAGE 1	L	H	L	L	L	L	L	H
PAGE 2	L	H	L	L	L	L	H	L
PAGE 3	L	H	L	L	L	L	H	H
PAGE 4	L	H	L	L	L	H	L	L
PAGE 5	L	H	L	L	L	H	L	H
PAGE 6	L	H	L	L	L	H	H	L
PAGE 7	L	H	L	L	L	H	H	H
PAGE n		OUTPUTS = n (BINARY) ACTIVE HIGH						
PAGE 63	L	H	H	H	H	H	H	H

FIGURE 3.4.1-7
2 TO 64 X 16K BY 8 PAGE SELECT EPROM IN DIP

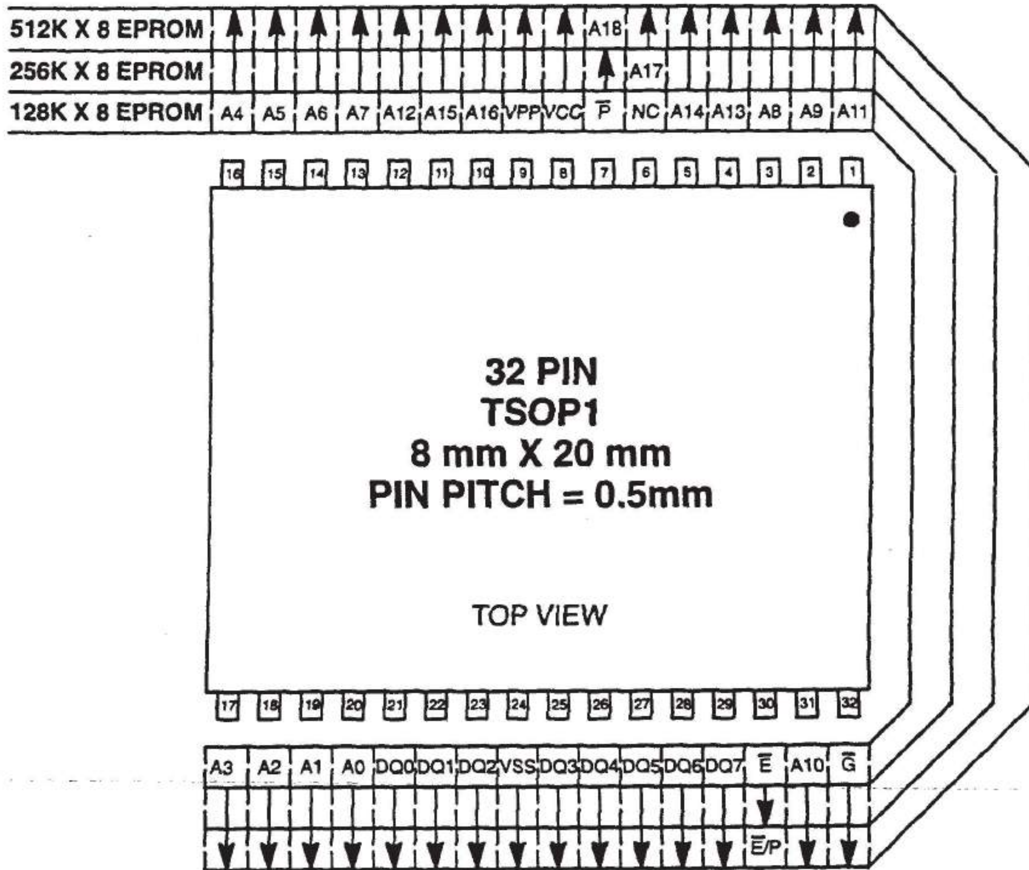

FIGURE 3.4.1–8
128K TO 512K BY 8 EPROM IN TSOP–1

Release 4

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3.4.2.1 – 32K TO 256K BY 16 EPROM IN DIP

CAPACITY—32K TO 256K WORDS OF 16 BITS,
PACKAGE—40 PIN DIP, 0.6" WIDE
PIN ASSIGNMENTS—Fig. 3.4.2–1

3.4.2.2 – 32K TO 256K BY 16 EPROM IN SCC

CAPACITY—32K TO 256K WORDS OF 16 BITS,
PACKAGE—44 PAD (PIN) RCC, 0.650" X 0.650"
PIN ASSIGNMENTS—Fig. 3.4.2–2

3.4.2.3 – 16K TO 256K BY 16 ADDRESS/DATA MX EPROM IN DIP

CAPACITY—16K TO 256K WORDS OF 16 BITS,
LOGIC FEATURES—Address and Data MULTIPLEXED onto common pins.
PACKAGE—28 PIN DIP, 0.6" WIDE
PIN ASSIGNMENTS—Figs. 3.4.2–3

3.4.2.4 – 16K TO 256K BY 16 ADDRESS/DATA MX EPROM IN RCC

CAPACITY—16K TO 256K WORDS OF 16 BITS,
LOGIC FEATURES—Address and Data MULTIPLEXED onto common pins.
PACKAGE—32 PIN (PAD) RCC, 0.450" X 0.550"
PIN ASSIGNMENTS—Figs. 3.4.2–4

3.4.2.5 – 4M TO 128M BY 16 EPROM or OTP IN DIP AND SOP

CAPACITY—4M, 8M, 16M, 32M, 64M, 128M WORDS OF 16 BITS
PACKAGE—48 and 52 PIN DIP or SOP, 0.6" WIDE
PIN ASSIGNMENTS—Fig. 3.4.2–5

3.4.2.6 – 512K and 1M BY 16 EPROM IN SCC

CAPACITY—512K & 1M WORDS OF 16 BITS
PACKAGE—44TERMINAL SCC, 0.650" X 0.650"
PIN ASSIGNMENTS—Fig. 3.4.2–6

3.4.2.7 – 64K TO 256K BY 16 EPROM IN TSOP–1

CAPACITY—64K, 128K & 256K WORDS OF 16 BITS
PACKAGE—48 PIN TSOP–1 12 mm X 20 mm, PP=0.5 mm
PIN ASSIGNMENTS—Fig. 3.4.2–7

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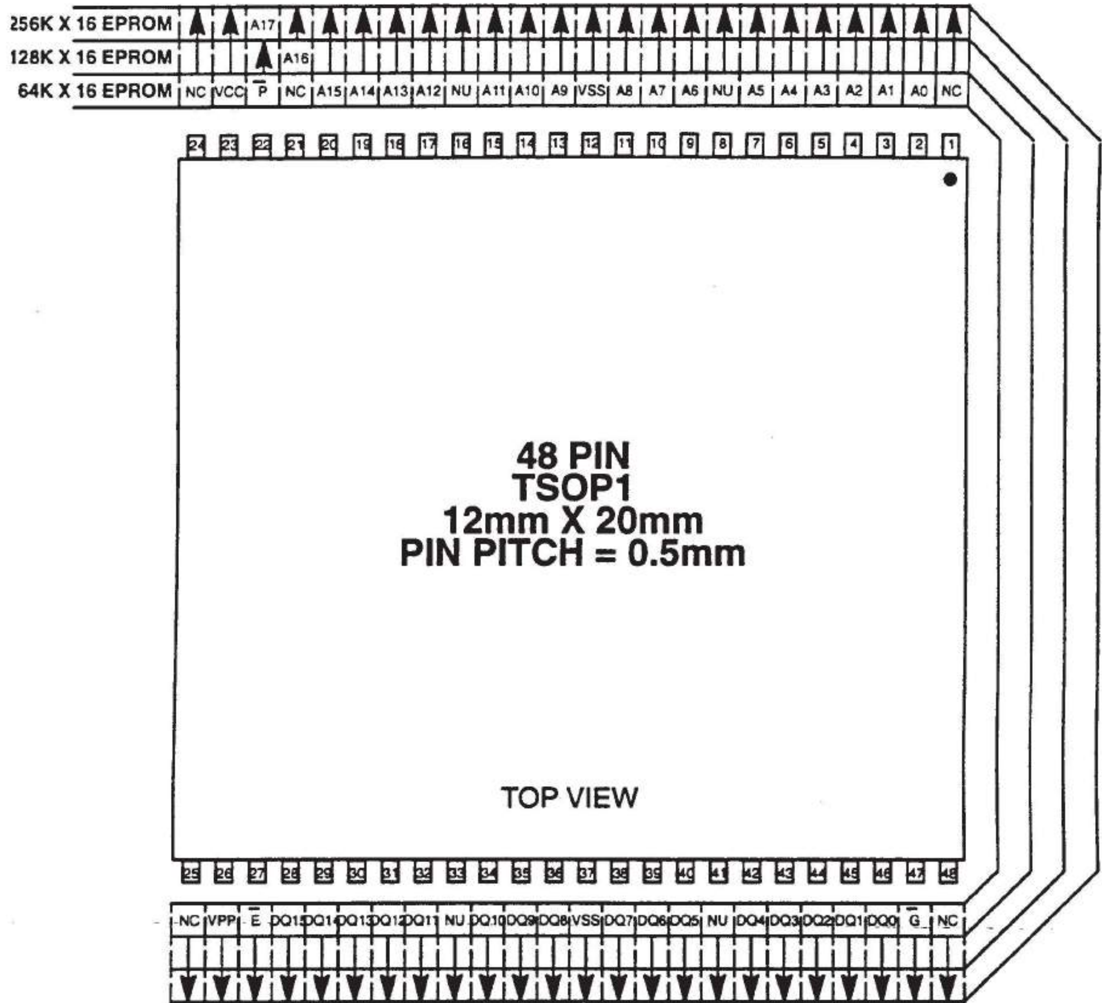

FIGURE 3.4.2–7

64K BY 256K BY 16 EPROM IN TSOP–1

3.7 Static Random Access Memory (SRAM)

The following SRAM standards were developed by Committees 42.1 and 42.3. The devices described are compatible with one of several logic circuit families as defined. The device standards require that the memory devices must operate with signal levels and power supply voltages that are consistent with those used in the logic family(s) specified. The nominal power supply voltages for the three families in use are as follows:

TTL, VCC = 5.0 V
10K ECL, VEE = 5.2 V
100K ECL, VEE = 4.5 V

The standards described on this page are applicable to multiple device configurations as noted in the individual standards.

3.7.1 – JTAG Extension to Revolutionary Pinout SRAM Devices

This standard establishes a convention to provide uniform guidance when it is desired to add the IEEE 1149.1 Boundary Scan feature (JTAG) to a device with a pinout that follows the JEDEC SRAM Revolutionary pinout (RPO, devices with redundant centered power pins). The convention shown if Fig. 3.7–1 shows the convention for this addition. This convention applies to all existing and future RPO SRAM devices in DIP, SOJ, TSOP2, and any other two–sided packages that might be used in the future.

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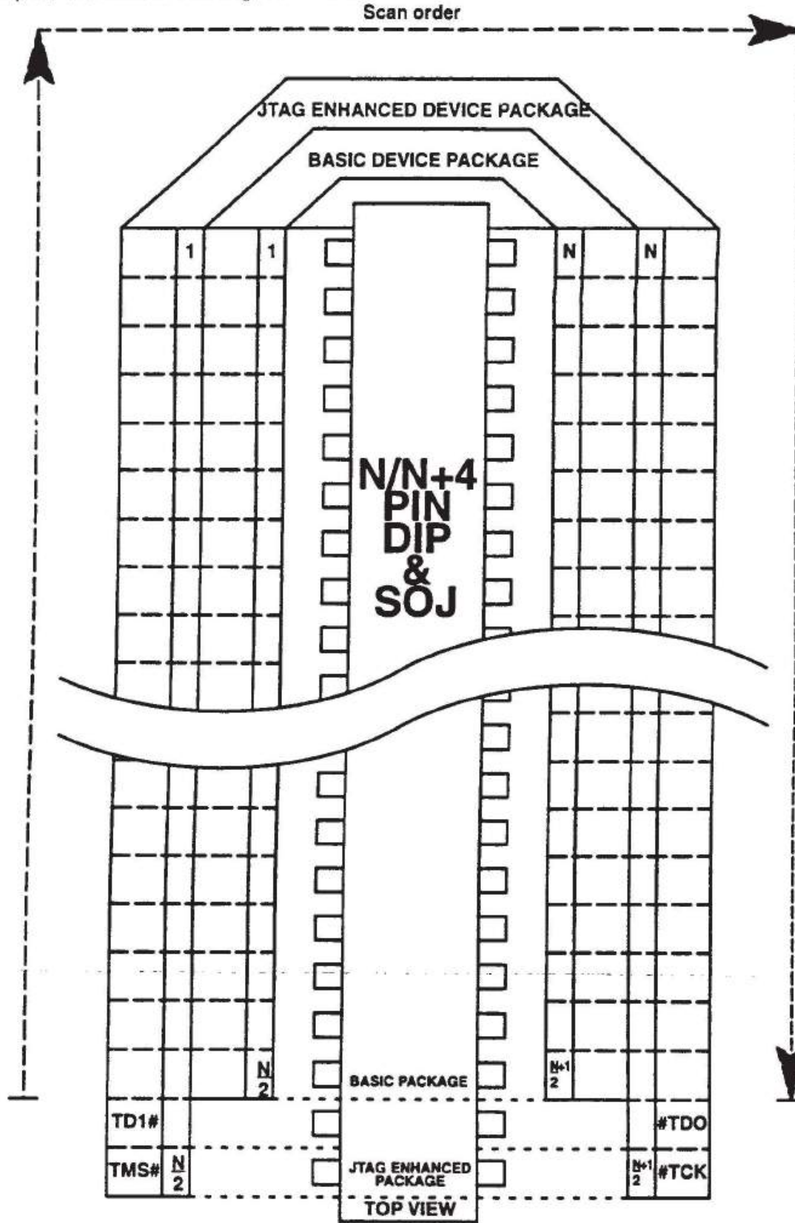
Add IEEE 1149.1 Boundary–Scan (JTAG), as an option, to any existing or future two–sided JEDEC Revolutionary SRAM pinouts by increasing package pin count by 4 as shown. Scan all of the original signal pins clockwise starting from TDI.



– These pins are JTAG specific pins defined in IEEE Std. 1149.1

FIGURE 3.7–1

JTAG ADDITION TO REVOLUTIONARY PINOUT SRAM

3.7.1.1 – .25K & 1K BY 1 TTL SRAM IN DIP

CAPACITY—.25K & 1K WORDS OF 1 BIT
PACKAGE—16 PIN DIP, 0.3" WIDE
PIN ASSIGNMENT—Fig. 3.7.1–1
This standard was developed by Committee 42.1.

3.7.1.2 – .25K & 1K BY 1 TTL SRAM IN SCC

CAPACITY—.25K & 1K WORDS OF 1 BIT
PACKAGE—20 PIN (PAD) SCC, 0.350" X 0.350"
PIN ASSIGNMENT—Fig. 3.7.1–2
This standard was developed Committee 42.1.

3.7.1.3 – 4K TO 2M BY 1 TTL SRAM FAMILY IN DIP

CAPACITY—4K, 16K, 64K, 256K, 1M, 2M WORDS OF 1 BIT
PACKAGE—18, 20, 22, 24, or 28 PIN DIP, 0.3", or 0.4" wide or UNDEFINED
PIN ASSIGNMENT—Fig. 3.7.1–3

3.7.1.4 – 16K BY 1 TTL SRAM IN RCC

CAPACITY—16K WORDS OF 1 BIT
PACKAGE—20 PAD (PIN) RCC, 0.290" x 0.425"
PIN ASSIGNMENT—Fig. 3.7.1–4

3.7.1.5 – 64K BY 1 TTL SRAM IN RCC

CAPACITY—64K WORDS OF 1 BIT
PACKAGE—22 PAD (PIN) RCC, 0.290" X 0.490"
PIN ASSIGNMENT—Fig. 3.7.1–5

3.7.1.6 – 16K TO 2M BY 1 TTL SRAM IN SOJ

CAPACITY—16K, 64K, 256K, 1M, 2M WORDS OF 1 BIT
PACKAGE—24 or 28 PIN SOJ, 0.3" or 0.4" wide or UNDEFINED
PIN ASSIGNMENT—Fig. 3.7.1–6

3.7.1.7 – 256K TO 16M BY 1 TTL SRAM AND 4M BY 1 SSRAM IN DIP, SOJ, AND TSOP–2

CAPACITY—256K, 1M, 4M, AND 16M WORDS OF 1 BIT
LOGIC FEATURES—OPTIONAL OUTPUT ENABLE FOR SOME DENSITIES
—SEPARATE DATA INPUT & OUTPUT PINS
—4M DENSITY PART APPROVED AS SYNCHRONOUS SRAM
PACKAGE—28 or 32 PIN SOJ, & TSOP2, 0.3", 0.4". or 0.5" WIDE with PP=0.05"
—28 0r 32 PIN DIP, 0.3", 0.4" with PP=0.1", or 0.6" with PP=0.07".
SPECIAL FEATURES—MILTIPLE CENTERED POWER PINS
PIN ASSIGNMENT—Fig. 3.7.1–7

3.7.1.8 – 256K BY 1 TTL SRAM IN RCC

CAPACITY—256K WORDS OF 1 BIT
PACKAGE—28 PAD (PIN) RCC, 0.350" X 0.550"
PIN ASSIGNMENT—Fig. 3.7.1–8

3.7.1.9 – 4M AND 16M SRAM, CONFIGURABLE TO X1 OR X4 IN DIP, SOJ, AND TSOP–2

CAPACITY—4M, 16M WORDS OF 1 BITOR 1M, 4M WORDS OF 4 BITS
LOGIC FEATURES—THE DATA INTERFACE CONFIGURATION MAY BE SET TO X1 OR X4 UNDER CONTROL OF THE SIGNAL LEVEL TO A CONFIGURATION INPUT
PACKAGE—4M DENSITY, 32 PIN DIP, 0.6" with PP=0.07"; 32 PIN SOJ and TSOP–2, 0.4"
—16M DENSITY; 36 PIN SOJ AND TSOP–2, 0.5"
PIN ASSIGNMENT—Fig. 3.7.1–9

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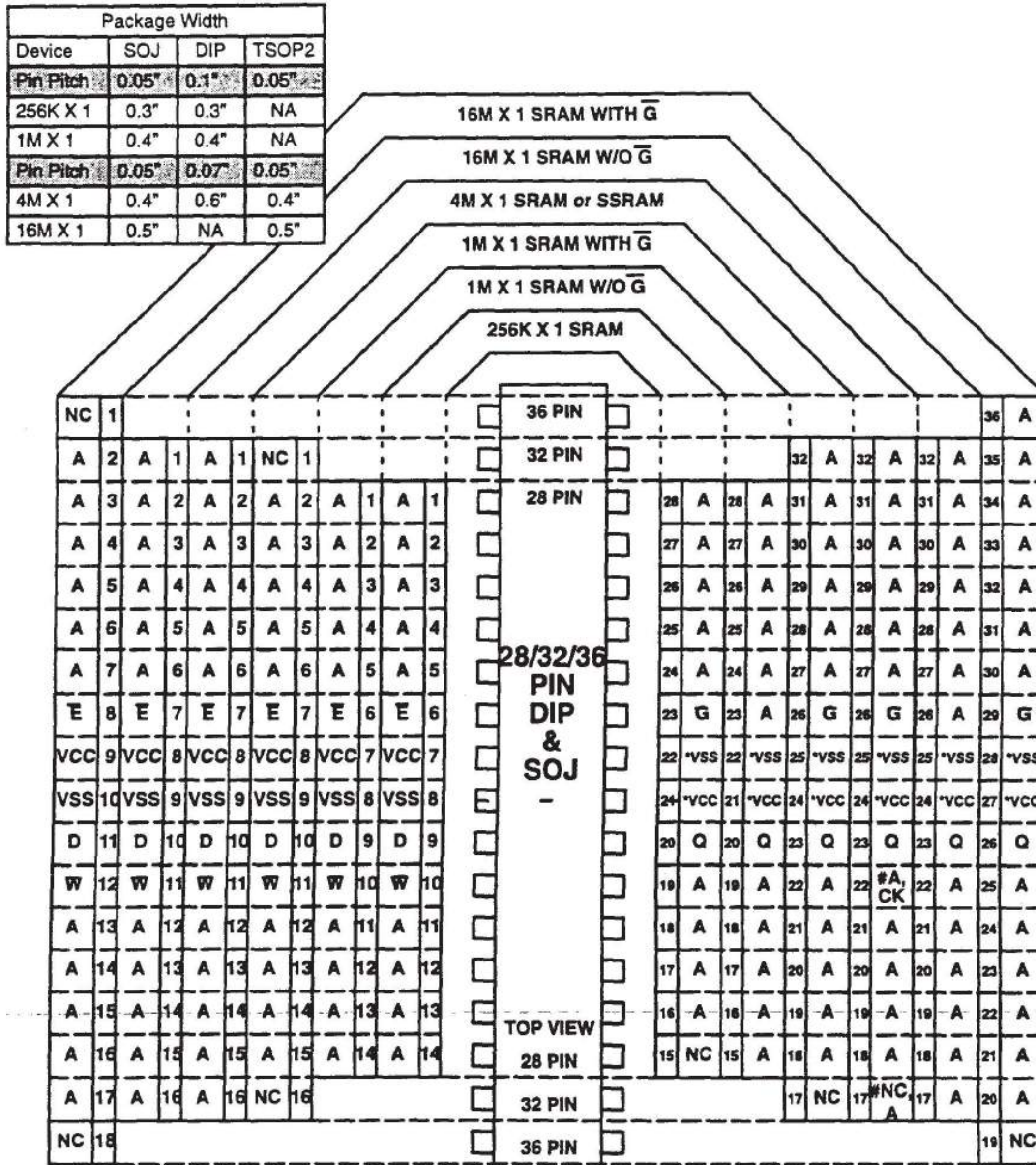
jx0056-032



Package Width			
Device	SOJ	DIP	TSOP2
Pin Pitch	0.05"	0.1"	0.05"
256K X 1	0.3"	0.3"	NA
1M X 1	0.4"	0.4"	NA
Pin Pitch	0.05"	0.07"	0.05"
4M X 1	0.4"	0.6"	0.4"
16M X 1	0.5"	NA	0.5"

* These power pins may be VCC OR VCCA (VSS OR VSSA) as a Manufacturer option

NOTE: For the 4M X 1 devices, the pin assignments for pins 17 & 22 are different for the SRAM and SSRAM as follows.
For SRAM, P17 = NC, P22 = A
For SSRAM, P17 = A, P22 = CK

FIGURE 3.7.1-7

256K TO 16M BY 1 TTL SRAM AND SSRAM FAMILY IN DIP, TSOP2, AND SOJ

Jedec 0007712

jx0056-033

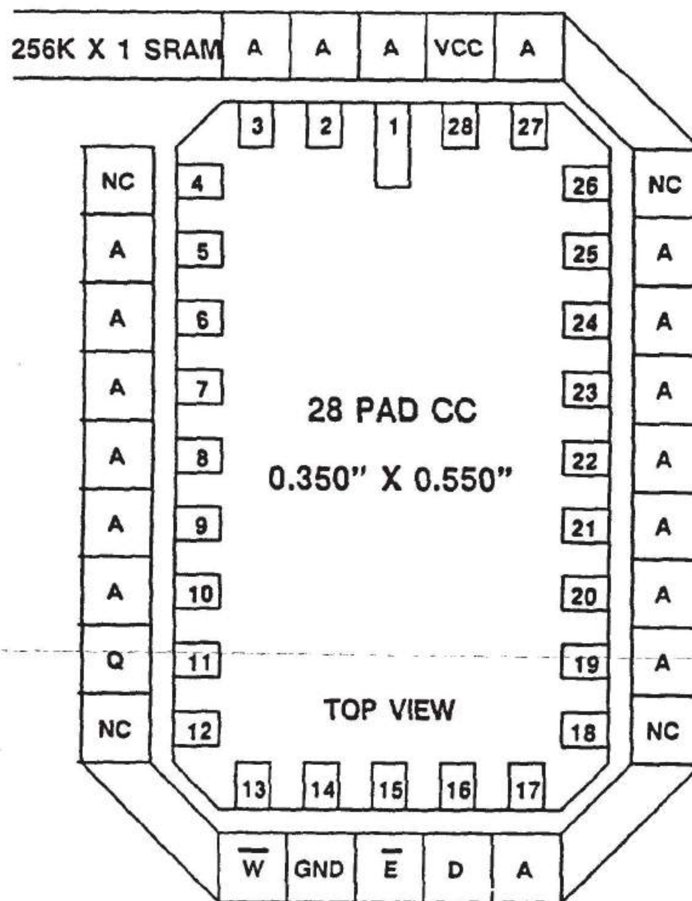


FIGURE 3.7.1-8
256K BY 1 TTL SRAM IN RCC

Jedec 0007713

jx0056-034

Package Width			
Device	SOJ	DIP	TSOP2
Pin Pitch	0.05"	0.07"	0.05"
4M	0.4"	0.6"	0.4"
16M	0.5"	NA	0.5"

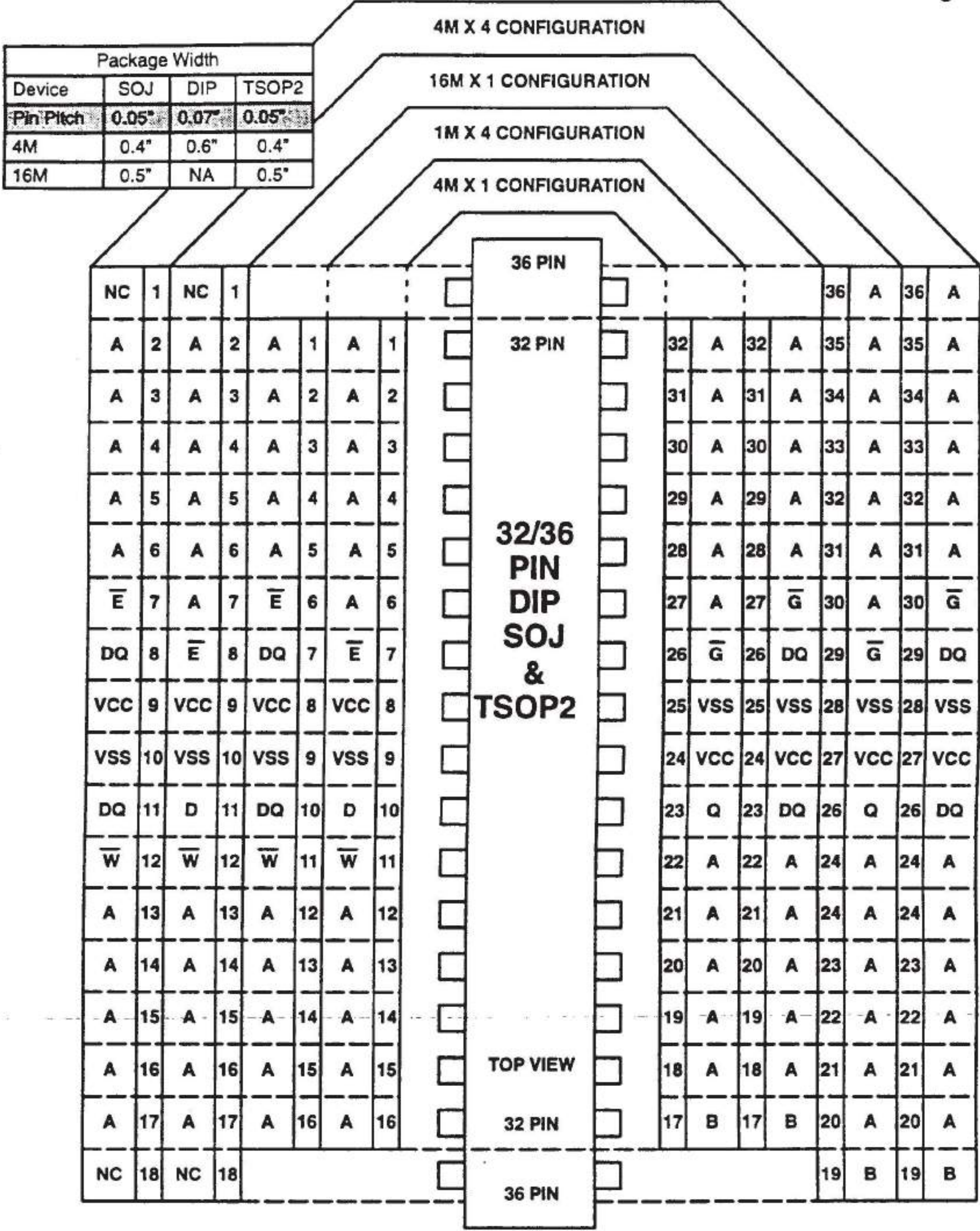


FIGURE 3.7.1-9

4M AND 16M CONFIGURABLE SRAM IN DIP, TSOP2, AND SOJ

3.7.2.1 – 1K TO 256K BY 1 ECL SRAM FAMILY IN DIP

CAPACITY—1K, 4K, 16K, 64K & 256K WORDS OF 1 BIT
ELECTRICAL INTERFACE—10K or 100K ECL
FAMILY—1K, 4K, 16K, & 256K = 10K & 100K ECL
—64K = 10K ECL
PACKAGE—16, 18, 20 OR 22 DIP, 0.4" WIDE
PIN ASSIGNMENT—Fig. 3.7.2-1

3.7.2.2 – 256K TO 16M BY 1 ECL SRAM AND 4M BY 1 SSRAM IN DIP, SOJ, AND TSOP-2

CAPACITY—256K, 1M, 4M, AND 16M WORDS OF 1 BIT
ELECTRICAL INTERFACE—10K or 100K ECL
LOGIC FEATURES—OPTIONAL OUTPUT ENABLE FOR SOME DENSITIES
—SEPARATE DATA INPUT & OUTPUT PINS
—4M DENSITY PART APPROVED AS SYNCHRONOUS SRAM
CAPACITY—256K, 1M, 4M, AND 16M WORDS OF 1 BIT
PACKAGE—28 or 32 PIN SOJ, & TSOP2, 0.3", 0.4". or 0.5" WIDE with PP=0.05"
—28 Or 32 PIN DIP, 0.3", 0.4" with PP=0.1", or 0.6" with PP=0.07".
SPECIAL FEATURES—MILTIPLE CENTERED POWER PINS
PIN ASSIGNMENT—Fig. 3.7.2-2

3.7.2.3 – 64K AND 256K BY 1 ECL SRAM IN FLATPACK

CAPACITY—64K, & 256K WORDS OF 1 BIT
ELECTRICAL INTERFACE—10K or 100K ECL
PACKAGE—22, OR 24 PIN FP, 0.535" WIDE, 0.030 LEAD PITCH
PIN ASSIGNMENT—Fig. 3.7.2-3

3.7.2.4 – 256K TO 16M BY 1 ECL SSRAM FAMILY IN DIP, SOJ, AND TSOP-2

CAPACITY—256K, 1M, 4M, & 16M WORDS OF 1 BIT
ELECTRICAL INTERFACE—10K or 100K ECL
PACKAGE—28, 32, or 36 PIN SOJ, & TSOP2, 0.3", 0.4". or 0.5" wide, PP=0.05"
—28 Or 32 PIN DIP, 0.3", 0.4" with PP=0.1", or 0.6" with PP=0.07".
SPECIAL FEATURES—MILTIPLE CENTERED POWER PINS
—DIFFERENTIAL CLOCKS
PIN ASSIGNMENT—Fig. 3.7.2-4

Jedec 0007715

jx0056-036

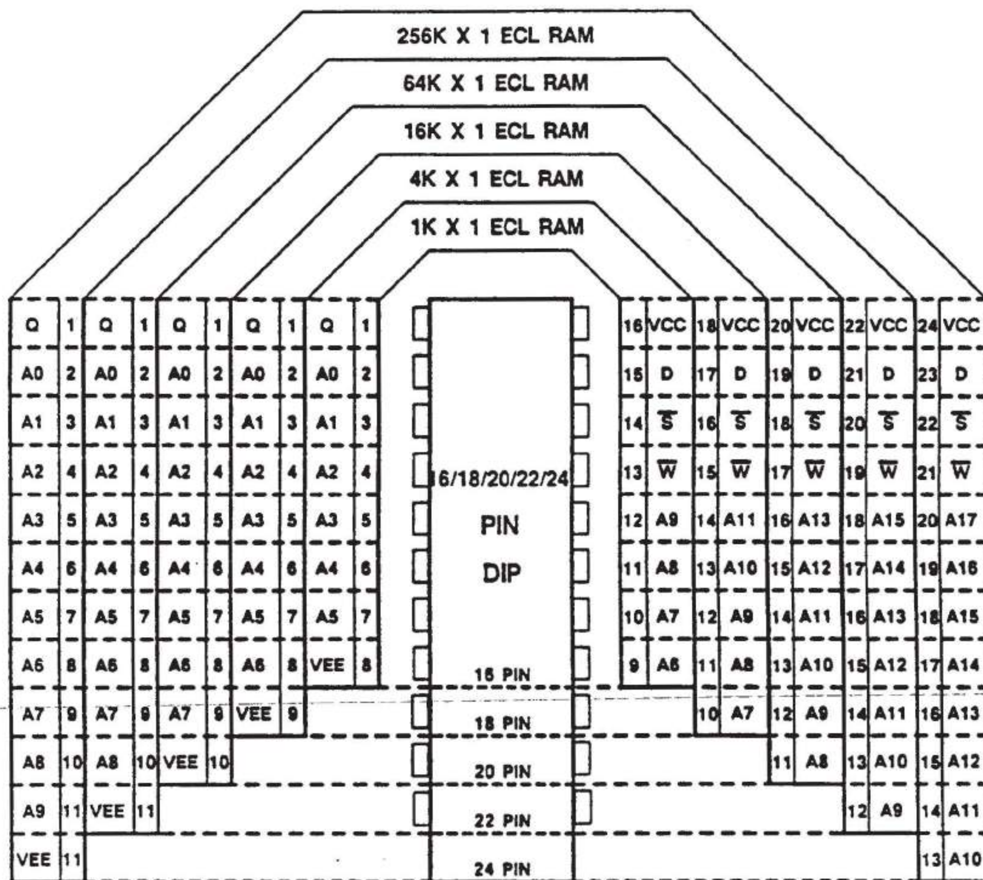
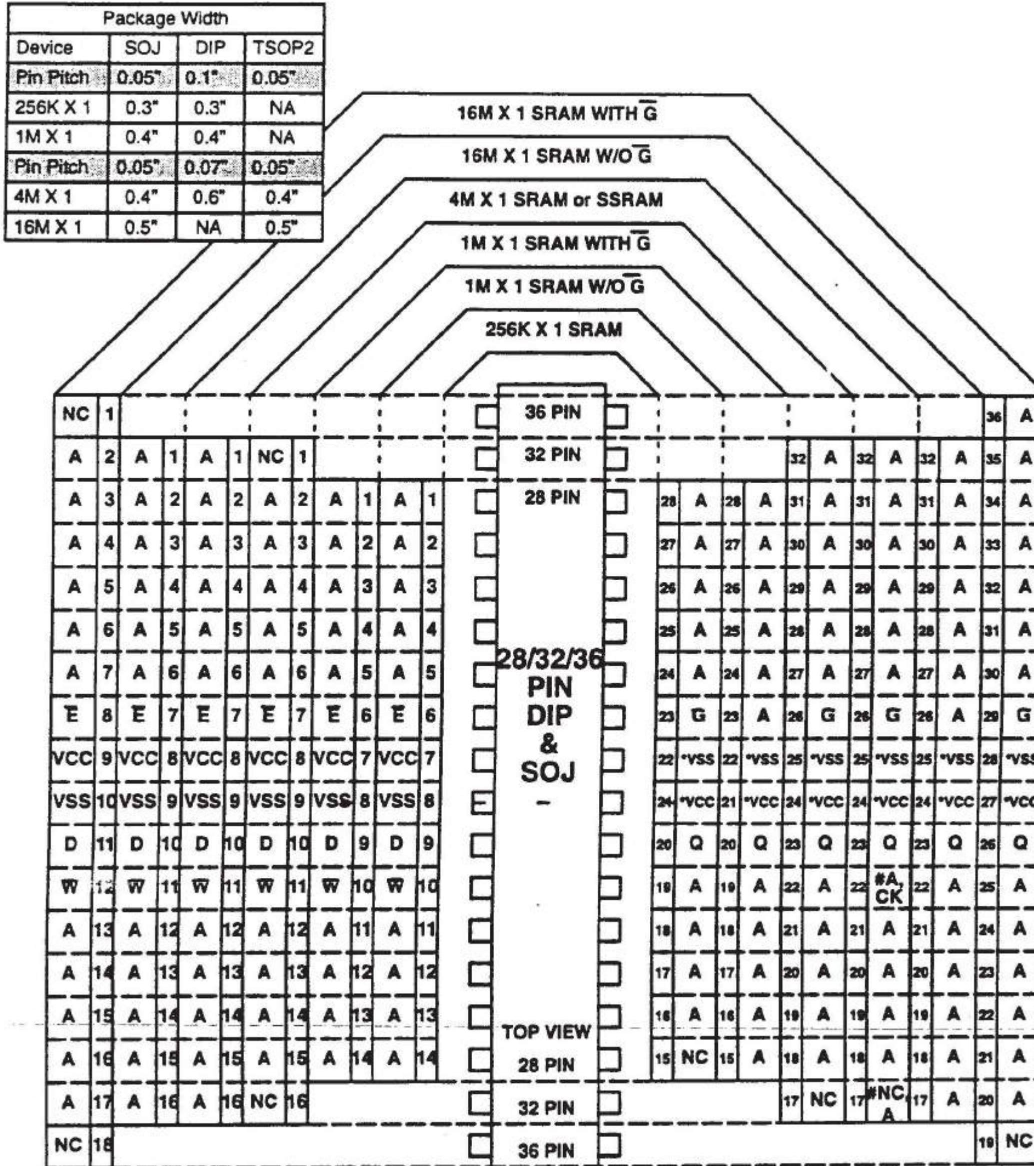


FIGURE 3.7.2-1
1K TO 256K BY 1 ECL SRAM FAMILY IN DIP

Jedec 0007716

jx0056-037



Package Width			
Device	SOJ	DIP	TSOP2
Pin Pitch	0.05"	0.1"	0.05"
256K X 1	0.3"	0.3"	NA
1M X 1	0.4"	0.4"	NA
Pin Pitch	0.05"	0.07"	0.05"
4M X 1	0.4"	0.6"	0.4"
16M X 1	0.5"	NA	0.5"

* These power pins may be VCC OR VCCA (VSS OR VSSA) as a Manufacturer option

NOTE: For the 4M X 1 devices, the pin assignments for pins 17 & 22 are different for the SRAM and SSRAM as follows.
For SRAM, P17 = NC, P22 = A
For SSRAM, P17 = A, P22 = CK

FIGURE 3.7.2-2

256K TO 16M BY 1 ECL SRAM AND SSRAM FAMILY IN DIP, TSOP2, & SOJ

Release 4

Jedec 0007717

jx0056-038

64K X 4	Pin	256K X 1	Pin	64K X 1	Pin		Pin	64K X 1	Pin	256K X 1	Pin	64K X 4
D0	1	A	1	A	1		22	A	24	A	28	$\overline{S}$
D1	2	A	2	A	2		21	A	23	A	27	$\overline{W}$
D2	3	$\overline{W}$	3	$\overline{W}$	3		20	A	22	A	26	A
D3	4	$\overline{S}$	4	$\overline{S}$	4		19	A	21	A	25	A
Q0	5	D	5	D	5		18	A	20	A	24	A
Q1	6	VCC	6	VCC	6		17	VEE	19	A	23	A
VCC	7	Q	7	Q	7		16	A	18	VEE	22	A
Q2	8	A	8	A	8		15	A	17	A	21	VEE
Q3	9	A	9	A	9		14	A	16	A	20	A
A	10	A	10	A	10		13	A	15	A	19	A
A	11	A	11	A	11		12	A	14	A	18	A
A	12	A	12						13	A	17	A
A	13										16	A
A	14										15	A

FIGURE 3.7.2–3
64K AND 256K BY 1 ECL RAM IN FP

Jedec 0007718

ix0056-039

Package Width			
Device	SOJ	DIP	TSOP2
Pin Pitch	0.05"	0.1"	0.05"
256K X 1	0.3"	0.3"	NA
1M X 1	0.4"	0.4"	NA
Pin Pitch	0.05"	0.07"	0.05"
4M X 1	0.4"	0.6"	0.4"
16M X 1	0.5"	NA	0.5"

16M X 1 SSRAM

4M X 1 SSRAM

1M X 1 SSRAM

256K X 1 SSRAM

16M X 1	Pin	4M X 1	Pin	1M X 1	Pin	256K X 1	Pin	28/32/36 PIN DIP & SOJ	Pin	256K X 1	Pin	1M X 1	Pin	4M X 1	Pin	16M X 1
NC	1							36 PIN							36	A
A	2	A	1	NC	1			32 PIN			32	A	32	A	35	A
A	3	A	2	A	2	A	1	28 PIN	28	A	31	A	31	A	34	A
A	4	A	3	A	3	A	2		27	A	30	A	30	A	33	A
A	5	A	4	A	4	A	3		26	A	29	A	29	A	32	A
A	6	A	5	A	5	A	4		25	A	28	A	28	A	31	A
A	7	A	6	A	6	A	5		24	A	27	A	27	A	30	A
$\overline{E}$	8	$\overline{E}$	7	$\overline{E}$	7	$\overline{E}$	6		23	A	26	A	26	A	29	A
VCC	9	VCC	8	VCC	8	VCC	7		22	*VSSA	25	*VSSA	24	*VSSA	28	*VSSA
VSS	10	VSS	9	VSS	9	VSS	8		21	*VCCA	24	*VCCA	24	*VCCA	27	*VCCA
D	11	D	10	D	10	D	9		20	Q	23	Q	23	Q	26	Q
$\overline{W}$	12	$\overline{W}$	11	$\overline{W}$	11	$\overline{W}$	10		19	CK	22	CK	22	CK	25	CK
A	13	A	12	A	12	A	11		18	$\overline{CK}$	21	$\overline{CK}$	21	$\overline{CK}$	24	$\overline{CK}$
A	14	A	13	A	13	A	12		17	A	20	A	20	A	23	A
A	15	A	14	A	14	A	13		16	A	19	A	19	A	22	A
A	16	A	15	A	15	A	14	TOP VIEW 28 PIN	15	A	18	A	18	A	21	A
A	17	A	16	NC	16			28 PIN			17	A	17	A	20	A
NC	18							36 PIN							19	A

* These power pins may be VCC OR VCCA (VSS OR VSSA) as a Manufacturer option

FIGURE 3.7.2–4

256K TO 16M BY 1 ECL SSRAM FAMILY IN DIP, SOJ, & TSOP2

Jedec 0007719

jx0056-040

3.7.3.1 16 BY 4, INVERTING AND NON INVERTING TTL SRAM IN DIP & SCC

CAPACITY--16 WORDS OF 4 BITS
LOGIC FEATURES--This part is available in DATA non inverting and inverting versions
There are two package versions of this part: one in DIP and the other in SCC

PACKAGE--16 PIN DIP, 0.300" WIDE
PIN ASSIGNMENT--Fig. 3.7.3-1
PACKAGE--20 PAD (PIN) SCC, 0.350" BY 0.350"
PIN ASSIGNMENT--Fig. 3.7.3-2
This standard was developed by Committee 42.1.

3.7.3.2 .25K BY 4 TTL SRAM IN DIP & RCC

CAPACITY--.25K WORDS OF 4 BITS
FAMILY--TTL
There are two versions of this part: one in DIP and the other in RCC

PACKAGE--22 PIN DIP, 0.400" WIDE
PIN ASSIGNMENT--Fig. 3.7.3-3
PACKAGE--28 PAD (PIN) RCC, 0.350" BY 0.550"
PIN ASSIGNMENT--Fig. 3.7.3-4
This standard was developed by Committee 42.1.

3.7.3.3 256 BY 4 TTL SRAM WITH $\overline{G}$ IN SCC

256 WORDS OF 4 BITS
LOGIC FEATURES--SEPARATE DATA INPUT & OUTPUT PINS
PACKAGE--24 PAD (PIN) SCC, 0.4" X 0.4"
PIN ASSIGNMENT--Fig. 3.7.3-5
This standard was developed by Committee 42.1.

3.7.3.4 4K TO 64K BY 4 TTL SRAM WITHOUT G FAMILY IN DIP

4K, 16K, 64K WORDS OF 4 BITS
PACKAGE--20,22, or 24 PIN DIP, 0.3" WIDE
PIN ASSIGNMENT--Fig. 3.7.3-6

3.7.3.5 4K BY 4 TTL SRAM IN RCC

CAPACITY--4K WORDS OF 4 BITS
PACKAGE--20 PAD (PIN) RCC, 0.290" BY 0.425"
PIN ASSIGNMENT--Fig. 3.7.3-7

3.7.3.6 4K TO 1M BY 4 TTL SRAM WITH $\overline{G}$ FAMILY IN DIP

4K, 16K, 64K, 256K, & 1M WORDS OF 4 BITS
LOGIC FEATURES--Output Enable, $\overline{G}$
PACKAGE--22, 24 PIN DIP, 0.3" WIDE
--28 PIN DIP, 0.4" WIDE
--32 PIN DIP, UNDEFINED
PIN ASSIGNMENT--Fig. 3.7.3-8

3.7.3.7 16K TO 256K BY 4 TTL SRAM WITH AND WITHOUT $\overline{G}$ FAMILY IN RCC

16K, 64K, 256K WORDS OF 4 BITS
LOGIC FEATURES--Optional Output Enable
PACKAGE--28 PAD (PIN) RCC, 0.350" X 0.550"
PIN ASSIGNMENT--Fig. 3.7.3-9

3.7.3.8 16K BY 4 TTL SRAM IN RCC

CAPACITY--16K WORDS OF 4 BITS
PACKAGE--22 PAD (PIN) RCC, 0.290" X 0.490"
PIN ASSIGNMENT--Fig. 3.7.3-10

Jedec 0007720

jx0056-041

3.7.3.9 – 4K TO 1M BY 4 TTL SRAM WITH AND WITHOUT G FAMILY IN SOJ

4K, 16K, 64K, 256K, & 1M WORDS OF 4 BITS
LOGIC FEATURES—Optional Output Enable for some densities
—COMMON DATA INPUT & OUTPUT PINS
PACKAGE—24 or 28 PIN SOJ, 0.3" WIDE
—28 PIN SOJ, 0.4" WIDE
—32 PIN SOJ, UNDEFINED
PIN ASSIGNMENT—Fig. 3.7.3–11

3.7.3.10 – 64K TO 4M BY 4 TTL SRAM IN DIP, SOJ, AND TSOP–2

CAPACITY—64K, 256K, 1M, AND 4M WORDS OF 4 BIT
LOGIC FEATURES—COMMON DATA INPUT & OUTPUT PINS
—OPTIONAL OUTPUT ENABLE FOR SOME DENSITIES
PACKAGE—28, 32, or 36 PIN SOJ, & TSOP–2, 0.3", 0.4". or 0.5" WIDE with PP=0.05"
—28 Or 32 PIN DIP, 0.3", 0.4" with PP=0.1", or 0.6" with PP=0.07".
SPECIAL FEATURES—REDUNDANT CENTERED POWER PINS
PIN ASSIGNMENT—Fig. 3.7.3–12

3.7.3.11 – 64K TO 4M BY 4 TTL SRAM WITH SEPARATE DATA I/O IN DIP, SOJ, AND TSOP–2

CAPACITY—64K, 256K, 1M, AND 4M WORDS OF 4 BIT
LOGIC FEATURES—SEPARATE DATA INPUT AND OUTPUT PINS
—OPTIONAL OUTPUT ENABLE FOR SOME DENSITIES
PACKAGE—32 or 36 or 40 PIN SOJ, & TSOP2, 0.3", 0.4". or 0.5" WIDE with PP=0.05"
—32 Or 36 PIN DIP, 0.3", 0.4" with PP=0.1", or 0.6" with PP=0.07".
CAPACITY—32K, 64K, 128K, 256K WORDS OF 8 BITS
SPECIAL FEATURES—REDUNDANT CENTERED POWER PINS
PIN ASSIGNMENT—Fig. 3.7.3–13

3.7.3.12 – 64K TO 4M BY 4 SYNCHRONOUS SRAM (SSRAM) IN DIP, SOJ, AND TSOP–2

CAPACITY—64K, 256K, 1M, AND 4M WORDS OF 4 BIT
LOGIC FEATURES—SEPARATE DATA INPUT AND OUTPUT PINS
—OUTPUT ENABLE FOR ALL DENSITIES
PACKAGE—32, 36, or 40 PIN SOJ, & TSOP2, 0.3", 0.4". or 0.5" WIDE with PP=0.05"
—32 or 36 PIN DIP, 0.3", 0.4" with PP=0.1", or 0.6" with PP=0.07".
SPECIAL FEATURES—REDUNDANT CENTERED POWER PINS
PIN ASSIGNMENT—Fig. 3.7.3–14

3.7.3.13 – 4K AND 16K BY 4 CACHE TAG SRAM IN DIP AND SOJ

CAPACITY—4K, 16K WORDS OF 4 BIT
LOGIC FEATURES—OPTIONAL ASHYNCHRONOUS CLEAR INPUT
PACKAGE—4K X 4, 22 PIN DIP AND SOJ, 0.3"
—16K X 4, 24 PIN DIP AND SOJ, 0.3"
PIN ASSIGNMENT—Fig. 3.7.3–15

3.7.3.14 – 4M AND 16M SRAM, CONFIGURABLE TO X1 OR X4 IN DIP AND SOJ

SEE PAR. 3.7.1.9 AND FIG. 3.7.1–9 FOR DETAILS OF THIS STANDARD

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jx0056-042

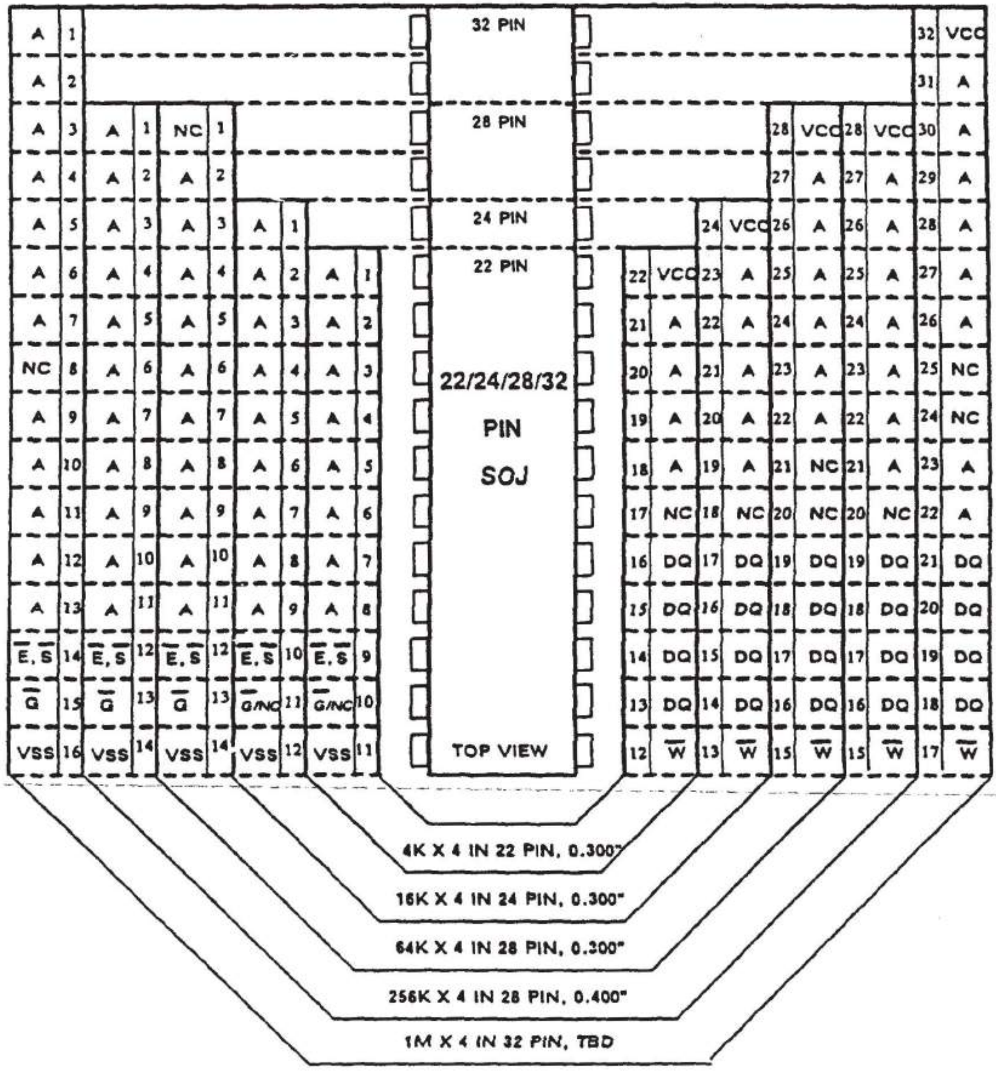
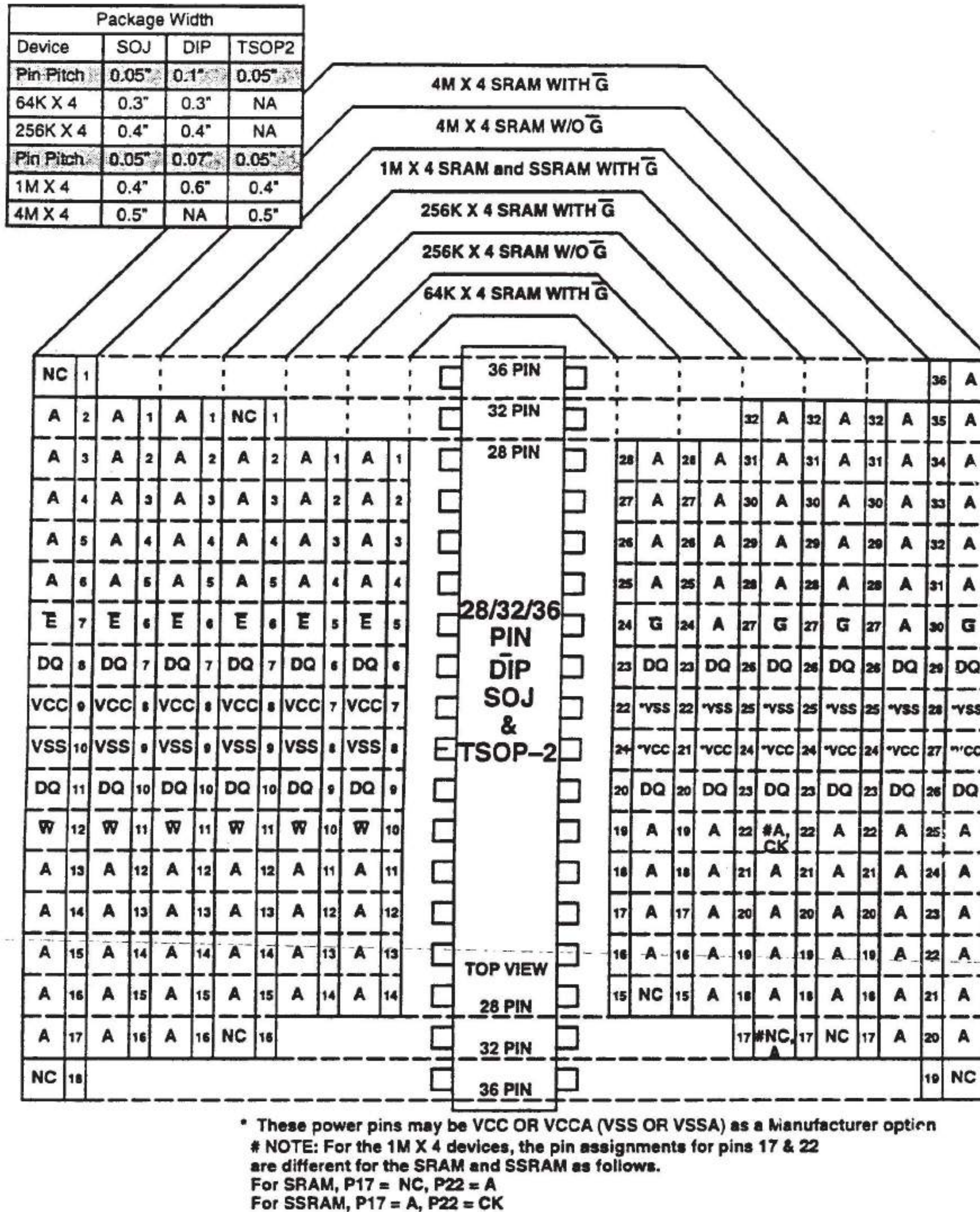


FIGURE 3.7.3-11
4K TO 1M BY 4 TTL SRAM WITH AND WITHOUT G FAMILY IN SOJ

Jedec 0007722

jx0056-043



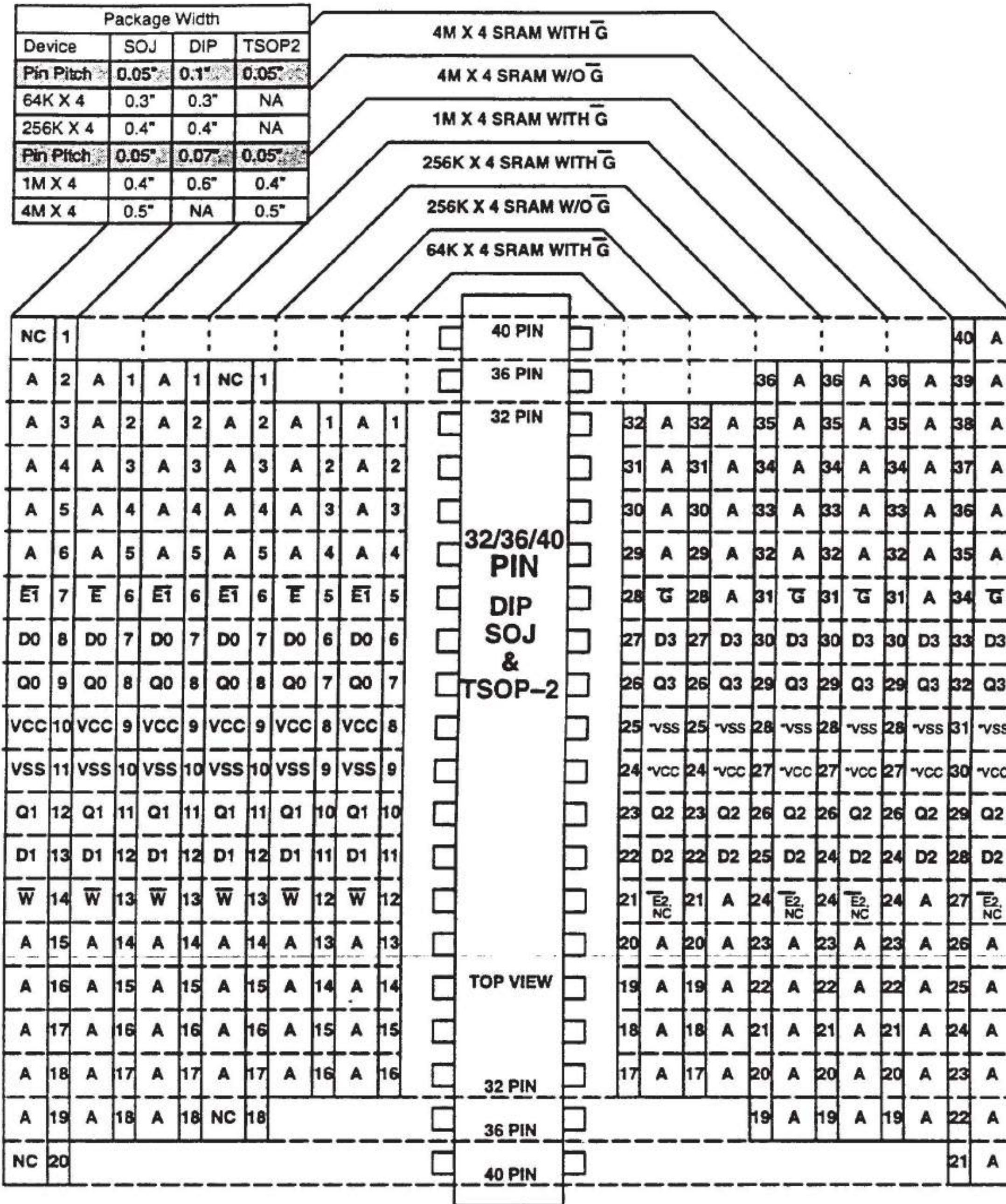
Package Width			
Device	SOJ	DIP	TSOP2
Pin Pitch	0.05"	0.1"	0.05"
64K X 4	0.3"	0.3"	NA
256K X 4	0.4"	0.4"	NA
Pin Pitch	0.05"	0.07"	0.05"
1M X 4	0.4"	0.6"	0.4"
4M X 4	0.5"	NA	0.5"

* These power pins may be VCC OR VCCA (VSS OR VSSA) as a Manufacturer option
\# NOTE: For the 1M X 4 devices, the pin assignments for pins 17 & 22 are different for the SRAM and SSRAM as follows.
For SRAM, P17 = NC, P22 = A
For SSRAM, P17 = A, P22 = CK

FIGURE 3.7.3–12
64K TO 4M BY 4 TTL SRAM FAMILY IN DIP, TSOP2, AND SOJ

Jedec 0007723

jx0056-044



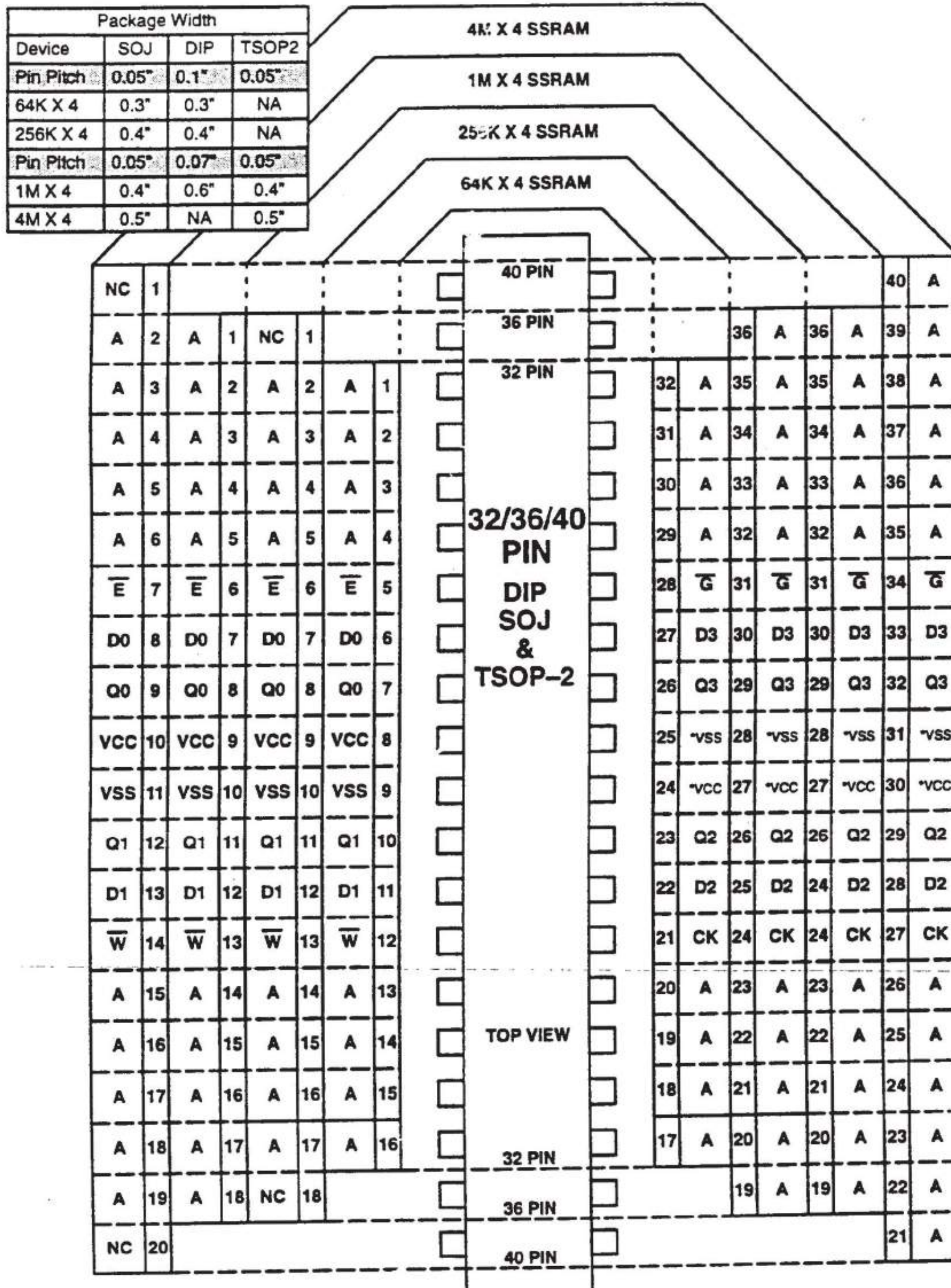
Package Width			
Device	SOJ	DIP	TSOP2
Pin Pitch	0.05"	0.1"	0.05"
64K X 4	0.3"	0.3"	NA
256K X 4	0.4"	0.4"	NA
Pin Pitch	0.05"	0.07"	0.05"
1M X 4	0.4"	0.6"	0.4"
4M X 4	0.5"	NA	0.5"

FIGURE 3.7.3–13

64K TO 4M BY 4 TTL SRAM FAMILY WITH SEPARATE DATA I/O IN DIP, TSOP2, AND SOJ

Jedec 0007724

jx0056-045



* These power pins may be VCC OR VCCA (VSS OR VSSA) as a Manufacturer option

FIGURE 3.7.3-14

64K TO 4M BY 4 SYNCHRONOUS SRAM (SSRAM) FAMILY IN DIP,SOJ,AND TSOP-2

Release 4

Jedec 0007725

3.7.4.1 – .25K AND 1K BY 4, 100K ECL SRAM IN DIP AND SFP

CAPACITY—256, WORDS OF 4 BITS
ELECTRICAL INTERFACE—100K ECL
There are two versions of this part: one in SFP and the other in DIP
PACKAGE—24 PIN DIP, 0.4" WIDE
PIN ASSIGNMENT—Fig. 3.7.4–1
PACKAGE—24 PIN SFP, 0.380" BY 0.380"
PIN ASSIGNMENT—Fig. 3.7.4–2
This standard was developed by Committee 42.1.

3.7.4.2 – 1K TO 16K BY 4, 10K & 100K ECL SRAM IN DIP

CAPACITY—1K, 4K, & 16K, WORDS OF 4 BITS
ELECTRICAL INTERFACE—10K or 100K ECL
—USES 100K ECL CENTERED POWER PINS
PACKAGE—1K in 24 PIN DIP, 0.4" WIDE
—4K & 16K in 28 PIN DIP, 0.4" WIDE
PIN ASSIGNMENT—Fig. 3.7.4–1
This standard was developed by Committee 42.1.

3.7.4.3 – .25K TO 16K BY 4, 10K & 100K ECL SRAM FAMILY IN DIP

CAPACITY—256, 1K, 4K, 16K WORDS OF 4 BITS
ELECTRICAL INTERFACE—10K ECL
—USES 10K ECL CORNERED POWER PINS
—4K part, also 100K ECL
PACKAGE—.25K & 1K, 24 PIN DIP, 0.4" WIDE
—4K & 16K, 28 PIN DIP, 0.4" WIDE
PIN ASSIGNMENT—Fig. 3.7.4–4
This standard was developed by Committee 42.1.

3.7.4.4 – 16K BY 4,10K & 100K ECL SSRAM IN DIP

CAPACITY—16K, WORDS OF 4 BITS
ELECTRICAL INTERFACE—10K or 100K ECL
—USES 100K ECL CENTERED POWER PINS
PACKAGE—32 PIN DIP, 0.4" WIDE
THESE DEVICES CONTAIN BUILT IN WRITE CYCLE TIMING
PIN ASSIGNMENT—Fig. 3.7.4–5
This standard was developed by Committee 42.1.

3.7.4.5 – 64K TO 4M BY 4 ECL SRAM IN DIP, SOJ, AND TSOP–2

CAPACITY—64K, 256K, 1M, AND 4M WORDS OF 4 BIT
LOGIC FEATURE—COMMON DATA INPUT & OUTPUT PINS
—OPTIONAL OUTPUT ENABLE FOR SOME DENSITIES
ELECTRICAL INTERFACE—ECL
PACKAGE—28, 32, or 36 PIN SOJ, & TSOP–2, 0.3", 0.4". or 0.5" WIDE with PP=0.05"
—28 0r 32 PIN DIP, 0.3", 0.4" with PP=0.1", or 0.6" with PP=0.07".
SPECIAL FEATURES—MULTIPLE CENTERED POWER PINS
PIN ASSIGNMENT—Fig. 3.7.4–6

3.7.4.6 – 64K TO 4M BY 4 ECL SRAM WITH SEPARATE DATA I/O IN DIP, SOJ, AND TSOP–2

CAPACITY—64K, 256K, 1M, AND 4M WORDS OF 4 BIT
LOGIC FEATURES—SEPARATE DATA INPUT AND OUTPUT PINS
—OPTIONAL OUTPUT ENABLE FOR SOME DENSITIES
ELECTRICAL INTERFACE—ECL
PACKAGE—32, 36, or 40 PIN SOJ, & TSOP–2, 0.3", 0.4". or 0.5" WIDE with PP=0.05"
—32 or 36 PIN DIP, 0.3", 0.4" with PP=0.1", or 0.6" with PP=0.07".
SPECIAL FEATURES—MULTIPLE CENTERED POWER PINS
PIN ASSIGNMENT—Fig. 3.7.4–7

Jedec 0007726

ix0056-047

3.7.4.7 – 64K TO 4M BY 4 ECL SYNCHRONOUS SRAM (SSRAM) IN DIP, SOJ, AND TSOP–2

CAPACITY—64K, 256K, 1M, AND 4M WORDS OF 4 BIT
LOGIC FEATURES—SEPARATE DATA INPUT AND OUTPUT PINS
—OUTPUT ENABLE FOR ALL DENSITIES
ELECTRICAL INTERFACE—10K or 100K ECL
PACKAGE—32, 36, or 40 PIN SOJ, & TSOP–2, 0.3", 0.4". or 0.5" WIDE with PP=0.05"
—32 or 36 PIN DIP, 0.3", 0.4" with PP=0.1", or 0.6" with PP=0.07".
SPECIAL FEATURES—REDUNDANT CENTERED POWER PINS
PIN ASSIGNMENT—Fig. 3.7.4–8

3.7.4.8 – 64K BY 4 ECL SRAM IN FP

CAPACITY—64K WORDS OF 4 BITS
LOGIC FEATURES—SEPARATE DATA INPUT AND OUTPUT PINS
ELECTRICAL INTERFACE—10K or 100K ECL
PACKAGE—28 PIN FP, 0.535" WIDE, 0.030" LEAD PITCH
PIN ASSIGNMENT—Fig. 3.7.4–9

3.7.4.9 – 256K BY 4/512K BY 2 RECONFIGURABLE SRAM IN DIP & SOJ

CAPACITY—256K WORDS OF 4 BITS OR 512K WORDS OF 2 BITS
LOGIC FEATURES—RECONFIGURABLE CAPACITY & DATA INTERFACE
ELECTRICAL INTERFACE—10K or 100K ECL
PACKAGE—32 PIN DIP or SOJ, 0.4" wide
SPECIAL FEATURES—REDUNDANT CENTERED POWER PINS
PIN ASSIGNMENT—Fig. 3.7.4–10

3.7.4.10 – 64K TO 4M BY 4 SRAM FAMILY IN DIP AND SOJ IN DIP, SOJ, AND TSOP–2

CAPACITY—64K, 256K, 1M, AND 4M WORDS OF 4 BIT
LOGIC FEATURES—SEPARATE DATA INPUT AND OUTPUT PINS
—BIT SELECTION
ELECTRICAL INTERFACE—10K or 100K ECL
PACKAGE—36 or 40 PIN SOJ, & TSOP–2, 0.3", 0.4". or 0.5" WIDE with PP=0.05"
—36 or 40 PIN DIP, 0.3", 0.4" with PP=0.1", or 0.6" with PP=0.07".
SPECIAL FEATURES—REDUNDANT CENTERED POWER PINS
PIN ASSIGNMENT—Fig. 3.7.4–11

3.7.4.11 – 64K TO 4M BY 4 SSRAM FAMILY IN SIP AND SOJ IN DIP, SOJ, AND TSOP–2

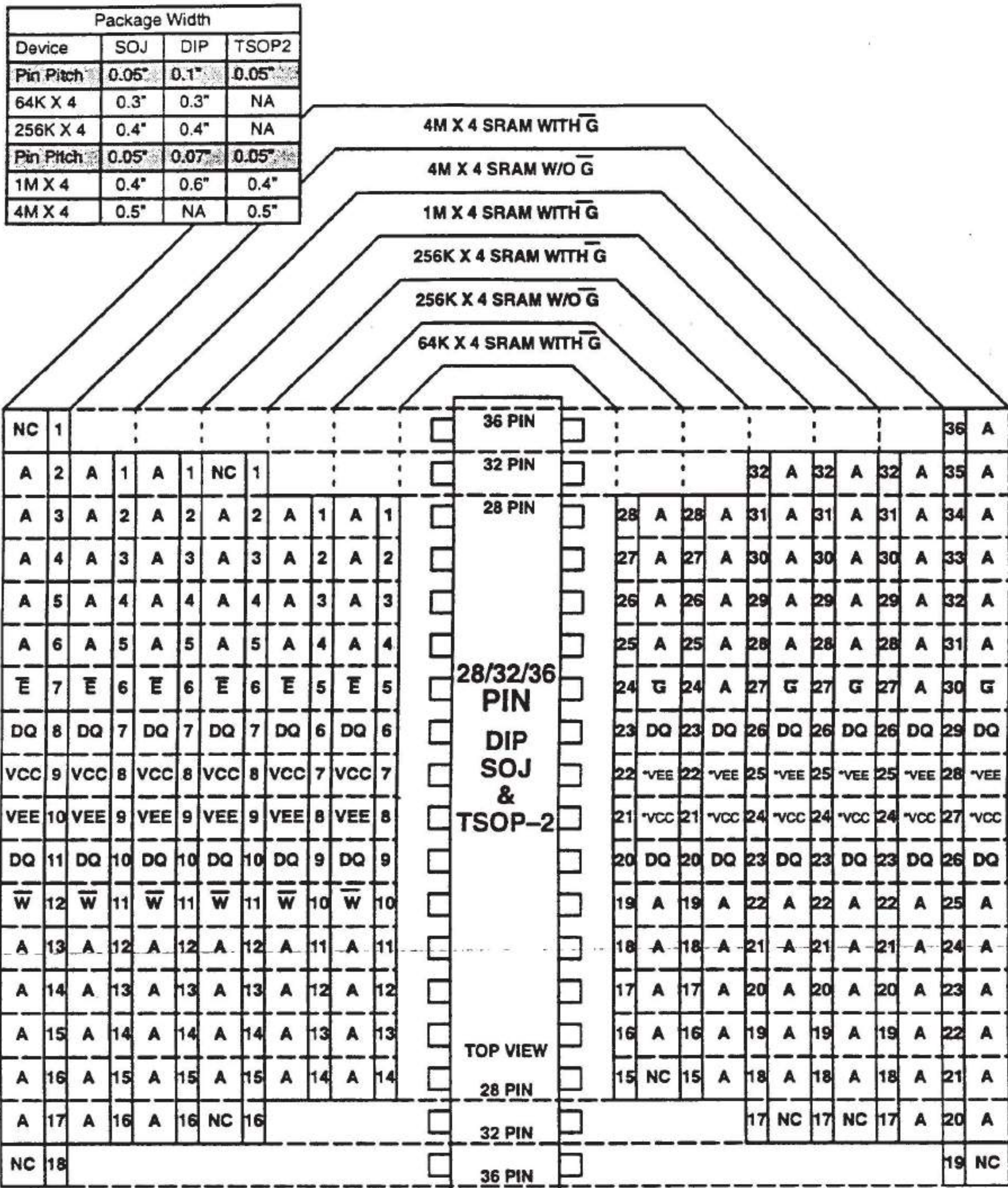
CAPACITY—64K, 256K, 1M, AND 4M WORDS OF 4 BIT
LOGIC FEATURES—SEPARATE DATA INPUT AND OUTPUT PINS
—DIFFERENTIAL CLOCKS
ELECTRICAL INTERFACE—10K or 100K ECL
PACKAGE—32, 36, or 40 PIN SOJ, & TSOP–2, 0.3", 0.4". or 0.5" WIDE with PP=0.05"
—32 or 36 PIN DIP, 0.3", 0.4" with PP=0.1", or 0.6" with PP=0.07".
SPECIAL FEATURES—REDUNDANT CENTERED POWER PINS
PIN ASSIGNMENT—Fig. 3.7.4–12

3.7.4.12 – 64K TO 4M BY 4 SSRAM FAMILY IN SIP AND SOJ IN DIP, SOJ, AND TSOP–2

CAPACITY—64K, 256K, 1M, AND 4M WORDS OF 4 BIT
LOGIC FEATURES—SEPARATE DATA INPUT AND OUTPUT PINS
—BIT SELECTION
ELECTRICAL INTERFACE—10K or 100K ECL
PACKAGE—36, 40, or 44 PIN SOJ, & TSOP2, 0.3", 0.4". or 0.5" wide
—36, 40, or 44 PIN DIP, 0.3", 0.4", or 0.6" wide..
PACKAGE—36, 40, or 44 PIN SOJ, & TSOP–2, 0.3", 0.4". or 0.5" WIDE with PP=0.05"
—36 or 40 PIN DIP, 0.3", 0.4" with PP=0.1", or 0.6" with PP=0.07".
SPECIAL FEATURES—REDUNDANT CENTERED POWER PINS
PIN ASSIGNMENT—Fig. 3.7.4–13

Jedec 0007727

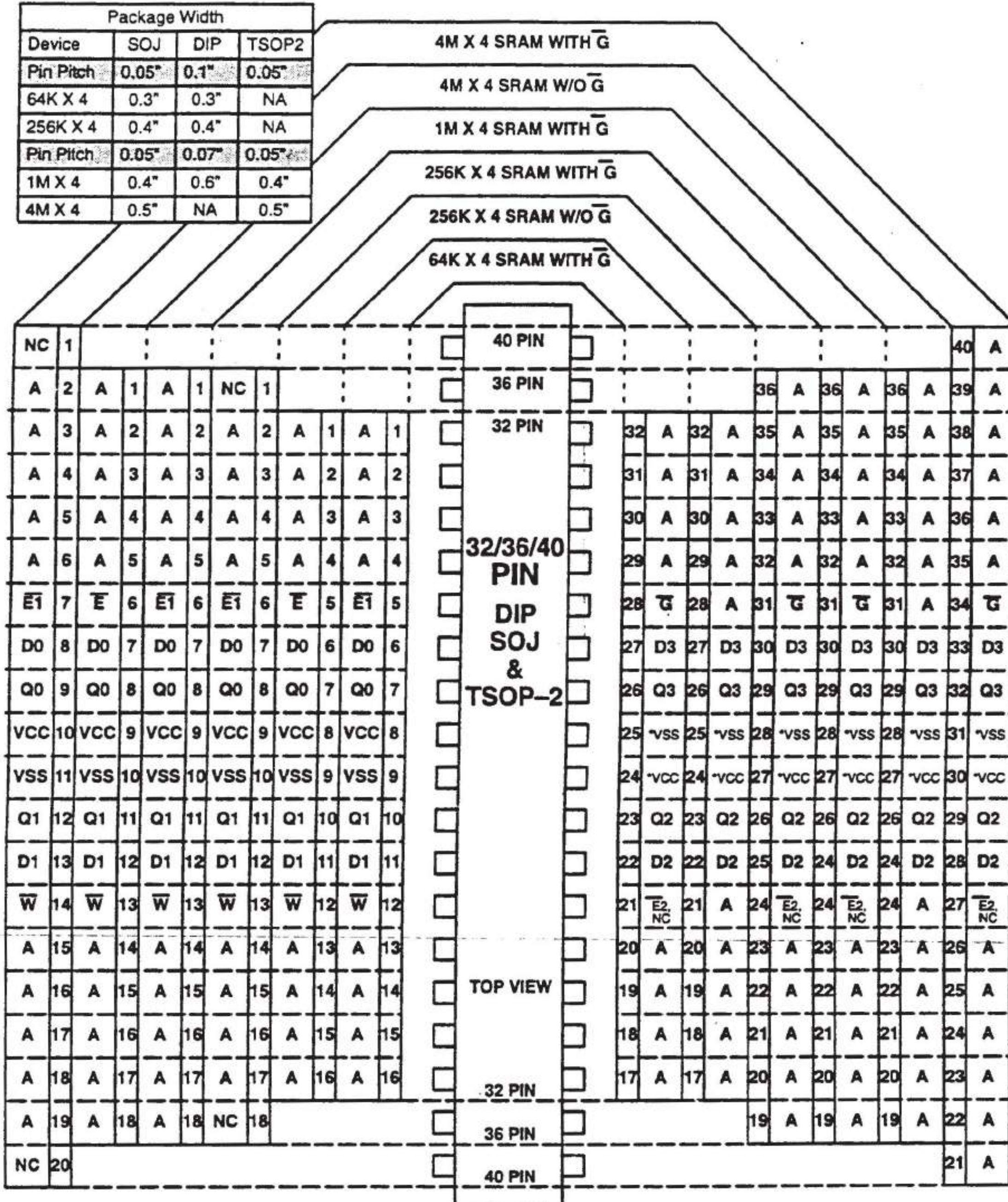
jx0056-048



* These power pins may be VCC OR VCCA (VSS OR VSSA) as a Manufacturer option

FIGURE 3.7.4–6

64K TO 4M BY 4 ECL SRAM FAMILY IN DIP, SOJ, AND TSOP–2



* These power pins may be VCC OR VCCA (VSS OR VSSA) as a Manufacturer option

FIGURE 3.7.4–7

64K TO 4M BY 4 ECL SRAM WITH SEPARATE I/O FAMILY IN DIP, SOJ, AND TSOP–2

Release 4

Package Width			
Device	SOJ	DIP	TSOP2
Pin Pitch	0.05"	0.1"	0.05"
64K X 4	0.3"	0.3"	NA
256K X 4	0.4"	0.4"	NA
Pin Pitch	0.05"	0.07"	0.05"
1M X 4	0.4"	0.6"	0.4"
4M X 4	0.5"	NA	0.5"

32/36/40 PIN DIP SOJ & TSOP–2 — TOP VIEW

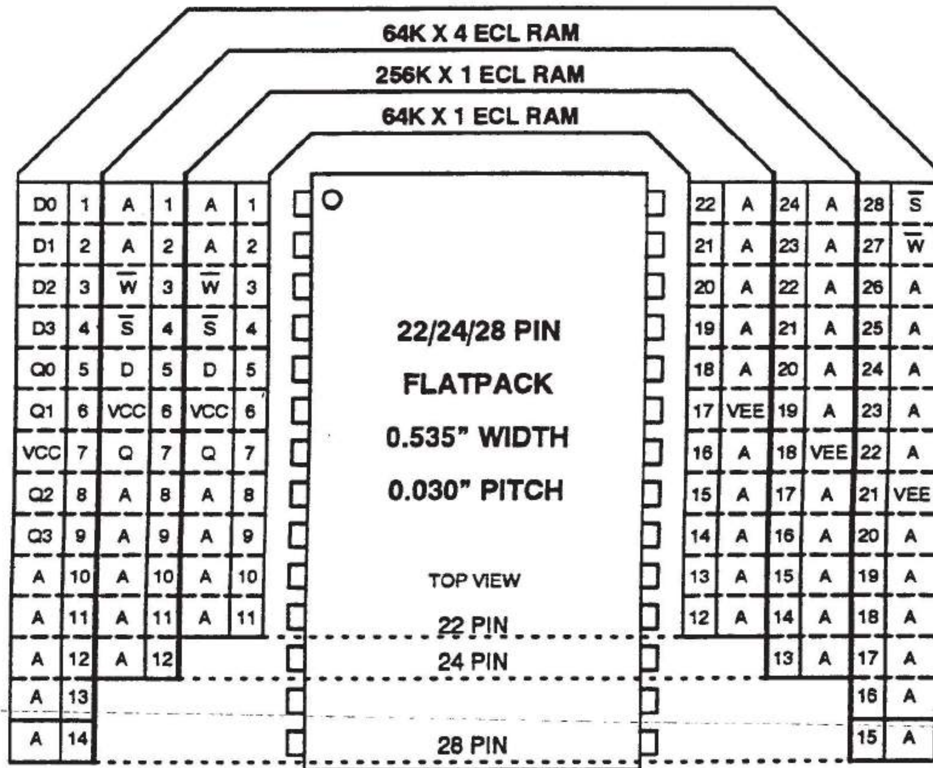
4M X 4 SSRAM	Pin	1M X 4 SSRAM	Pin	256K X 4 SSRAM	Pin	64K X 4 SSRAM	Pin	64K X 4 SSRAM Pin		256K X 4 SSRAM Pin		1M X 4 SSRAM Pin		4M X 4 SSRAM Pin	
NC	1													40	A
A	2	A	1	NC	1					36	A	36	A	39	A
A	3	A	2	A	2	A	1	32	A	35	A	35	A	38	A
A	4	A	3	A	3	A	2	31	A	34	A	34	A	37	A
A	5	A	4	A	4	A	3	30	A	33	A	33	A	36	A
A	6	A	5	A	5	A	4	29	A	32	A	32	A	35	A
$\overline{E}$	7	$\overline{E}$	6	$\overline{E}$	6	$\overline{E}$	5	28	$\overline{G}$	31	$\overline{G}$	31	$\overline{G}$	34	$\overline{G}$
D0	8	D0	7	D0	7	D0	6	27	D3	30	D3	30	D3	33	D3
Q0	9	Q0	8	Q0	8	Q0	7	26	Q3	29	Q3	29	Q3	32	Q3
VCC	10	VCC	9	VCC	9	VCC	8	25	*VEE	28	*VEE	28	*VEE	31	*VEE
VEE	11	VEE	10	VEE	10	VEE	9	24	*VCC	27	*VCC	27	*VCC	30	*VCC
Q1	12	Q1	11	Q1	11	Q1	10	23	Q2	26	Q2	26	Q2	29	Q2
D1	13	D1	12	D1	12	D1	11	22	D2	25	D2	24	D2	28	D2
$\overline{W}$	14	$\overline{W}$	13	$\overline{W}$	13	$\overline{W}$	12	21	CK	24	CK	24	CK	27	CK
A	15	A	14	A	14	A	13	20	A	23	A	23	A	26	A
A	16	A	15	A	15	A	14	19	A	22	A	22	A	25	A
A	17	A	16	A	16	A	15	18	A	21	A	21	A	24	A
A	18	A	17	A	17	A	16	17	A	20	A	20	A	23	A
A	19	A	18	A	18					19	A	19	A	22	A
NC	20													21	A

* These power pins may be VCC OR VCCA (VEE or VEEA) as a Manufacturer option

FIGURE 3.7.4–8
64K TO 4M BY 4 ECL SSRAM FAMILY IN DIP, SOJ, AND TSOP–2

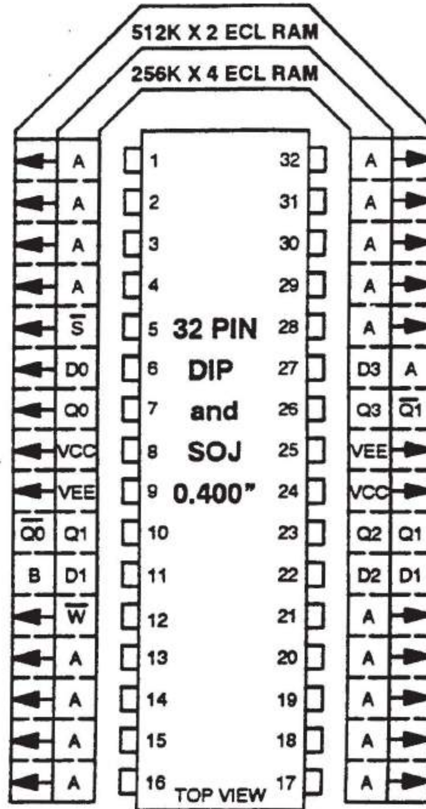
Jedec 0007730

jx0056-051



64K X 4		256K X 1		64K X 1		64K X 1		256K X 1		64K X 4	
D0	1	A	1	A	1	22	A	24	A	28	$\overline{S}$
D1	2	A	2	A	2	21	A	23	A	27	$\overline{W}$
D2	3	$\overline{W}$	3	$\overline{W}$	3	20	A	22	A	26	A
D3	4	$\overline{S}$	4	$\overline{S}$	4	19	A	21	A	25	A
Q0	5	D	5	D	5	18	A	20	A	24	A
Q1	6	VCC	6	VCC	6	17	VEE	19	A	23	A
VCC	7	Q	7	Q	7	16	A	18	VEE	22	A
Q2	8	A	8	A	8	15	A	17	A	21	VEE
Q3	9	A	9	A	9	14	A	16	A	20	A
A	10	A	10	A	10	13	A	15	A	19	A
A	11	A	11	A	11	12	A	14	A	18	A
A	12	A	12					13	A	17	A
A	13									16	A
A	14									15	A

FIGURE 3.7.4–9
64K AND 256K BY 1 ECL RAM
64K BY 4 ECL RAM
IN FLATPACK



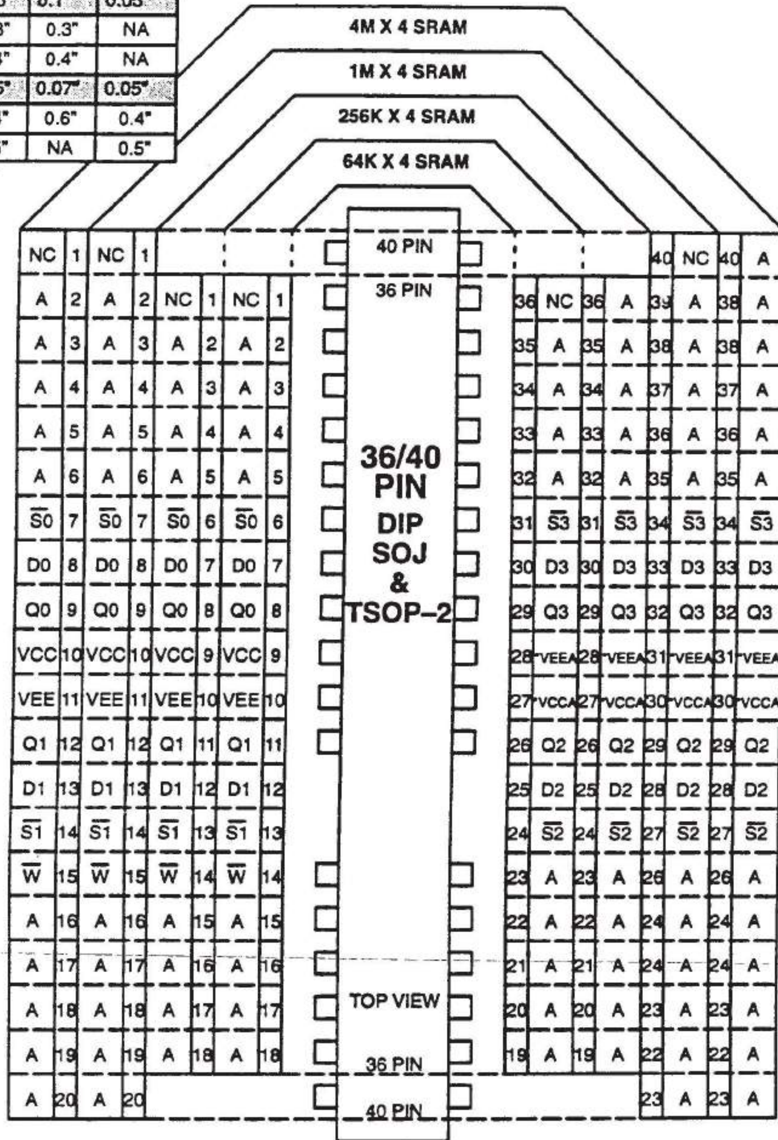
Multi–function Pin Truth Table Function vs. Mode Select Pin (11) Level		
Pin 11 Level/Function	> VEE / D1	VEE / B
RAM Organization	256K X 4	512K X 2
Pin #		
6	D0	D0
7	Q0	Q0
10	Q1	$\overline{Q0}$
11	D1	B (VEE)
22	D2	D1
23	Q2	Q1
26	Q3	$\overline{Q1}$
27	D3	A18

FIGURE 3.7.4–10
256K X 4 or 512K X 2 CONFIGURABLE SRAM
IN SOJ & DIP

Jedec 0007732

jx0056-053

Package Width			
Device	SOJ	DIP	TSOP2
Pin Pitch	0.05"	0.1"	0.05"
64K X 4	0.3"	0.3"	NA
256K X 4	0.4"	0.4"	NA
Pin Pitch	0.05"	0.07"	0.05"
1M X 4	0.4"	0.6"	0.4"
4M X 4	0.5"	NA	0.5"



* These power pins may be VCC OR VCCA (VSS OR VSSA) as a Manufacturer option

FIGURE 3.7.4–11
64K TO 4M BY 4 BIT SELECTABLE ECL SRAM FAMILY IN DIP, SOJ, AND TSOP–2

Release 4

Jedec 0007733

Package Width			
Device	SOJ	DIP	TSOP2
Pin Pitch	0.05"	0.1"	0.05"
64K X 4	0.3"	0.3"	NA
256K X 4	0.4"	0.4"	NA
Pin Pitch	0.05"	0.07"	0.05"
1M X 4	0.4"	0.6"	0.4"
4M X 4	0.5"	NA	0.5"

4M X 4 SSRAM
1M X 4 SSRAM
256K X 4 SSRAM
64K X 4 SSRAM

32/36/40 PIN DIP SOJ & TSOP–2 (TOP VIEW)

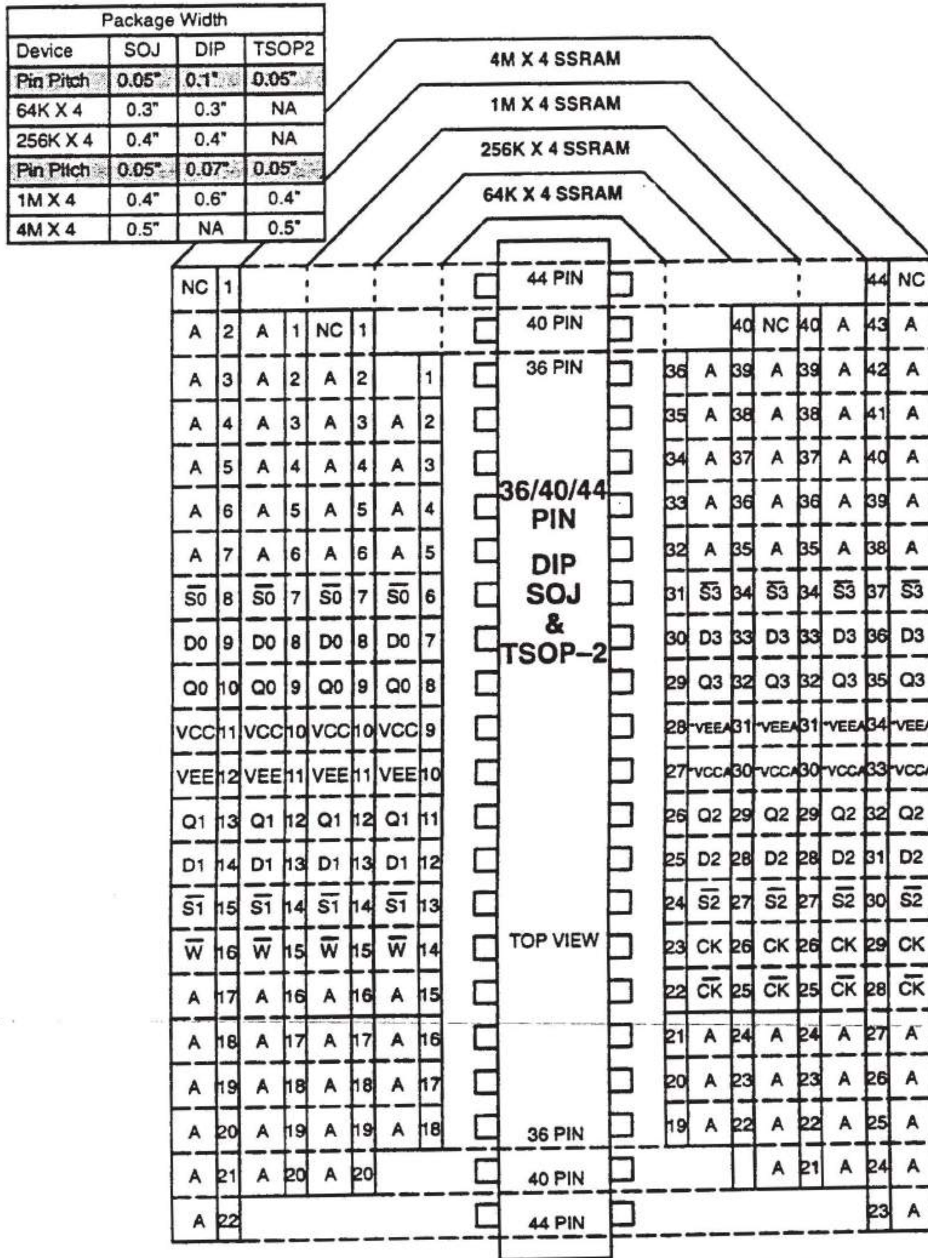
4M X 4	pin	1M X 4	pin	256K X 4	pin	64K X 4	pin		pin	64K X 4	pin	256K X 4	pin	1M X 4	pin	4M X 4
NC	1							40 PIN							40	A
A	2	A	1	NC	1			36 PIN			36	A	36	A	39	A
A	3	A	2	A	2	A	1	32 PIN	32	A	35	A	35	A	38	A
A	4	A	3	A	3	A	2		31	A	34	A	34	A	37	A
A	5	A	4	A	4	A	3		30	A	33	A	33	A	36	A
A	6	A	5	A	5	A	4		29	A	32	A	32	A	35	A
$\overline{E}$	7	$\overline{E}$	6	$\overline{E}$	6	$\overline{E}$	5		28	A	31	A	31	A	34	A
D0	8	D0	7	D0	7	D0	6		27	D3	30	D3	30	D3	33	D3
Q0	9	Q0	8	Q0	8	Q0	7		26	Q3	29	Q3	29	Q3	32	Q3
VCC	10	VCC	9	VCC	9	VCC	8		25	*VEE	28	*VEE	28	*VEE	31	*VEE
VEE	11	VEE	10	VEE	10	VEE	9		24	*VCC	27	*VCC	27	*VCC	30	*VCC
Q1	12	Q1	11	Q1	11	Q1	10		23	Q2	26	Q2	26	Q2	29	Q2
D1	13	D1	12	D1	12	D1	11		22	D2	25	D2	24	D2	28	D2
$\overline{W}$	14	$\overline{W}$	13	$\overline{W}$	13	$\overline{W}$	12		21	CK	24	CK	24	CK	27	CK
A	15	A	14	A	14	A	13		20	$\overline{CK}$	23	$\overline{CK}$	23	$\overline{CK}$	26	$\overline{CK}$
A	16	A	15	A	15	A	14	TOP VIEW	19	A	22	A	22	A	25	A
A	17	A	16	A	16	A	15		18	A	21	A	21	A	24	A
A	18	A	17	A	17	A	16	32 PIN	17	A	20	A	20	A	23	A
A	19	A	18	A	18			36 PIN			19	A	19	A	22	A
NC	20							40 PIN							21	A

* These power pins may be VCC OR VCCA (VEE or VEEA) as a Manufacturer option

FIGURE 3.7.4–12
64K TO 4M BY 4 ECL SSRAM FAMILY IN DIP, SOJ, AND TSOP–2

Jedec 0007734

jx0056-055



Package Width			
Device	SOJ	DIP	TSOP2
Pin Pitch	0.05"	0.1"	0.05"
64K X 4	0.3"	0.3"	NA
256K X 4	0.4"	0.4"	NA
Pin Pitch	0.05"	0.07"	0.05"
1M X 4	0.4"	0.6"	0.4"
4M X 4	0.5"	NA	0.5"

* These power pins may be VCC OR VCCA (VSS OR VSSA) as a Manufacturer option

FIGURE 3.7.4–13

64K TO 4M BY 4 BIT SELECTABLE ECL SSRAM FAMILY IN DIP, SOJ, AND TSOP–2

Jedec 0007735

jx0056-056

3.7.5.1 – 64 BY 9 TTL SRAM IN SCC

CAPACITY—64 WORDS OF 9 BITS
PACKAGE—28 PAD (PIN) SCC, 0.450" X 0.450"
PIN ASSIGNMENTS—Fig. 3.7.5–1
This standard was developed by Committee 42.1.

3.7.5.2 – 1K & 2K BY 8 TTL SRAM IN DIP

CAPACITY—1K, 2K WORDS OF 8 BITS
PACKAGE—24 PIN DIP, 0.6" WIDE
PIN ASSIGNMENT—Fig. 3.7.5–2

3.7.5.3 – 2K & 4K BY 8 TTL SRAM IN RCC

CAPACITY—2K, 4K WORDS OF 8 BITS
PACKAGE—32 PAD (PIN) RCC, 0.450" BY 0.550"
PIN ASSIGNMENT—Fig. 3.7.5–3
These parts are CC equivalents of 24 Pin DIP devices.

3.7.5.4 – 2K TO 32K BY 8 TTL SRAM FAMILY IN DIP & SOJ,

CAPACITY—2K, 4K, 8K, 16K, & 32K WORDS OF 8 BITS,
PACKAGE—28 PIN DIP, 0.6" WIDE
—28 PIN DIP, 0.3" WIDE OPTIONAL FOR 8K & 32K DEVICES
PIN ASSIGNMENT—Fig. 3.7.5–4

3.7.5.5 – .5K TO 32K BY 8 TTL SRAM FAMILY IN RCC

CAPACITY—.5K, 1K, 2K, 4K, 8K, 16K, 32K WORDS OF 8 BITS
PACKAGE—32 PAD (PIN) RCC, 0.450" BY 0.550"
PIN ASSIGNMENT—Fig. 3.7.5–5

3.7.5.6 – 32K TO 512K BY 8 TTL SRAM FAMILY IN SOJ or TSOP–2,

CAPACITY—32K, 128K, 256K, 512K WORDS OF 8 BITS,
PACKAGE—28 OR 32 PIN SOJ, 0.3", 0.4" WIDE OR NOT DEFINED
—32 PIN TSOP–2 (see Fig. 3.7.5–6 for package approvals)
PIN ASSIGNMENT—Fig. 3.7.5–6

3.7.5.7 – 64K TO 512K BY 8 TTL SRAM FAMILY IN DIP,

CAPACITY—64K, 128K, 256K, 512K WORDS OF 8 BITS,
PACKAGE—32 PIN DIP, 0.6" WIDE
PIN ASSIGNMENT—Fig. 3.7.5–7

3.7.5.8 – 32K TO 256K BY 9 TTL SRAM FAMILY IN DIP,

CAPACITY—32K, 64K, 128K, 256K WORDS OF 9 BITS,
PACKAGE—32 PIN DIP, 0.6" WIDE
—OPTIONAL 32 PIN DIP & SOJ, 0.3" WIDE FOR 32K DEVICE
PIN ASSIGNMENT—Fig. 3.7.5–8

3.7.5.9 – 32K TO 2M BY 8 AND 512K TO 2M BY 9 TTL SRAM IN DIP, SOJ, AND TSOP–2

CAPACITY—32K, 128K, 512K, 2M WORDS OF 8 BIT AND 512K, 2M WORDS OF 9 BITS
LOGIC FEATURES—COMMON DATA INPUT & OUTPUT PINS
—OUTPUT ENABLE FOR ALL DENSITIES
PACKAGE—32, 36, or 40 PIN SOJ, & TSOP–2, 0.3", 0.4". or 0.5" WIDE with PP=0.05"
—32 or 36 PIN DIP, 0.3", 0.4" with PP=0.1", or 0.6" with PP=0.07".
SPECIAL FEATURES—MULTIPLE CENTERED POWER PINS
PIN ASSIGNMENT—Fig. 3.7.5–9

Jedec 0007736

jx0056-057

3.7.5.10 – 32K and 128K BY 8 TTL SSRAM IN DIP AND SOJ

CAPACITY—32K, & 128K WORDS OF 8 BIT
LOGIC FEATURES—SEPARATE DATA INPUT & OUTPUT PINS
—OUTPUT ENABLE
PACKAGE—40 PIN DIP, 0.6" wide
—40 PIN SOJ, UNDEFINED
SPECIAL FEATURES—MULTIPLE CENTERED POWER PINS
PIN ASSIGNMENT—Fig. 3.7.5–10

3.7.5.11 – 2K TO 32K BY 9 DPSRAM FAMILY IN 68 SCC

CAPACITY—2K, 8K, 32K WORDS OF 9 BITS,
LOGIC FEATURES—Two identical access ports
PACKAGE—68 PAD (PIN) SCC, 0.950" X 0.950"
PIN ASSIGNMENT—Fig. 3.7.5–11
This part contains two identical ports for access to the storage array. These ports include full sets of address, data, and control signals.

3.7.5.12 – 32K BY 9 CACHE SRAM IN 44 SCC

CAPACITY—32K WORDS OF 9 BITS,
LOGIC FEATURES—Internal CACHE data compare logic
PACKAGE—44 TERMINAL SCC, 0.500" X 0.500"
PIN ASSIGNMENT—Fig. 3.7.5–12
This part contains specialized logic functions which allow it to be used to implement the CACHE memory function conveniently.

3.7.5.13 – 128K BY 8 SRAM IN TSOP1

CAPACITY—128K WORDS OF 8 BITS
PACKAGE—32 PIN TSOP1, 20 mm X 8 mm, 0.5 mm PIN PITCH
PIN ASSIGNMENTS—Fig. 3.7.5–13

3.7.5.14 – 128K BY 8 & 9 SSRAM IN SOJ

CAPACITY—128K WORDS OF 8 BITS
PACKAGE—32 PIN SOJ, 0.400"
PIN ASSIGNMENTS—Fig. 3.7.5–14

3.7.5.15 – 1K AND 2K BY 8 DPSRAM FAMILY IN 48 DIP

CAPACITY—1K, 2K WORDS OF 8 BITS,
LOGIC FEATURES—Two identical access ports
PACKAGE—48 PIN DIP, 0.600"
PIN ASSIGNMENT—Fig. 3.7.5–15
This part contains two identical ports for access to the storage array. These ports include full sets of address, data, and control signals.

3.7.5.16 – 128K TO 512K BY 8 SRAM FAMILY IN 32 CDSO–N

CAPACITY—128K, 256K, 512K WORDS OF 8 BITS,
PACKAGE—32 PIN LEADLESS CERAMIC SO, 0.400"
PIN ASSIGNMENT—Fig. 3.7.5–16
This family of parts is based on the evolutionary SRAM pinout family described in Sec. 3.7.5.7

3.7.5.17 – 128K TO 512K BY 8 & 9 SSRAM AND 128K BY 9 SRAM IN 33 DIP, TSOP2, AND SOJ

CAPACITY—128K & 512K WORDS OF 8 OR 9 BITS,
LOGIC FEATURES—Both Synchronous and Asynchronous versions of the 128K part
PACKAGE—36 PIN DIP, TSOP2, or SOJ, 0.400" or 0.600",
— See Fig. 3.7.5–17 for specific package approvals and dimensions.
PIN ASSIGNMENT—Fig. 3.7.5–17

Jedec 0007737

jx0056-058

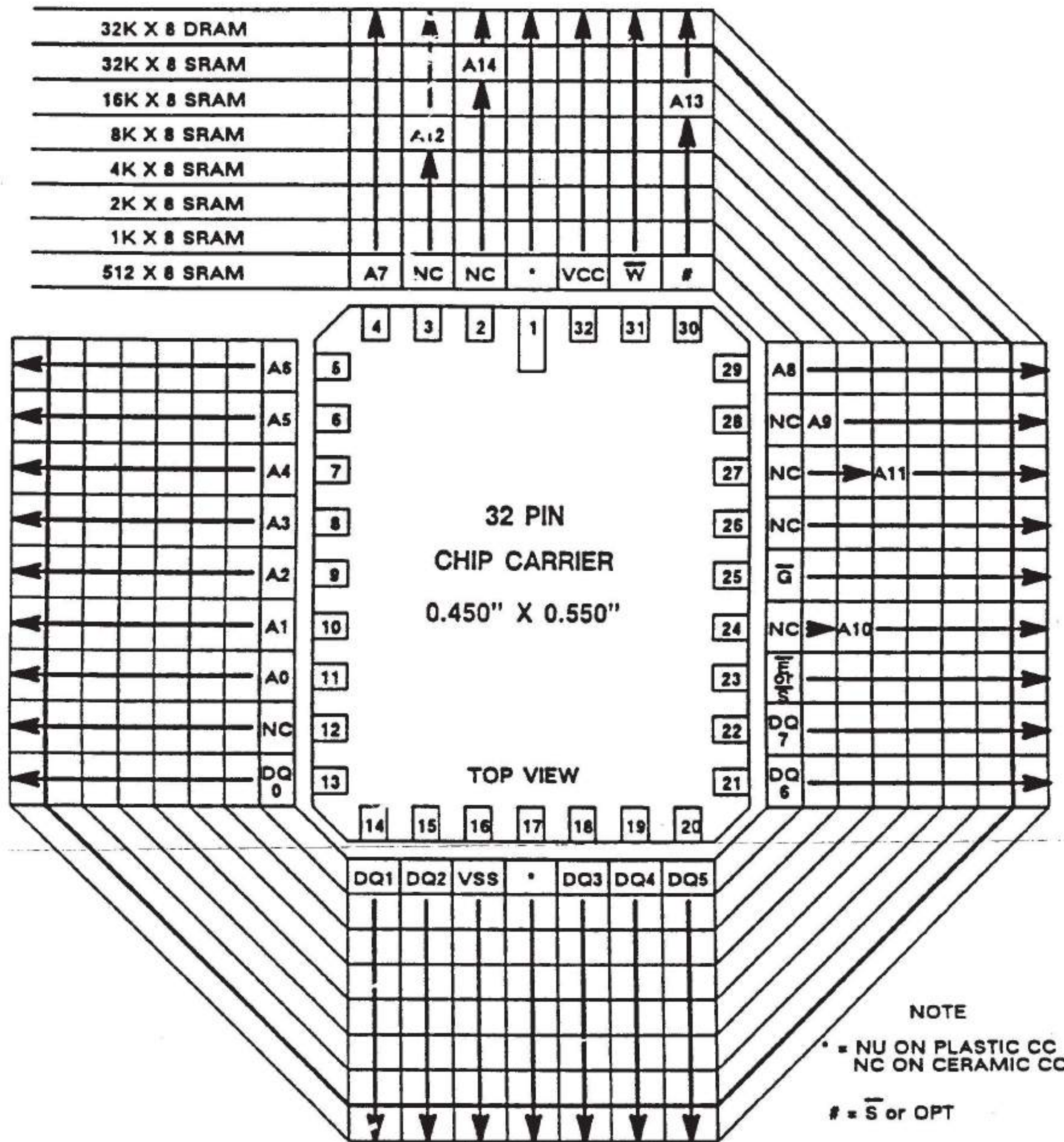
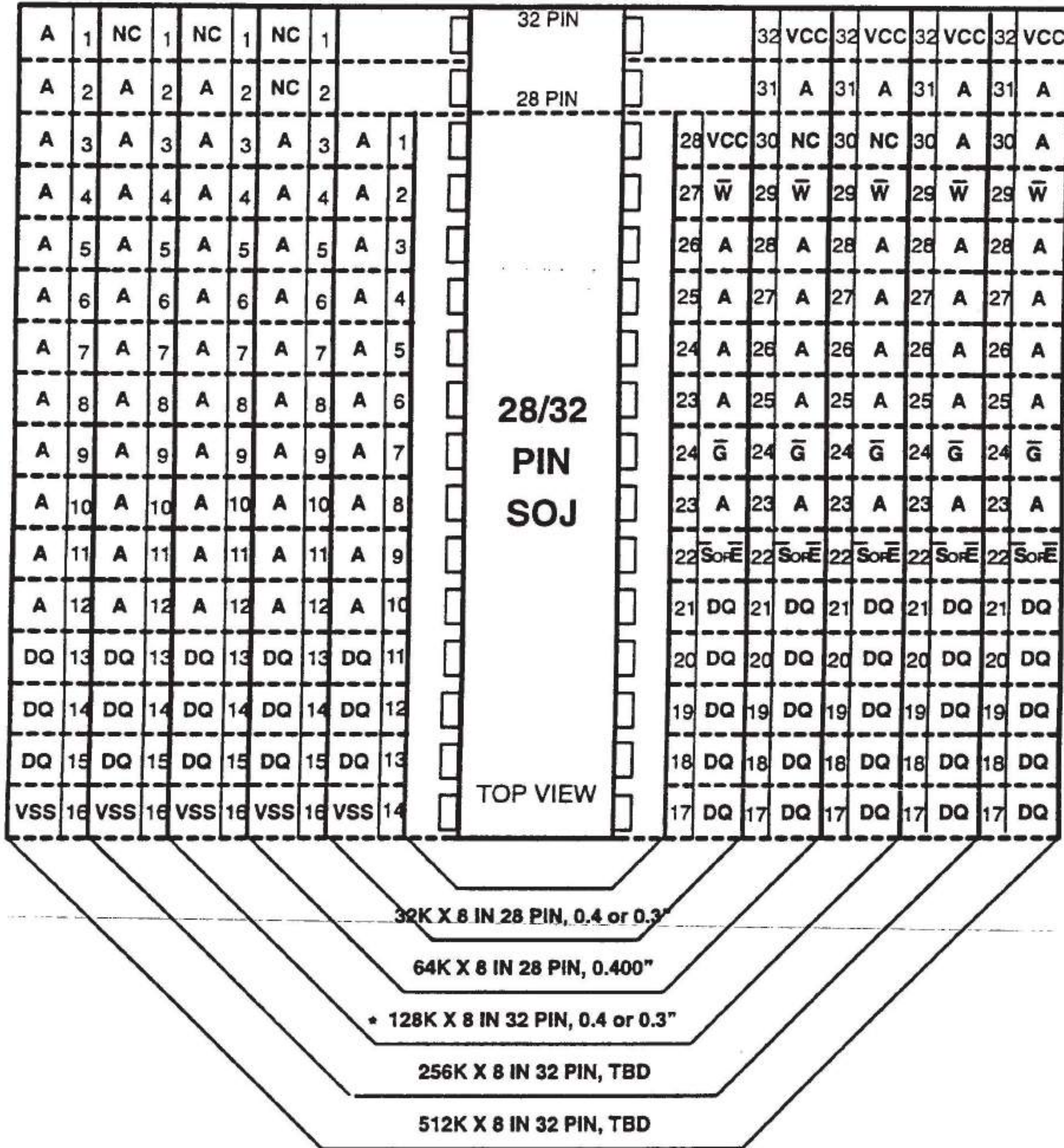


FIGURE 3.7.5-5
.5K TO 32K BY 8 TTL SRAM FAMILY IN RCC

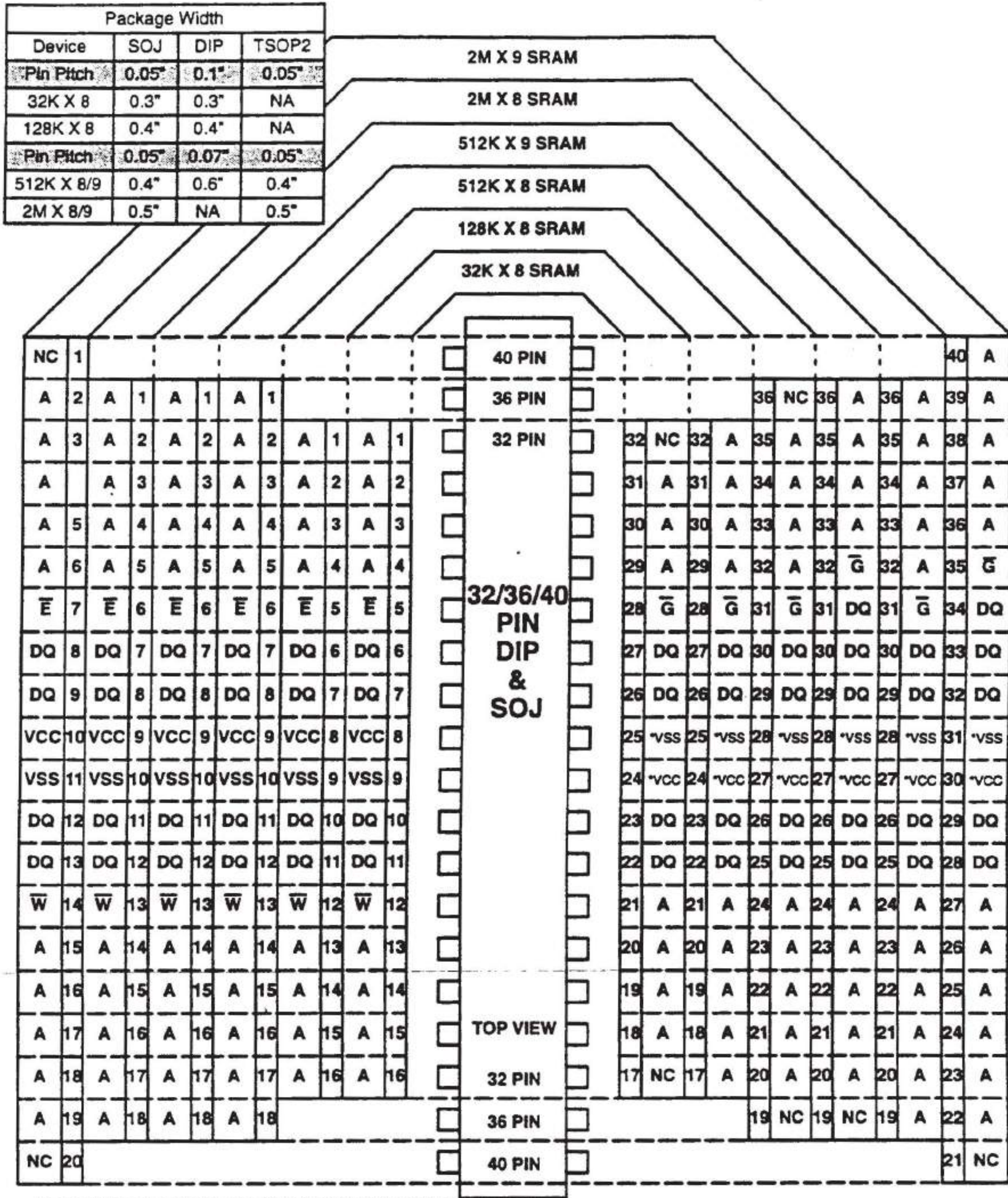


* The 128K X 8 device is also approved for use in 0.300" wide TSOP–2 (PDSO–G) package with a pin pitch of 0.050"

FIGURE 3.7.5–6
32K TO 512K BY 8 TTL SRAM FAMILY IN SOJ

Jedec 0007739

jx0056-060

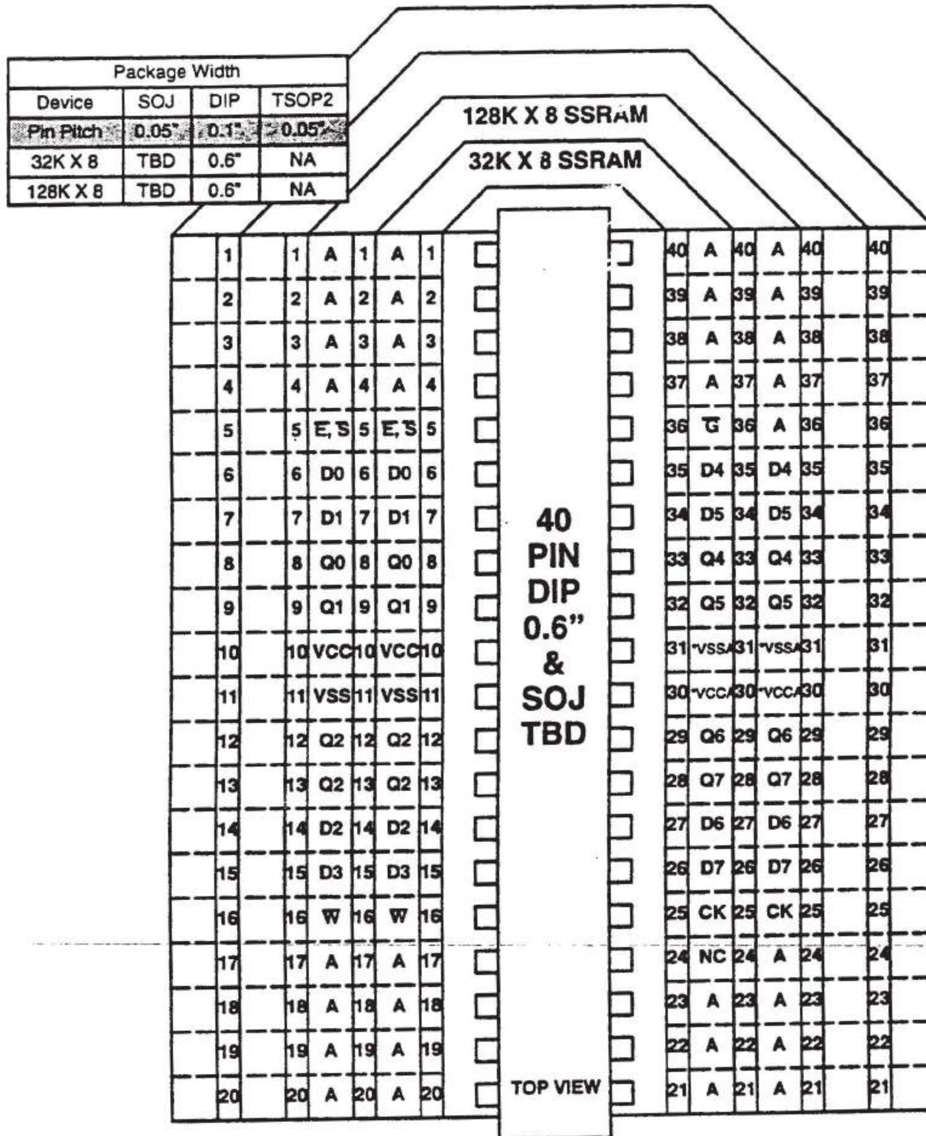


Package Width			
Device	SOJ	DIP	TSOP2
Pin Pitch	0.05"	0.1"	0.05"
32K X 8	0.3"	0.3"	NA
128K X 8	0.4"	0.4"	NA
Pin Pitch	0.05"	0.07"	0.05"
512K X 8/9	0.4"	0.6"	0.4"
2M X 8/9	0.5"	NA	0.5"

FIGURE 3.7.5–9
32K TO 2M BY 8 AND 9 TTL SRAM FAMILY IN DIP, TSOP2, AND SOJ

Jedec 0007740

ix0056-061

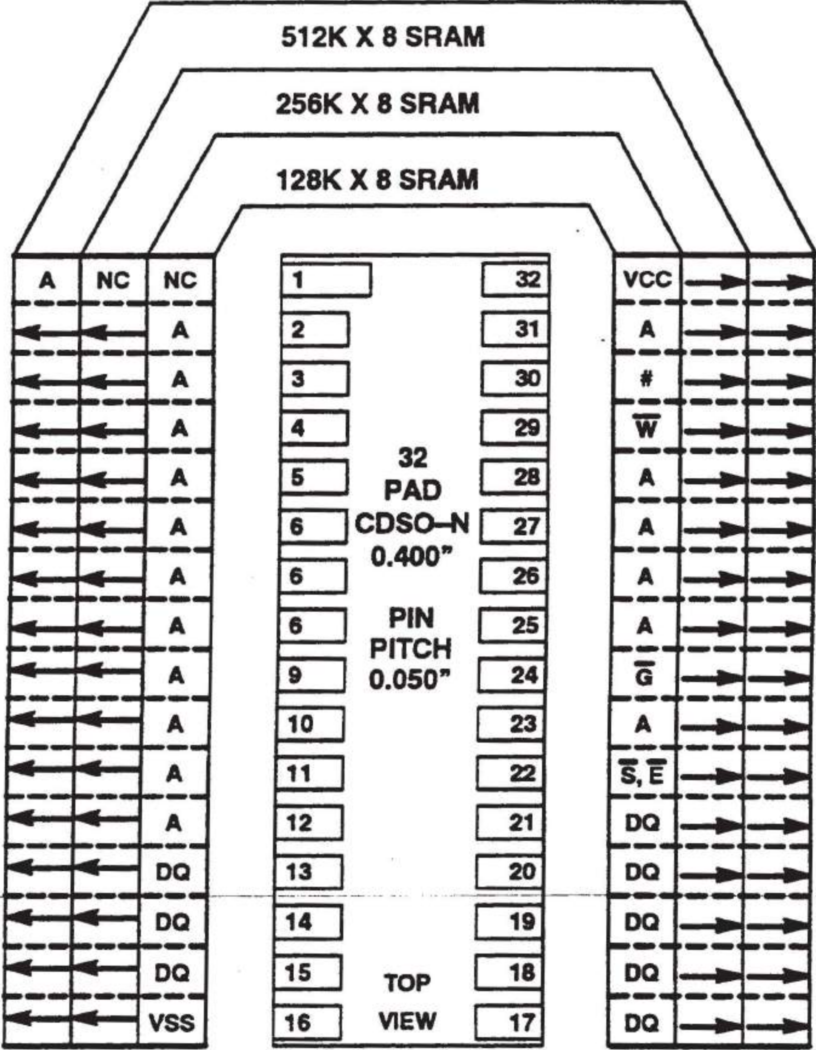


* These power pins may be VCC OR VCCA (VSS OR VSSA) as a Manufacturer option

FIGURE 3.7.5–10
32K AND 128K BY 8 TTL SSRAM IN DIP, TSOP2, AND SOJ

Jedec 0007741

jx0056-062



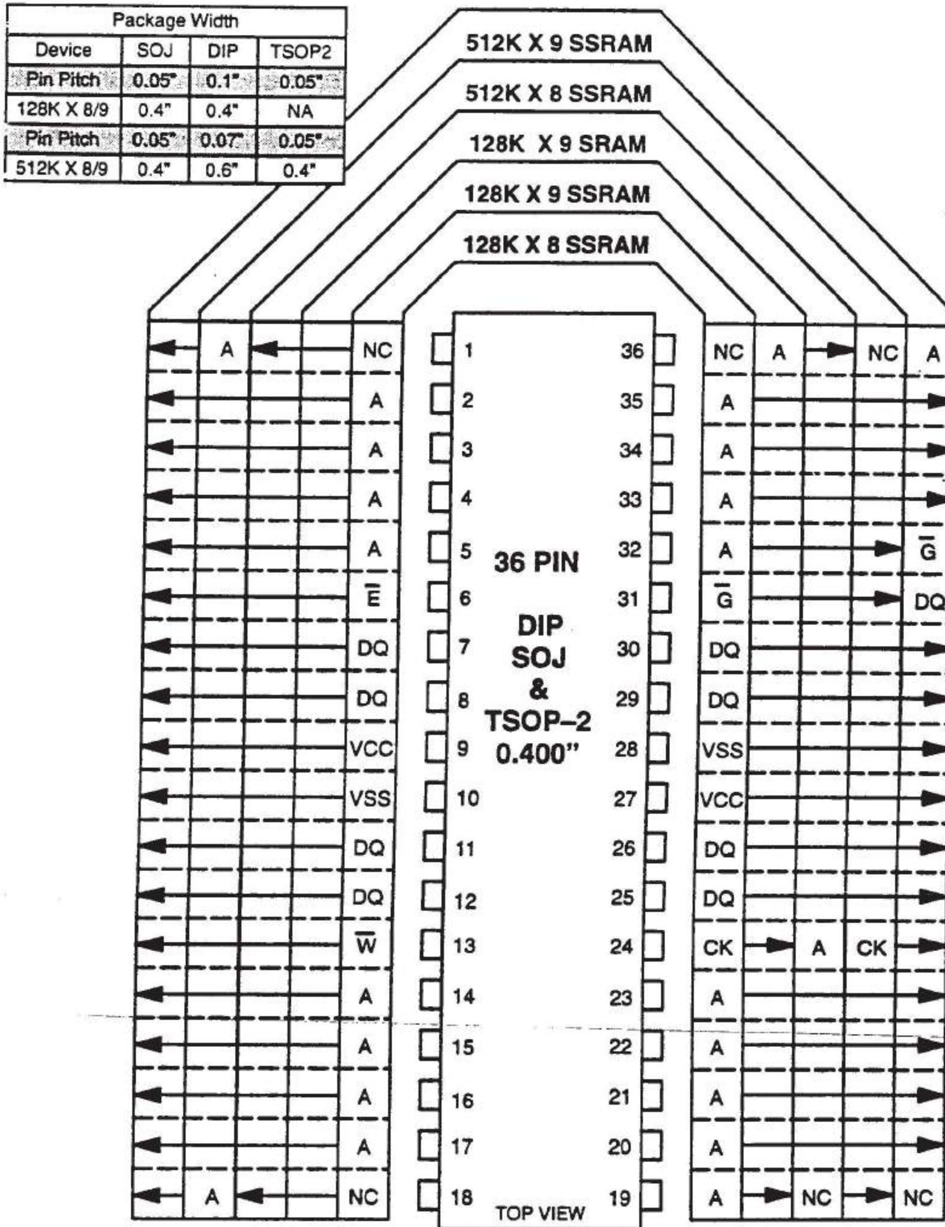
NOTE: CDSO–N is the JEDEC Standard 30 term for a LEADLESS CERAMIC SO Package

FIGURE 3.7.5–16

128K TO 512K BY 8 SRAM IN CDSO–N

Jedec 0007742

ix0056-063



Package Width			
Device	SOJ	DIP	TSOP2
Pin Pitch	0.05"	0.1"	0.05"
128K X 8/9	0.4"	0.4"	NA
Pin Pitch	0.05"	0.07"	0.05"
512K X 8/9	0.4"	0.6"	0.4"

FIGURE 3.7.5–17
128K AND 512K BY 8 & 9 SSRAM AND 128K BY 9 SRAM IN DIP, TSOP2, & SOJ
Release 4

Jedec 0007743

3.7.7.1 – 4K TO 64K BY 16 TTL SRAM IN DIP

CAPACITY—4K TO 64K WORDS OF 16 BITS,
ELECTRICAL INTERFACE—TTL
PACKAGE—40 PIN DIP, 0.6" WIDE
PIN ASSIGNMENTS—Fig. 3.7.7-1

3.7.7.2 – 4K TO 256K BY 16 TTL SRAM IN SCC

CAPACITY—4K TO 256K WORDS OF 16 BITS,
PACKAGE—44 PAD (PIN) RCC, 0.650" X 0.650"
PIN ASSIGNMENTS—Fig. 3.7.7-2

3.7.7.3 – 16K TO 256K BY 16 ADDRESS/DATA MX TTL SRAM IN DIP

CAPACITY—16K TO 256K WORDS OF 16 BITS,
LOGIC FEATURES—Address and Data MULTIPLEXED onto common pins.
PACKAGE—28 PIN DIP, 0.6" WIDE
PIN ASSIGNMENTS—Figs. 3.7.7-3

3.7.7.4 – 16K TO 256K BY 16 ADDRESS/DATA MX TTL SRAM IN RCC

CAPACITY—16K TO 256K WORDS OF 16 BITS,
LOGIC FEATURES—Address and Data MULTIPLEXED onto common pins.
PACKAGE—32 PIN (PAD) RCC, 0.450" X 0.550"
PIN ASSIGNMENTS—Figs. 3.7.7-4

3.7.7.5 – 16K AND 64K BY 18 SRAM IN SCC

CAPACITY—16K, 64K WORDS OF 18 BITS,
LOGIC FEATURES—ASYNCHRONOUS ADDRESS LATCH
—UPPER BYTE AND LOWER BYTE SELECTABLE
PACKAGE—52 TERMINAL SCC, 0.750" X 0.750"
PIN ASSIGNMENTS—Figs. 3.7.7-5

3.7.7.6 – 64K BY 16 & 18 SRAM IN 44 SOJ

CAPACITY—64K WORDS OF 16 OR 18 BITS,
LOGIC FEATURES—ASYNCHRONOUS WITH OPTIONAL ADDRESS LATCH
—UPPER BYTE AND LOWER BYTE SELECTABLE
—COMMON DATA I/O
PACKAGE—44 PIN SOJ, TBD
PIN ASSIGNMENT—Fig. 3.7.5-6

3.7.7.7 – 32K AND 64K BY 16 & 18 SRAM AND SSRAM IN 52 SCC WITH LOGIC FEATURES

CAPACITY—64K WORDS OF 16 OR 18 BITS,
NOTE: These parts are optimized for use as CACHE memory for Microprocessors and come in 5 versions, each with a different set of logic features that are optimized for different environments. In addition, there are features common to all parts.
LOGIC FEATURES—ALL VERSIONS ARE UPPER AND LOWER BYTE SELECTABLE
—ALL VERSIONS HAVE COMMON DATA I/O
—SYNCHRONOUS WITH NO SPECIAL LOGIC FEATURES.
—ASYNCHRONOUS WITH DATA LATCH ENABLE.
—SYNCHRONOUS WITH DATA LATCH ENABLE.
—SYNCHRONOUS WITH BURST MODE.
—SYNCHRONOUS WITH BURST MODE, BASE ADDRESS LATCH(S) AND WRITE CLOCK (KW). SEE FIG. 3.7.7-8 FOR KW TIMING.
PACKAGE—52 TERMINAL SCC, 0.750" X 0.750" WITH A 0.050" LEAD PITCH
PIN ASSIGNMENT—Fig. 3.7.7-7

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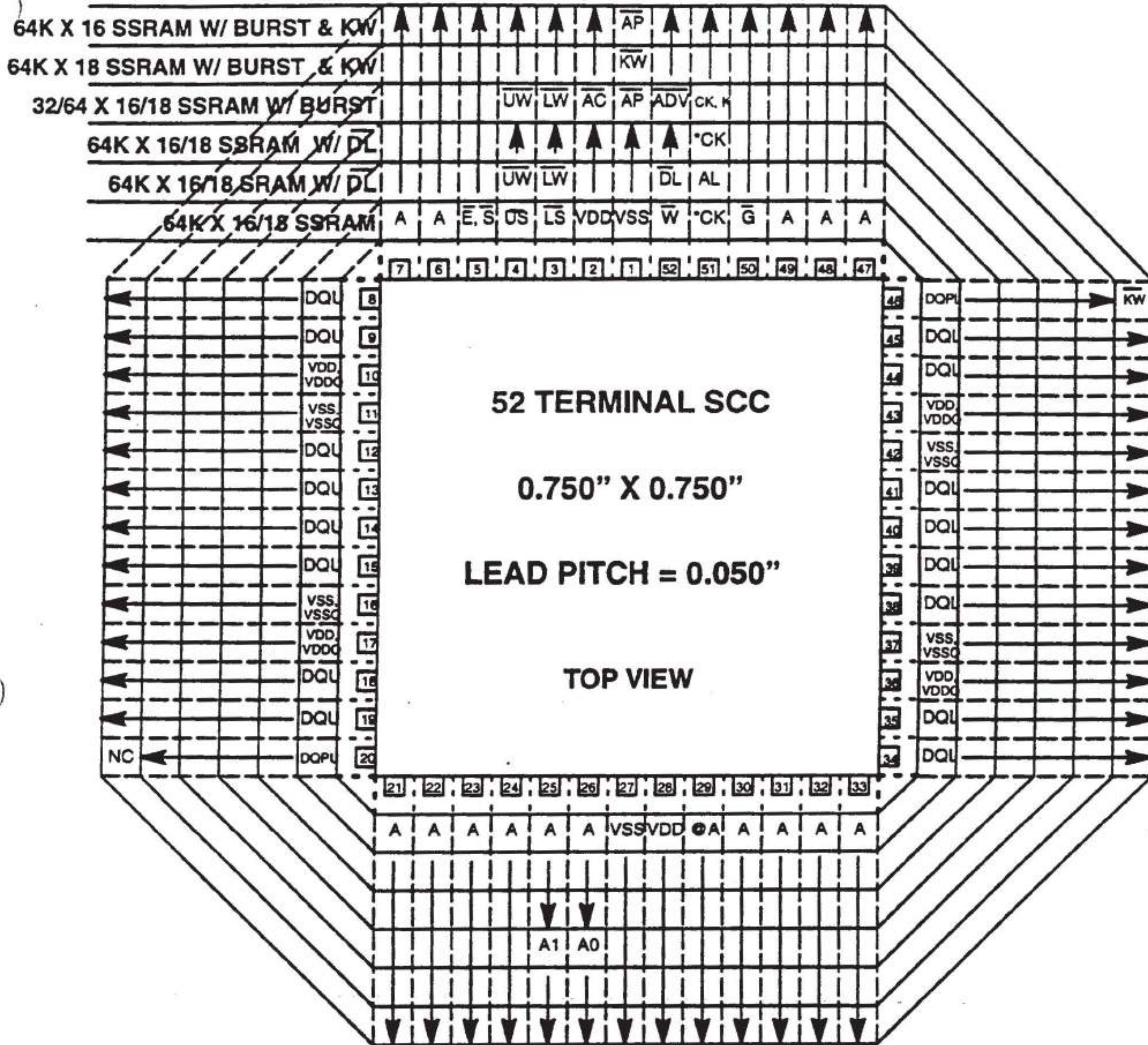
jx0056-065



1. The suffix U or L on DATA or CONTROL pins designate UPPER or LOWER byte.
2. DQPU or DQPL designate upper and lower BYTE PARITY data pins for X18 devices.
3. *CK – These clock inputs may be I/O (CK), input (C), or output (K) clock.
4. On the X16 version of X16/18 devices, the DQP pins, # 20 & 46, are NC.
5. @A – On the 32K SSRAM with Burst, P 29 is a NC.

NOTE: Some of the pins on these devices have names that are application specific and are not defined in section 2 of this Standard. They are as follows: AC is the address strobe from a microprocessor cache controller and latches the base address.
AP is the address strobe from a microprocessor and latches the base address.
ADV advances the burst address counter.
DL is DATA LATCH ENABLE.
AL is ADDRESS LATCH ENABLE.
A0 & A1 are specified due to their signficance as burst addresses. If more than two burst address bits are provided, the additional bits are supplied on pins 24 & 25.

FIGURE 3.7.7–7 A

32K & 64K BY 16 & 18 SRAM AND SSRAM WITH LOGIC FEATURES IN SCC

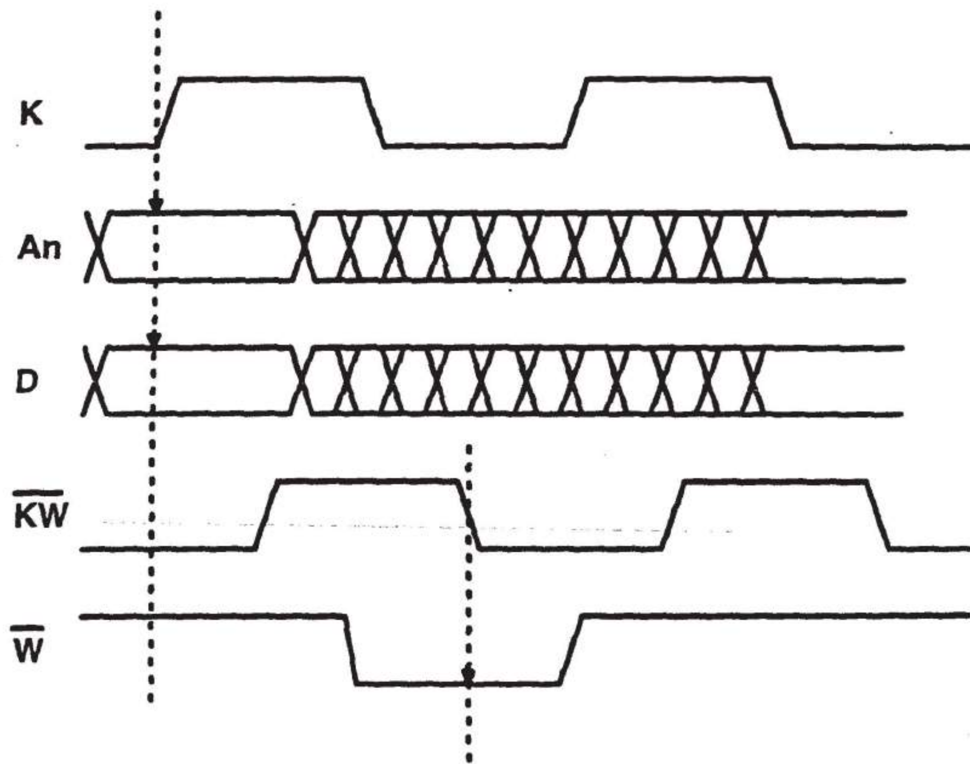


FIGURE 3.7.7–7 B
WRITE CLOCK TIMING FOR SSRAM WITH BURST MODE

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ix0056-067

3.9.1.1 – 16K BY 1 DRAM IN DIP WITH 3 SUPPLY VOLTAGES

CAPACITY—16K WORDS OF 1 BIT
LOGIC FEATURES—Multiplexed Address
PACKAGE—16 PIN DIP, 0.3" wide
POWER VOLTAGES—VDD=+12 V, VCC=+5 V, VBB=–5 V
PIN ASSIGNMENT—Fig. 3.9.1–1

3.9.1.2 – 16K TO 256K BY 1 DRAM FAMILY IN DIP

CAPACITY—16K, 64K, 256K WORDS OF 1 BIT
LOGIC FEATURES—Multiplexed Address
PACKAGE—16 PIN DIP, 0.3" wide
PIN ASSIGNMENT—Fig. 3.9.1–1

3.9.1.3 – 16K TO 256K BY 1 DRAM IN RCC

CAPACITY—16K, 64K, 256K WORDS OF 1 BIT
LOGIC FEATURES—Multiplexed Address
PACKAGE—18 PAD (PIN) RCC, 0.290" by 0.425" (16K & 64K)
—18 PAD (PIN) RCC, 0.290" by 0.490" (256K)
PIN ASSIGNMENT—Fig. 3.9.1–2

3.9.1.4 – 64K & 256K BY 1 DRAM IN ZIP

CAPACITY—64K, 256K WORDS OF 1 BIT
LOGIC FEATURES—Multiplexed Address
PACKAGE—16 PIN ZIP
PIN ASSIGNMENT—Fig. 3.9.1–3

3.9.1.5 – 1M AND 4M BY 1 DRAM FAMILY IN DIP

CAPACITY—1M, & 4M WORDS OF 1 BIT
LOGIC FEATURES—Multiplexed Address
PACKAGE—18 PIN DIP, Width: 0.3" for 1M, 0.35" for 4M,
PIN ASSIGNMENT—Fig. 3.9.1–4

3.9.1.6 – 1M TO 16M BY 1 DRAM FAMILY IN SOJ OR TSOP2

CAPACITY—1M, 4M, & 16M WORDS OF 1 BIT
LOGIC FEATURES—Multiplexed Address
PACKAGE—26/20 PIN SOJ: 0.3" by 0.675" for 1M,
— : 0.3" or 0.35" by .675" for 4M
—26/20 PIN TSOP2: 0.3" by 0.675" and 0.050" PIN PITCH for 4M
—26/20 PIN SOJ OR TSOP–2: 0.3" FOR 16M
—28/24 PIN SOJ OR TSOP–2: 0.4" BY 0.725" for 16M
SUPPLY VOLTAGE—The 16M part with an 8K refresh is approved for use with the LVTTL power and interface standard developed by Committee JC–16.
PIN ASSIGNMENT—Fig. 3.9.1–5

3.9.1.7 – 1M TO 16M BY 1 DRAM FAMILY IN ZIP

CAPACITY—1M, 4M, 16M WORDS OF 1 BIT
LOGIC FEATURES—Multiplexed Address
PACKAGE—20 PIN ZIP, 0.400" WIDE FOR THE 1M & 4M PARTS
PACKAGE—28 PIN ZIP, 0.475" WIDE FOR THE 16M PART
SUPPLY VOLTAGE—The 16M part with an 8K refresh is approved for use with the LVTTL power and interface standard developed by Committee JC–16.
PIN ASSIGNMENT—Fig. 3.9.1–6

3.9.1.8 – 1M TO 16M BY 1 NON–MUX DRAM FAMILY IN SOJ

CAPACITY—1M, 4M, & 16M WORDS OF 1 BIT
LOGIC FEATURES—Non–Multiplexed Address
PACKAGE—28, 32, OR 34 PIN DIP
PIN ASSIGNMENT—Fig. 3.9.1–7

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jx0056-068

3.9.1.9 – 1M BY 1 DRAM IN TSOP1

CAPACITY—1M WORDS OF 1 BIT
LOGIC FEATURES—Multiplexed Address
PACKAGE—24/20 PIN TSOP1
PIN ASSIGNMENT—Fig. 3.9.1–8

3.9.1.10 – 16M BY 1/4M BY 4 CONFIGURABLE DRAM IN SOJ

CAPACITY—16M WORDS OF 1 BIT *or* 4M WORDS OF 4 BITS
LOGIC FEATURES—Configurable as a X1 or a X4 part
—The data access mode can be chosen by logic control
PACKAGE—28 PIN SOJ
PIN ASSIGNMENT—Fig. 3.9.1–9

3.9.1.11 – 64M BY 1 DRAM IN SOJ OR TSOP2

CAPACITY—64M WORDS OF 1 BIT
LOGIC FEATURES—Multiplexed Addresses
PACKAGE—34 PIN SOJ, 0.500" Wide
—34 PIN TSOP2, 0.500" WIDE, 0.050" PP
PIN ASSIGNMENT—Fig. 3.9.1–10

3.9.1.12 – 2 X 16M BY 1 DRAM IN TSOP2

CAPACITY—32M WORDS OF 1 BIT
LOGIC FEATURES—Multiplexed Addresses and Two arrays of 16M x1 with common data pins and separate $\overline{RE}$ & $\overline{CE}$ inputs.
PACKAGE—28/24 PIN TSOP2, 0.400" WIDE, 0.050" PIN PITCH
PIN ASSIGNMENT—Fig. 3.9.1–11

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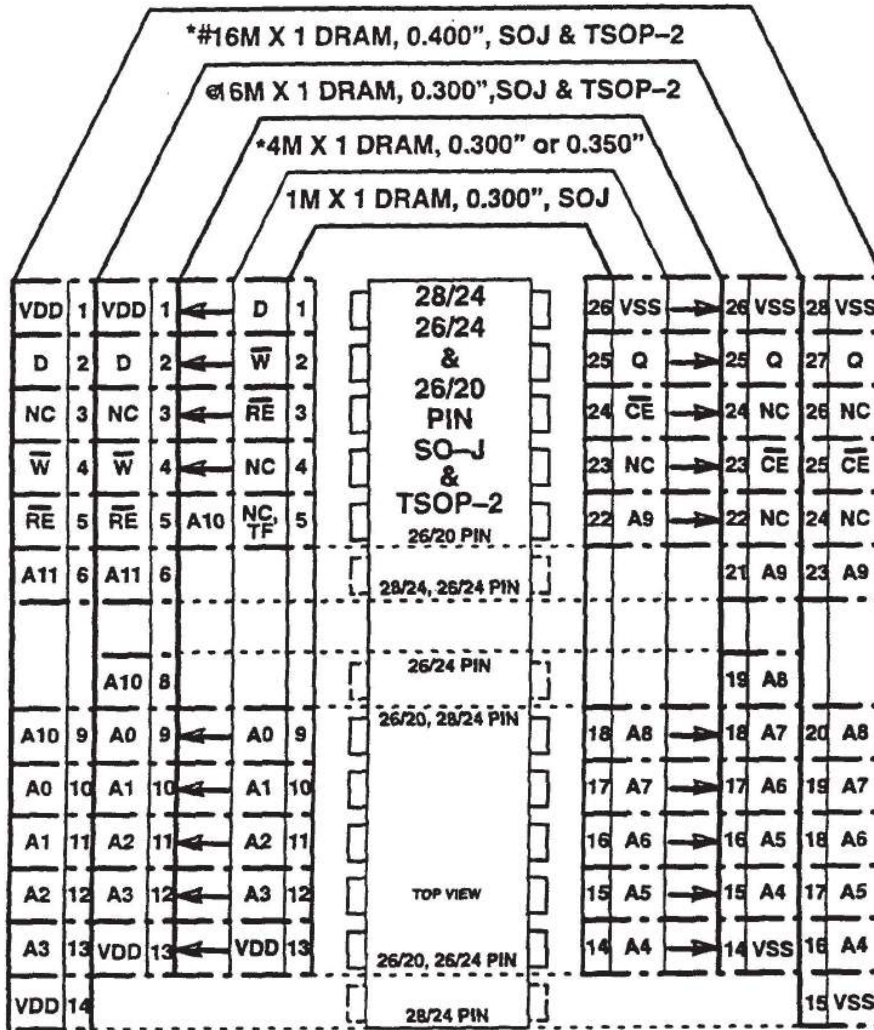
jx0056-069



REFRESH, ROW, & COLUMN, ADDRESS CONFIGURATION					
DEVICE CONFIGURATION	1M X 1	4M X 1	16M X 1	16M X 1	16M X 1, 3.3V
REFRESH COUNT	512	1K	2K	4K	8K
REFRESH ADDRESSES	A0 to A8	A0 to A9	A0 to A10	A0 to A11	A0 to A12
ROW ADDRESSES	A0 to A9	A0 to A10	A0 to A11	A0 to A11	A0 to A12
COLUMN ADDRESS	A0 to A9	AO to A10	A0 to A11	A0 to A11	A0 to A10

* NOTE – The 4M x 1 part is approved for use in 0.300" TSOP–2 and the 16M x 1 part in 0.400" TSOP–2 (PDSO–G) packages.
# NOTE – The 16M x 1 part with an 8K Refresh is approved for use with a 3.3V VCC.
@ NOTE – The 16M X 1 part in a 26/24 pin package is approved in both SOJ and TSOP–2 (PDSO–G) packages with 4K refresh.

FIGURE 3.9.1–5
1M TO 16M BY 1 DRAM FAMILY IN SOJ and TSOP–2

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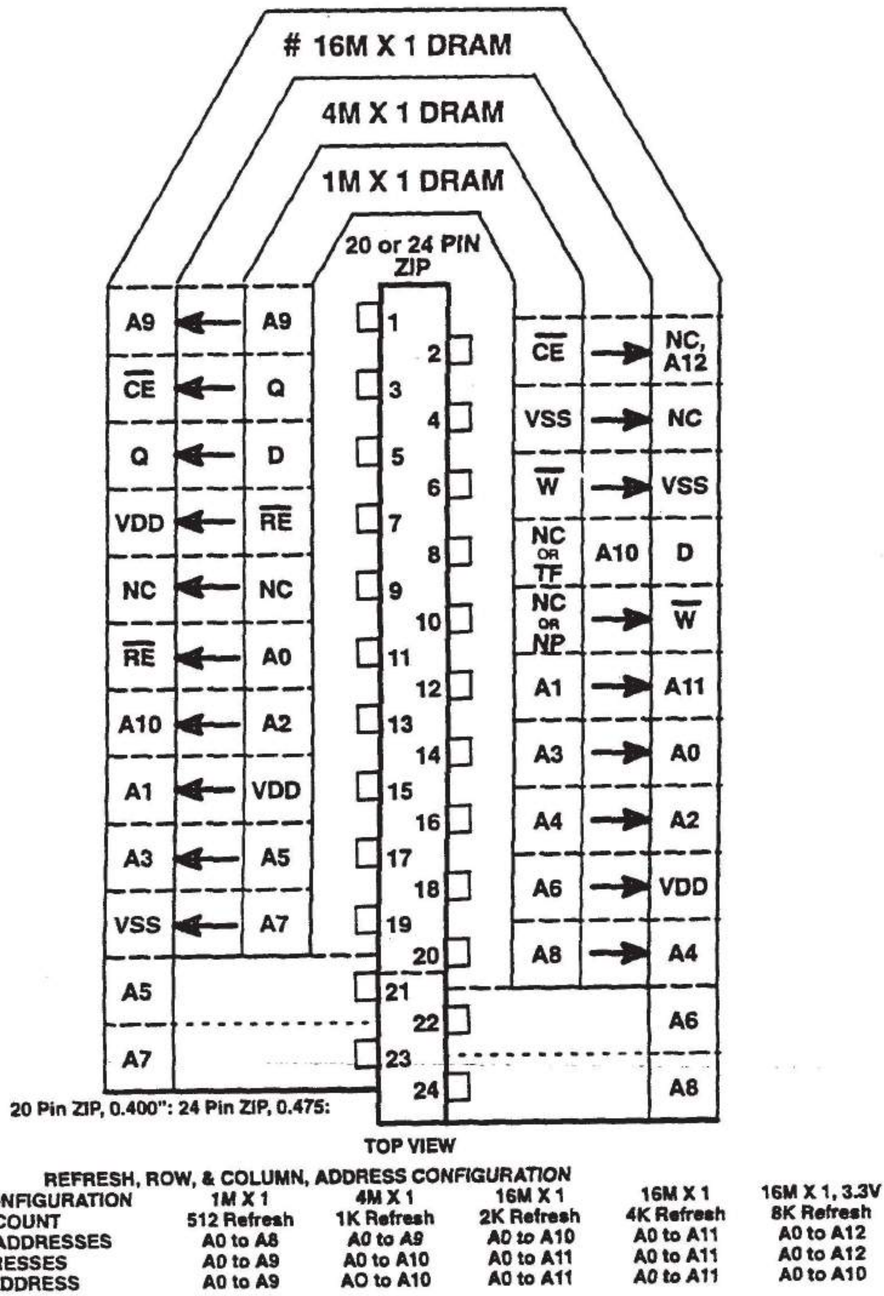
jx0056-070



REFRESH, ROW, & COLUMN, ADDRESS CONFIGURATION

DEVICE CONFIGURATION	1M X 1	4M X 1	16M X 1	16M X 1	16M X 1, 3.3V
REFRESH COUNT	512 Refresh	1K Refresh	2K Refresh	4K Refresh	8K Refresh
REFRESH ADDRESSES	A0 to A8	A0 to A9	A0 to A10	A0 to A11	A0 to A12
ROW ADDRESSES	A0 to A9	A0 to A10	A0 to A11	A0 to A11	A0 to A12
COLUMN ADDRESS	A0 to A9	AO to A10	A0 to A11	A0 to A11	A0 to A10

NOTE – The 16M x 1 part with an 8K Refresh is approved for use with a 3.3V VDD.

FIGURE 3.9.1–6
1M TO 16M BY 1 DRAM FAMILY IN ZIP

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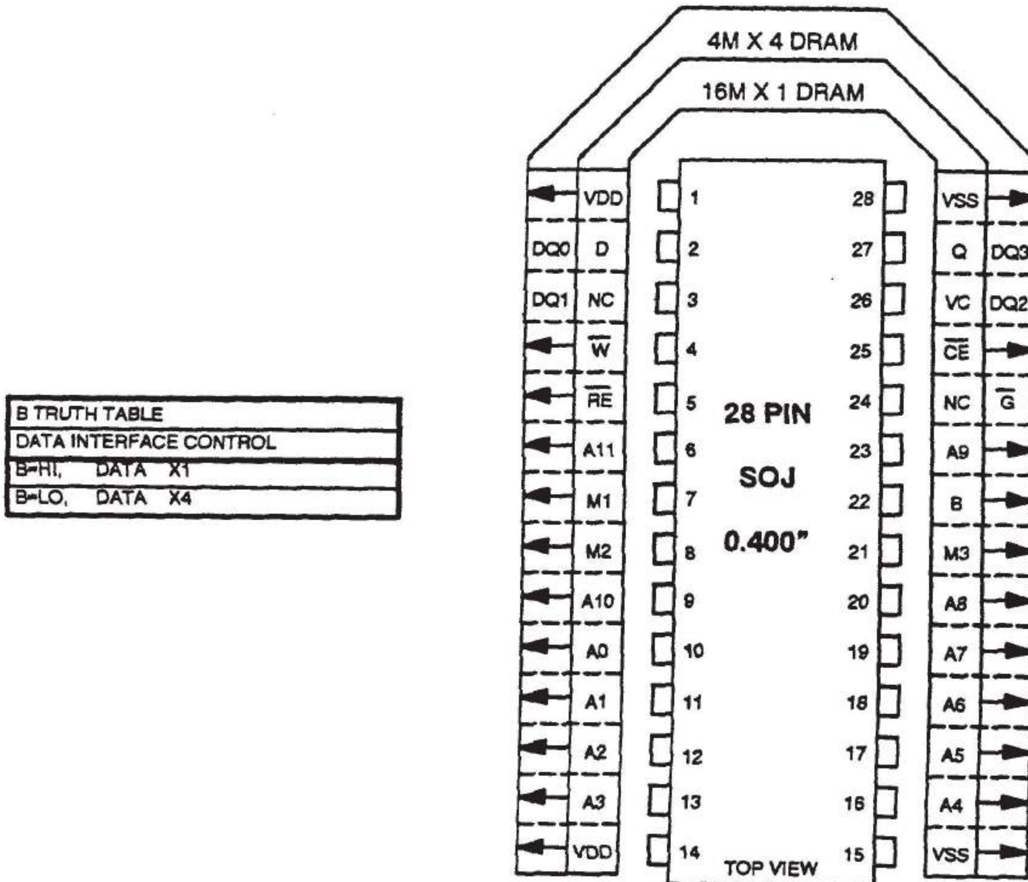
jx0056-071



B TRUTH TABLE		
DATA INTERFACE CONTROL		
B=HI,	DATA	X1
B=LO,	DATA	X4

The default state for M1, M2, M3, and B ahould be HI when no external connection is made.

M1/M2/M3 TRUTH TABLE		M1	M2	M3
MANDATORY MODE	FAST PAGE	HI	HI	HI
OPTIONAL MODES	NIBBLE	LO	HI	HI
	BYTE	LO	LO	HI
	BURST	LO	HI	LO
	STATIC COLUMN	HI	LO	HI
	VENDOR SPECIFIC	LO	LO	LO
	VENDOR SPECIFIC	HI	HI	LO
	VENDOR SPECIFIC	HI	LO	LO

FIGURE 3.9.1–9
16M X 1/4M X 4 CONFIGURABLE DRAM IN SOJ

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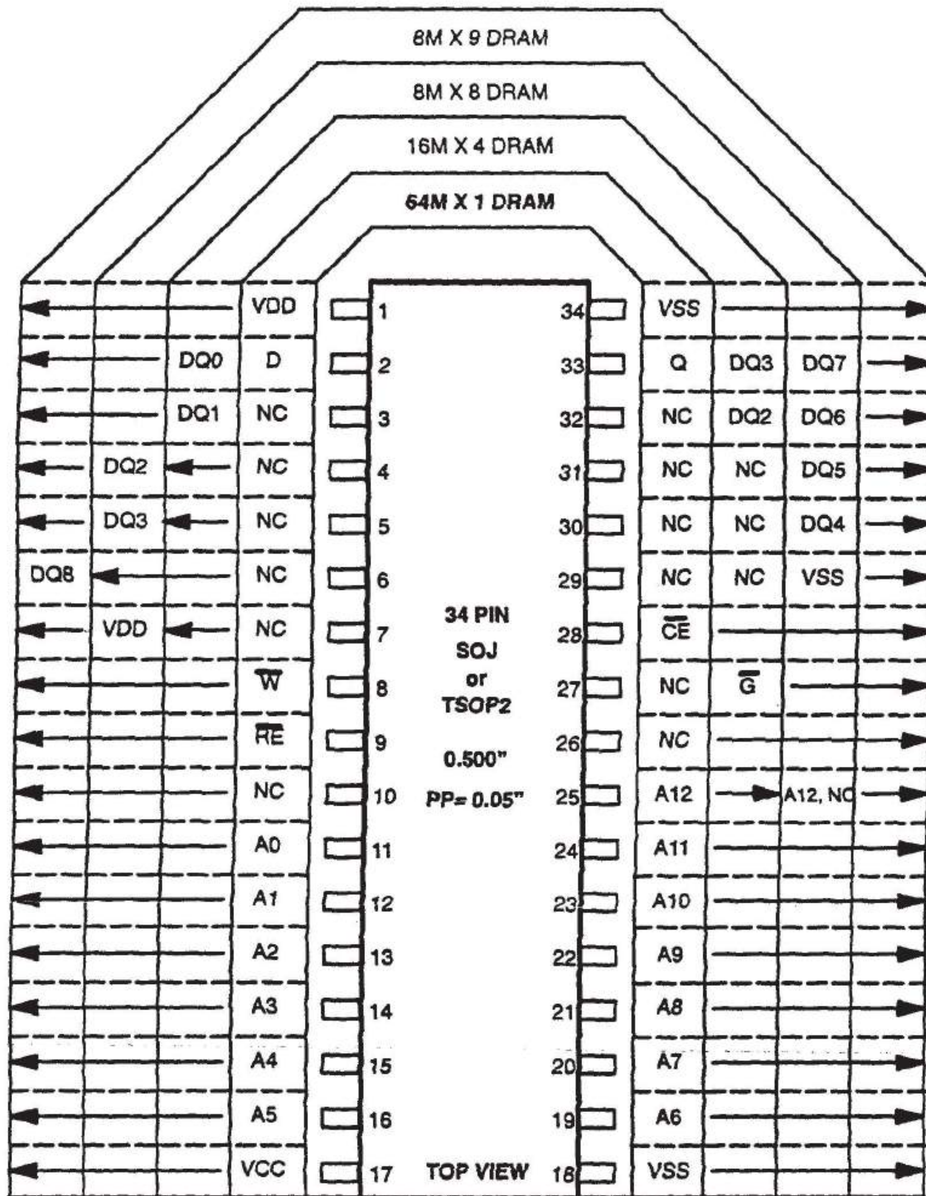
jx0056-072



ROW, COLUMN, & REFRESH ADDRESS CONFIGURATIONS

DEVICE CONFIGURATION REFRESH COUNT	64M X 1	16M X 4	8M X 8(9) 4K Refresh	8M X 8(9) 8K Refresh
ROW/REFRESH ADDRESSES	A0 Through A12	A0 Through A12	A0 Through A11	A0 Through A12
COLUMN ADDRESSES	A0 Through A12	A0 Through A10	A0 Through A10	A0 Through A9

FIGURE 3.9.1–10
64M BY 1 DRAM IN SOJ & TSOP2

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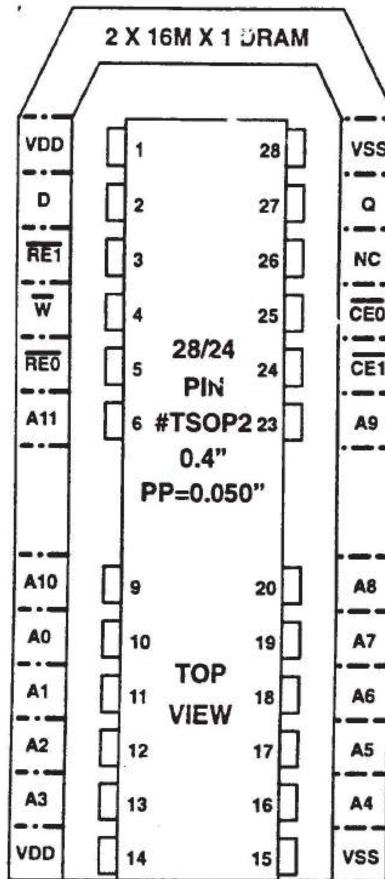
jx0056-073



The JEDEC approved term for this package is PDSO–G

ROW, REFRESH, & COLUMN ADDRESS CONFIGURATION

DEVICE CONFIGURATION	2 X 16M X 1	2 X 16M X 1
REFRESH COUNT	2048 Refresh	4096 Refresh
ROW ADDRESS	A0 → A11	A0 → A11
REFRESH ADDRESS	A0 → A10	A0 → A11
COLUMN ADDRESS	A0 → A11	A0 → A11

FIGURE 3.9.1–11
2 X 16M BY 1 DRAM IN TSOP2

3.9.2.1 – 16K & 64K BY 4 DRAM IN DIP

CAPACITY—16K, 64K WORDS OF 4 BITS
LOGIC FEATURES—Multiplexed Address, Common DATA I/O
PACKAGE—18 PIN DIP, 0.3" WIDE
PIN ASSIGNMENT—Fig. 3.9.2-1

3.9.2.2 – 16K BY 4 DRAM IN DIP

CAPACITY—16K WORDS OF 4 BITS
LOGIC FEATURES—Multiplexed Address, Separate DATA I/O
PACKAGE—20 PIN DIP, 0.3" WIDE
PIN ASSIGNMENT—Fig. 3.9.2-1
NOTE: At the time that this document was published, this standard was in the process of being rescinded by the Committee.

3.9.2.3 – 64K BY 4 DRAM IN RCC

CAPACITY—64K WORDS OF 4 BITS
LOGIC FEATURES—Multiplexed Address with Common DATA I/O
PACKAGE—22 PAD (PIN) RCC, 0.290" X 0.490"
PIN ASSIGNMENT—Fig. 3.9.2-2

3.9.2.4 – 256K & 1M BY 4 DRAM FAMILY IN DIP

CAPACITY—256K, 1M WORDS OF 4 BITS
LOGIC FEATURES—Multiplexed Address
PACKAGE—20 PIN DIP, Width: 0.3" for 256K & 1M,
PIN ASSIGNMENT—Fig. 3.9.2-3

3.9.2.5 – 256K TO 4M BY 4 DRAM FAMILY IN SOJ & TSOP2

CAPACITY—256K, 1M, 4M WORDS OF 4 BITS
LOGIC FEATURES—Multiplexed Address
PACKAGE—26/20 PIN SOJ: 0.3" by 0.675" for 256K
—26/20 PIN SOJ or TSOP2: 0.3" or 0.35" by 0.675" for 1M
—26/24 PIN SOJ OR TSOP-2: 0.3" for 4M
—28/24 PIN SOJ: 0.4" by 0.725 for 4M
PIN ASSIGNMENT—Fig. 3.9.2-4

3.9.2.6 – 64K TO 4M BY 4 DRAM IN ZIP

CAPACITY—64K, 256K, 1M, 4M WORDS OF 4 BITS
LOGIC FEATURES—Multiplexed Address
PACKAGE—20 PIN ZIP, 0.400" WIDE FOR 64K, 256K, & 1M PARTS
—24 PIN ZIP, 0.475" WIDE FOR 4M PART
PIN ASSIGNMENT—Fig. 3.9.2-5

3.9.2.7 – 256K & 1M BY 4 DRAM WITH 4 CE IN SOJ & TSOP2

CAPACITY—256K, 1M WORDS OF 4 BITS
LOGIC FEATURES—Multiplexed Address with 4 CE clocks controlling the 4 data bits
PACKAGE—26/24 PIN SOJ, Width: 0.3"
—26/24 PIN TSOP2, WIDTH: 0.3", PIN PITCH: 0.050"
PIN ASSIGNMENT—Fig. 3.9.2-6

3.9.2.8 – 256K BY 4 DRAM IN TSOP1

CAPACITY—256K WORDS OF 4 BITS
LOGIC FEATURES—Multiplexed Address
PACKAGE—24/20 PIN TSOP1, 14.4 mm x 6.0 mm, 0.5 mm LEAD PITCH
PIN ASSIGNMENT—Fig. 3.9.2-7

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jx0056-075

3.9.2.9 – 16M BY 1/4M BY 4 CONFIGURABLE DRAM IN SOJ

CAPACITY—16M WORDS OF 1 BIT or 4M WORDS OF 4 BITS
LOGIC FEATURES—Configurable as a X1 or a X4 part
—The data access mode can be chosen by logic control
PACKAGE—28 PIN SOJ
PIN ASSIGNMENT—Fig. 3.9.2–8

3.9.2.10 – 256K TO 4M BY 4 NON–MUX DRAM FAMILY IN SOJ

CAPACITY—256K, 1M, 4M WORDS OF 4 BITS
LOGIC FEATURES—Non–Multiplexed Address
PACKAGE—28, 32, OR 34 PIN SOJ, WIDTH Not yet defined
PIN ASSIGNMENT—Fig. 3.9.2–9

3.9.2.11 – 4M BY 4 DRAM WITH 1 $\overline{CE}$ AND 4 $\overline{CE}$ IN TSOP2

CAPACITY—4M WORDS OF 4 BITS
LOGIC FEATURES—Multiplexed Address
—There are two versions of this part, one with 1 $\overline{CE}$ and one with 4 $\overline{CE}$ controlling each of the data bits
PACKAGE—28/24 PIN TSOP2, 0.4" WIDE FOR THE 1 $\overline{CE}$ PART
— 28 PIN TSOP2, 0.4" WIDE FOR THE 4 $\overline{CE}$ PART
PIN ASSIGNMENT—Fig. 3.9.2–10

3.9.2.12 – 16M BY 4 DRAM IN SOJ & TSOP2

CAPACITY—16M WORDS OF 4 BITS
LOGIC FEATURES—Multiplexed Address
PACKAGE—34 PIN SOJ, WIDTH: 0.5"
—34PIN TSOP2, WIDTH: 0.5", PIN PITCH: 0.050"
PIN ASSIGNMENT—Fig. 3.9.2–11

3.9.2.13 – 2M BY 2 DRAM IN SOJ & TSOP2

CAPACITY—2M WORDS OF 2 BITS
LOGIC FEATURES—Multiplexed Address and a separate $\overline{CE}$ control for each data bit.
PACKAGE—26/24 PIN SOJ or TSOP2, WIDTH: 0.3", PIN PITCH: 0.050"
PIN ASSIGNMENT—Fig. 3.9.2–12

Jedec 0007755

jx0056-076

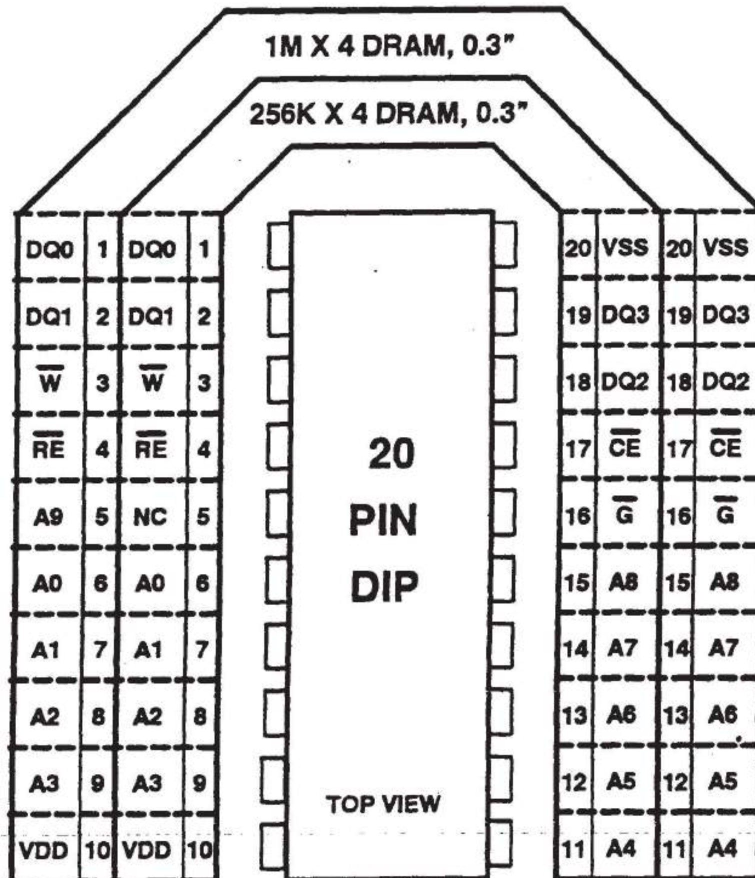

FIGURE 3.9.2–3

256K & 1M BY 4 ADDRESS MULTIPLEXED DRAM IN DIP

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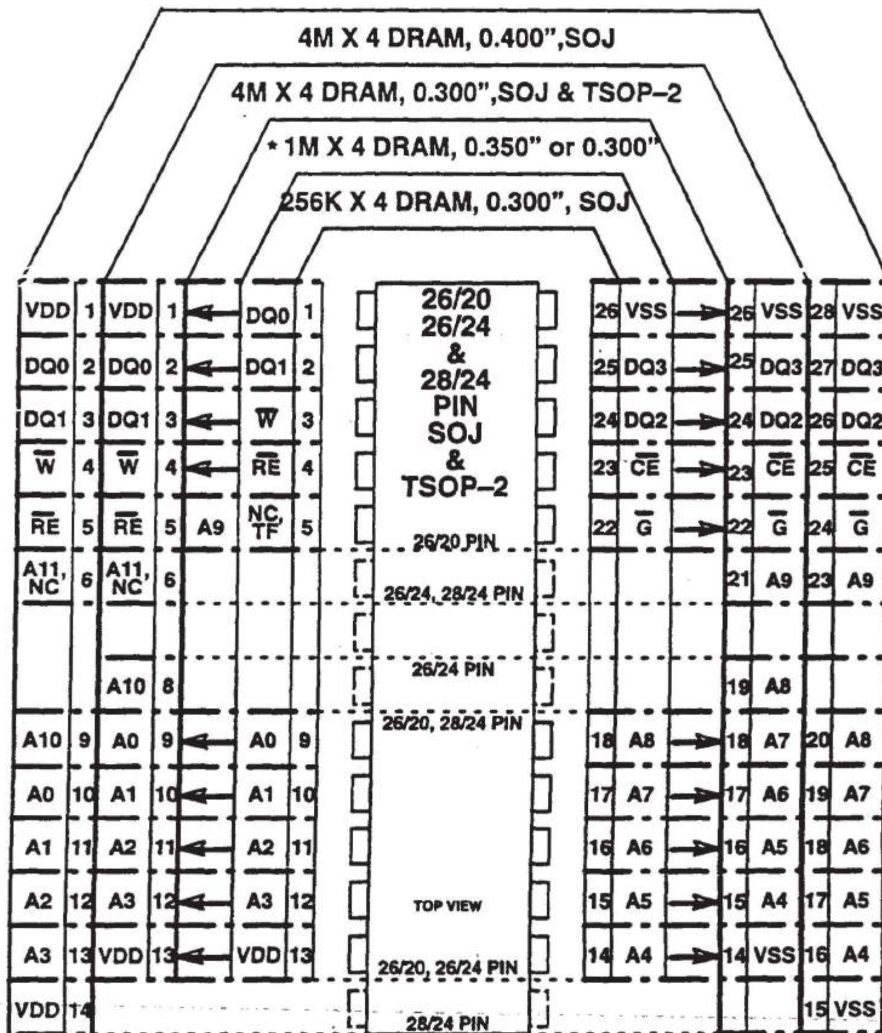
jx0056-077



REFRESH, ROW, & COLUMN, ADDRESS CONFIGURATION

DEVICE CONFIGURATION	256K X 4	1M X 4	4M X 4	4M X 4
REFRESH COUNT	512 Refresh	1K Refresh	2K Refresh	4K Refresh
REFRESH ADDRESSES	A0 → A8	A0 → A9	A0 → A10	A0 → A11
ROW ADDRESSES	A0 → A8	A0 → A9	A0 → A10	A0 → A11
COLUMN ADDRESS	A0 → A8	AO → A9	A0 → A10	A0 → A9

* NOTE – The 1M X 4 part is approved for use in a 0.300" TSOP2 package
The JEDEC Std. 30 approved term for the TSOP-2 package is PDSO-G.

FIGURE 3.9.2-4
256K TO 4M BY 4 DRAM IN SOJ AND TSOP-2

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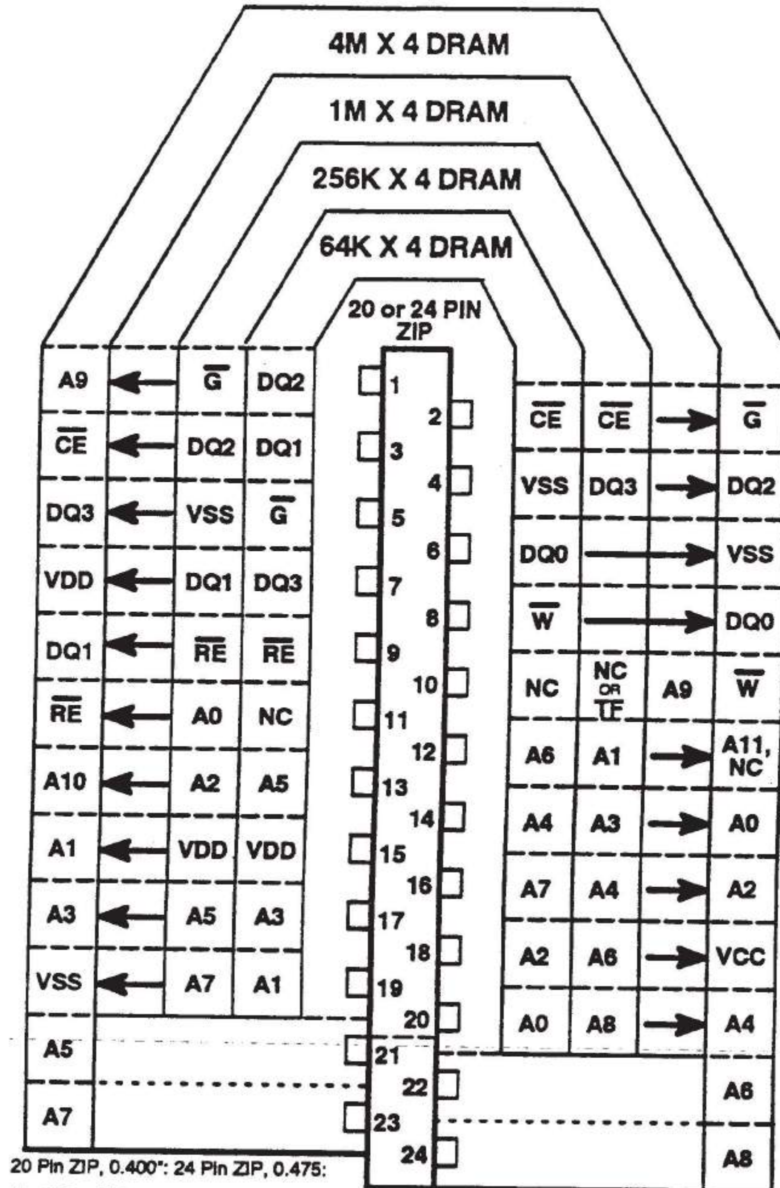
jx0056-078



REFRESH, ROW, & COLUMN, ADDRESS CONFIGURATION

DEVICE CONFIGURATION	64K X 4	256K X 4	1M X 4	4M X 4	4M X 4
REFRESH COUNT	256 Refresh	512 Refresh	1K Refresh	2K Refresh	4K Refresh
REFRESH ADDRESSES	A0 TO A7	A0 TO A7	A0 TO A9	A0 TO A10	A0 TO A11
ROW ADDRESSES	A0 TO A7	A0 TO A7	A0 TO A9	A0 TO A10	A0 TO A11
COLUMN ADDRESS	AO TO A7	A0 TO A7	A0 TO A9	A0 TO A10	A0 TO A9

FIGURE 3.9.2–5
64K TO 4M BY 4 DRAM IN ZIP

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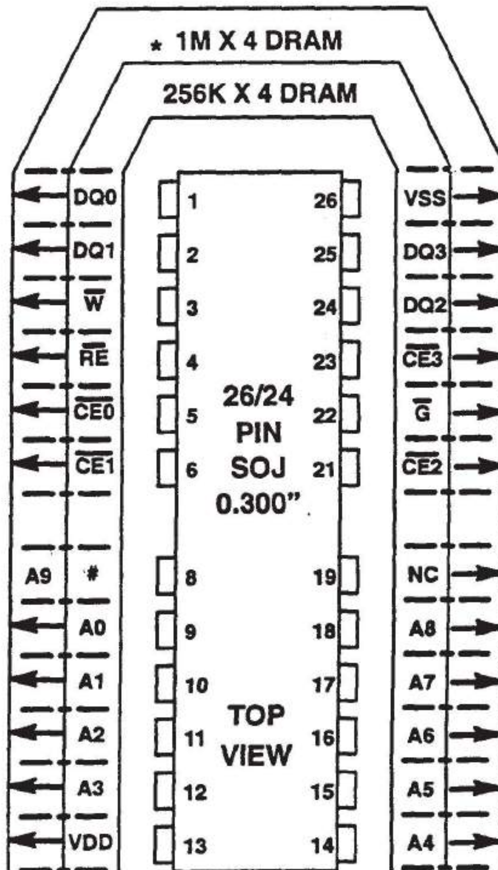
jx0056-079



= NC or TF * THE 1M X 4 PART IS ALSO APPROVED FOR USE IN A TSOP2 PACKAGE WITH A PIN PITCH OF 0.050"

CAUTION: At the time that Release 4 of Standard 21–C was being prepared for publication, there was an unresolved patent dispute involving DRAM with 4 $\overline{CE}$.

FIGURE 3.9.2–6
256K & 1M BY 4 DRAM WITH 4 $\overline{CE}$ IN SOJ & TSOP2

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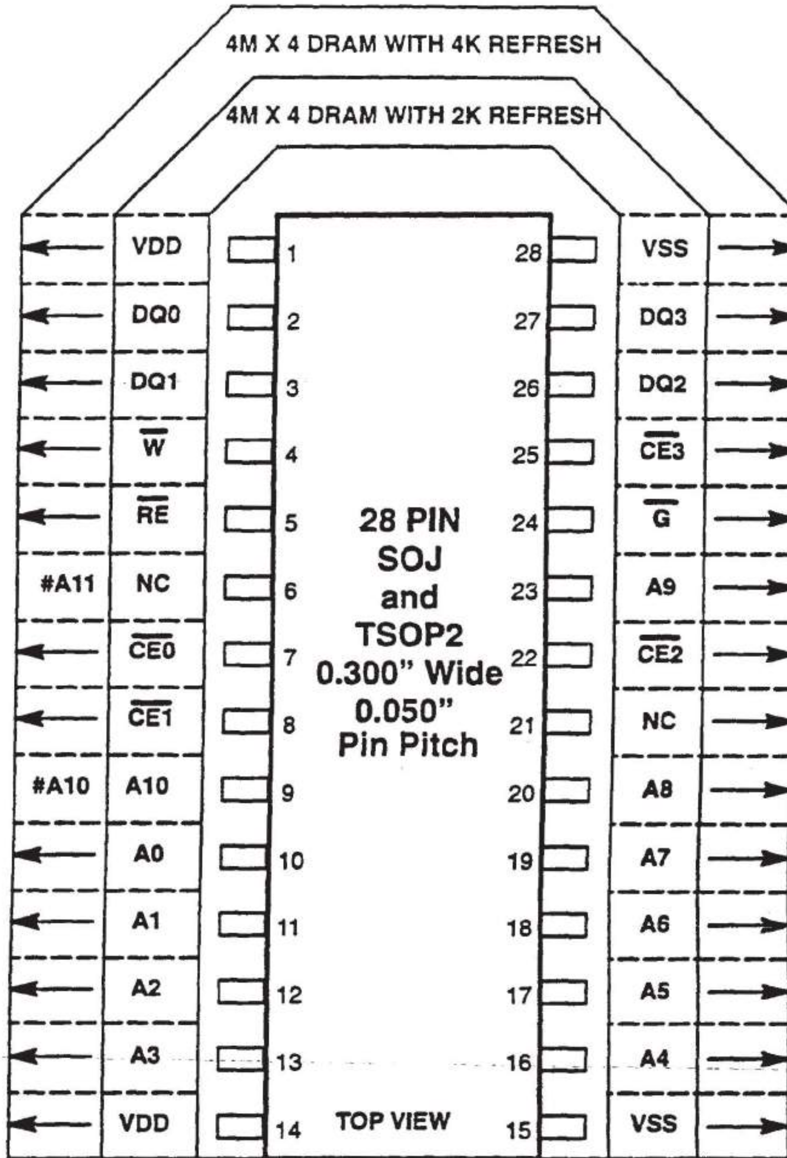
jx0056-080

Pin	4M X 4	Pin	1M X 4	Pin	256K X 4	Pin		Pin	256K X 4	Pin	1M X 4	Pin	4M X 4	Pin
1	VSS	1										34	VCC	34
2	A14	2	VSS	1						32	VCC	33	A15	33
3	A13	3	A14	2						31	A15	32	A16	32
4	A12	4	A13	3	A13	1		28	VCC	30	A16	31	A17	31
5	A11	5	A12	4	A12	2		27	A14	29	A17	30	A18	30
6	A5	6	A11	5	A11	3		26	A15	28	A18	29	A6	29
7	A4	7	A5	6	A10	4		25	A16	27	A6	28	A7	28
8	A3	8	A4	7	A9	5		24	A8	26	A7	27	A8	27
9	A2	9	A3	8	A3	6		23	A7	25	A8	26	A9	26
10	A1	10	A2	9	A2	7		22	A6	24	A9	25	A10	25
11	A0	11	A1	10	A1	8		21	A5	23	A10	24	A20	24
12	A21	12	A0	11	A0	9		20	A4	22	A19	23	A19	23
13	F	13	F	12	F	10		19	A17	21	DQ	22	DQ	22
14	$\overline{E}$	14	$\overline{E}$	13	$\overline{E}$	11		18	DQ	20	DQ	21	DQ	21
15	$\overline{G}$	15	$\overline{G}$	14	$\overline{G}$	12		17	DQ	19	DQ	20	DQ	20
16	$\overline{W}$	16	$\overline{W}$	15	$\overline{W}$	13		16	DQ	18	DQ	19	DQ	19
17	VSS	17	VSS	16	VSS	14		15	DQ	17	VCC	18	VCC	18

FIGURE 3.9.2–9
256K TO 4M BY 4 NON–MULTIPLEXED DRAM IN SOJ



The JEDEC Std. No 30 designator for the TSOP2 package is PDSO–G

NOTE: A10 & A11 are used as defined in the following table as a function of the refresh count implemented.

Device Configuration	4M X 4,	4M X 4,
Refresh Count	2K	4K
Row/Refresh Address	A0 → A10	A0 → A11
Column Address	A0 → A10	A0 → A9

CAUTION: At the time that Release 4 of Standard 21–C was being prepared for publication, there was an unresolved patent dispute involving DRAM with 4 $\overline{CE}$.

FIGURE 3.9.2–10

4M BY 4 DRAM WITH 4 $\overline{CE}$ IN SOJ AND TSOP2

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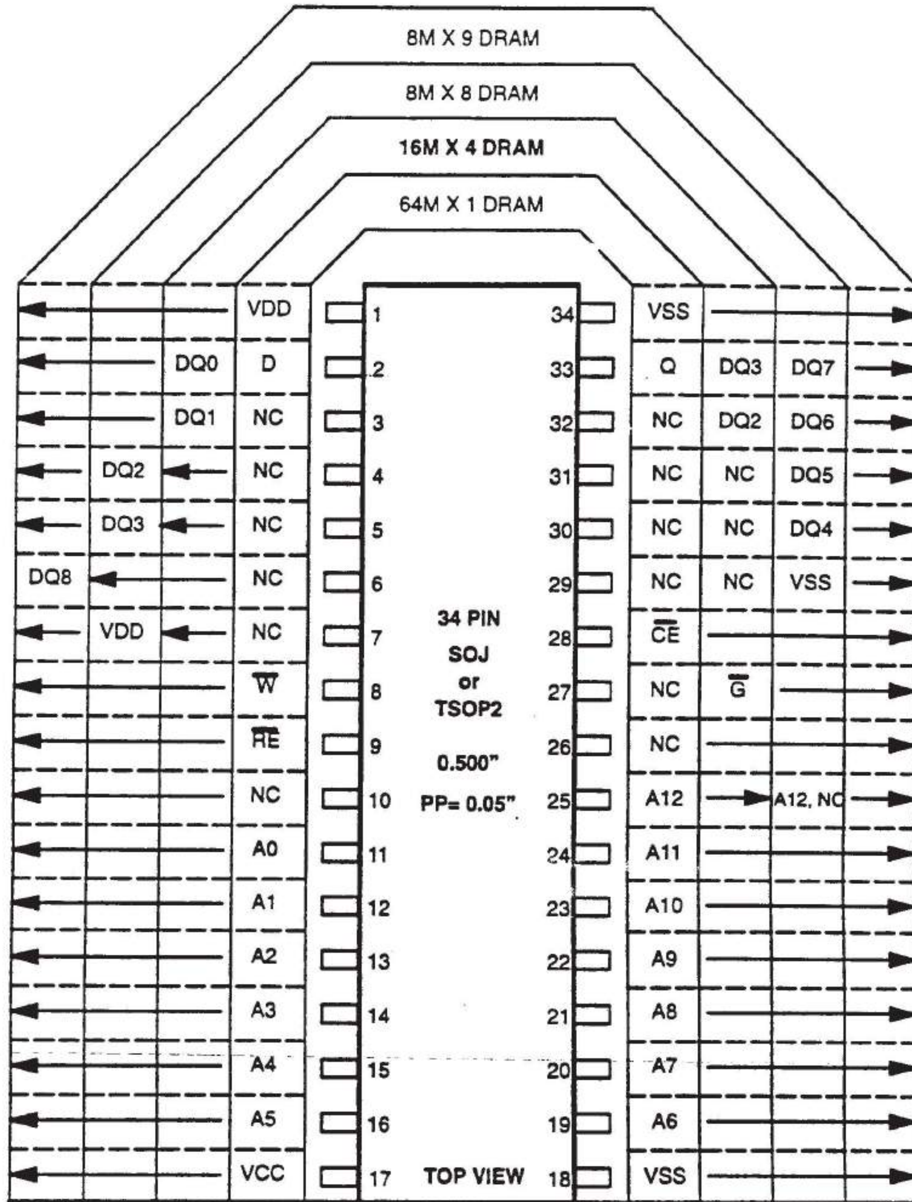
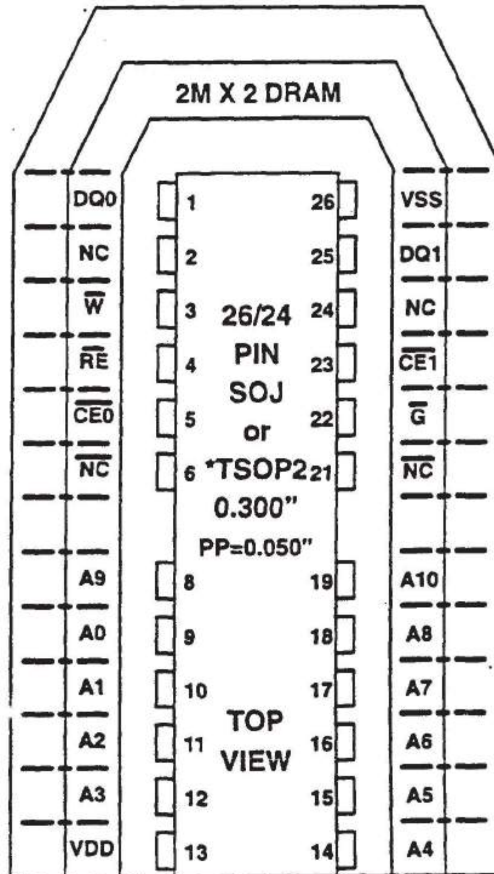
ix0056-082



ROW, COLUMN, & REFRESH ADDRESS CONFIGURATIONS

DEVICE CONFIGURATION REFRESH COUNT	64M X 1	16M X 4	8M X 8(9) 4K Refresh	8M X 8(9) 8K Refresh
ROW/REFRESH ADDRESSES	A0 Through A12	A0 Through A12	A0 Through A11	A0 Through A12
COLUMN ADDRESSES	A0 Through A12	A0 Through A10	A0 Through A10	A0 Through A9

FIGURE 3.9.2–11
16M BY 4 DRAM IN SOJ & TSOP2



* The JEDEC approved term for this package is PDSO-G

ROW, REFRESH, & COLUMN ADDRESS CONFIGURATION

DEVICE CONFIGURATION	2M X 2
REFRESH COUNT	1024 Refresh
ROW ADDRESS	A0 → A10
REFRESH ADDRESS	A0 → A9
COLUMN ADDRESS	A0 → A9

FIGURE 3.9.2-12
2M BY 2 DRAM WITH 2 CE IN SOJ AND TSOP2

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3.9.3.1 – 32K BY 8 DRAM IN DIP

CAPACITY—32K WORDS OF 8 BITS,
PACKAGE—28 PIN DIP, 0.6" WIDE
PIN ASSIGNMENT—Fig. 3.9.3–1

3.9.3.2 – 32K BY 8 DRAM IN RCC

CAPACITY—32K WORDS OF 8 BITS,
PACKAGE—32 PAD (PIN) RCC, 0.450" X 0.550"
PIN ASSIGNMENT—Fig. 3.9.3–2

3.9.3.3 – 512K BY 8 & BY 9 DRAM IN SOJ, TSOP2, & ZIP

CAPACITY—512K WORDS OF 8 & 9 BITS,
LOGIC FEATURES—MULTIPLEXED ADDRESS
PACKAGE—28 PIN SOJ, 0.400" WIDE
—28 PIN TSOP2, 0.400" WIDE
—28 PIN ZIP, 0.475" WIDE
PIN ASSIGNMENT—SOJ & TSOP2, Fig. 3.9.3–3
—ZIP, Fig. 3.9.3–4

3.9.3.4 – 512K BY 8 & BY 9 NON–MUX DRAM IN SOJ

CAPACITY—512K WORDS OF 8 & 9 BITS,
LOGIC FEATURES—NON–MULTIPLEXED ADDRESS
PACKAGE—36 PIN SOJ, 0.400" WIDE
PIN ASSIGNMENT—Fig. 3.9.3–5

3.9.3.5 – 2M BY 8 & 9 DRAM IN SOJ & TSOP2

CAPACITY—2M WORDS OF 8 & 9 BITS,
LOGIC FEATURES—MULTIPLEXED ADDRESS
—At the option of the manufacturer, these parts may utilize either 2K or 4K refresh cycles
PACKAGE—28 PIN SOJ or TSOP2, 0.400" WIDE, 0.050" PIN PITCH for 2M BY 8 Part
—32 PIN SOJ or TSOP2, 0.400" WIDE, 0.050" PIN PITCH for 2M BY 8 or 9 Part
PIN ASSIGNMENT—Fig. 3.9.3–6

3.9.3.6 – 8M BY 8 & 9 DRAM IN SOJ & TSOP2

CAPACITY—8M WORDS OF 8 or 9 BITS,
LOGIC FEATURES—MULTIPLEXED ADDRESS
—At the option of the manufacturer, these parts may utilize either 4K or 8K refresh cycles
PACKAGE—34 PIN SOJ, 0.500" WIDE
—34 PIN TSOP2, 0.500" WIDE, 0.025" PIN PITCH
PIN ASSIGNMENT—Fig. 3.9.3–7

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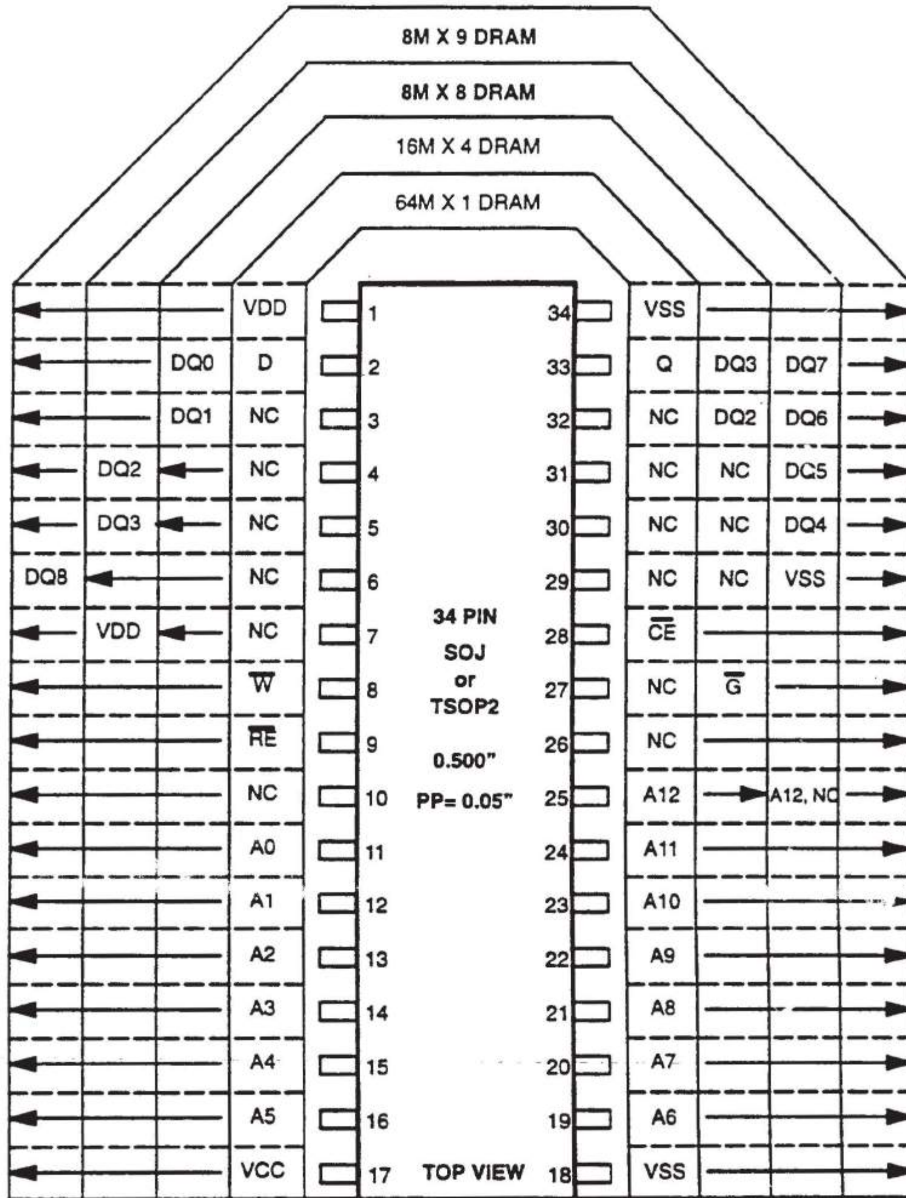

ROW, COLUMN, & REFRESH ADDRESS CONFIGURATIONS

DEVICE CONFIGURATION REFRESH COUNT	64M X 1	16M X 4	8M X 8(9) 4K Refresh	8M X 8(9) 8K Refresh
ROW/REFRESH ADDRESSES	A0 Through A12	A0 Through A12	A0 Through A11	A0 Through A12
COLUMN ADDRESSES	A0 Through A12	A0 Through A10	A0 Through A10	A0 Through A9

FIGURE 3.9.3–7
8M BY 8 & 9 DRAM IN SOJ & TSOP2

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jx0056-086

3.9.4.1 – 64K BY 16 DRAM WITH 2 $\overline{W}$ IN SOJ & TSOP2

CAPACITY—64K WORDS OF 16 BITS,
LOGIC FEATURES—MULTIPLEXED ADDRESS
PACKAGE—40 PIN SOJ, 0.400" WIDE
—44/40 PIN TSOP2, 0.400" WIDE, 0.8mm PIN PITCH
PIN ASSIGNMENT—Fig. 3.9.4–1 (SOJ)
—Fig. 3.9.4–6 (TSOP2)

3.9.4.2 – 256K & 1M BY 16 & 18 WITH 2 $\overline{CE}$ OR 2 $\overline{W}$ DRAM IN SOJ & TSOP2

CAPACITY—256K, 1M WORDS OF 16 & 18 BITS,
LOGIC FEATURES—MULTIPLEXED ADDRESS
—There are two versions of these parts, one with 2 $\overline{W}$ and the other with 2 $\overline{CE}$.
—The two clocks control the LOWER BYTE and UPPER BYTE data bits.
—The 1M part allows the option of the manufacturer to utilize either 1K or 4K refresh cycles
PACKAGE—256K in 40 PIN SOJ, 0.400" WIDE
—256K in 44/40 PIN TSOP2, 0.400" WIDE, 0.8 mm PIN PITCH
—1M IN 42 PIN SOJ, 0.400" WIDE
—1M in 50/44 PIN TSOP2, 0.400" WIDE, 0.8 mm PIN PITCH
PIN ASSIGNMENT—Fig. 3.9.4–2 (256K SOJ)
—Fig. 3.9.4–3 (256K TSOP2)
—Fig. 3.9.4–4 (1M SOJ)
—Fig. 3.9.4–5 (1M TSOP2)

3.9.4.3 – 256K BY 16 DRAM WITH EXTENDED FUNCTIONS IN DIP AND SOJ

CAPACITY—256K WORDS OF 16 BITS
LOGIC FEATURES—This part contains multiple logic functions that are similar to those used in MPDRAMS and that are keyed for VIDEO memory applications. All devices meeting this standard must contain all functions which must be implemented as defined in the TRUTH TABLE.
PACKAGE—40 PIN DIP, 0.400" WIDE, 0.100" PIN PITCH
—40 PIN SOJ, 0.400" WIDE, 0.050" PIN PITCH
PIN ASSIGNMENT—Fig. 3.9.4–7A
FUNCTION TRUTH TABLE—Fig. 3.9.4–7B

3.9.4.4 – 4M BY 16 DRAM IN TSOP2

CAPACITY—4M WORDS OF 16 BITS
LOGIC FEATURES—MULTIPLEXED ADDRESS
—These part utilizes 4K or 8K refresh cycles
PACKAGE—54 PIN TSOP2, 0.500" WIDE, 0.8 mm PIN PITCH
PIN ASSIGNMENT—Fig. 3.9.4–8

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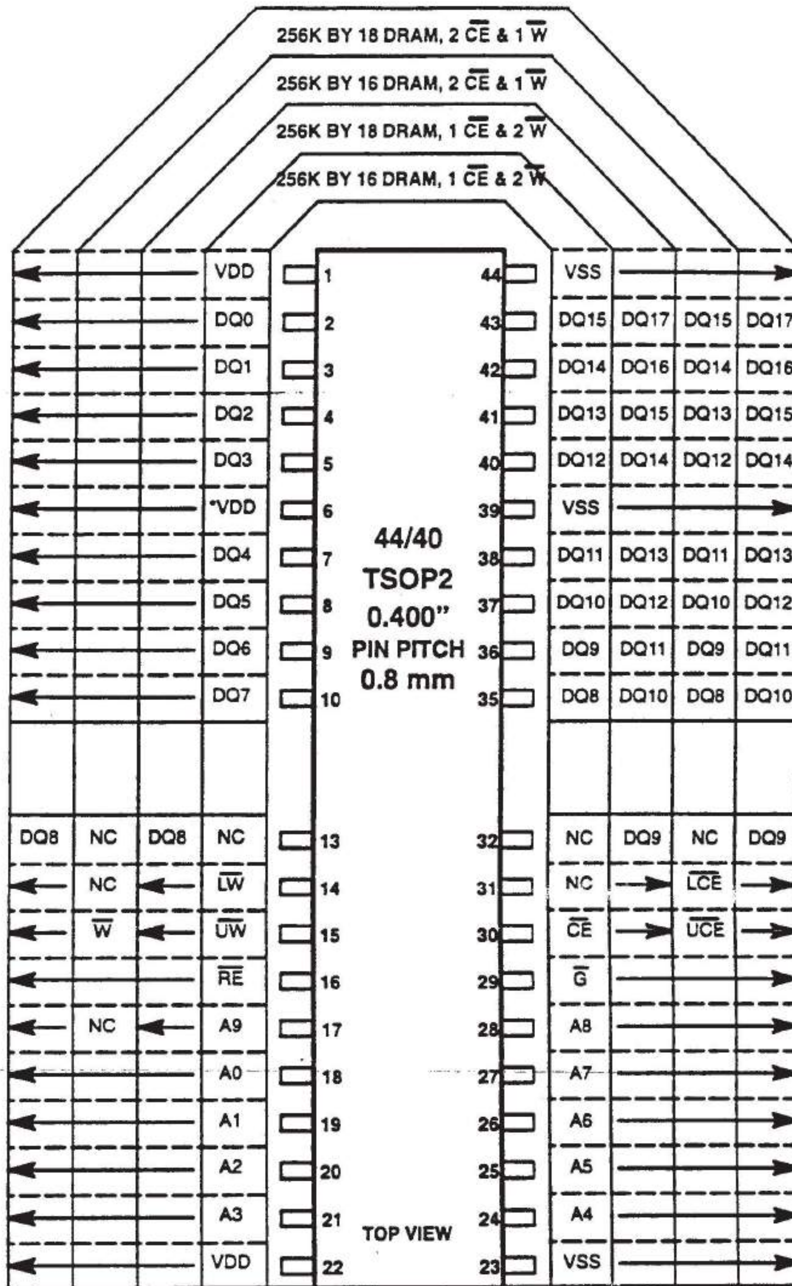


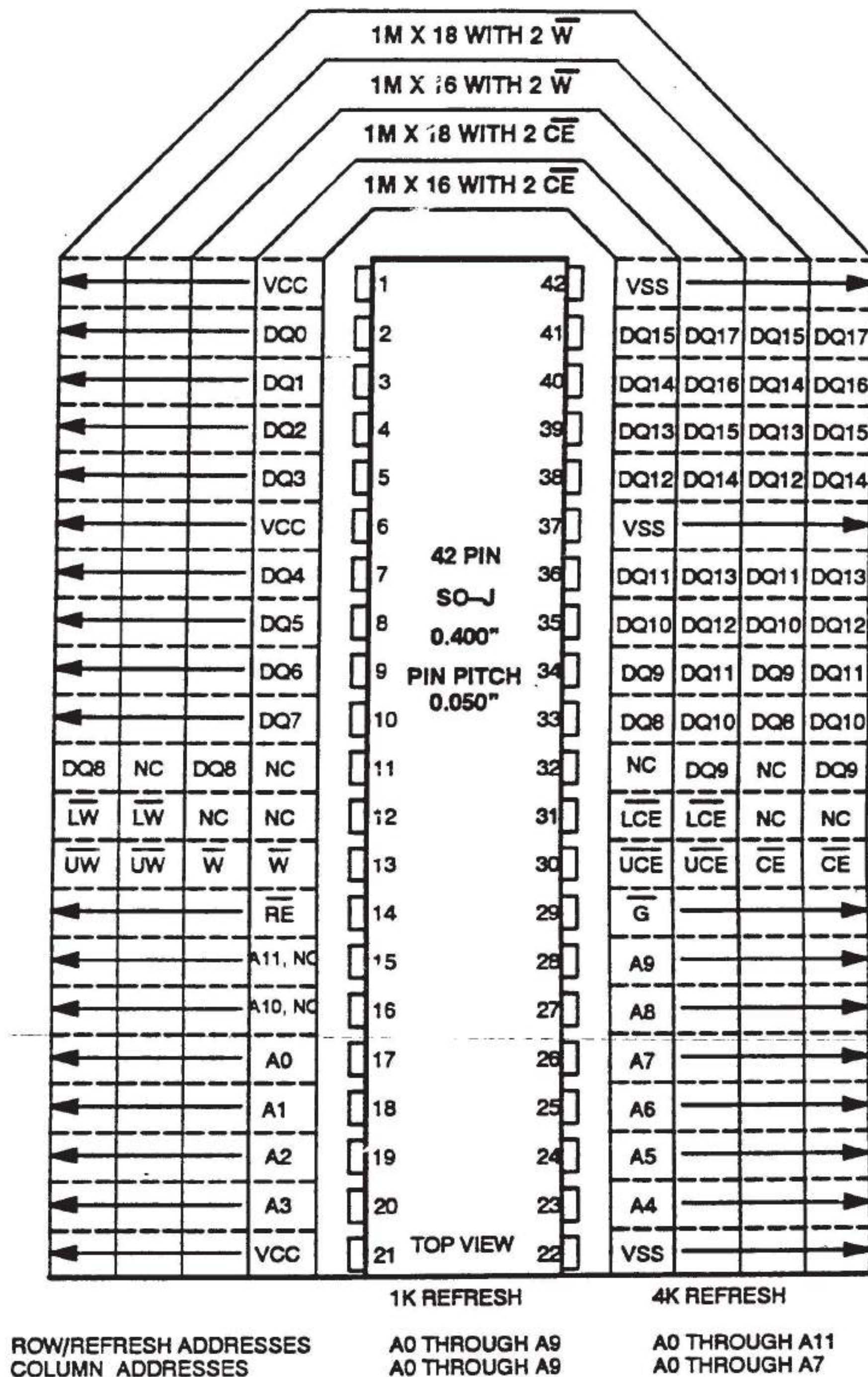
CONFIGURATION	1 $\overline{CE}$, 2 $\overline{W}$	2 $\overline{CE}$, 1 $\overline{W}$
REFRESH COUNT	1024 Cycles	512 Cycles
REFRESH ADDRESS	A0 TO A9	A0 TO A8
ROW ADDRESS	A0 TO A9	A0 TO A8
COLUMN ADDRESS	A0 TO A7	A0 TO A8

The JEDEC Std. No 30 designator for the TSOP2 package is PDSO–G

* NOTE: In the first release of this standard, Pin 6 was a VSS connection. This was in error and this release changes Pin 6 to VDD.

FIGURE 3.9.4–3

256K BY 16 & 18 DRAM WITH 2 $\overline{W}$ OR 2 $\overline{CE}$ IN TSOP2



	1K REFRESH	4K REFRESH
ROW/REFRESH ADDRESSES	A0 THROUGH A9	A0 THROUGH A11
COLUMN ADDRESSES	A0 THROUGH A9	A0 THROUGH A7

FIGURE 3.9.4–4

1M BY 16 & 18 DRAM WITH 2 $\overline{W}$ & 2 $\overline{CE}$ IN SO–J

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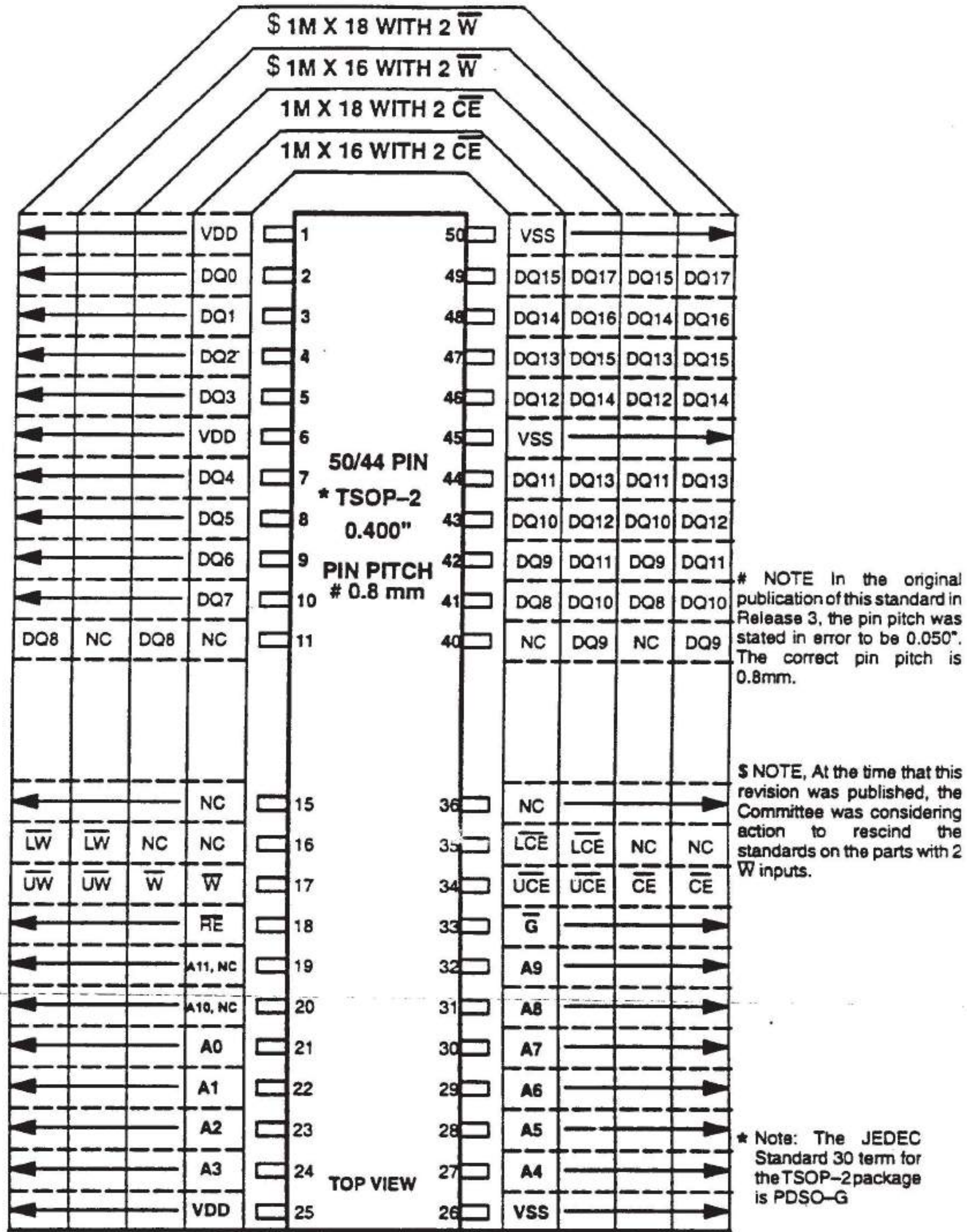

NOTE In the original publication of this standard in Release 3, the pin pitch was stated in error to be 0.050". The correct pin pitch is 0.8mm.

$ NOTE, At the time that this revision was published, the Committee was considering action to rescind the standards on the parts with 2 W inputs.

* Note: The JEDEC Standard 30 term for the TSOP–2 package is PDSO–G

	1K REFRESH	4K REFRESH
ROW/REFRESH ADDRESSES	A0 THROUGH A9	A0 THROUGH A11
COLUMN ADDRESSES	A0 THROUGH A9	A0 THROUGH A7

FIGURE 3.9.4–5

1M BY 16 & 18 DRAM WITH 2 W OR 2 CE IN TSOP2