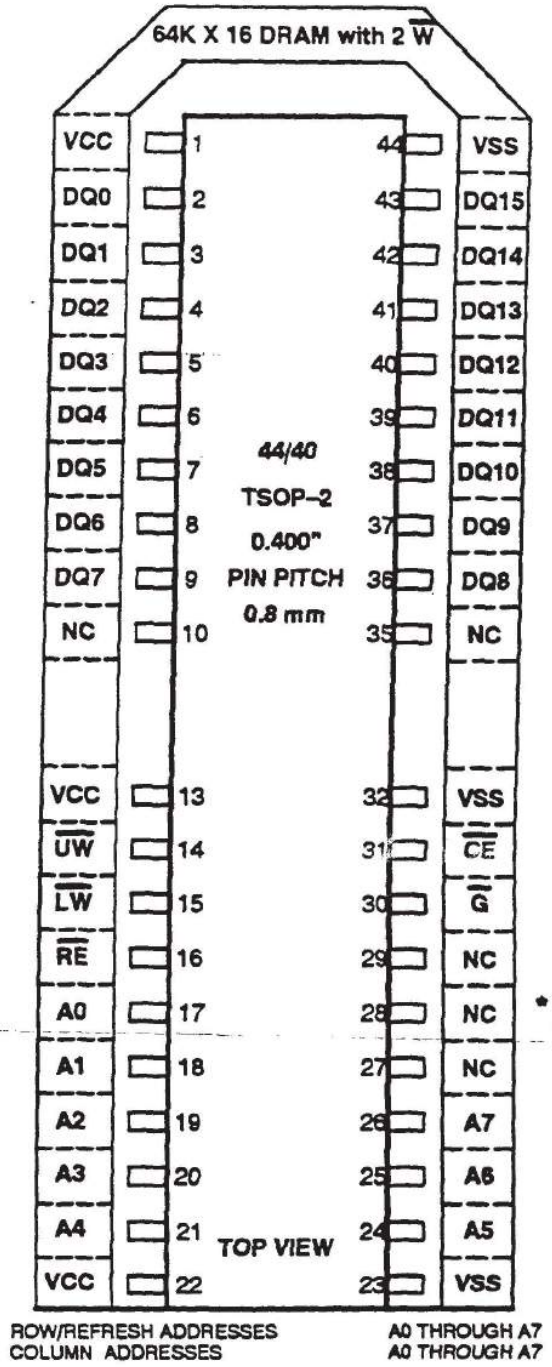
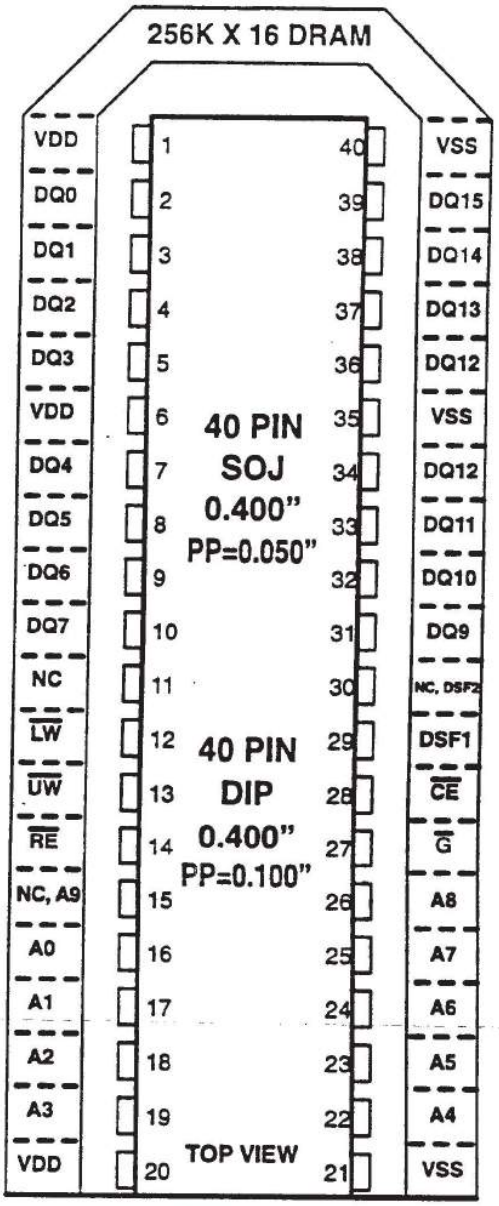


★ Note: The JEDEC Standard 30 term for the TSOP–2 package is PDSO–G

FIGURE 3.9.4–6
64K BY 16 DRAM WITH 2 W IN TSOP–2



	512 REFRESH	1K REFRESH
ROW/REFRESH ADDRESSES	A0 TO A8	A0 TO A9
COLUMN ADDRESSES	A0 TO A8	A0 TO A7

FIGURE 3.9.4–7 A

256K BY 16 DRAM WITH EXTENDED FUNCTIONS IN DIP AND SOJ

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MANDATORY TRUTH TABLE FOR 256K BY 16 DRAM with EXTENDED FUNCTIONS

Mnem.	Function	Valid at RE					Valid at CE
		CE	G	W	DSF(1)	*DSF2	DSF(1)
RW	READ/WRITE	1	1	1	0	0	0
BW	BLOCK WRITE	1	1	1	0	0	1
LMR	LOAD MASK REGISTER	1	1	1	1	0	0
LCR	LOAD COLOR REGISTER	1	1	1	1	0	1
RWM	WRITE, MASKED	1	1	0	0	0	0
BWM	BLOCK WRITE, MASKED	1	1	0	0	0	1
CBR	CBR REFRESH (1)	0	X	1	0	0	X
CBRN	CBR REFRESH (2)	0	X	1	1	0	X
FWT	FLASH WRITE	1	1	0	1	0	X

* IF DSF2 IS PRESENT

*CBR(1) – All optional modes reset

CBR(2) – Any optional modes remain active

FIGURE 3.9.4–7 B

256K BY 16 DRAM MANDATORY EXTENDED FUNCTION TRUTH TABLE

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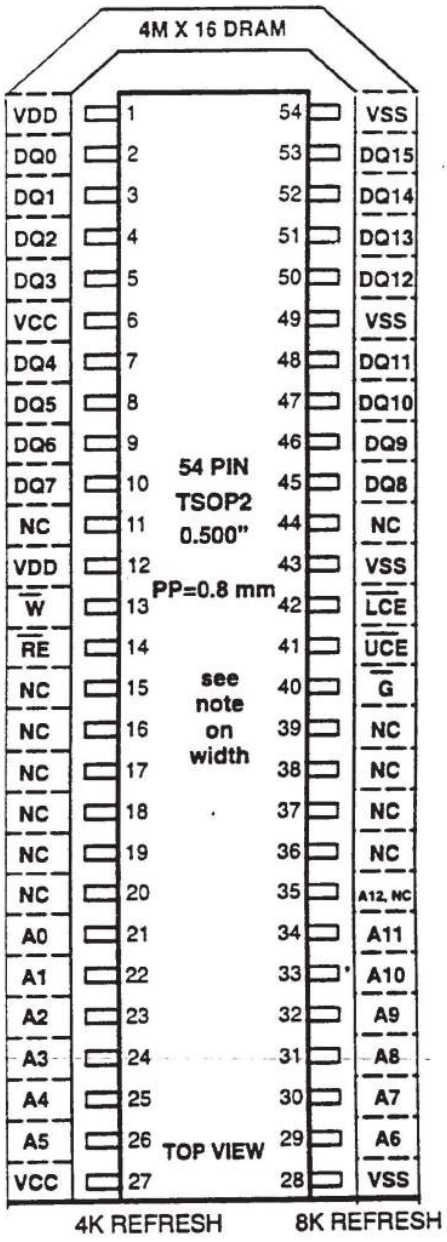


ROW/REFRESH ADDRESSES	A0 → A11	A0 → A12
COLUMN ADDRESSES	A0 → A9	A0 → A8

* NOTE: Pin 25 is A12 for 8K refresh and NC for 4K refresh
* NOTE: The JEDEC Std. 30 term for the TSOP–2 package is PDSO–G.
This standard recognizes that some early deliveries of this part may have to be in a 0.6" wide package

FIGURE 3.9.4–8
4M BY 16 DRAM IN TSOP–2

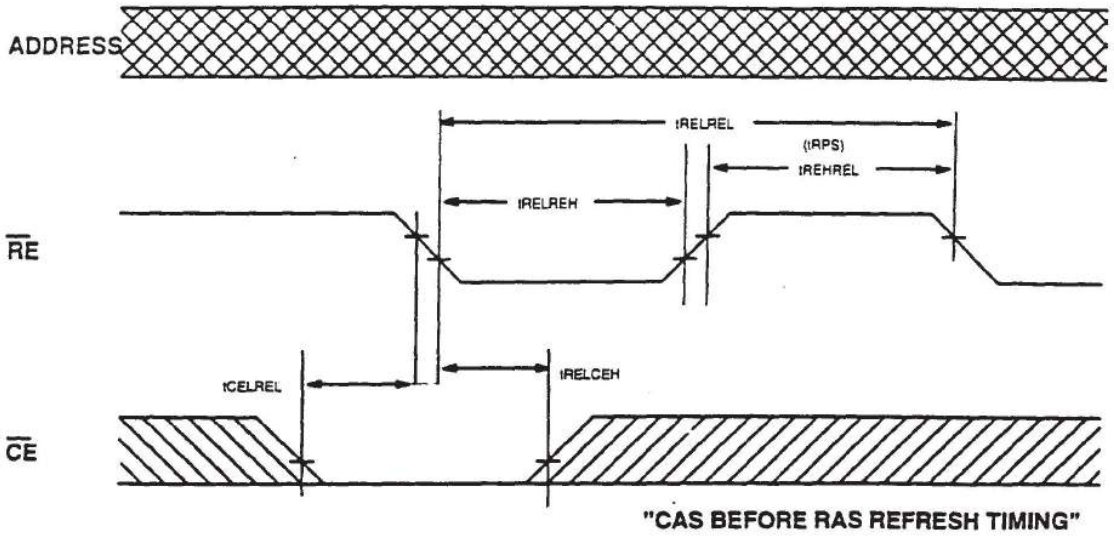
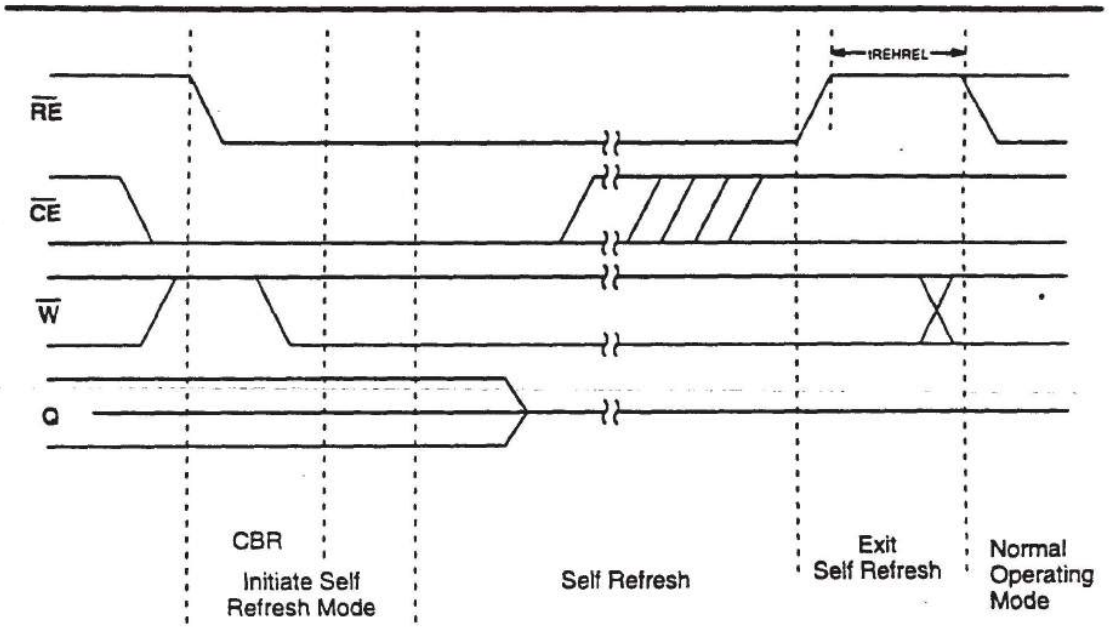


FIGURE 3.9.5–1A
DRAM ON CHIP REFRESH TIMING



Data Out may be either Tristate or Active depending on the state of CE\ when the cycle is entered.

FIGURE 3.9.5–1 B
DRAM SELF REFRESH MODE TIMING

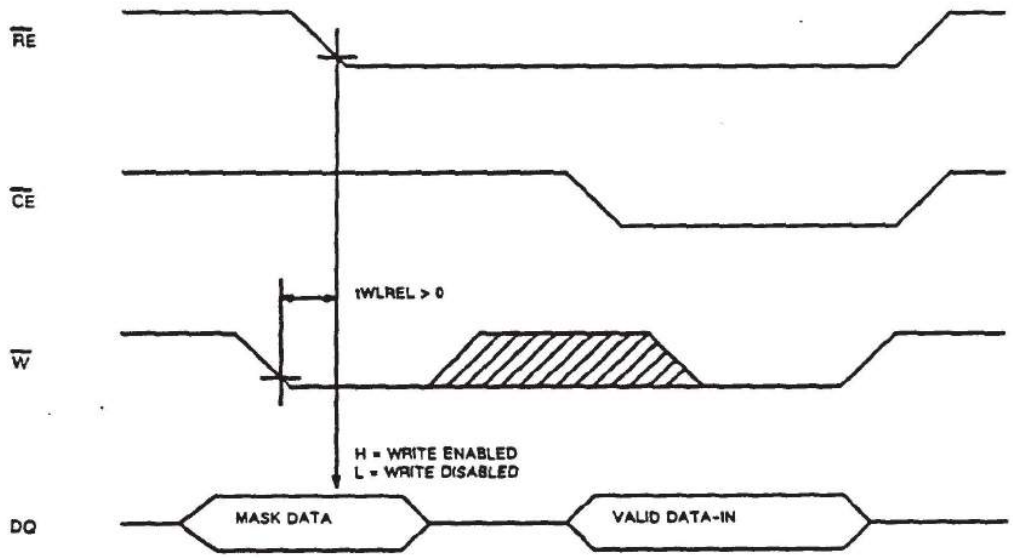


FIGURE 3.9.5-2
DRAM BIT WRITE TIMING

DRAM SPECIAL TEST AND OPERATIONAL MODES

1 PURPOSE

This standard defines a scheme for controlling a series of special modes for address multiplexed DRAM. The standard defines the logic interface required to enter, control, and exit from the special modes. In addition, it defines a basic special test mode plus a series of other special test and operational modes.

2 SPECIAL MODE INITIATE

The special modes will be initiated by the W\ AND CE\ BEFORE RE\ clock sequence shown in Fig.A2–1. This sequence is called "Write Enable and CAS before RAS" or "WCBR". When this clock sequence is generated, the state of the 8 low order Row Address bits (address key) will define the mode to be selected (see Par. 4) if optional modes are implemented. This mode will be latched and remain in effect until a special release cycle is generated or a new initiate cycle defining some other special mode is generated.

Following the initiate cycle, all subsequent cycles except refresh cycles (see pars. 3 & 5), will be operating cycles as allowed by the special mode selected.

3 MODE EXIT

A special mode will be cleared and the memory device returned to its normal operational state by the application of any normal REFRESH cycle, "RAS only refresh", (ROR) or "CAS before RAS refresh" (CBRR).

4 MODE SELECTION

Devices meeting this standard must have an implementation of the BASIC TEST MODE (see par 6) but also may contain other modes as options. When optional special modes are implemented, they will be selected by the state of the 8 least significant ROW Address bits at the time that INITIATE clock sequence is provided. The address space for the mode selection is defined as follows.

The special modes as selected by the 8–bit Address Key will be partitioned into four (4) subsets as follows:

1 – JEDEC Registered Modes

2 – Reserved for future expansion

3 – Vendor Specific Modes

4 – Customer Specific Modes

4.1 MODE PARTITIONING

These modes and their partitioning will be as diagrammed in Table A2–2. Additional address bits above A7 can be used to select additional pages of MODE definition (see par.4.3). Mode subgroups 1 and 2 will be further subdivided into "Test" and "Operational" modes as follows:

TEST MODES are those that implement some special test or measurement function or algorithm designed to enhance the ability of the Vendor or User to determine the integrity of, or to characterize, the part.

OPERATIONAL MODES are those that alter the operational characteristics of the part but do not interfere with its function as a storage device and are intended to be used in system operation.

4.2 MODE CHANGES

The special mode can be changed at any time by the application of a mode initiate clock sequence with the appropriate address key to define the new mode.

4.3 ADDITIONAL MODES

The additional address bits above A7 can be used as needed to define additional pages of MODE definitions.

5 JEDEC REGISTERED SPECIAL MODE REFRESH

–Refresh can be performed while in a special mode by the following means.

(1) – An initiate cycle is generated (W\ and CE\ before RE\) with the address key used to select the mode currently in effect.
(2) – Any normal read or write cycle will perform REFRESH.

–The Initiate Special Mode clock sequence will always perform an on–chip refresh cycle even when the MODE is being changed.

–This refresh applies to JEDEC Special Registered Modes only

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6 BASIC TEST MODE DATA ALGORITHM

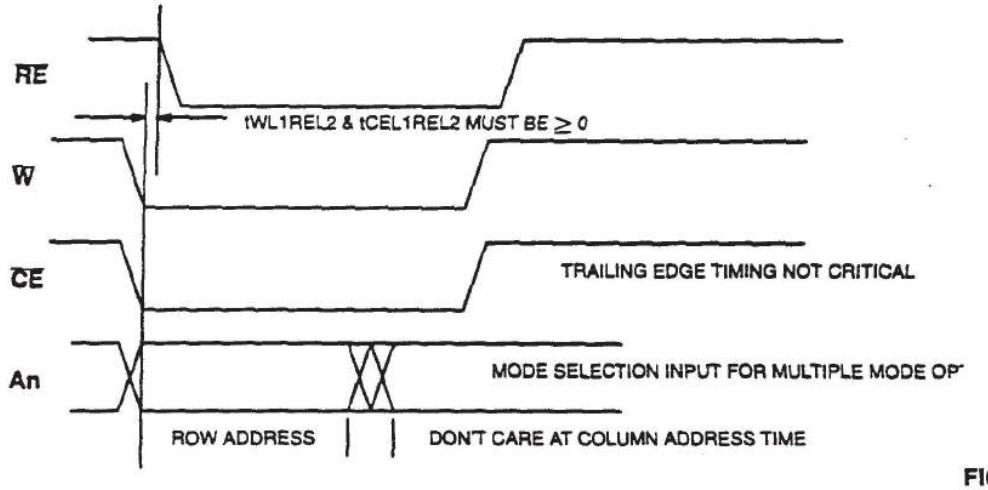
Any memory device that implements the JEDEC Registered modes must implement the "Basic Test Mode" as a minimum. Any other of the special modes which are registered and listed in Table A2-3, may be implemented at the option of the manufacturer. Additional MODES and test algorithms may be registered as needed.

When a memory device is operating in the Basic Test Mode, data that are presented to be written into the memory will be written into multiple locations depending upon the internal device organization and the number of parallel bits in the internal data bus (4, 8, 16, or other) (see par. 7). When a Read Operation is done, the data recovered will include the same set of data bits on the parallel data bus. The internal logic of the memory device will compare the states of all bits of the internal data bus. If all internal bits are equal, the "Q" pin will take the state equal to "1". If any internal data bits are not equal , then "Q" will equal "0". This is called the "1/0/=" test algorithm.

The BASIC TEST MODE is assigned the address keys, "All 1's" and all subsets of this key from 2 low order 1's to all 1's (see Appendix 2). It is acceptable for a device which implements the BASIC TEST MODE and optional test modes to sense a low order subset of the key address field but it is recomended that at least 3 bits be used to minimize the chances of ambiguities in the mode selection.

7 ADDRESS SPACE COMPRESSION CONTROL

Any Standard or Registered test algorithm in which the address space of the device is compressed by test operations on multiple internal data bits will have the address bits which control the internal data bits as defined in Table A2-1. In any test operations, the state of these bits will be "don't care".



FIG

A2-1 SPECIAL OPERATIONAL MODE INITIATE CYCLE

NOTE: The timing parameters of the pulses are not specified in this standard but care must be taken in the device specification to define minimum and maximum pulse durations to insure that noise pulses will be rejected and that intentional control sequencies will be recognized.

Table A2–1–A, 1M TO 16M DRAM ADDRESS COMPRESSION CONTROL BITS

Data Bus Width (# bits)	Control Address Bits	
	X1 DATA INTERFACE	X4 DATA INTERFACE
2		CA0
4	RA(MSB), CA(MSB)	CA0, CA1
8	RA(MSB), CA(MSB), CA0	
16	RA(MSB), CA(MSB), CA0, CA1	(MSB = Most Significant Bit)

Table A2–1–B 64M DRAM ADDRESS COMPRESSION CONTROL BITS

Compression Address = CA(MSB), CA(MSB–1), ...,CA(MSB–n)
where 2n–1 = the number of internal parallel data test bits = Compression factor

PARALLEL TEST BITS	64M X 1	16M X 4	8M X 8	4M X 16
32(n=4)	CA12>CA8			
8(n=2)		CA10>CA8		
4(n=1)			CA10>CA9(4K)	
2(n=0)				CA9(4K)

TABLE A2–1–C 64M DRAM ADDRESS ASSIGNMENT TABLE

Test Bits	DEVICE	RFSH CYCLES	Address Assignments
32	64M X 1	–	
32	64M X 1	8K	0/0 1/1 2/2 3/3 4/4 5/5 6/6 7/7 8/(8) 9/(9) 10/(10) 11/(11) 12/(12)
8	16M X 4	–	
8	16M X 4	8K	0/0 1/1 2/2 3/3 4/4 5/5 6/6 7/7 8/(8) 9/(9) 10/(10) 11 12
4	8M X 8	4K	0/0 1/1 2/2 3/3 4/4 5/5 6/6 7/7 8/8 9/(9) 10/(10) 11 12
4	8M X 8	8K	0/0 1/1 2/2 3/3 4/4 5/5 6/6 7/7 8/(8) 9/(9) 10 11 12
2	4M X 16	4K	0/0 1/1 2/2 3/3 4/4 5/5 6/6 7/7 8/8 9/(9) 10 11 12
2	4M X 16	8K	0/0 1/1 2/2 3/3 4/4 5/5 6/6 7/7 8/(8) 9 10 11 12
1	2M X 32	4K	0/0 1/1 2/2 3/3 4/4 5/5 6/6 7/7 8 9 10 11 12
1	2M X 32	8K	0/0 1/1 2/2 3/3 4/4 5/5 6/6 7 8 9 10 11 12

These addresses can be used as common addresses for 64M X 1, 16M X 4, 8M X 8, & 16M X 32 devices

(n) = compression address
n/n = RAn/CAn

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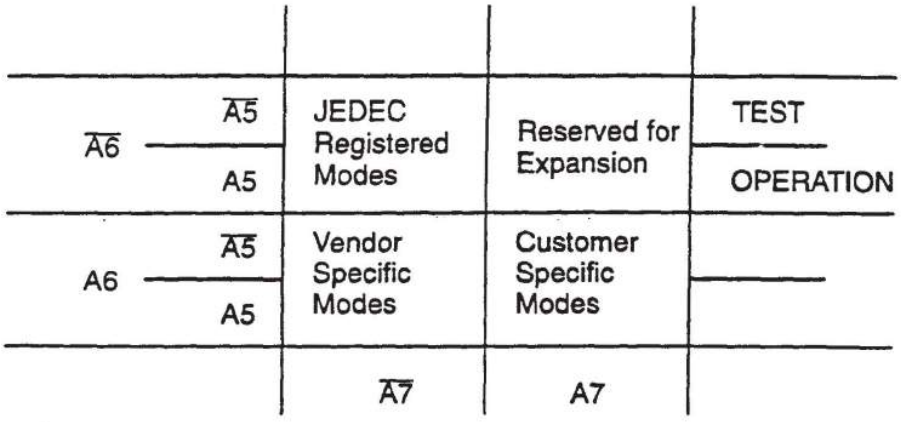
TABLE A2–2 SPECIAL MODE ADDRESS KEY SPACE

The SPECIAL MODE Address Key space will be as shown in the following Karnaugh map with the exception of those codes reserved for the BASIC TEST MODE:



A0 – A4 define individual modes within a block

JEDEC REGISTERED MODES – These are the modes that are defined in detail in registration documents. The function(s) shall be performed as defined with no variations (see Appendix 2 for list of registered modes).

VENDOR SPECIFIC MODES – These are those modes that are implemented by a Vendor for his own in–house use. The details will be revealed only at the discretion of the Vendor. The code assignments will have no standardization from vendor to vendor except at their discretion.

CUSTOMER SPECIFIC MODES – These modes are implemented by a vendor at the request of a specific customer. The information on these modes is not revealed except at their discretion.

TABLE A2–3

REGISTERED MODE ASSIGNMENT PAGE 0 TABLE

ROW ADDRESS BIT	FUNCTION
7, 6, 5, 4, 3, 2, 1, 0	
0, 0, 0, 0, 0, 0, 0, 0	NOT ASSIGNED
0, 0, 0, 0, 0, 0, 1, 1	BASIC TEST MODE, 1/0/=
0, 0, 0, 0, 0, 1, 1, 1	BASIC TEST MODE, 1/0/=
0, 0, 0, 0, 1, 1, 1, 1	BASIC TEST MODE, 1/0/=
0, 0, 0, 1, 1, 1, 1, 1	BASIC TEST MODE, 1/0/=
0, 0, 1, 1, 1, 1, 1, 1	BASIC TEST MODE, 1/0/=
* 0, 1, 1, 1, 1, 1, 1, 1	BASIC TEST MODE, 1/0/=
* 1, 1, 1, 1, 1, 1, 1, 1	BASIC TEST MODE, 1/0/=

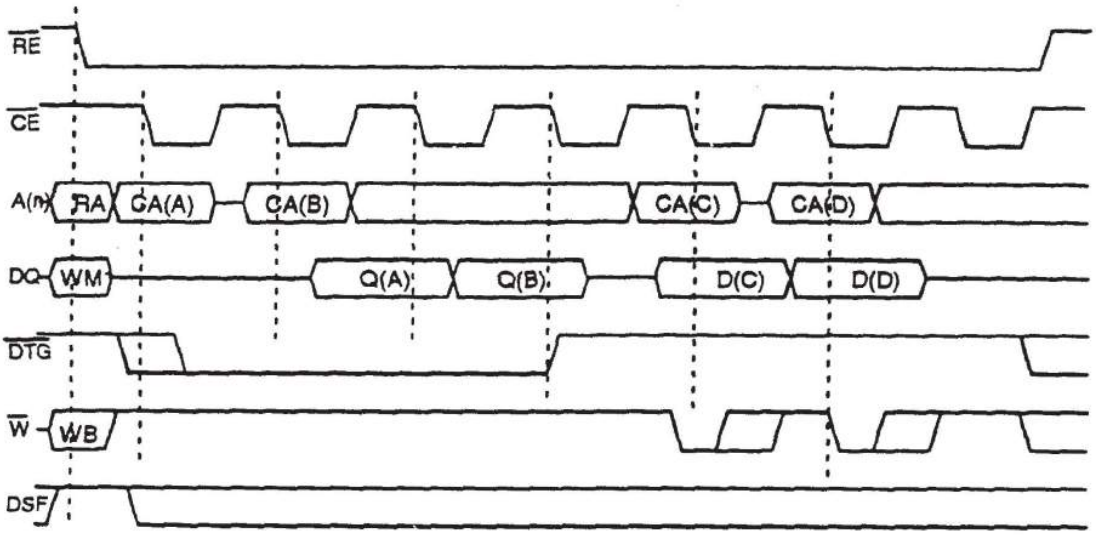
Additional address bits above A7 can be used to select additional pages of MODE definition.

* It should be noted that these pre–assigned address codes do not fall into the address space assigned to JEDEC Registered Modes.

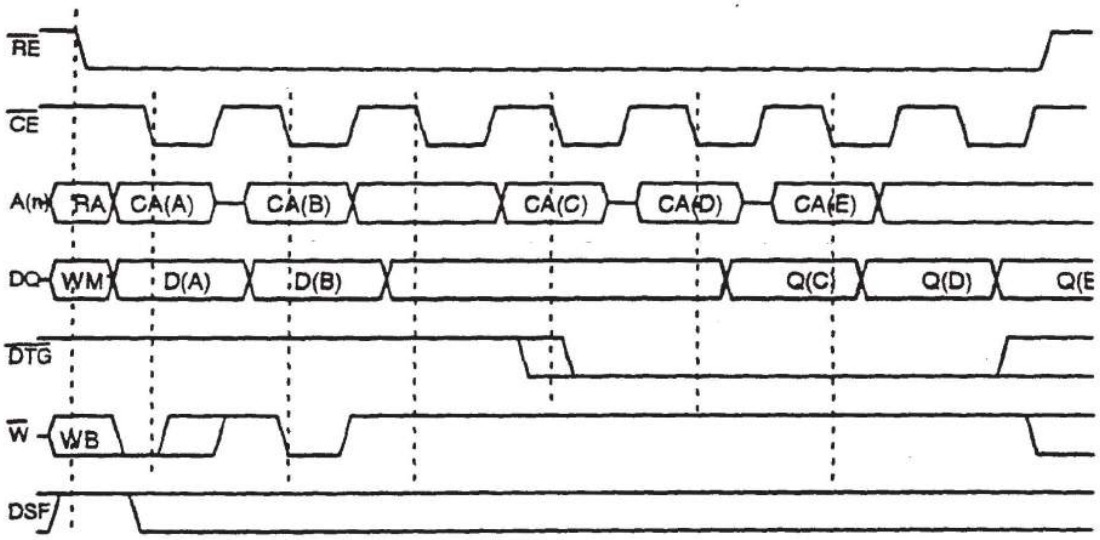
NOTE:: A table of registered optional modes along with definitions will be compiled by the Committee and published periodically.

PIPELINED FAST PAGE MODE

PIPELINED FAST PAGE MODE READ – WRITE



PIPELINED FAST PAGE MODE WRITE – READ



NOTE: BOTH EARLY WRITES AND LATE WRITES ARE REPRESENTED

FIGURE 3.10.4–3B

MPDRAM OPTIONAL MODES and CYCLES

This Standard defines an optional READ mode for address multiplexed Multi–Port DRAMs.

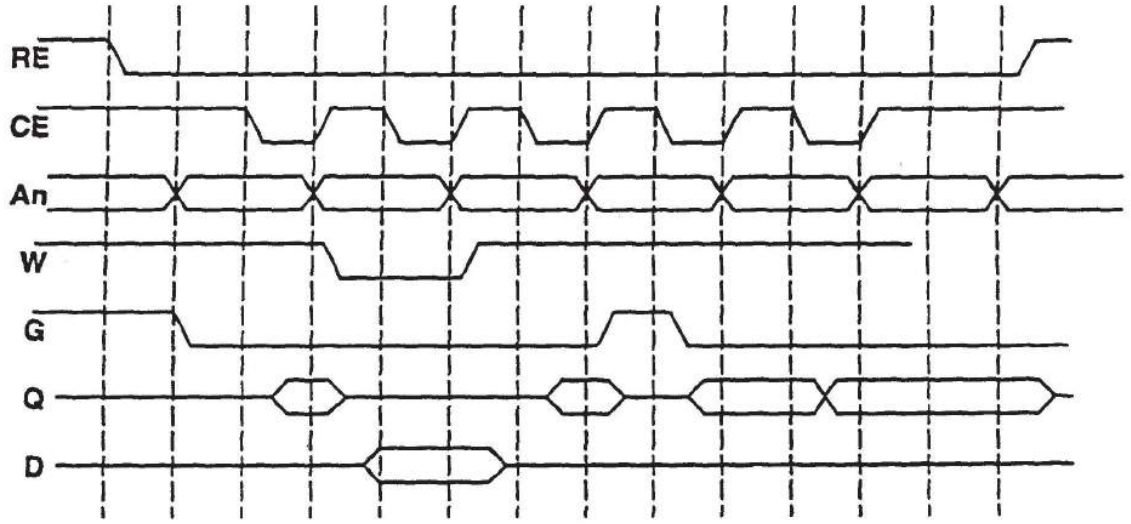
EXTENDED DATA OUT FAST PAGE MODE

This is a variation of the Fast Page Mode defined in Sec. 3.9.5.4, Par. 1.3.. It differs from Fast Page Mode as follows: 1) in a READ operation, the LH transition of CE\ with RE\ active will not cause the data out terminals to go into a high impedence state. Instead, the data out will remain valid with data from the previously read address. During sequential READ operations, the data out terminals will transition from old data to new data at a time defined by the performance specification for the part.
Any of the following conditions will cause the data out terminals to go to the high impedence state:

1) RE\ and CE\ are both inactive.
2) G\ is inactive.
3) W\ in active.

The following timing diagram illustrates this operating mode but is included for reference only.

EXTENDED DATA OUT FAST PAGE MODE



Data Out may be either translate or Active depending on the state of CE\ when the cycle is entered.

FIGURE 3.10.4–4
MPDRAM EXTENDED DATA OUT FAST PAGE MODE

3.11 Synchronous Dynamic Random Access Memory (SDRAM)

The following SDRAM standards were developed by Committee 42.3. The devices described are compatible with TTL and/or one or more of the low voltage interface standards adopted by Committee JC–16 as defined in the individual device standards. The device standards require that the memory devices must operate with signal levels and power supply voltages that are consistent with those used in the logic family(s) specified.

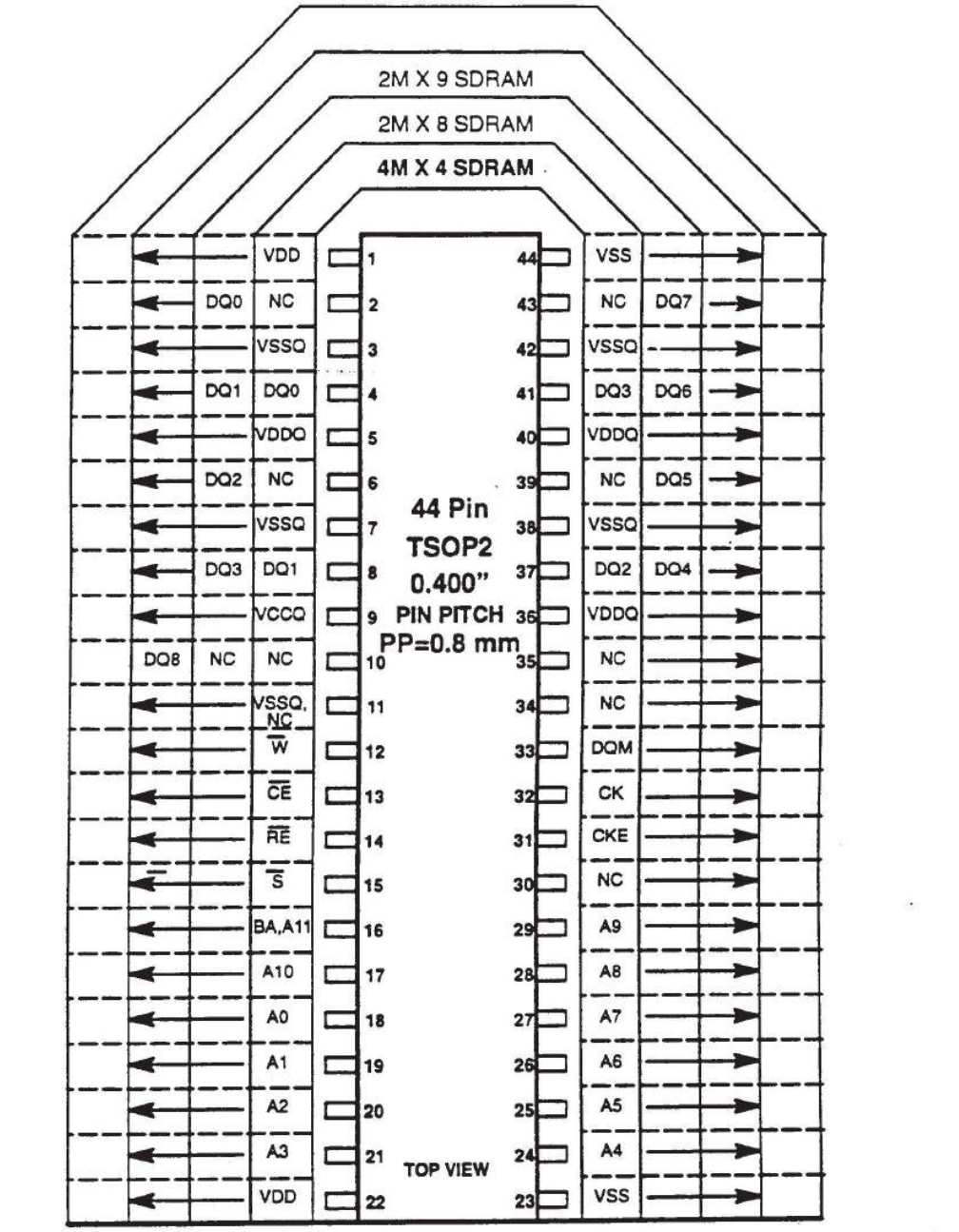
3.11.1 Bit Wide SDRAM

No standards have been developed for devices with this configuration.

3.11.2 NIBBLE WIDE SDRAM

3.11.2.1 – 4M BY 4 SDRAM IN TSOP2

CAPACITY—4M WORDS OF 4 BITS
LOGIC FEATURES—This device will contain all of the logic features described in Sec. 3.11.5
ELECTRICAL INTERFACE—TTL or LVTTL
PACKAGE—44 Pin TSOP2, 0.4" WIDE, 0.8mm PIN PITCH
PIN ASSIGNMENT—Fig. 3.11.2–1



CONFIGURATION	4M X 4	2M X 8/9
ROW ADDRESS	A0 TO A11	A0 TO A11
COLUMN ADDRESS	A0 TO A9 & A11	A0 TO A8 & A11

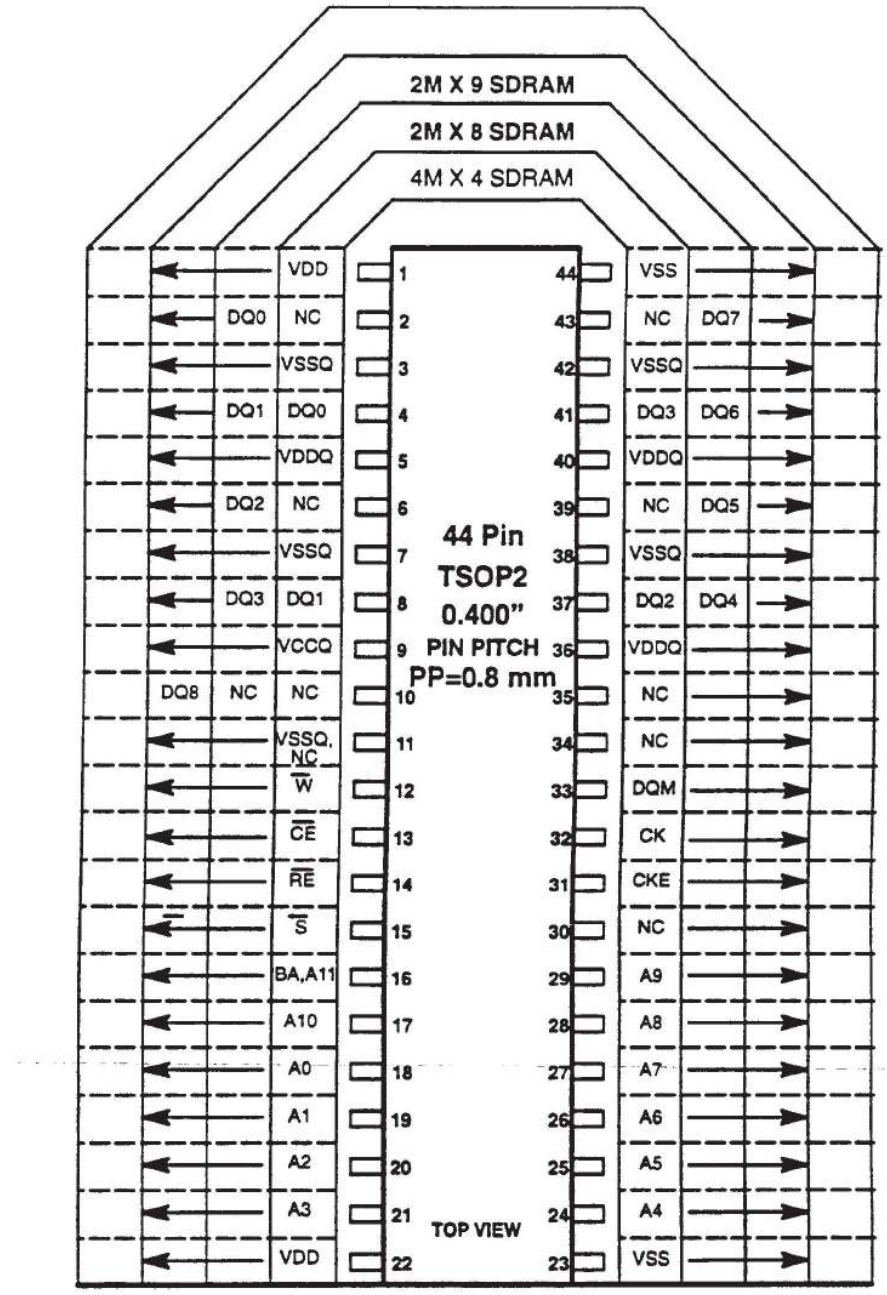
The JEDEC Std. No 30 designator for the TSOP2 package is PDSO–G

FIGURE 3.11.2–1
4M X 4 SDRAM IN TSOP2

3.11.3 BYTE WIDE SDRAM

3.11.3.1 – 2M BY 8 or 9 SDRAM IN TSOP2

CAPACITY—2M WORDS OF 8 or 9 BITS
LOGIC FEATURES—This device will contain all of the logic features described in Sec. 3.11.5
ELECTRICAL INTERFACE—TTL or LVTTL
PACKAGE—44 Pin TSOP2, 0.4" WIDE, 0.8mm PIN PITCH
PIN ASSIGNMENT—Fig. 3.7.3–1



CONFIGURATION	4M X 4	2M X 8/9
ROW ADDRESS	A0 TO A11	A0 TO A11
COLUMN ADDRESS	A0 TO A9 & A11	A0 TO A8 & A11

The JEDEC Std. No 30 designator for the TSOP2 package is PDSO–G

FIGURE 3.11.3–1
2M BY 8 OR 9 SDRAM IN TSOP2

3.11.5 SDRAM Architectural and Operational Features

The following standards describe features or characteristics that are applicable to one or more of the SDRAM devices described in section 3.11 of Std. 21–C.

3.11.5.1 – SDRAM FUNCTION TRUTH TABLE

This table defines the interface states required to execute the standard SDRAM operational functions.

3.11.5.2 – SDRAM FUNCTION TRUTH TABLE FOR CKE

This table defines the interface states required to execute the standard SDRAM operational functions with respect to the CKE input.

3.11.5.3 – SDRAM MODE REGISTER ARCHITECTURE

This standard describes the architecture of the SDRAM internal MODE REGISTER and the codes that are allowable for use in it.

3.11.5.4 through 3.11.5.15 — SDRAM OPERATIONAL CYCLES AND MODES

The following standards define and describe a number of operational cycles and modes of SDRAM. They are ordered roughly in the sequence in which they would be used in normal SDRAM operation.

3.11.5.4 – POWER ON SEQUENCE (RECOMMENDED)

This standard gives a recommended power, clock, and logic–level sequence to be used on power–up to prevent data bus contention.

3.11.5.5 – AUTO PRECHARGE

This standard gives the logic function used to active the AUTO–PRECHARGE function.

3.11.5.6 – PRECHARGE ALL BANKS

This standard gives the logic function used to activate the PRECHARGE–ALL–BANKS function.

3.11.5.7 – MODE REGISTER WRITE TIMING

This standard defines the logic sequence and timing required to write into the MODE REGISTER.

3.11.5.8 – AUTO REFRESH

This standard defines the logic state and interface sequence required to perform an AUTO REFRESH

3.11.5.9 – WRITE LATENCY

This standard defines WRITE LATENCY and illustrates it with a timing diagram.

3.11.5.10 – DQM LATENCY FOR READS AND WRITES

In this standard DQM LATENCY is defined and the relationships between the DQM signal and the interface data for READs and WRITEs is defined and shown in timing diagrams.

3.11.5.11 – PRECHARGE TIMING FOR READS

This standard describes the relationship between the assertion of a PRECHARGE command and data out from a READ command.

3.11.5.12 – COLUMN ADDRESS TO COLUMN ADDRESS DELAY

This standard defines constraints imposed on the CA to CA delay and illustrates them with a timing diagram.

3.11.5.13 – CKE TIMING FOR POWER DOWN

This standard describes the interface sequence required to place the SDRAM into the POWER–DOWN state using CKE.

3.11.5.14 – SELF REFRESH ENTRY AND EXIT

This standard defines the logic states and timing sequence used to enter and exit the SELF–REFRESH mode.

3.11.5.15 – CKE TIMING FOR CLOCK SUSPEND

This standard describes the interface timing sequence when CKE is used to suspend the clock.

SDRAM FUNCTION TRUTH TABLE

CURRENT STATE	$\overline{S}$	$\overline{RE}$	$\overline{CE}$	$\overline{W}$	An	ACTION
IDLE	H	X	X	X	X	NOP
	L	H	H	H	X	NOP
	L	H	H	L	BA	ILLEGAL[2]
	L	H	L	X	BA, CA	ILLEGAL[2]
	L	L	H	H	BA, RA	Row (& Bank) active; Latch Row Address
	L	L	H	L	BA, A10	NOP[4]
	L	L	L	H	X	Auto–Refresh[5]
	L	L	L	L	Op–code	Mode Register Access[5]
ROW ACTIVE	H	X	X	X	X	NOP
	L	H	H	X	X	NOP
	L	H	L	H	BA, CA, A10	Begin Read; Latch CA; Determine AP
	L	H	L	L	BA, CA, A10	Begin Write; Latch CA; Determine AP
	L	L	H	H	BA, RA	ILLEGAL[2]
	L	L	H	L	BA, A10	Precharge
	L	L	L	X	X	ILLEGAL
READ	H	X	X	X	X	NOP (Continue Burst to End;⇒Row Active)
	L	H	H	H	X	NOP(Continue Burst to End;⇒Row Active)
	L	H	H	L	BA	RESERVED (Term. Burst);⇒Row Active
	L	H	L	H	BA, CA, A10	Term Burst, New Read, Determine AP[3]
	L	H	L	L	BA, CA, A10	Term Burst, Start Write, Determine AP[3]
	L	L	H	H	BA, RA	ILLEGAL[2]
	L	L	H	L	BA, A10	Term Burst, Precharge Timing for Reads
	L	L	L	X	X	ILLEGAL
WRITE	H	X	X	X	X	NOP(Continue Burst to End;⇒Row Active)
	L	H	H	H	X	NOP(Continue Burst to End;⇒Row Active)
	L	H	H	L	BA	RESERVED (Term Burst);⇒Row Active
	L	H	L	H	BA, CA, A10	Term Burst, Start Read, Determine AP[3]
	L	H	L	L	BA, CA, A10	Term Burst, New Write, Determine AP[3]
	L	L	H	H	BA, RA	ILLEGAL[2]
	L	L	H	L	BA, A10	Term Burst, Precharge[3]
	L	L	L	X	X	ILLEGAL
READ with AUTO Precharge	H	X	X	X	X	NOP (Continue Burst to End;⇒Precharge)
	L	H	H	H	X	NOP (Continue Burst to End;⇒Precharge)
	L	H	H	L	BA	ILLEGAL[2]
	L	H	L	H	BA, CA, A10	ILLEGAL[2]
	L	L	L	L	X	ILLEGAL
	L	L	H	X	BA, RA, A10	ILLEGAL[2]
	L	L	L	X	X	ILLEGAL
WRITE with AUTO Precharge	H	X	X	X	X	NOP (Continue Burst to End;⇒Precharge)
	L	H	H	H	X	NOP (Continue Burst to End;⇒Precharge)
	L	H	H	L	BA	ILLEGAL[2]
	L	H	L	H	BA, CA, A10	ILLEGAL[2]
	L	H	L	L	X	ILLEGAL
	L	L	H	X	BA, RA, A10	ILLEGAL[2]
	L	L	L	X	X	ILLEGAL

TABLE 3.11.5–1
SDRAM FUNCTION TRUTH TABLE

SDRAM FUNCTION TRUTH TABLE (continued)

CURRENT STATE	$\overline{S}$	$\overline{RE}$	$\overline{CE}$	$\overline{W}$	An	ACTION
Precharging	H	X	X	X	X	NOP⇒idle after tRP
	L	H	H	H	X	NOP⇒idle after tRP
	L	H	H	L	BA	ILLEGAL[2]
	L	H	L	X	BA, CA	ILLEGAL[2]
	L	L	H	H	BA, RA	ILLEGAL[2]
	L	L	H	L	BA, A10	NOP[4]
	L	L	L	X	X	ILLEGAL
ROW Activating	H	X	X	X	X	NOP⇒Row Active after tRCD
	L	H	H	H	X	NOP⇒Row Active after tRCD
	L	H	H	H	L	ILLEGAL[2]
	L	H	L	X	BA, CA	ILLEGAL[2]
	L	L	H	H	BA, RA	ILLEGAL[2]
	L	L	H	L	BA, A10	ILLEGAL[2]
	L	L	L	X	X	ILLEGAL
WRITE Recovering	H	X	X	X	X	NOP
	L	H	H	H	X	NOP
	L	H	H	L	BA	ILLEGAL[2]
	L	H	L	X	BA, CA	ILLEGAL[2]
	L	L	H	H	BA, RA	ILLEGAL[2]
	L	L	H	L	BA, A10	ILLEGAL[2]
	L	L	L	X	X	ILLEGAL
Refreshing	H	X	X	X	X	NOP⇒idle after tRP
	L	H	H	X	X	NOP⇒idle after tRP
	L	H	L	X	X	ILLEGAL
	L	L	H	X	X	ILLEGAL
	L	L	L	X	X	ILLEGAL
Mode Register Accessing	H	X	X	X	X	NOP
	L	H	H	H	X	NOP
	L	H	H	L	X	ILLEGAL
	L	H	L	X	X	ILLEGAL
	L	L	X	X	X	ILLEGAL

ABBREVIATIONS

RA = Row Address BA = Bank Address Term = Terminate

CA = Column Address AP = Auto Precharge NOP = No Operation

NOTES:

1. All entries assume that CKE was active (HIGH) during the preceeding clock cycle and the current clock cycle.
2. Illegal to bank in specified state; function may be legal in the bank indicated by BA, depending on the state of that bank.
3. Must satisfy the "2n–rule", bus contention, but turn around, and/or write recovery requirements.
4. NOP to bank precharging or in idle state. May precharge bank(s) indicated by BA (and A10).
5. Illegal if any bank is not idle.

ILLEGAL = Device operation and/or data–integrity are not guaranteed

TABLE 3.11.5–1
SDRAM FUNCTION TRUTH TABLE (Continued)

SDRAM FUNCTION TRUTH TABLE for CKE

CURRENT STATE	CKE_{n-1}	CKE_n	$\overline{S}$	$\overline{RE}$	$\overline{CE}$	$\overline{W}$	An	ACTION
Self–refresh[6]	H	X	X	X	X	X	X	INVALID
	L	H	H	X	X	X	X	EXIT Self–Refresh⇒ ABI
	L	H	L	H	H	H	X	EXIT Self–Refresh⇒ ABI
	L	H	L	H	H	L	X	ILLEGAL
	L	H	L	H	L	X	X	ILLEGAL
	L	H	L	L	X	X	X	ILLEGAL
	L	L	X	X	X	X	X	NOP (Maintain Self–Refresh)
Power–Down	H	H	H	X	X	X	X	INVALID
	L	L	L	H	H	H	X	EXIT Power Down⇒ABI
	L	L	L	H	H	H	X	EXIT Power Down⇒ABI
	L	L	L	H	L	X	X	ILLEGAL
	L	L	L	L	H	H	X	ILLEGAL
	L	L	L	L	H	L	X	ILLEGAL
	L	L	L	L	L	X	X	NOP(Maintain Low–Power Mode)
All Banks Idle[7]	H	H	X	X	X	X	X	Refer to Table 1
	H	L	H	X	X	X	X	Enter Power–Down
	H	L	L	H	H	H	X	Enter Power–Down
	H	L	L	H	H	L	X	ILLEGAL
	H	L	L	H	L	X	X	ILLEGAL
	H	L	L	L	H	X	X	ILLEGAL
	H	L	L	L	L	H	X	Enter Self–Refresh
	H	L	L	L	L	L	X	ILLEGAL
	L	L	X	X	X	X	X	NOP
Any State other than listed above	H	H	X	X	X	X	X	Refer to operations Table 1
	H	L	X	X	X	X	X	Begin Clock Suspend next cycle[8]
	L	H	X	X	X	X	X	Exit Clock Suspend next cycle[8]
	L	L	X	X	X	X	X	Maintain Clock Suspend.

ABBREVIATIONS
ABI = All Banks Idle
NOTES:

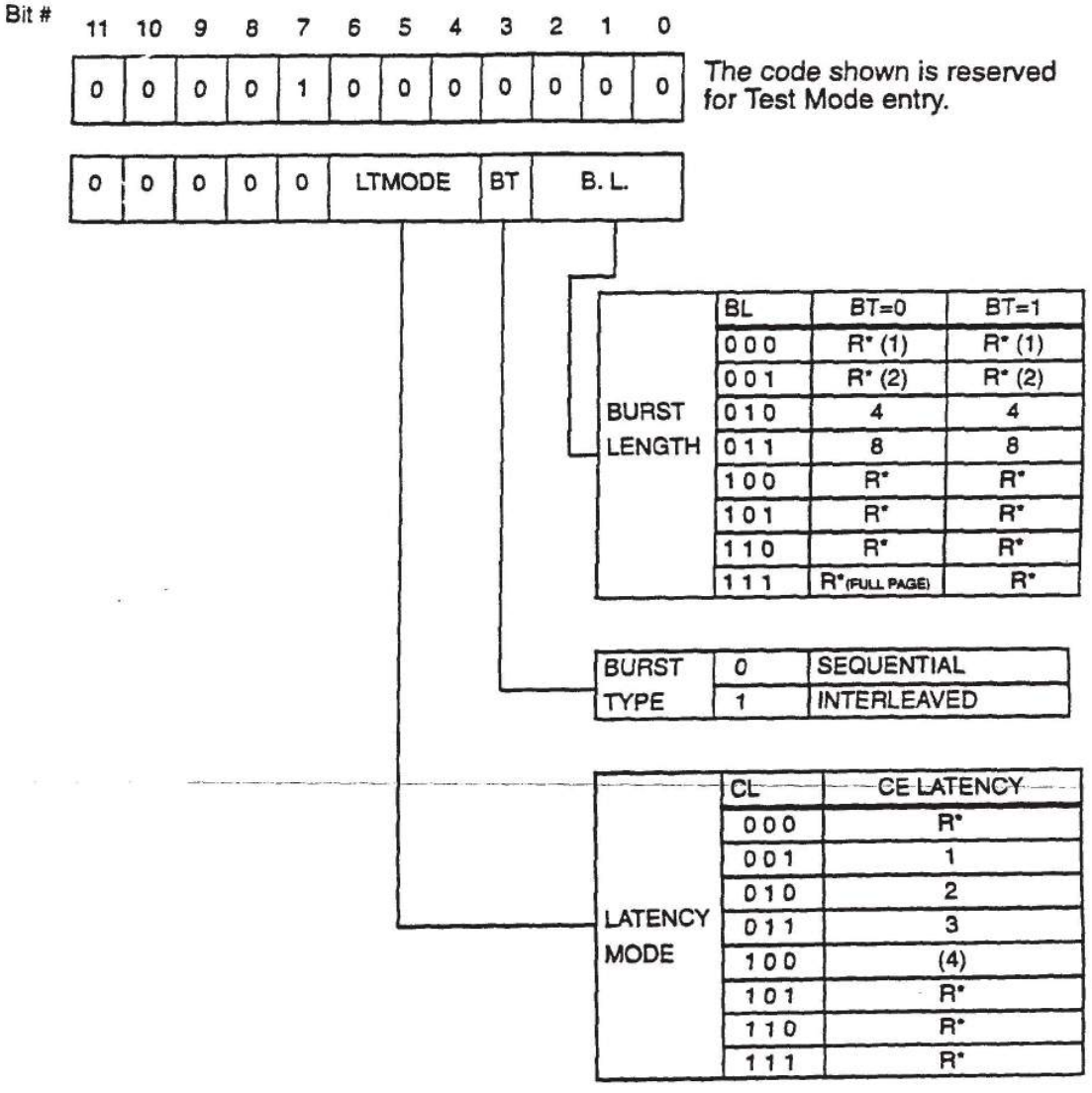
6. CKE Low–to–High transition will re–enable CK and other inputs asynchronously. A minimum setup time must be satisfied before any command other than EXIT.
7. Power–Down and Self–Refresh can be entered only from the All Banks Idle State.
8. Must be legal command.

TABLE 3.11.5–2
SDRAM FUNCTION TRUTH TABLE for CKE

SDRAM Mode Register

This Mode Register is located on the Synchronous DRAM (SDRAM) chip. Its purpose is to store the mode–of–operation data. This data is written after power–on and before normal operation. The data contains the Burst Length, the Burst Type, the $\overline{CE}$ Latency, and whether it is to be operating in Test Mode, or Normal operating mode. During operation, this register (and therefore operation of the chip) may be changed, according to the requirements of the Mode–Register–Write Timing diagram. So, while operating in one mode, for example Burst of 4 in sequential addresses; it can change to Burst of 8 in Interleaved address mode.

16M/18M SDRAM Mode Register architecture:



NOTE: All items in parentheses are optional

FIGURE 3.11.5–1
SDRAM MODE REGISTER ARCHITECTURE

Release 4

Jedec 0007793

3.11.5.4–Power On Sequence (Recommended)

The synchronous nature of the inputs and outputs of the SDRAM device create the possibility that a SDRAM device could power up in a state with data being driven out of the part, and in a multipart system, such a condition may cause data contention and possibly device damage in the long term. In an attempt to reduce the possibility of data contention, both system and device designers should strive toward ensuring a High–Z output state during the initial power up sequence. The following recommended power on sequence is offered for both system and device designers as a means to help the device power up with the outputs in a High–Z state.

The default power on value for the mode register is supplier specific and may be undefined.

The default power on value for the device is supplier specific and may be undefined.

The recommended power on sequence is as follows:

1. Apply power and start clock. Attempt to maintain a NOP condition at the inputs
2. Maintain stable power, stable clock, and NOP input conditions for a minimum of 200 µS.
3. Issue precharge commands for all banks of the device.
4. Issue 8 or more autorefresh commands.
5. Issue a mode register set command to initialize the mode register.

The device is now in the IDLE state and is ready for normal operation.

3.11.5.5–Auto Precharge

The user may specify that the bank currently being accessed precharge itself as soon as the burst is completed. This is done using address bit A10 during the column address cycle. The following table defines the options available from A10 during the column address portion of any cycle.

A10	Option
0	Do not auto precharge, leave bank active at end of burst.
1	Auto precharge bank specified by A11 at end of burst.

The user must wait until the precharge is completed before issuing another command to the device. Timing for auto precharge is required to be the same as or less than the minimum requirement of external precharge.

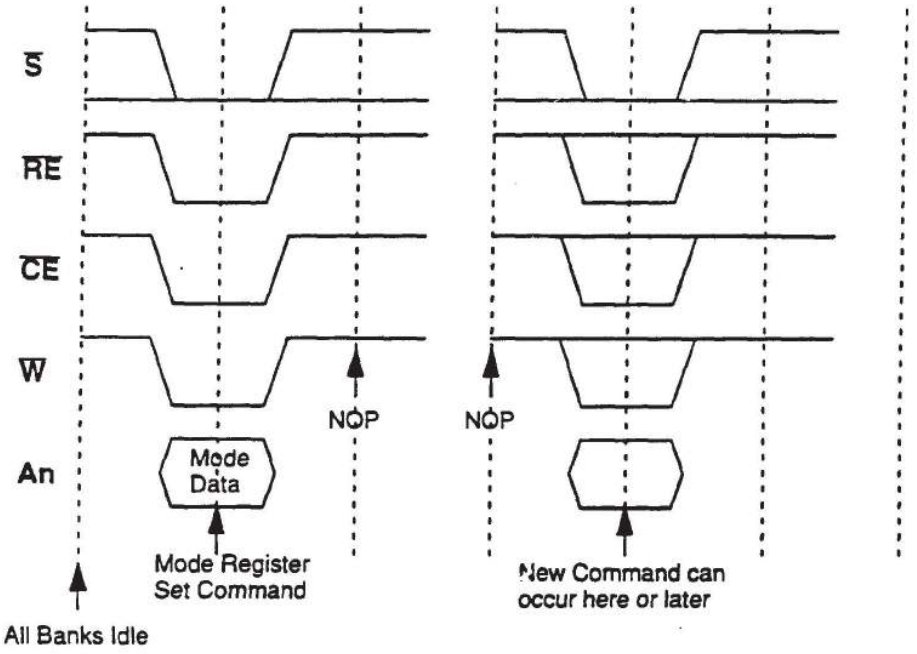
3.11.5.6–Precharge All Banks

The user may specify, during a precharge command, whether to precharge only the specified bank or to precharge all banks. A11 is used to specify the bank to be precharge, and A10 is used to indicate the precharge option. The following table defines the options available from A10 during the precharge cycle.

A10	Option
0	Precharge bank specified by A11
1	Precharge All banks

3.11.5.7–Mode Register Write Timing

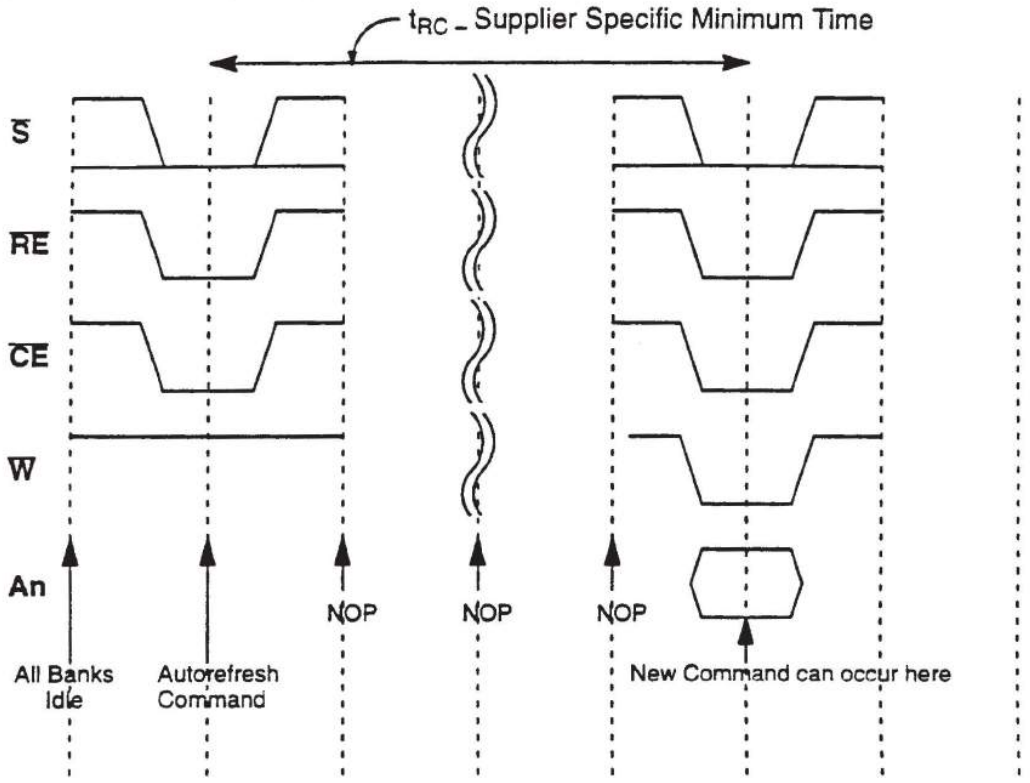
The Mode Register Set Cycle is initiated by holding the $\overline{S}$, $\overline{RE}$, $\overline{CE}$, and $\overline{W}$ signals low at the clock rising edge. The address lines at the same clock edge contain the mode register set opcode and the valid mode information to be written into the mode register. A mode register set cycle can be followed by a new command in no less than 3 clock cycles as illustrated in the diagram below.



Note: Clock Low–to–high transitions occur at the dotted lines.

3.11.5.8–Auto Refresh

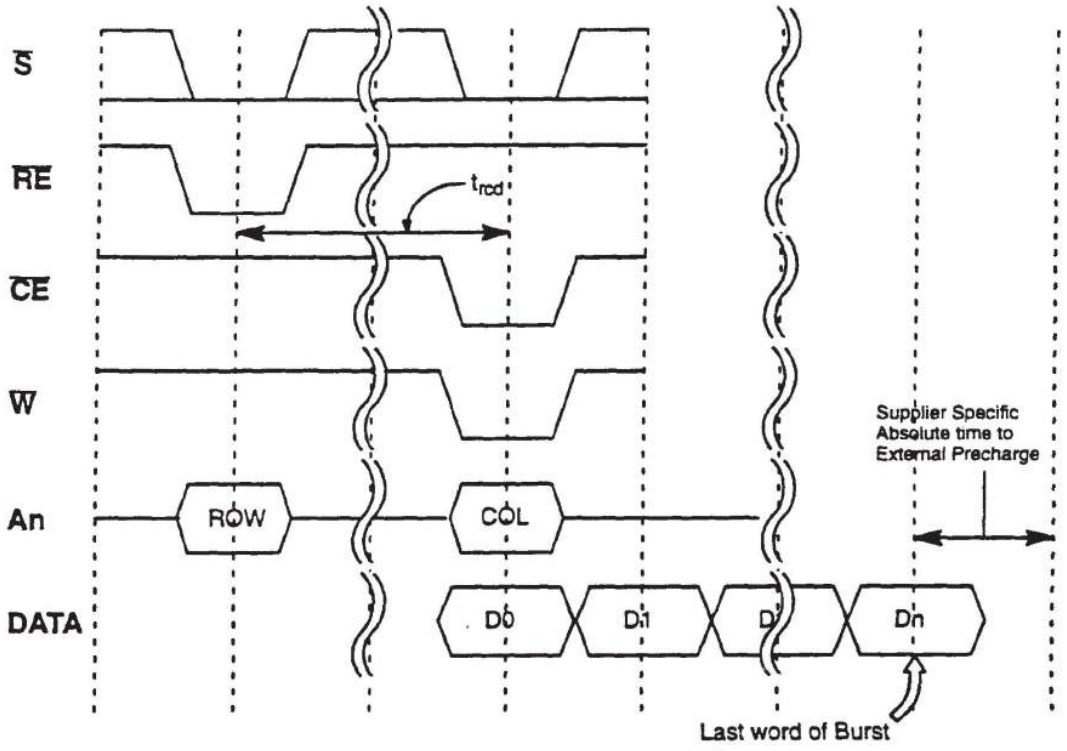
AutoRefresh is an operation that initiates a single refresh cycle for an SDRAM, but that once initiated, is completed by internal control in the device with the refresh address being supplied by an internal register in the device. Before performing an Autorefresh, all banks of the device must be precharged (IDLE). Autorefresh is entered by asserting RE and CE on the same clock cycle. All banks will automatically precharge at the end of the refresh cycle. Additional commands must not be supplied to the device during the minimum refresh time specified. The following timing diagram illustrates the refresh cycle requirements.



Note: Clock Low–to–high transitions occur at the dotted lines.

3.11.5.9–Write Latency
(Write Latency = 0)

Write Latency for Synchronous DRAM shall be as defined as the clock cycle difference between the clock where write command and collumn address are asserted and the clock where first data to be written is asserted.

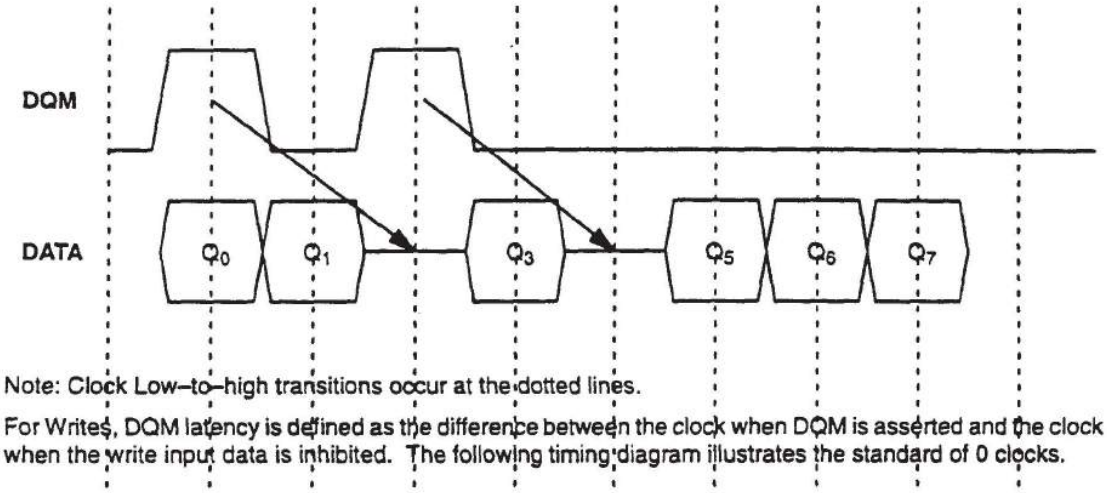


Note: Clock Low–to–high transitions occur at the dotted lines.

3.11.5.10–DQM Latency for Reads and Writes (DQM Write Latency = 0)

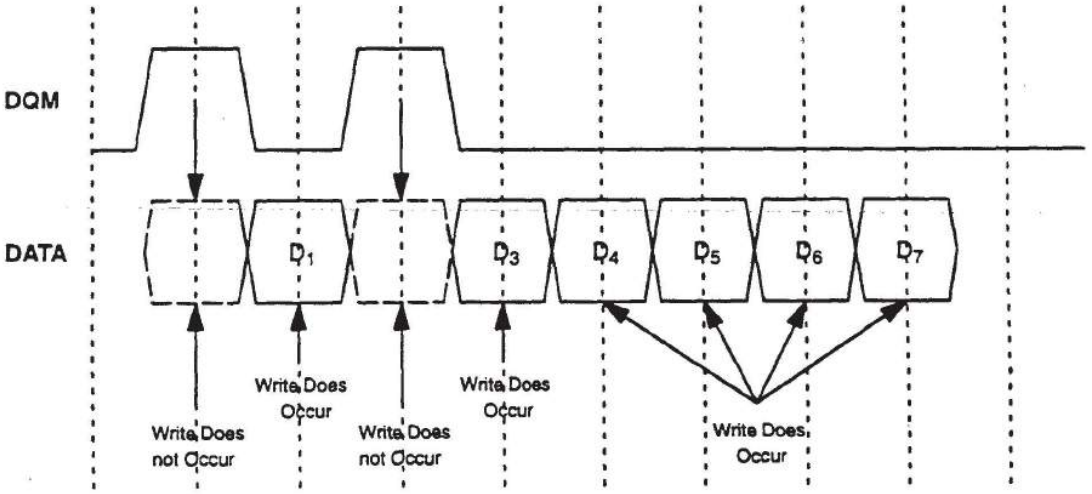
DQM is a multiple–function signal defined as the data mask for both reads and writes. During reads, DQM performs synchronous output enable. During writes, DQM performs write data masking. The requirement for high–speed operation, and the synchronous nature of SDRAM devices requires that DQM latency be different for reads than it is for writes.

For Reads, DQM latency is defined as the difference between the clock when DQM is asserted and the clock when the output bus has been forced to High–Z. The following timing diagram illustrates the standard of 2 clocks.



Note: Clock Low–to–high transitions occur at the dotted lines.

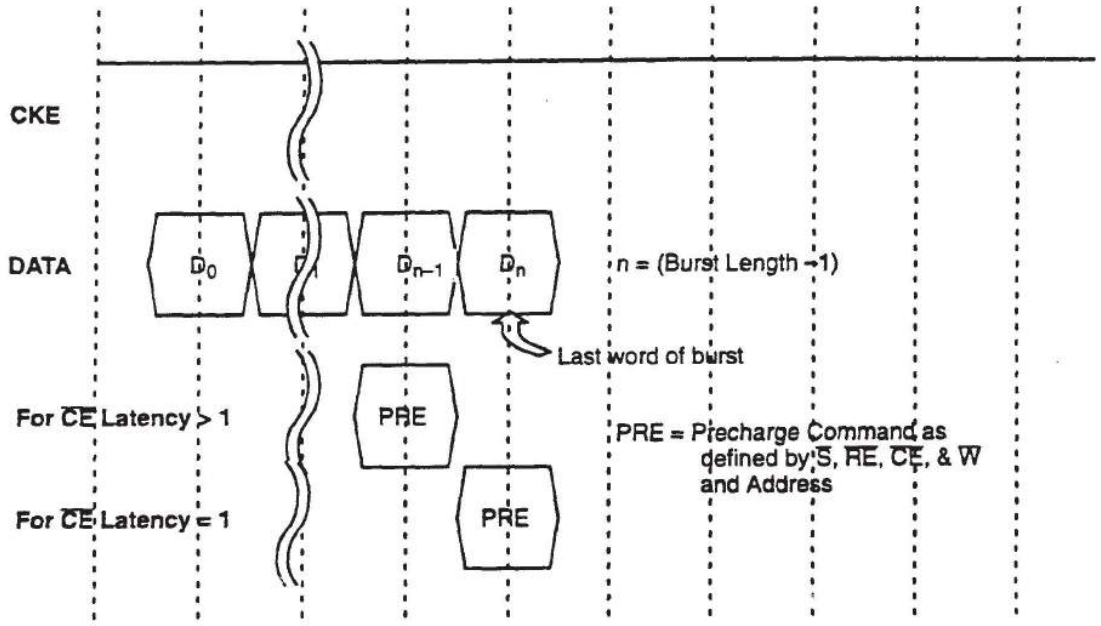
For Writes, DQM latency is defined as the difference between the clock when DQM is asserted and the clock when the write input data is inhibited. The following timing diagram illustrates the standard of 0 clocks.



Note: Clock Low–to–high transitions occur at the dotted lines.

3.11.5.11–Precharge Timing for Reads

The assertion of the precharge command has a direct relationship to the timing of data out for a read cycle. For a CE latency of 1, the minimum requirements is that the precharge command will be allowed to coincide with output of the last data from a burst regardless of burst length. For a CE latency greater than 1, the minimum requirement is that the precharge command will be allowed to coincide with output of the next–to–last data from a burst, regardless of burst length, without interrupting burst data. The following timing diagrams illustrate the requirements.



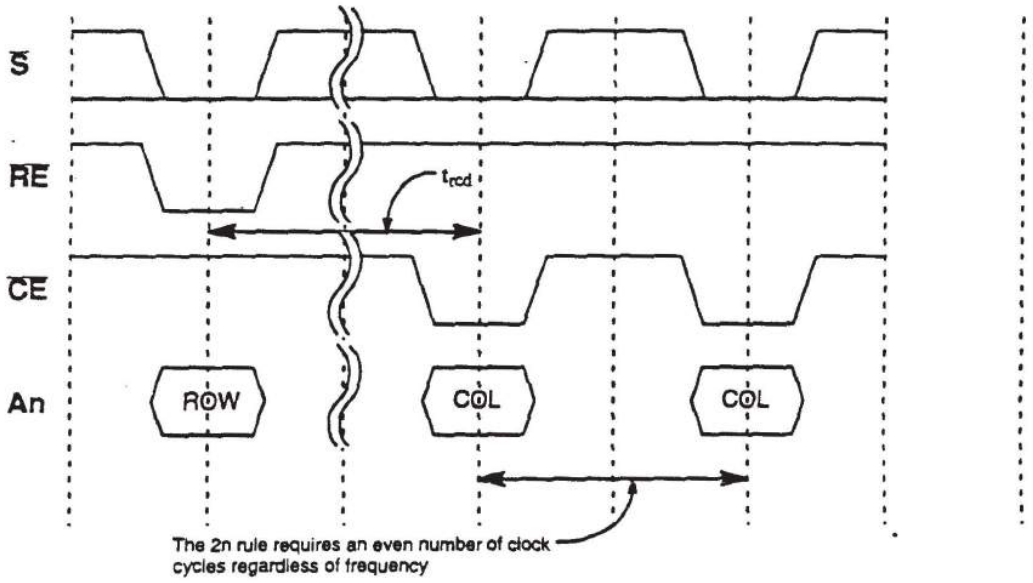
Note: Clock Low–to–high transitions occur at the dotted lines.

3.11.5.12–Column Address to Column Address Delay

The minimum column–address–to–column–address delay time, for page mode accesses, is two clock cycles, independent of operating frequency.

For interrupted bursts, column addresses must, at a minimum, follow the "2n rule" while a read or write burst is in progress. 2n rule: after the initial read or write command, a new column address can be presented to the device every other clock cycle. That is, if the initial read–or–write command occured on an odd clock cycle, the new column addresses must presented on an odd clock cycle while the burst is in progress.

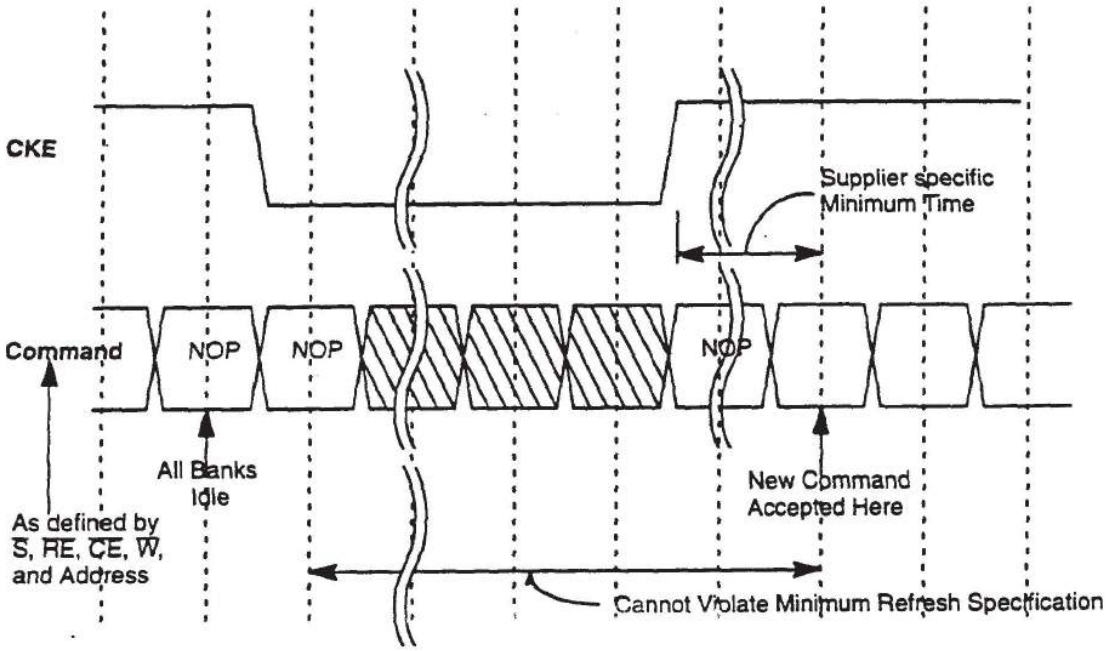
After the burst is completed, the 2n rule no longer applies, and a new column address may be presented to the device on any clock cycle. Essentially the 2n rule remains in effect for (CE Latency + burst length) clock cycles for reads and (write recovery + burst length) clock cycles for writes.



Note: Clock Low–to–high transitions occur at the dotted lines.

3.11.5.13–CKE Timing for Power Down

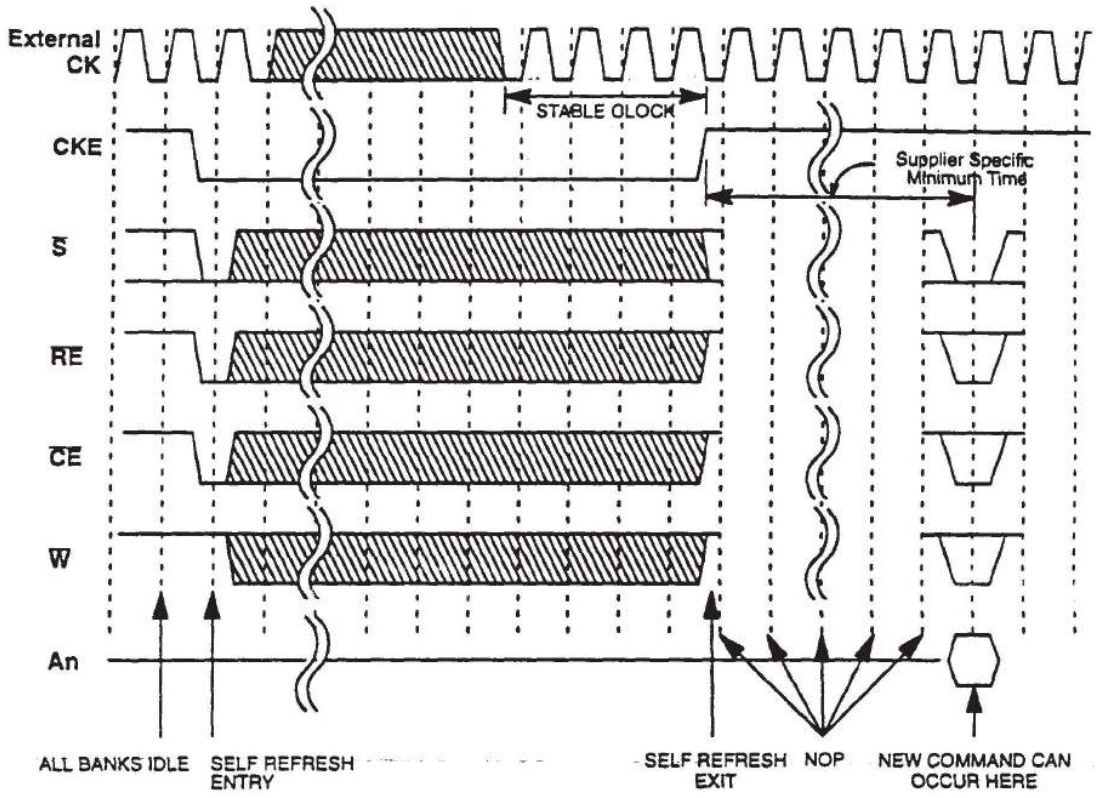
CKE is defined as the clock–enable signal and actually has the dual purpose of also being the signal that puts an SDRAM into a low power state. Using CKE to enter the low power state can only be performed while all internal banks of the device are precharged (IDLE). If all internal banks have been precharged, then CKE is used to gate the input buffers of the device. During power down the device is not refreshed. Therefore the minimum refresh specification still applies during power down. The following timing diagram illustrates power down mode.



Note: Clock Low–to–high transitions occur at the dotted lines.

3.11.5.14–Self–Refresh Entry and Exit

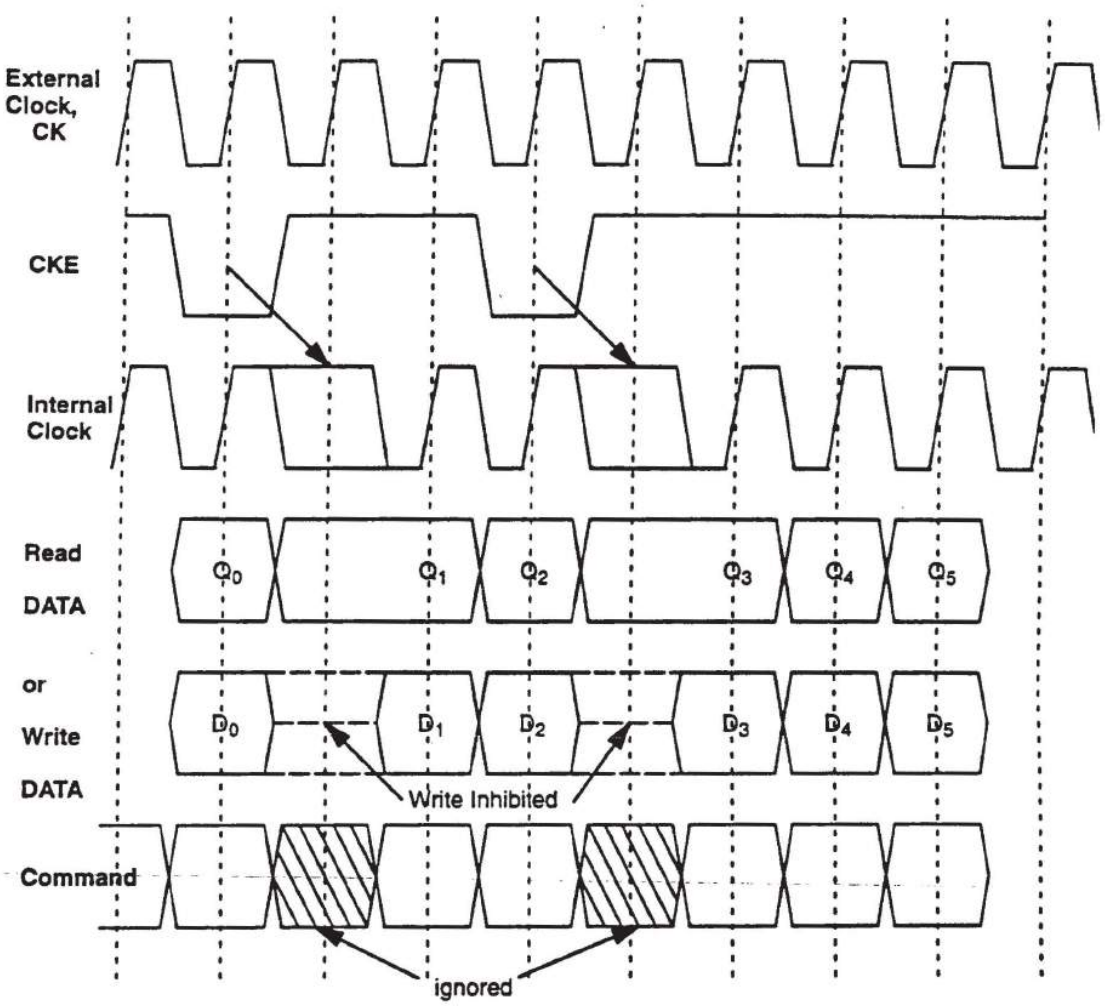
In self refresh mode, the device refreshes itself without outside intervention. While the device is in self–refresh mode, CKE is the only enabled input to the device. All other inputs including the clock are disabled and any input is ignored. Self–refresh mode is entered by precharging all banks and then inserting an auto–refresh command with CKE low. Exit from self–refresh mode is accomplished by starting the clock and then asserting CKE. NOP commands must be asserted for a supplier–specified minimum period, which must include 3 clocks, to allow the device to return to the IDLE state.



Note: Clock Low–to–high transitions occur at the dotted lines.

3.11.5.15–CKE Timing for Clock Suspend

The following timing diagram is shown for CKE when 1 or more banks of the device are active. The effect on read data, write data, and command are all shown on the same diagram for reference only. The clock may be suspended for one or more clock cycles.



Note: Clock Low–to–high transitions occur at the dotted lines.

4.2 SRAM Modules

4.2.1 – 60 PIN ZIP/SIMM SRAM MODULE

CAPACITY—2 X 64K, 2 X 256K, 2 X 1M WORDS OF 4 BITS
CONFIGURATION—DUAL BANK MODULE USING DEVICES WITH 64K, 256K, OR 1M WORDS—SELECTABLE AS 64K, 256K, OR 1M BY 8, 128K, 512K, OR 2M BY 4
PACKAGE—60 PIN SIP MODULE WITH ZIP TERMINAL CONFIGURATION
PIN ASSIGNMENTS—Fig. 4–1A

4.2.2 – 64 PIN ZIP/SIMM SRAM MODULE

CAPACITY—4 X 16K, 4 X 64K, 4 X 256K WORDS OF 8 BITS
CONFIGURATION—FOUR BANK MODULE USING DEVICES WITH 16K, 64K, OR 256K WORDS—SELECTABLE AS 64K, 256K, OR 1M BY 8
32K, 128K, OR 512K, BY 16
16K, 64K, OR 256K BY 32
PACKAGE—64 PIN SIP MODULEWITH ZIP TERMINAL CONFIGURATION
PIN ASSIGNMENTS—Fig. 4–1B

4.2.3 – 70 PIN ZIP/SIMM SRAM MODULE

CAPACITY—64K, 256K, 1M WORDS OF 9 BITS
CONFIGURATION—SINGLE BANK MODULE USING DEVICES WITH 64K, 256K, OR 1M WORDS—SELECTABLE AS 64K, 256K, OR 1M BY 9
LOGIC FEATURE—SEPARATELY CONTROLLABLE BIT FOR USE AS PARITY BIT
PACKAGE—70 PIN SIP MODULE WITH ZIP TERMINAL CONFIGURATION
PIN ASSIGNMENTS—Fig. 4–1C

4.2.4 – 76 PIN ZIP/SIMM SRAM MODULE

CAPACITY—2 X 64K, 2 X 256K, 2 X 1M WORDS OF 9 BITS
CONFIGURATION—DUAL BANK MODULE USING DEVICES WITH 64K, 256K, OR 1M WORDS—SELECTABLE AS 64K, 256K, OR 1M BY 18
128K, 512K, OR 2M BY 9
LOGIC FEATURE—2 SEPARATELY CONTROLLABLE BITS FOR USE AS PARITY BITS
PACKAGE—76 PIN SIP MODULE WITH ZIP TERMINAL CONFIGURATION
PIN ASSIGNMENTS—Fig. 4–1D

4.3 DRAM Modules and Cards

4.3.1 – 22 PIN SIP/SIMM DRAM MODULE

CAPACITY—64K, 256K WORDS OF 4 BITS
CONFIGURATION—SINGLE SIDED MODULE USING 64K OR 256K DEVICES
PACKAGE—22 PIN SIP MODULE
PIN ASSIGNMENTS—Fig. 4–2

4.3.2 – 24 PIN SIP/SIMM DRAM MODULE

CAPACITY—128K, 512K WORDS OF 4 BITS
CONFIGURATION—DOUBLE SIDED MODULE USING 64K OR 256K DEVICES
PACKAGE—24 PIN SIP MODULE
PIN ASSIGNMENTS—Fig. 4–2

4.3.3 – 30 PIN SIP/SIMM DRAM MODULE

CAPACITY—64K, 256K, 1M, 4M WORDS OF 8 OR 9 BITS, & 16M WORDS OF 8 BITS
CONFIGURATION—SINGLE SIDED MODULE
—USING 64K, 256K, 1M, 4M, OR 16M MEMORY DEVICES
LOGIC FEATURES—Some of the modules contain a "presence detect" feature which conists of outputs that supply an encoded value which defines the storage capacity of the module.
PACKAGE—30 PIN SIP MODULE
PIN ASSIGNMENTS—Fig. 4–2

4.3.4 – 30 PIN SIP/SIMM DRAM MODULE FAMILY

CAPACITY —64K TO 8M WORDS OF 4 OR 5 BITS
—128K TO 16M WORDS OF 2 BITS
—256K TO 32M WORDS OF 1 BIT
CONFIGURATION—ONE OR TWO SIDED,
—USING 64K, 256K, 1M, OR 4M DEVICES
CAPACITY—32K, 64K, 128K, 256K WORDS OF 8 BITS
PACKAGE—30 PIN SIP MODULE
PIN ASSIGNMENT Fig. 4–3

4.3.5 – 40 PIN SIP/SIMM DRAM MODULE FAMILY

CAPACITY —64K TO 4M WORDS OF 16 OR 18 BITS
—64K TO 8M WORDS OF 8 OR 9 BITS
—128K TO 16M WORDS OF 4 BITS
—256K TO 32M WORDS OF 2 BITS
—512K TO 64M WORDS OF 1 BIT
CONFIGURATION—ONE OR TWO SIDED,
—USING 64K, 256K, 1M, OR 4M DEVICES
PACKAGE—40 PIN SIP MODULE
PIN ASSIGNMENTS—Fig. 4–4

4.3.6 – 23/25/26/28 PIN ZIP/SIMM DRAM MODULE FAMILY

CAPACITY —256K TO 16M WORDS OF 4 BIT
—1M TO 64M WORDS OF 1 BIT
CONFIGURATION—DOUBLE SIDED, USING 1M, 4M, 16M, OR 64M DEVICES
PACKAGE—THE X4 MODULES, 26 PIN ZIP/SIP MODULE
THE X1 MODULES, 23 PIN ZIP/SIP MODULE
PIN ASSIGNMENTS—Fig. 4–5
NOTE: At the highest density using 64M memory devices, the modules must be expanded to 25 or 28 pins to provide the needed addresses. These modules will be defined in more detail when the packages for the 64M memory devices have been defined.

4.3.7 – 72 PIN SIMM DRAM MODULE FAMILY

CAPACITY—256K, 512K, 1M, 2M, 4M, 8M WORDS OF 36 BITS
CONFIGURATION—SINGLE OR DOUBLE SIDED MODULES
—USING 1M, 4M, OR 16M. MEMORY DEVICES
LOGIC FEATURES, These modules contain a "presence detect" feature which conists of output pins which supply an encoded value which defines the storage capacity and speed of the module.
PACKAGE—72 PIN SIMM MODULE
PIN ASSIGNMENTS—Fig. 4–6

4.3.8 – 60 PIN DRAM CARD FAMILY

CAPACITY—512K, 1M, 2M, 4M, & 8M WORDS OF 16 OR 18 BITS
CONFIGURATION—SEVEN DIFFERENT CONFIGURATIONS
—USING 1Mb & 4Mb DEVICES AND WITH 1, 2, OR 4 RE CLOCKS.
LOGIC FEATURES, The cards contain a "PRESENCE DETECT" feature which conists of output pins which supply an encoded value which defines the storage capacity, configuration, and speed of the card.
PACKAGE—60 PIN JEDEC MEMORY CARD
PIN ASSIGNMENTS—Fig. 4–7A
CONFIGURATION BLOCK DIAGRAMS—Fig. 4–7B

4.3.9 – 88 PIN DRAM CARD FAMILY

CAPACITY—256K, 512K, 1M, 2M, 4M, 8M, 16M, 32M, 64M, & 128M WORDS OF 36 BITS
CONFIGURATION—Ten Different Configurations Using 1mb, 4mb, 16mb, 64mb, & 256mb Devices And With 2, Or 4 $\overline{RE}$ Clocks.
LOGIC FEATURES—The cards may be used with DATA BUS widths of X16/18 or X32/36— The cards contain a "PRESENCE DETECT" feature which conists of output pins which supply an encoded value which defines the storage capacity, configuration, and speed of the card.
PACKAGE—88 PIN JEDEC MEMORY CARD
PIN ASSIGNMENTS—Fig. 4–8A
CONFIGURATION BLOCK DIAGRAMS—Figs. 4–8C, 4–8D, 4–8E, & 4–8F

4.3.10 – 72 PIN SIMM DRAM ECC MODULE FAMILY

CAPACITY—256K, 512K, 1M, 2M, 4M, 8M WORDS OF 36 or 40 BITS
CONFIGURATION—SINGLE OR DOUBLE SIDED MODULES
—USING 1M, 4M, OR 16M. MEMORY DEVICES
LOGIC FEATURES, These modules are optimized for ECC applications. They are similar to but not the same as the modules described in Fig. 4–6. The Standard defines a "presence detect" feature which conists of output pins which supply an encoded value which defines the storage capacity and speed of the module. The PD code identifies the presence of an ECC module as well as the speed and organization of the module. The Standard also defines the logic organization of the modules in Figs. 4–10B & 4–10C.
PACKAGE—72 PIN SIMM MODULE
PIN ASSIGNMENTS—Fig. 4–10A

4.3.11 – 168 PIN DRAM SIMM FAMILY

CAPACITY—256K, 512K, 1M, 2M, 4M, 8M, 16M, 32M, & 64M WORDS OF 64, 72, OR 80 BITS
DATA CONFIGURATIONS—Four DATA Word configurations are defined:
—64 BIT without PARITY
—72 BIT for PARITY CODES
—72 BIT for ECC CODES
—80 BIT for ECC CODES
CONFIGURATION—21 Different Configurations are defined using various combinationa of X1, X4, X8, X9, X16 and X18 memory devices.
LOGIC FEATURES—The modules contain "PRESENCE DETECT" and "IDENTITY" featurs that conist of output pins in the PDn and IDn fields which supply encoded values that define the storage capacity, configuration, data word configuration, refresh mode, and speed of the module.
PACKAGE—168 PIN JEDEC MEMORY MODULE
PIN ASSIGNMENTS AND PD TABLES—Figs. 4–13 A, 4–13 B, & 4–13 C
CAPACITY / DEVICE CONFIGURATION TABLE—Fig. 4–13 D
CONFIGURATION BLOCK DIAGRAM—Figs. 4–13 E through 4–13 Y

4.4 MULTIPLE TECHNOLOGY MEMORY CARDS AND MODULES

4.4.1 – 68 PIN MULTIPLE TECHNOLOGY MEMORY CARD FAMILY

CAPACITY—UP TO 32M WORDS OF 16 BITS

CONFIGURATION—ONE BASIC CONFIGURATION that allows the use of SRAM, EEPROM, EPROM, or ROM memory devices with software or firmware control to accomidate the device characteristic differences.

LOGIC FEATURES,

—The card contains an internal MEMORY called the "ATTRIBUTE MEMORY"; the contents describe the hardware and software characteristics, and use of the card.

— The card contains a "PRESENCE DETECT" feature which conists of output pins which supply an encoded value which defines the storage capacity, configuration, and speed of the card.

PACKAGE—68 PIN JEDEC MEMORY CARD

PIN ASSIGNMENTS—Fig. 4–9

MEMORY CARD OPERATION TRUTH TABLE— Page 4–25

MEMORY CARD SPECIFIC TERMINOLOGY— Sec. 2.8, Page 2–13

4.4.2 – 80 PIN EEPROM SIMM FAMILY

CAPACITY—128K, 256K, 512K, 1M, 2M, 4M, & 8M WORDS OF 32 BITS

CONFIGURATION—Fifteen Different Configurations Using 1mb, 4mb, & 16mb Devices.

LOGIC FEATURES—The modules contain a "PRESENCE DETECT" feature which conists of output pins which supply an encoded value which defines the storage capacity, configuration, and speed of the module.

PACKAGE—88 PIN JEDEC MEMORY MODULE

PIN ASSIGNMENTS AND PD TABLES—Fig. 4–12 A

CONFIGURATION BLOCK DIAGRAM—Figs. 4–12 B

PHYSICAL CONFIGURATION	4 DEVICES LONG				8 OR 9 DEVICES LONG			
	SINGLE BANK		DOUBLE BANK		SINGLE BANK			DOUBLE BANK
VERSION	N X 4	@ 4N X 1	2N X 4	N X 8	* N X 8(9)	* N X 8(9)	16M X 8	* 2N X 8(9)
1	$ A8	VSS	** NC	% NC	VDD	VDD	VDD	VDD
2	VDD	VDD	A8	A8	CE	CE	CE	CE
3	D0	RE0	VDD	VDD	DQ0	DQ0	DQ0	DQ0
4	Q0	Q	D0	DQ0	A0	A0	A0	A0
5	CE	A3	Q0	DQ1	A1	A1	A1	A1
6	A7	A6	CE	CE	DQ1	DQ1	DQ1	DQ1
7	A5	D	A7	A7	A2	A2	A2	A2
8	A4	W	A5	A5	A3	A3	A3	A3
9	D1	RE1	A4	A4	VSS	VSS	VSS	VSS
10	Q1	A0	D1	DQ2	DQ2	DQ2	DQ2	DQ2
11	W	A7	Q1	DQ3	A4	A4	A4	A4
12	A1	A8	W	W	A5	A5	A5	A5
13	A3	CE	A1	A1	DQ3	DQ3	DQ3	DQ3
14	A6	RE2	A3	A3	A5	A6	A6	A6
15	Q2	A2	A6	A6	A7	A7	A7	A7
16	D3	A1	Q2	DQ4	DQ4	DQ4	DQ4	DQ4
17	A2	@ A9	D2	DQ5	A8	A8	A8	A8
18	A0	A4	A2	A2	* A9	* A9	A9	* A9
19	RE	RE3	A0	A0	* A10	NC	A10	RE2
20	D3	A5	RE1	RE	DQ5	DQ5	DQ5	DQ5
21	Q0	VDD	D3	DQ6	W	W	W	W
22	VSS	VSS	Q3	DQ7	VSS	VSS	VSS	VSS
23			VSS	VSS	DQ6	DQ6	DQ6	DQ6
24			*** RE2	NC	# NC	PD1	A11	PD1
25					DQ7	DQ7	DQ7	DQ7
26					Q8	PD2	NC	PD2
27					RE	RE	RE	RE1
28					CE8	NC	NC	NC
29					D8	DQ8	NC	DQ8
30					VDD	VDD	VDD	VDD

TOP VIEW

* ON THE 30 PIN MODULE, 1M & 4M DEVICES MAY BE USED. PINS 18 & 19 ARE USED TO PROVIDE ADDRESS EXPANSION. THE OTHER MODULES WILL ACCOMIDATE 64K & 256K DEVICES ONLY.

** OPTIONAL VSS

*** NC FOR SINGLE BANK VERSION

$ OPTIONAL VSS WHEN A8 NOT NEEDED

OPTIONAL REFRESH (F) FUNCTION

@ ON THE 22 PIN 4N X 1 MODULE, 1 MB & 4 MB DEVICES MAY BE USED. PIN 17 IS USED FOR ADDRESS EXPANSION

% POTENTIAL VSS

PRESENCE DETECT TRUTH TABLE			
SIZE	256K	512K	1M
PIN			
PD1	L	H	L
PD2	H	L	L

CONFIGURATION DEFINES THE PHYSICAL ARRANGEMENTS OF THE MEMORY DEVICES ON THE MODULE, GIVING LENGTH AND NUMBER OF SIDES POPULATED.

VERSION IS THE LOGIC ORGANIZATION OF THE MODULE WHERE "N" IS THE CAPACITY OF THE MEMORY DEVICE USED.

FIGURE 4–2
22, 24,& 30 PIN DRAM MODULES

PHYSICAL CONFIGURATION		4 OR 5 DEVICES LONG SINGLE SIDED			4 OR 5 DEVICES LONG DOUBLE SIDED		
VERSION		N X 4(5)	2N X 2	4N X 1	2N X 4(5)	4N X 2	8N X 1
1	1	VDD					
2	2	D4	NC	NC	D4	NC	NC
3	3	Q4	NC	NC	Q4	NC	NC
4	4	A8					
5	5	A9					
6	6	*A10					
7	7	D3	D1	NC	D3	D1	NC
8	8	Q3	Q1	NC	Q3	Q1	NC
9	9	VSS					
10	10	A6					
11	11	A7					
12	12	A2					
13	13	A1					
14	14	D2	NC	D	D2	NC	D
15	15	Q2	NC	Q	Q2	NC	Q
16	16	A4					
17	17	A5					
18	18	A3					
19	19	A0					
20	20	D1	D0	NC	D1	D0	NC
21	21	Q1	Q0	NC	Q1	Q0	NC
22	22	VSS					
23	23	$\overline{W}$					
24	24	$\overline{CE}$	$\overline{CE1}$				
25	25	NC	$\overline{CE2}$				
26	26	$\overline{RE}$			$\overline{RE1}$		
27	27	NC	NC	NC	$\overline{RE2}$		
28	28	D0	NC	$\overline{CE3}$	D0	NC	$\overline{CE3}$
29	29	Q0	NC	$\overline{CE4}$	Q0	NC	$\overline{CE4}$
30	30	VDD					

30 PIN
SIP MODULE
TOP VIEW

* PIN 6 RESERVED FOR OPTIONAL REFRESH (F) WHEN NOT NEEDED FOR A10

CONFIGURATION DEFINES THE PHYSICAL ARRANGEMENTS OF THE MEMORY DEFICES ON THE MODULE, GIVING LENGTH AND NUMBER OF SIDES POPULATED

VERSION IS THE LOGIC ORGANIZATION OF THE MODULE WHERE "N" IS THE CAPACITY OF THE MEMORY DEVICE USED

MEMORY DEVICES WITH A CAPACITY OF UP TO 4Mb BY 1 CAN BE ACCOMIDATED ON THE MODULES DEFINED IN THIS STANDARD

FIGURE 4-3
30 PIN DRAM MODULE FAMILY

PIN #	PIN NAME	PIN #	PIN NAME
1	VSS	37	DQ17
2	DQ0	38	DQ35
3	DQ18	39	VSS
4	DQ1	40	$\overline{CE0}$
5	DQ19	41	$\overline{CE2}$
6	DQ2	42	$\overline{CE3}$
7	DQ20	43	$\overline{CE1}$
8	DQ3	44	$\overline{RE0}$
9	DQ21	45	NC, $\overline{RE1}$
10	VDD	46	NC
11	NU	47	$\overline{W}$
12	A0	48	NC ($\overline{ECC}$)
13	A1	49	DQ9
14	A2	50	DQ27
15	A3	51	DQ10
16	A4	52	DQ28
17	A5	53	DQ11
18	A6	54	DQ29
19	NC, A10	55	DQ12
20	DQ4	56	DQ30
21	DQ22	57	DQ13
22	DQ5	58	DQ31
23	DQ23	59	VDD
24	DQ6	60	DQ32
25	DQ24	61	DQ14
26	DQ7	62	DQ33
27	DQ25	63	DQ15
28	A7	64	DQ34
29	NC, A11	65	DQ16
30	VDD	66	NC
31	A8	67	PD1
32	NC, A9	68	PD2
33	NC, $\overline{RE3}$	69	PD3
34	$\overline{RE2}$	70	PD4
35	DQ26	71	NC
36	DQ8	72	VSS

PRESENCE DETECT TRUTH TABLE

CONFIGURATION	tRAC	$\overline{ECC}$	PD1	PD2	PD3	PD4
1MB (256K X 36/40)	100 nS	O	S	O	S	S
	80 nS	O	S	O	O	S
	70 nS	O	S	O	S	O
	60 nS	O	S	O	O	O
2MB (512K X 36)	100 nS	O	O	S	S	S
	80 nS	O	O	S	O	S
	70 nS	O	O	S	S	O
	60 nS	O	O	S	O	O
4MB (1M X 36)	100 nS	O	S	S	S	S
	80 nS	O	S	S	O	S
	70 nS	O	S	S	S	O
	60 nS	O	S	S	O	O
8MB (2M X 36)	100 nS	O	O	O	S	S
	80 nS	O	O	O	O	S
	70 nS	O	O	O	S	O
	60 nS	O	O	O	O	O
16MB (4M X 36)	100 nS	O	S	O	S	S
	80 nS	O	S	O	O	S
	70 nS	O	S	O	S	O
	60 nS	O	S	O	O	O
32MB (8M X 36)	100 nS	O	O	S	S	S
	80 nS	O	O	S	O	S
	70 nS	O	O	S	S	O
	60 nS	O	O	S	O	O

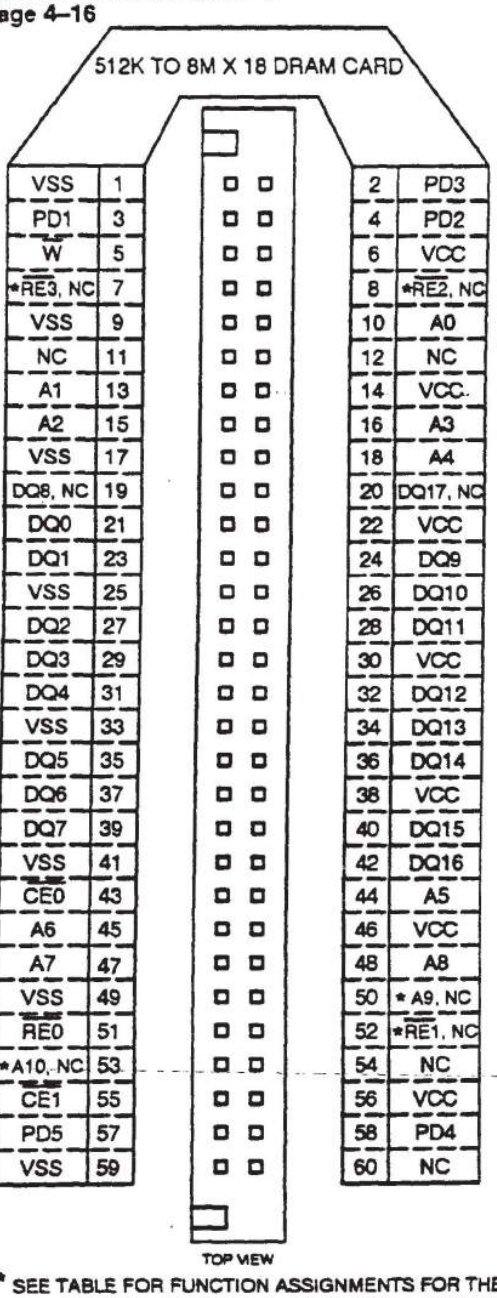
O = OPEN CIRCUIT (NO CONNECTION)
S = CONNECTED TO VSS
Note: The $\overline{ECC}$ Function (Pin 48) is not a defined function for the devices in this standard, however, it is used in a companion Standard for 72 pin ECC modules shown in Fig. 4–10. The presence of a VSS connection on this pin signifies that an ECC module has been inserted.

CONFIGURATION PIN ASSIGNMENT TABLE

	MODULE SIZE, 36 BIT WORDS					
PIN #	256K	512K	1M	2M	4M	8M
19	NC	NC	NC	NC	A10	A10
*29	NC	NC	NC	NC	A11	A11
32	NC	NC	A9	A9	A9	A9
33	NC	$\overline{RE3}$	NC	$\overline{RE3}$	NC	$\overline{RE3}$
45	NC	$\overline{RE1}$	NC	$\overline{RE1}$	NC	$\overline{RE1}$

*A11 on Pin 29 is used on modules containing devices that require 12 ROW and 10 COLUMN addresses.
NOTE – This family of pinouts is approved for use in SIMM modules which are nominally 4.25" long and with a height which varies depencing on the configuration and the memory devices used. See JEDEC Publication 95.

FIGURE 4–6
256K TO 8M BY 36. 72 PIN DRAM MODULE FAMILY



* SEE TABLE FOR FUNCTION ASSIGNMENTS FOR THESE PINS AS A FUNCTION OF CARD CAPACITY AND CONFIGURATION

	PD4	PD5
SPEED (tRAC)	58	57
80 NS	VSS	VSS
70 NS	VSS	NC
60 NS	NC	VSS
50 NS	NC	NC

PD SPEED TABLE

	PD1	PD2	PD3
CONFIGURATION	3	4	2
512K X 16/18 2 RE	VSS	NC	VSS
1M X 16/18 4 RE	VSS	NC	NC
2M X 16/18 2 RE	NC	VSS	VSS
4M X 16/18 4 RE	NC	VSS	NC
1M X 16/18 1 RE	VSS	VSS	VSS
4M X 16/18 1 RE	NC	NC	VSS
8M X 16/18 2 RE	VSS	VSS	NC
NO CARD	NC	NC	NC

PD CONFIGURATION TABLE

	PIN NUMBER				
CONFIGURATION	50	53	52	8	7
512K X 16/18 2 RE	NC	NC	RE1	NC	NC
1M X 16/18 4 RE	NC	NC	RE1	RE2	RE3
2M X 16/18 2 RE	A9	NC	RE1	NC	NC
4M X 16/18 4 RE	A9	NC	RE1	RE2	RE3
1M X 16/18 1 RE	A9	NC	NC	NC	NC
4M X 16/18 1 RE	A9	A10	NC	NC	NC
8M X 16/18 2 RE	A9	A10	RE1	NC	NC

CONFIGURATION PIN ASSIGNMENT TABLE

Pins 19 & 20 (DQ8 & DQ 17) are NC for X16 Versions

FIGURE 4–7A
512K TO 8M BY 16 or 18 DRAM CARD

PD BITS 5 4 3 2 1	CARD DENSITY	DRAM ORGANIZATION	CARD ADDR. REQ'D	RE ADDR.	CE ADDR.	AVAIL. PAGE DEPTH	AVERAGE REFRESH INTERVAL	NOTES
1 1 1 1 1	NO CARD							NO CARD INSTALLED
1 0 0 0 0	1 MB	256K X 1, 4, 16, 18	18	9	9	512	125 mS	
0 0 0 0 0	2 MB	256K X 1, 4, 16, 18	18	9	9	512	125 mS	
1 0 0 0 1	2 MB	512K X 8, 9	19	10	9	512	125 mS	
0 0 0 0 1	4 MB	512K X 8, 9	19	10	9	512	125 mS	
1 0 0 1 0	4 MB	1M X 1, 4, 16, 18	20	10	10	1024	125 mS	
0 0 0 1 0	8 MB	1M X 1, 4, 16, 18	20	10	10	1024	125 mS	
1 1 0 1 0	4 MB	1M X 16, 18	20	12	8	256	62 mS	
0 1 0 1 0	8 MB	1M X 16, 18	20	12	8	256	62 mS	
1 0 0 1 1	8 MB	2M X 8, 9	21	11	10	1024	125 mS	
0 0 0 1 1	16 MB	2M X 8, 9	21	11	10	1024	125 mS	
1 0 1 0 0	16 MB	4M X 1, 4, 16, 18	22	12	*11	**1024	62 mS	SUPPORT 12/10 AND 11/11 ADDRESS
0 0 1 0 0	32 MB	4M X 1, 4, 16, 18	22	12	*11	**1024	62 mS	SUPPORT 12/10 AND 11/11 ADDRESS
1 0 1 0 1	32 MB	8M X 8, 9	23	13	*11	**1024	62 mS	SUPPORT 13/10 AND 12/11 ADDRESS
0 0 1 0 1	64 MB	8M X 8, 9	23	13	*11	**1024	62 mS	SUPPORT 13/10 AND 12/11 ADDRESS
1 0 1 1 0	64 MB	16M X 1, 4, 16, 18	24	14	*11	**1024	31 mS	SUPPORT 13/11 AND 14/10 ADDRESS
0 0 1 1 0	128MB	16M X 1, 4, 16, 18	24	14	*11	**1024	31 mS	SUPPORT 13/11 AND 14/10 ADDRESS

* INDICATES REDUNDANT ADDRESS THAT MUST BE PROVIDED AT CE\ TIME (TO ALLOW USE OF MIXED DRAM ADDRESSING)
** PAGE DEPTH DETERMINED BY THE SMALLEST CE\ ADDRESS DRAM
*** ALL DENSITIES ASSUME 4 BYTE CARD DATA WIDTH (32 OR 36 BITS)
FOR THE PDn PINS, 1 = NC, 0 = VSS

MEMORY CARD ORGANIZATION AND ADDRESS STRUCTURE

BASE DEVICE	CONFIG'N	PIN NUMBER 9	11	15	17	25	27	35	37
1M	256K X 36, 2 $\overline{RE}$	5 V	NC	5 V	NC	NC	5 V	NC	5 V
1M	512K X 36, 4 $\overline{RE}$	5 V	NC	5 V	NC	NC	5 V	NC	5 V
4M	1M X 36, 2 $\overline{RE}$	5 V	NC	5 V	NC	NC	5 V	NC	5 V
4M	2M X 36, 4 $\overline{RE}$	5 V	NC	5 V	NC	NC	5 V	NC	5 V
16M	4M X 36, 2 $\overline{RE}$	5 V, NC	NC, 3.3 V	5 V, NC	NC, 3.3 V	NC, 3.3 V	5 V, NC	NC, 3.3 V	5 V, NC
16M	8M X 36, 4 $\overline{RE}$	5 V, NC	NC, 3.3 V	5 V, NC	NC, 3.3 V	NC, 3.3 V	5 V, NC	NC, 3.3 V	5 V, NC
64M	16M X 36, 2 $\overline{RE}$	NC	3.3 V	NC	3.3 V	3.3 V	NC	3.3 V	NC
64M	32M X 36, 4 $\overline{RE}$	NC	3.3 V	NC	3.3 V	3.3 V	NC	3.3 V	NC
256M	64M X 36, 2 $\overline{RE}$	NC	3.3 V	NC	3.3 V	3.3 V	NC	3.3 V	NC
256M	128M X 36, 4 $\overline{RE}$	NC	3.3 V	NC	3.3 V	3.3 V	NC	3.3 V	NC

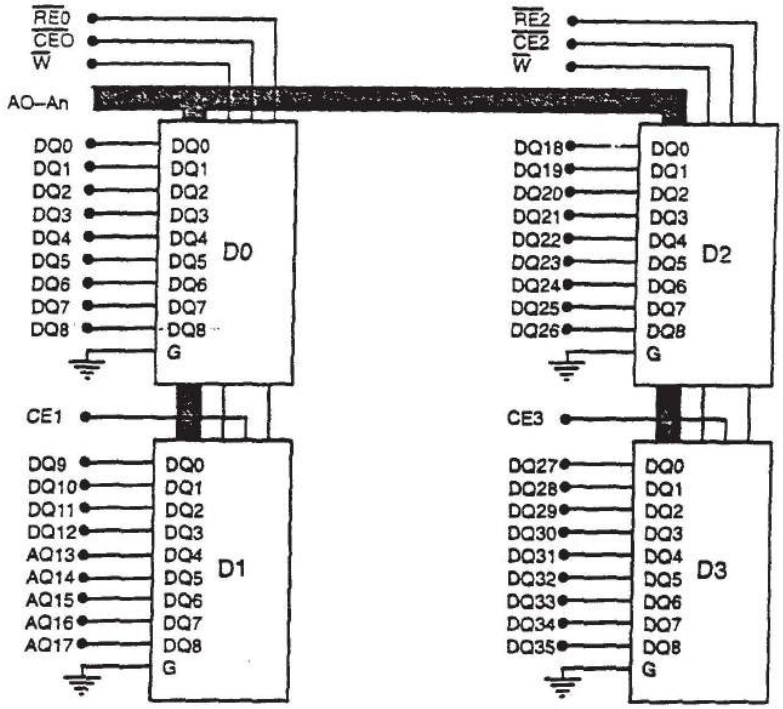
VCC POWER PIN ASSIGNMENT TABLE

FIGURE 4–8B

256K TO 128M BY 36, 88 PIN DRAM CARD FAMILY CONFIGURATION TABLES

Release 4

BLOCK DIAGRAM for 512K /2M/8M/32M X 36 or 1M/4M/16M/64M X 18
USING X8 or X9 DRAM



WORD ORGANIZATION	* BASE MEMORY DEVICE	
	D0 – D3	ADDRESS
512K X 36 or 1M X 18	4M (X9)	A0 – A9
2M X 36 or 4M X 18	16M (X9)	A0 – A10
8M X 36 or 16M X 18	64M (X9)	A0 – A12

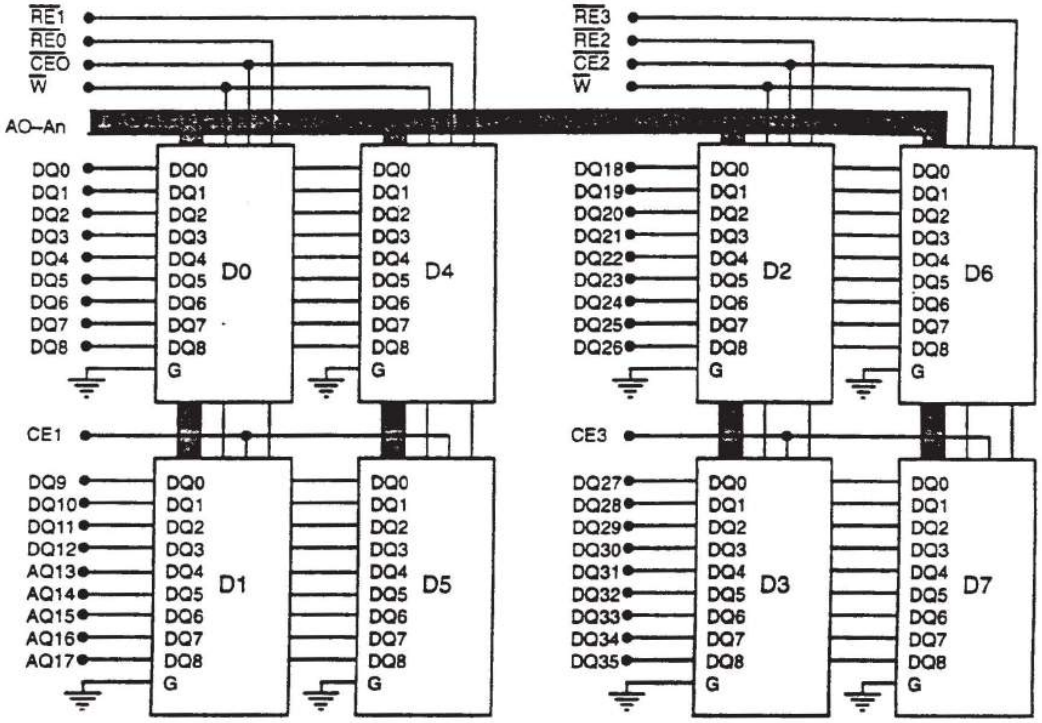
* NOTE: The BASE MEMORY DEVICE columns give the total device capacity in bits and the data interface configuration

note 1: In an 18 bus system, RE0 and RE2 will be controlled independently and the data bus will be connected to for an 18 bit bus ourside the card
In a 36 bit system, RE0 and RE2 will be actuated simultaneously
note 2: The card contains 4 bytes of data; 2 byte operation is allowed.

FIGURE 4–8C
256K TO 128M BY 36, 88 PIN DRAM CARD FAMILY BLOCK DIAGRAMS
Release 4

Jedec 0007813

BLOCK DIAGRAM for 1M /4M/16M/64M X 36 or 2M/8M/32M/128M X 18
USING X8 or X9 DRAM



WORD ORGANIZATION	* BASE MEMORY DEVICE	
	D0 – D7	ADDRESS
1M X 36 or 2M X 18	4M (X9)	A0 – A9
4M X 36 or 8M X 18	16M (X9)	A0 – A10
16M X 36 or 32M X 18	64M (X9)	A0 – A12

* NOTE: The BASE MEMORY DEVICE columns give the total device capacity in bits and the data interface configuration

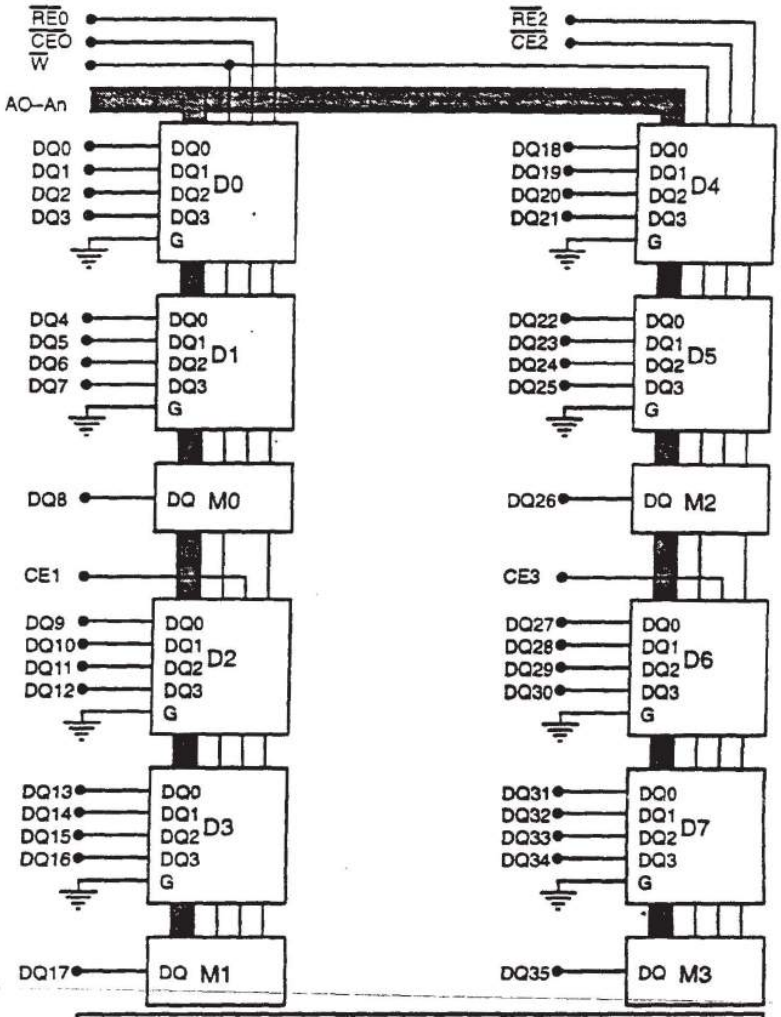
note 1: In an 18 bus system, RE0 and RE2 (also RE1 and RE3) will be controlled independently and the data bus will be connected to for an 18 bit bus ourside the card
In a 36 bit system, RE0 and RE2 (also RE1 and RE3) will be actuated simultaneously
note 2: The card contains 4 bytes of data; 2 byte operation is allowed.

FIGURE 4–8D

256K TO 128M BY 36, 88 PIN DRAM CARD FAMILY BLOCK DIAGRAMS

Release 4

BLOCK DIAGRAM for 256K /1M/4M/16M/64M X 36 or 512K/2M/8M/32M/128M X 18
USING X4 and X1 DRAM



WORD ORGANIZATION	* BASE MEMORY DEVICE		
	D0 – D7	M0 – M3	ADDRESS
256K X 36 or 512K X 18	1M (X4)	256K (X1)	A0 – A8
1M X 36 or 2M X 18	4M (X4)	1M (X1)	A0 – A9
4M X 36 or 8M X 18	16M (X4)	4M (X1)	A0 – A11
16M X 36 or 32M X 18	64M (X4)	16M (X1)	A0 – A13

* NOTE: The BASE MEMORY DEVICE columns give the total device capacity in bits and the data interface configuration

note 1: In an 18 bus system, RE0 and RE2 will be controlled independently and the data bus will be connected to for an 18 bit bus ourside the card
In a 36 bit system, RE0 and RE2 will be actuated simultaneously

note 2: The card contains 4 bytes of data; 2 byte operation is allowed.

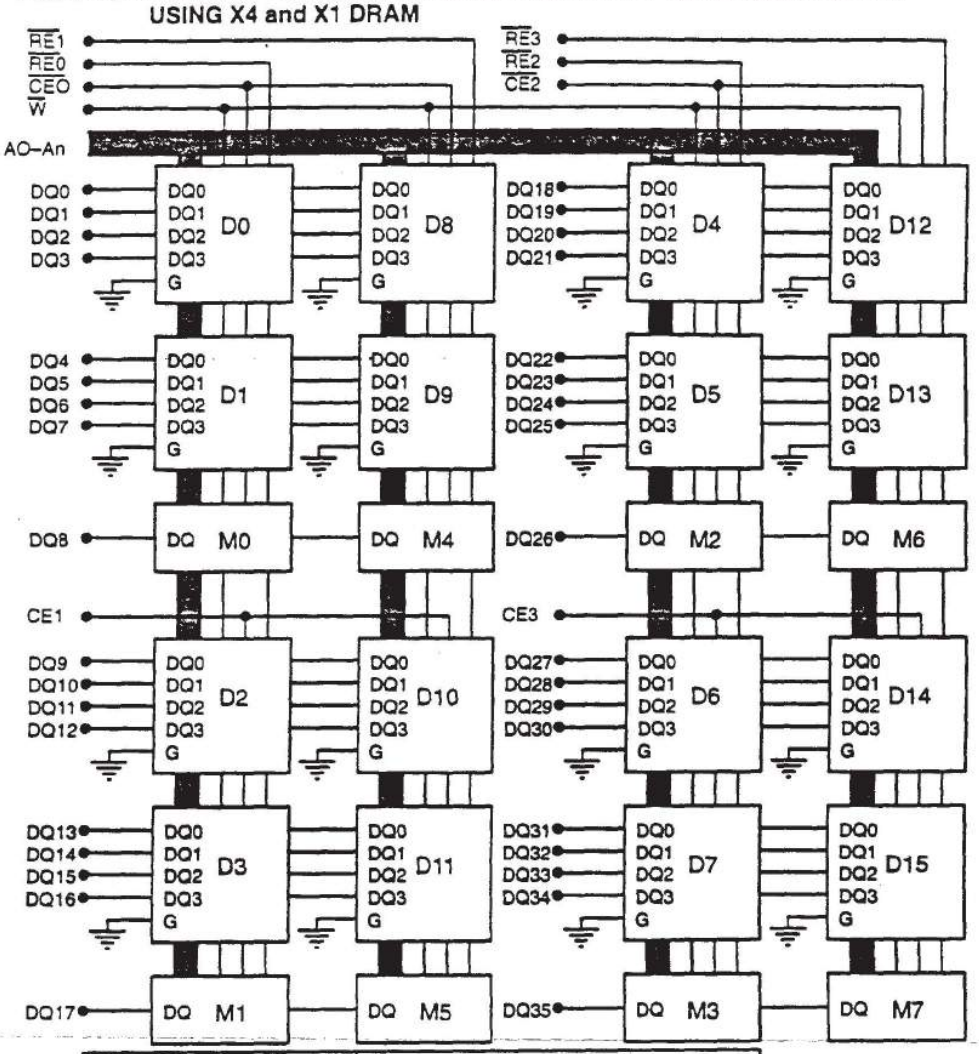
FIGURE 4–8E

256K TO 128M BY 36, 88 PIN DRAM CARD FAMILY BLOCK DIAGRAMS

Release 4

Jedec 0007815

BLOCK DIAGRAM for 512K/2M/8M/32M/32M/128M X 36 or 1M/4M/16M/256M X 18
USING X4 and X1 DRAM



WORD ORGANIZATION	* BASE MEMORY DEVICE		
	D0 – D15	M0 – M7	ADDRESS
512K X 36 or 1M X 18	1M (X4)	256K(X1)	A0 – A8
2M X 36 or 4M X 18	4M (X4)	1M (X1)	A0 – A9
8M X 36 or 16M X 18	16M (X4)	4M (X1)	A0 – A11
32M X 36 or 64M X 18	64M (X4)	16M (X1)	A0 – A13

* NOTE: The BASE MEMORY DEVICE columns give the total device capacity in bits and the data interface configuration

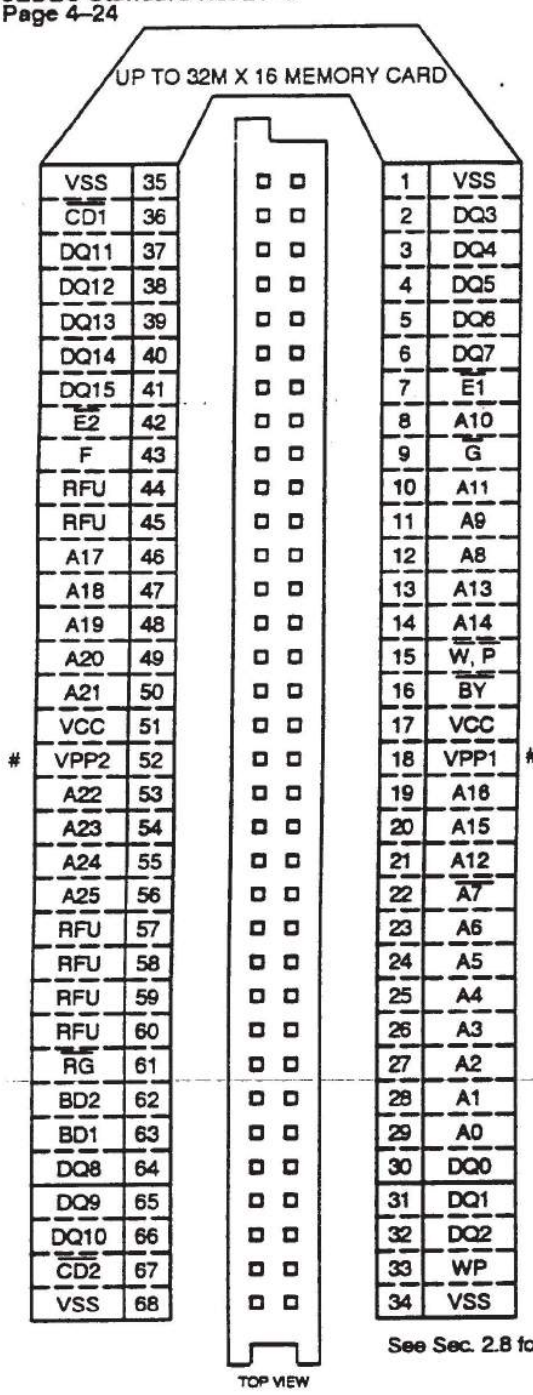
note 1: In an 18 bus system, RE0 and RE2 (also RE1 AND RE3) will be controlled independently and the data bus will be connected to for an 18 bit bus ourside the card.
In a 36 bit system, RE0 and RE2 (also RE1 and RE3) will be actuated simultaneously

note 2: The card contains 4 bytes of data; 2 byte operation is allowed.

FIGURE 4–8F

256K TO 128M BY 36, 88 PIN DRAM CARD FAMILY BLOCK DIAGRAMS

Release 4



NOTE: When the VPP1 & VPP2 pins are not active and connected to the programming supply for the purpose of altering programmable memory, these pins must be connected to VCC.

* NOTE: This Standard is applicable to SRAM, EPROM, OTPROM, EEPROM, and FLASH Memory. It is not applicable to DRAM.

See Sec. 2.8 for definitions of the special pin names used in this standard

FIGURE 4–9A
UP TO 32M by 16 MULTIPLE TECHNOLOGY MEMORY CARD

Jedec 0007817

Release 3

Main Memory Read Function for all types of Memory Card except DRAM										
MODE	$\overline{RG}$	$\overline{E2}$	$\overline{E1}$	A0	$\overline{G}$	$\overline{W}$	VPP2	VPP1	DQ15–DQ8	DQ7–DQ0
Standby Mode	X	H	H	X	X	X	VCC	VCC	High–Z	High–Z
Byte Access (8 bits)	H	H	L	L	L	H	VCC	VCC	High–Z	Even–Byte
	H	H	L	H	L	H	VCC	VCC	High–Z	Odd–Byte
Word Access (16 bits)	H	L	L	X	L	H	VCC	VCC	Odd–Byte	Even–Byte
Odd–Byte Only Access	H	L	H	X	L	H	VCC	VCC	Odd–Byte	High–Z
Main Memory Write Function for SRAM and EEPROM										
MODE	$\overline{RG}$	$\overline{E2}$	$\overline{E1}$	A0	$\overline{G}$	$\overline{W}$	VPP2	VPP1	DQ15–DQ8	DQ7–DQ0
Standby Mode	X	H	H	X	X	X	VCC	VCC	XXX	XXX
Byte Access (8 bits)	H	H	L	L	H	L	VCC	VCC	XXX	Even–Byte
	H	H	L	H	H	L	VCC	VCC	XXX	Odd–Byte
Word Access (16 bits)	H	L	L	X	H	L	VCC	VCC	Odd–Byte	Even–Byte
Odd–Byte Only Access	H	L	H	X	H	L	VCC	VCC	Odd–Byte	High–Z
Main Memory Write Function for OTPROM, EPROM, and FLASH Memory										
MODE	$\overline{RG}$	$\overline{E2}$	$\overline{E1}$	A0	$\overline{G}$	$\overline{W}$	VPP2	VPP1	DQ15–DQ8	DQ7–DQ0
Standby Mode	X	H	H	X	X	X	VCC, VPP	VCC, VPP	XXX	XXX
Byte Access (8 bits)	H	H	L	L	H	L	VCC	VPP	XXX	Even–Byte
	H	H	L	H	H	L	VPP	VCC	XXX	Odd–Byte
Word Access (16 bits)	H	L	L	X	H	L	VPP	VPP	Odd–Byte	Even–Byte
Odd–Byte Only Access	H	L	H	X	H	L	VPP	VCC	Odd–Byte	XXX
Attribute Memory Read Function										
MODE	$\overline{RG}$	$\overline{E2}$	$\overline{E1}$	A0	$\overline{G}$	$\overline{W}$	VPP2	VPP1	DQ15–DQ8	DQ7–DQ0
Standby Mode	X	H	H	X	X	X	VCC	VCC	High–Z	High–Z
Byte Access (8 bits)	L	H	L	L	L	H	VCC	VCC	High–Z	Even–Byte
	L	H	L	H	L	H	VCC	VCC	High–Z	Not Valid
Word Access (16 bits)	L	L	L	X	L	H	VCC	VCC	Not Valid	Even–Byte
Odd–Byte Only Access	L	L	H	X	L	H	VCC	VCC	Not Valid	High–Z
Attribute Memory Write Function for SRAM and EEPROM										
MODE	$\overline{RG}$	$\overline{E2}$	$\overline{E1}$	A0	$\overline{G}$	$\overline{W}$	VPP2	VPP1	DQ15–DQ8	DQ7–DQ0
Standby Mode	X	H	H	X	X	X	VCC	VCC	XXX	XXX
Byte Access (8 bits)	L	H	L	L	H	L	VCC	VCC	XXX	Even–Byte
	L	H	L	H	H	L	VCC	VCC	XXX	XXX
Word Access (16 bits)	L	L	L	X	H	L	VCC	VCC	XXX	Even–Byte
Odd–Byte Only Access	L	L	H	X	H	L	VCC	VCC	XXX	XXX
Attribute Memory Write Function for OTPROM, EPROM, and FLASH Memory										
MODE	$\overline{RG}$	$\overline{E2}$	$\overline{E1}$	A0	$\overline{G}$	$\overline{W}$	VPP2	VPP1	XXX	DQ7–DQ0
Standby Mode	X	H	H	X	X	X	VCC, VPP	VCC, VPP	XXX	XXX
Byte Access (8 bits)	L	H	L	L	H	L	VCC	VPP	XXX	Even–Byte
	L	H	L	H	H	L	VCC	VCC	XXX	XXX
Word Access (16 bits)	L	L	L	X	H	L	VPP	VPP	XXX	Even–Byte
Odd–Byte Only Access	L	L	H	X	H	L	VPP	VCC	XXX	XXX

NOTE: For those pins in the above tables where "VCC, VPP" is specified, either supply may be used for programming at the option of the manufacturer. However those cards which use VCC must be able to withstand VPP without damage.

Release 3

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PIN #	PIN NAME	PIN #	PIN NAME
1	VSS	37	DQ19
2	DQ0	38	DQ20
3	DQ1	39	VSS
4	DQ2	40	$\overline{CE0}$
5	DQ3	41	NC, A10
6	DQ4	42	NC, A11
7	DQ5	43	NC, $\overline{CE1}$
8	DQ6	44	$\overline{RE0}$
9	DQ7	45	NC, $\overline{RE1}$
10	VDD	46	DQ21
11	PD5	47	$\overline{W}$
12	A0	48	$\overline{ECC}$
13	A1	49	DQ22
14	A2	50	DQ23
15	A3	51	DQ24
16	A4	52	DQ25
17	A5	53	DQ26
18	A6	54	DQ27
19	G	55	DQ29
20	DQ8	56	DQ29
21	DQ9	57	DQ30
22	DQ10	58	DQ31
23	DQ11	59	VDD
24	DQ12	60	DQ32
25	DQ13	61	DQ33
26	DQ14	62	DQ34
27	DQ15	63	DQ35
28	A7	64	DQ36/NC
29	DQ16	65	DQ37/NC
30	VDD	66	DQ38/NC
31	A8	67	PD1
32	A9	68	PD2
33	NC	69	PD3
34	NC	70	PD4
35	DQ26	71	DQ39/NC
36	DQ8	72	VSS

PRESENCE DETECT TRUTH TABLE							
TYPE	tRAC	ECC*	PD1	PD2	PD3	PD4	#PD5
256K X 36 or 40	100 nS	S	S	O	S	S	O
	80 nS	S	S	O	O	S	O
	70 nS	S	S	O	S	O	O
	60 nS	S	S	O	O	O	O
512K X 36 or 40	100 nS	S	O	S	S	S	O
	80 nS	S	O	S	O	S	O
	70 nS	S	O	S	S	O	O
	60 nS	S	O	S	O	O	O
1M X 36 or 40	100 nS	S	S	S	S	S	O
	80 nS	S	S	S	O	S	O
	70 nS	S	S	S	S	O	O
	60 nS	S	S	S	O	O	O
2M X 36 or 40	100 nS	S	O	O	S	S	O
	80 nS	S	O	O	O	S	O
	70 nS	S	O	O	S	O	O
	60 nS	S	O	O	O	O	O
4M X 36 or 40	80 nS	S	S	O	O	S	S
	70 nS	S	S	O	S	O	S
	60 nS	S	S	O	O	O	S
	50 nS	S	S	O	S	S	S
8M X 36 or 40	80 nS	S	O	S	O	S	S
	70 nS	S	O	S	S	O	S
	60 nS	S	O	S	O	O	S
	50 nS	S	O	S	S	S	S

O = OPEN CIRCUIT (NO CONNECTION)
S = CONNECTED TO VSS
*ECC Pin: VSS for ECC Module, OPEN for NON ECC Module
The connection of PD5 to VSS must be made through a 2..6 KΩ resistor

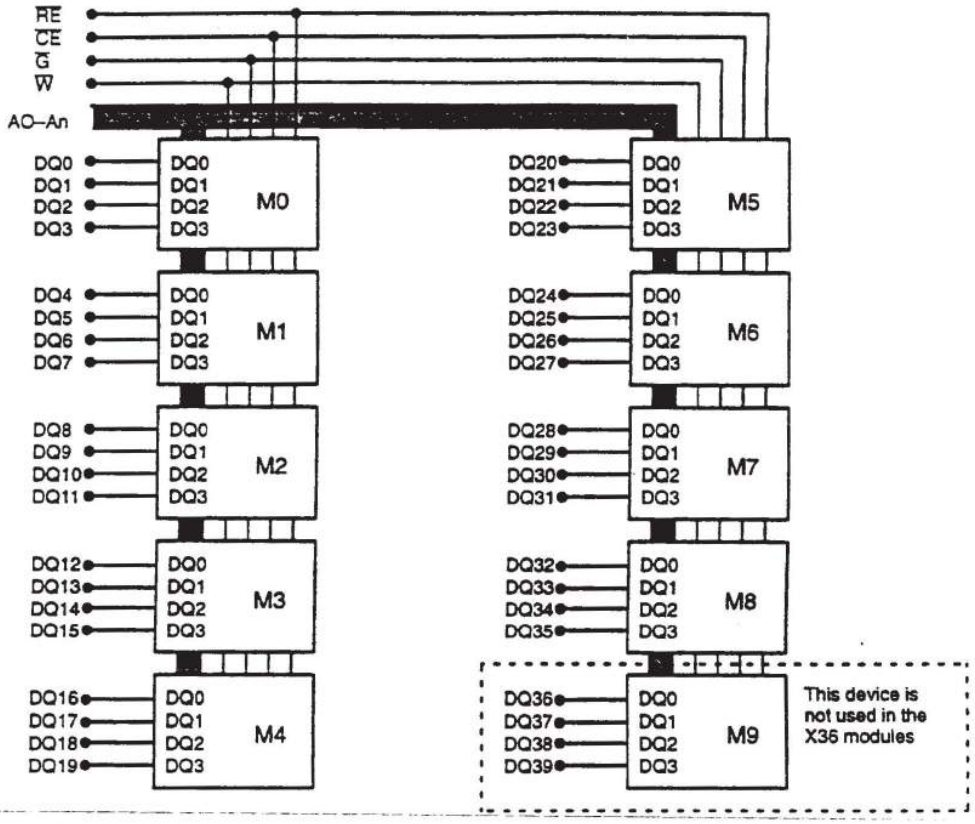
CONFIGURATION PIN ASSIGNMENT TABLE						
	MODULE SIZE, 36 or 40 BIT WORDS					
PIN #	256K	512K	1M	2M	4M	8M
32	NC	NC	A9	A9	A9	A9
41	NC	NC	NC	NC	A10	A10
42	NC	NC	NC	NC	A11	A11
43	NC	$\overline{CE1}$	NC	$\overline{CE1}$	NC	$\overline{CE1}$
45	NC	$\overline{RE1}$	NC	$\overline{RE1}$	NC	$\overline{RE1}$

NOTE – This family of pinouts is approved for use in SIMM modules which are nominally 4.25" long and with a height which varies depencing on the configuration and the memory devices used. See JEDEC Publication 95, section MO-XXX.

FIGURE 4-10A
256K TO 8M BY 36 or 40, 72 PIN ECC DRAM MODULE PINOUT

Release 4

Jedec 0007819

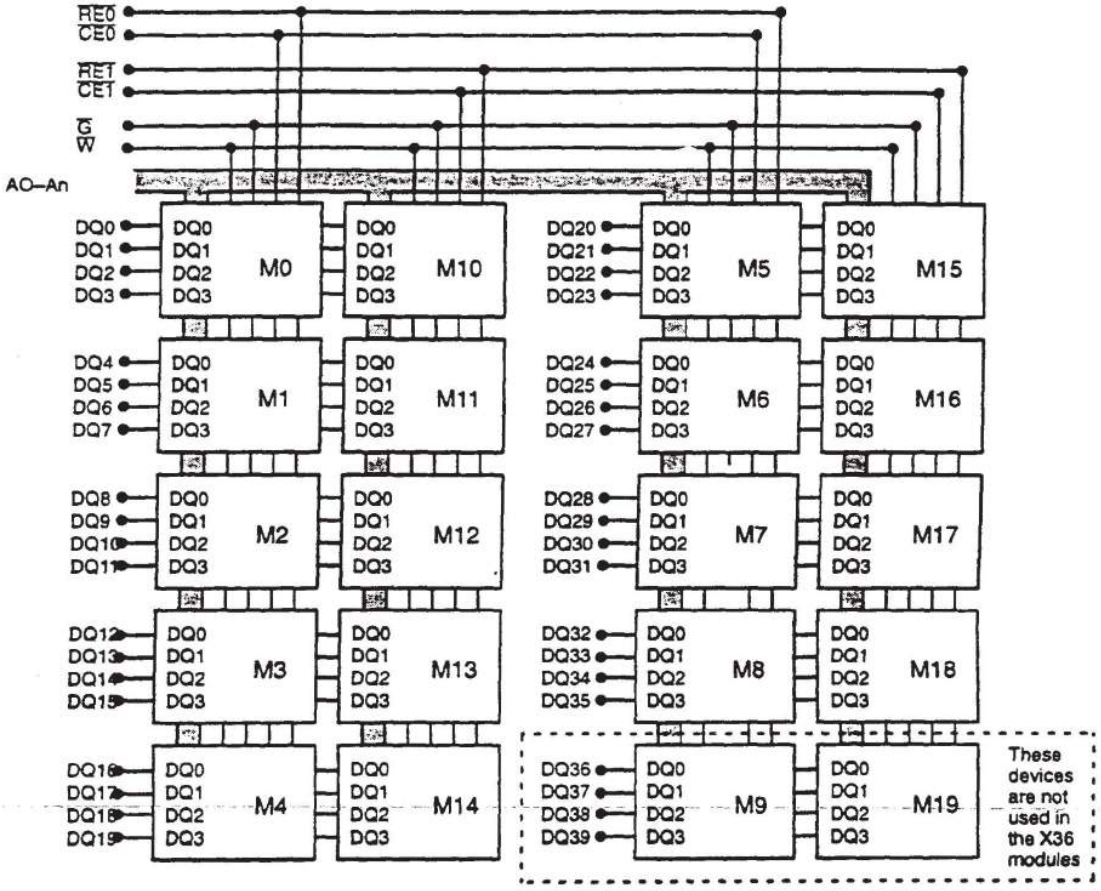


BLOCK DIAGRAM for 256K/1M/4M X 36 or 40 USING X4 DRAM

FIGURE 4–10B

256K TO 8M BY 36 or 40, 72 PIN ECC DRAM MODULE, BLOCK DIAGRAM

Release 4



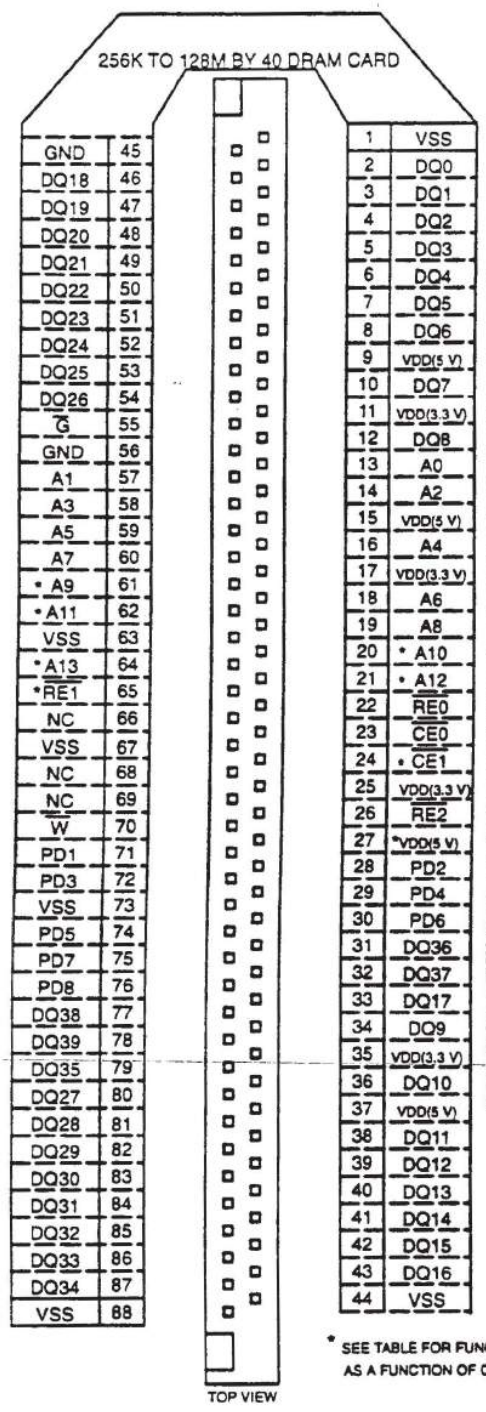
BLOCK DIAGRAM for 512K/2M/8M X 36 or 40 DRAM MODULE

FIGURE 4–10C

256K TO 8M BY 36 or 40, 72 PIN ECC DRAM MODULE BLOCK DIAGRAM

Release 4

Jedec 0007821



Pin Assignment, Cards based on X4 DRAM								
	Card Pin Number							
CONFIGURATION	20	21	24	27	61	62	64	65
256K X 40 (1M)	NC	NC	NC	5 V, NC	NC	NC	NC	NC
512K X 40 (1M)	NC	NC	$\overline{CE1}$	5 V, NC	NC	NC	NC	$\overline{RE1}$
1M X 40 (4M)	NC	NC	NC	5 V, NC	A9	NC	NC	NC
2M X 40 (4M)	NC	NC	$\overline{CE1}$	5 V, NC	A9	NC	NC	$\overline{RE1}$
4M X 40 (16M)	A10	NC	NC	5 V, NC	A9	A11	NC	NC
8M X 40 (16M)	A10	NC	$\overline{CE1}$	5 V, NC	A9	A11	NC	$\overline{RE1}$
16M X 40 (64M)	A10	A12	NC	NC	A9	A11	NC	NC
32M X 40 (64M)	A10	A12	$\overline{CE1}$	NC	A9	A11	NC	$\overline{RE1}$
64M X 40 (256M)	A10	A12	NC	NC	A9	A11	A13	NC
128M X 40 (256M)	A10	A12	$\overline{CE1}$	NC	A9	A11	A13	$\overline{RE1}$

Pin Assignment, Cards based on X8 DRAM								
	Card Pin Number							
CONFIGURATION	20	21	24	27	61	62	64	65
512K X 40 (4M)	NC	NC	NC	5 V, NC	A9	NC	NC	NC
1M X 40 (4M)	NC	NC	$\overline{CE1}$	5 V, NC	A9	NC	NC	$\overline{RE1}$
2M X 40 (16M)	A10	NC	NC	5 V, NC	A9	A11	NC	NC
4M X 40 (16M)	A10	NC	$\overline{CE1}$	5 V, NC	A9	A11	NC	$\overline{RE1}$
8M X 40 (64M)	A10	A12	NC	NC	A9	A11	NC	NC
16M X 40 (64M)	A10	A12	$\overline{CE1}$	NC	A9	A11	NC	$\overline{RE1}$
32M X 40 (256M)	A10	A12	NC	NC	A9	A11	A13	NC
64M X 40 (256M)	A10	A12	$\overline{CE1}$	NC	A9	A11	A13	$\overline{RE1}$

ADDRESS AND CLOCK PIN ASSIGNMENTS

* SEE TABLE FOR FUNCTIONAL ASSIGNMENTS FOR THESE PINS AS A FUNCTION OF CARD CAPACITY AND CONFIGURATION

FIGURE 4–11 A
256K TO 128M BY 40 DRAM CARD

Release 4

	PD7	PD6
SPEED (tRAC)	P 75	P 30
80 nS	VSS	NC
70 nS	NC	VSS
60 nS	NC	NC
50 nS	VSS	VSS

PD SPEED TABLE

	PD8
REFRESH MODE	P 76
80 nS	VSS
70 nS	NC

PD REFRESH MODE TABLE

PD BITS 5 4 3 2 1	CARD DENSITY	DRAM ORGANIZATION	RE ADDR.	CE ADDR.	REFRESH PERIOD (mS) NORMAL	SLOW
1 1 1 1 1	NO CARD					
1 0 0 0 0	1 MB	256K X 4	9	9	8	64
0 0 0 0 0	2 MB	256K X 4	9	9	8	64
1 0 0 0 1	2 MB	512K X 8	10	9	16	128
0 0 0 0 1	4 MB	512K X 8	10	9	16	128
1 0 0 1 0	4 MB	1M X 4	10	10	16	128
0 0 0 1 0	8 MB	1M X 4	10	10	16	128
1 0 0 1 1	8 MB	2M X 8	11	10	32	256
0 0 0 1 1	16 MB	2M X 8	11	10	32	256
1 0 1 0 0	16 MB	4M X 4	11/12	11/10	64	256
0 0 1 0 0	32 MB	4M X 4	11/12	11/10	64	256
1 0 1 0 1	32 MB	8M X 8	12/13	11/10	TBD	TBD
0 0 1 0 1	64 MB	8M X 8	12/13	11/10	TBD	TBD
1 0 1 1 0	64 MB	16M X 4	13	11	TBD	TBD
0 0 1 1 0	128 MB	16M X 4	13	11	TBD	TBD
1 0 1 0 1	128 MB	32M X 8	TBD	TBD	TBD	TBD
0 0 1 0 1	256 MB	32M X 8	TBD	TBD	TBD	TBD
1 0 1 1 0	256 MB	64M X 4	TBD	TBD	TBD	TBD
0 0 1 1 0	512 MB	64M X 4	TBD	TBD	TBD	TBD

FOR THE PDn PINS, 1 = NC, 0 = VSS
NOTE: In the above address table, optional address configurations are given for some devices to allow for different approved refresh counts.

MEMORY CARD ORGANIZATION AND ADDRESS STRUCTURE

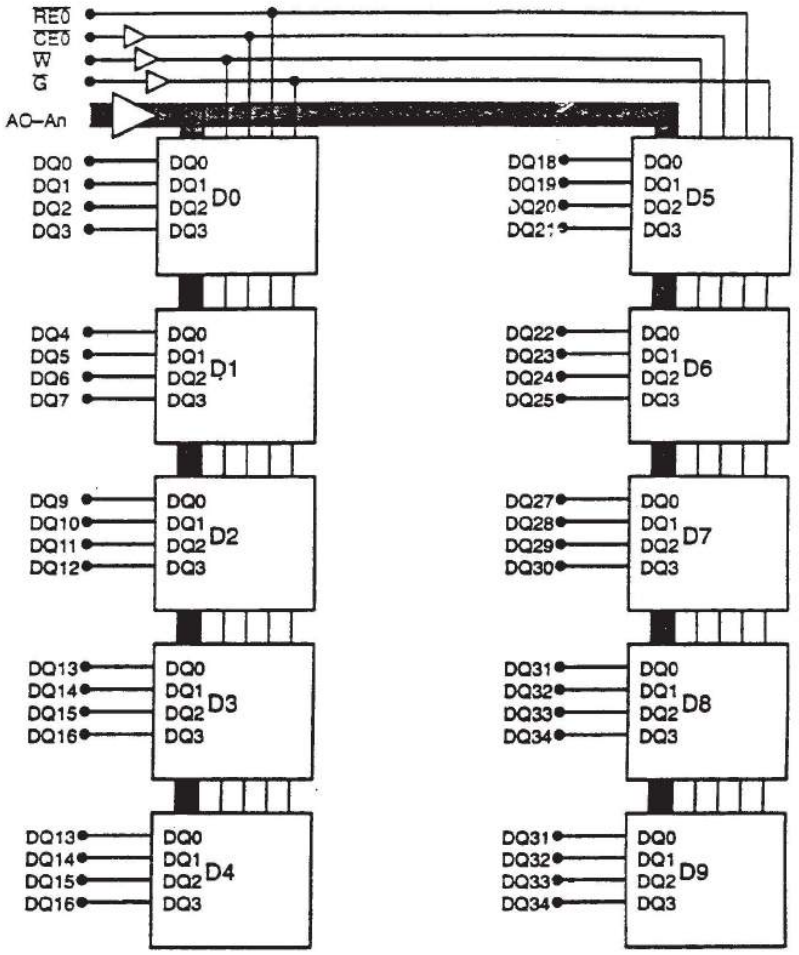
NOTE: The DRAM densities are shown in parentheses (xxxM)

FIGURE 4–11 B
256K TO 128M BY 40 DRAM CARD PD TRUTH TABLE

Release 4

Jedec 0007823

BLOCK DIAGRAM for 256K/1M/4M/16M/64M X 40 USING X4 DRAM



WORD ORGANIZATION	*Base Memory Device D0 to D9	ADDRESS FIELD	OPTIONAL ADDRESS
256K X 40	1M (X4)	A0 – A8	NA
1M X 40	4M (X8)	A0 – A9	NA
4M X 40	16M (X8)	A0 – A10	A0–A11
16M X 40	64M (X8)	A0 – A11	A0–A12
64M X 40	256M (X8)	TBD	TBD

* NOTE: The BASE MEMORY DEVICE columns give the total device capacity in bits and the data interface word width.

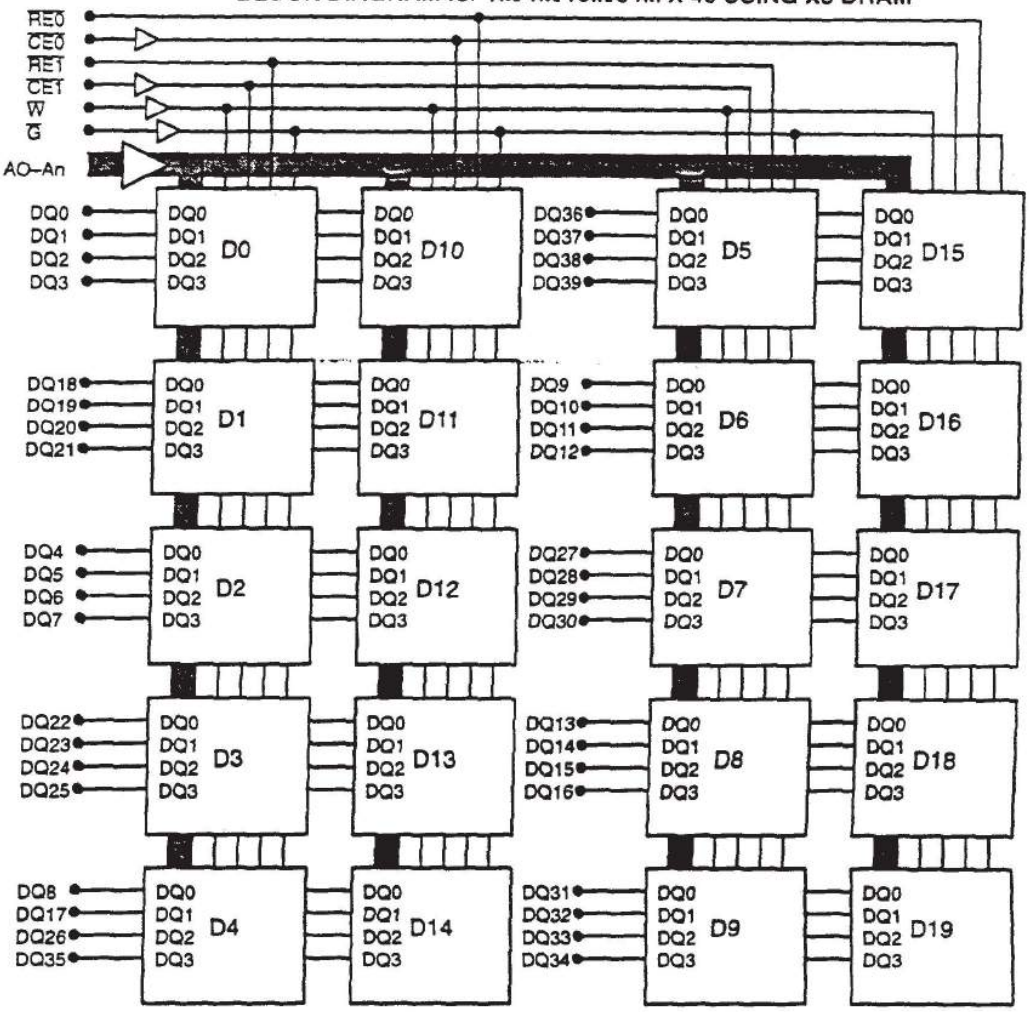
NOTE: There shall be one bypass capacitor between VDD and VSS fore each memory device on the card.

FIGURE 4–11 C

256K TO 64M BY 40 DRAM CARDUSING BY 4 DEVICES

Release 4

BLOCK DIAGRAM for 1M/4M/16M/64M X 40 USING X8 DRAM



WORD ORGANIZATION	*Base Memory Device D0 to D19	ADDRESS FIELD	OPTIONAL ADDRESS
512K X 40	1M (X4)	A0 – A8	NA
2M X 40	4M (X8)	A0 – A9	NA
8M X 40	16M (X8)	A0 – A10	A0–A11
32M X 40	64M (X8)	A0 – A11	A0–A12
128M X 40	256M (X8)	TBD	TBD

* NOTE: The BASE MEMORY DEVICE columns give the total device capacity in bits and the data interface word width.

NOTE: There shall be one bypass capacitor between VDD and VSS fore each pair of memory devices on the card. The value of the capacitors will be determined by the memory devices used.

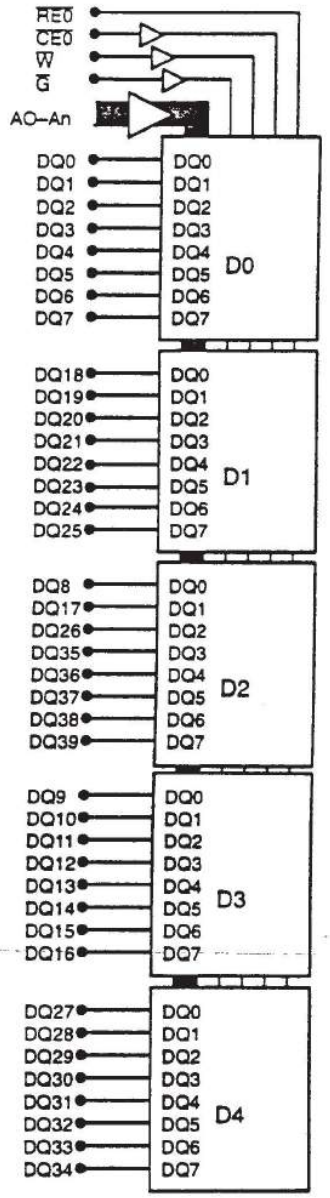
FIGURE 4–11 D

512K TO 128M BY 40 DRAM CARD USING BY 4 DEVICES

Release 4

Jedec 0007825

BLOCK DIAGRAM for 512K/2M/8M/32M X 40 USING X8 DRAM



WORD ORGANIZATION	*Base Memory Device D0 to D4	ADDRESS FIELD
512K X 40	4M (X8)	A0 – A9
2M X 40	16M (X8)	A0 – A10
8M X 40	8M (X8)	A0 – A11
32M X 40	32M (X8)	TBD

* NOTE: The BASE MEMORY DEVICE columns give the total device capacity in bits and the data interface word width.

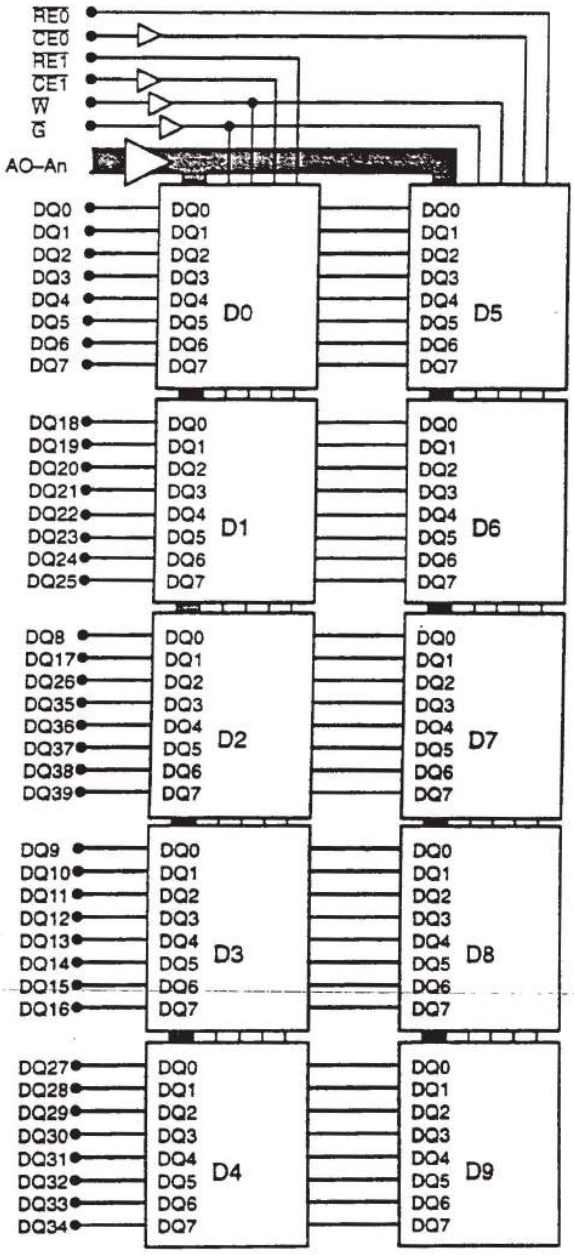
NOTE: There shall be one bypass capacitor between VDD and VSS fore each memory device on the card. The value of the capacitors will be determined by the memory devices used.

FIGURE 4–11 E

512K TO 32M BY 40 DRAM CARD USING BY 8 DEVICES

Release 4

BLOCK DIAGRAM for 1M/4M/16M/64M X 40 USING X8 DRAM



WORD ORGANIZATION	*Base Memory Device D0 to D9	ADDRESS FIELD
1M X 40	4M (X8)	A0 – A9
4M X 40	16M (X8)	A0 – A10
16M X 40	64M (X8)	A0 – A11
64M X 40	256M (X8)	TBD

* NOTE: The BASE MEMORY DEVICE columns give the total device capacity in bits and the data interface word width.

NOTE: There shall be one bypass capacitor between VDD and VSS fore each pair of memory devices on the card. The value of the capacitors will be determined by the memory devices used.

FIGURE 4–11 F
1M TO 64M BY 40 DRAM CARD USING BY 8 DEVICES

Release 4

Jedec 0007827

PIN #	PIN NAME	PIN #	PIN NAME
1	VSS	41	A11
2	VDD	42	A10
3	VPP/NC	43	A9
4	$\overline{G}$	44	A8
5	$\overline{W0}$	45	A7
6	$\overline{W1}$	46	A6
7	RFU	47	A5
8	DQ16	48	A4
9	DQ17	49	A3
10	DQ18	50	A2
11	DQ19	51	A1
12	DQ20	52	A0
13	DQ21	53	$\overline{W3}$
14	DQ22	54	VSS
15	DQ23	55	DQ15
16	DQ24	56	DQ14
17	DQ25	57	DQ13
18	DQ26	58	DQ12
19	DQ27	59	DQ11
20	DQ28	60	DQ10
21	$\overline{E3}$	61	DQ9
22	$\overline{E2}$	62	DQ8
23	$\overline{E1}$	63	DQ7
24	$\overline{E0}$	64	DQ6
25	VSS	65	DQ5
26	DQ29	66	DQ4
27	DQ30	67	DQ3
28	DQ31	68	DQ2
29	$\overline{W2}$	69	DQ1
30	A22	70	DQ0
31	A21	71	VPP/NC
32	A20	72	VDD
33	A19	73	PD1
34	A18	74	PD2
35	A17	75	PD3
36	A16	76	PD4
37	A15	77	PD5
38	A14	78	PD6
39	A13	79	PD7
40	A12	80	VSS

PRESENCE DETECT TRUTH TABLE							
Module Organization	Device Density	# of Dev	Module Capacity	PD1	PD2	PD3	PD4
No Module				1	1	1	1
.128K X 32	1M	4	512KB	0	1	1	1
256K X 32	1M	8	1MB	1	0	1	1
512K X 32	1M	16	2MB	0	0	1	1
256K X 32	2M	4	1MB	1	1	0	1
512K X 32	2M	8	2MB	0	1	0	1
1M X 32	2M	16	4MB	1	0	0	1
512K X 32	4M	4	2MB	0	0	0	1
1M X 32	4M	8	4MB	1	1	1	0
2M X 32	4M	16	8MB	0	1	1	0
1M X 32	8M	4	4MB	1	0	1	0
2M X 32	8M	8	8MB	0	0	1	0
4M X 32	8M	16	16MB	1	1	0	0
2M X 32	16M	4	8MB	0	1	0	0
4M X 32	16M	8	16MB	1	0	0	0
8M X 32	16M	16	32MB	0	0	0	0

1 = OPEN CIRCUIT (NO CONNECTION)
0 = CONNECTED TO VSS

MODULE SPEED IDENTIFICATION			
MAX ACCESS TIME	PRESENCE DETECT PIN		
	PD5	PD6	PD7
NOT DEFINED	1	1	1
45 nS	0	1	1
55 nS	1	0	1
70 nS	0	0	1
90 nS	1	1	0
120 nS	0	1	0
150 nS	1	0	0
200 nS	0	0	0

NOTE – This family of pinouts is approved for use in SIMM package that is nominally 4.65" long and a height of 0.85" See JEDEC Publication 95, section MO–XXX.

FIGURE 4–12 A
128K TO 8M BY 32 EEPROM SIMM, PINOUT AND PD TABLES

Release 4

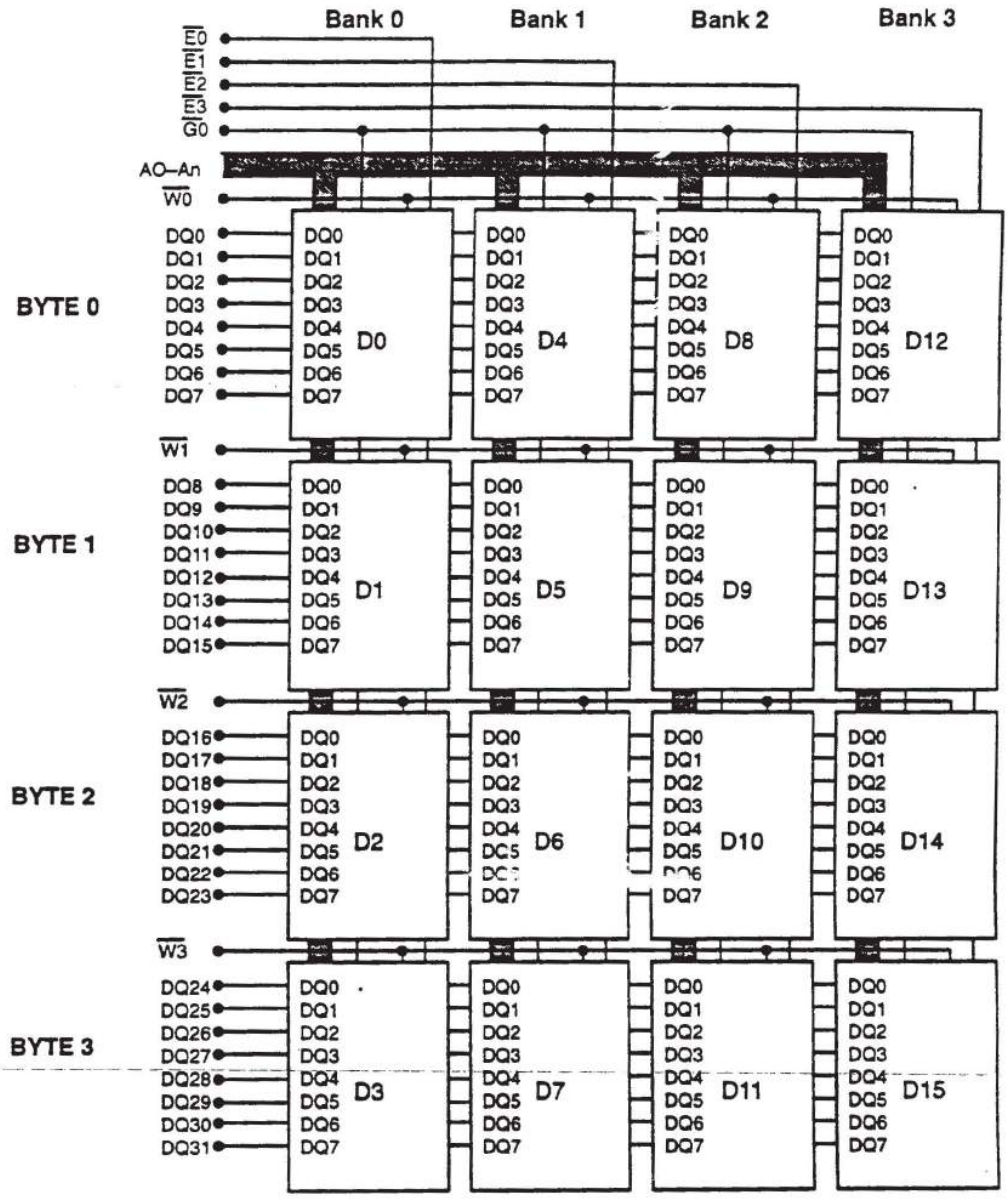


FIGURE 4–12 B
128K TO 8M BY 32 EEPROM SIMM BLOCK DIAGRAM

Release 4

Jedec 0007829

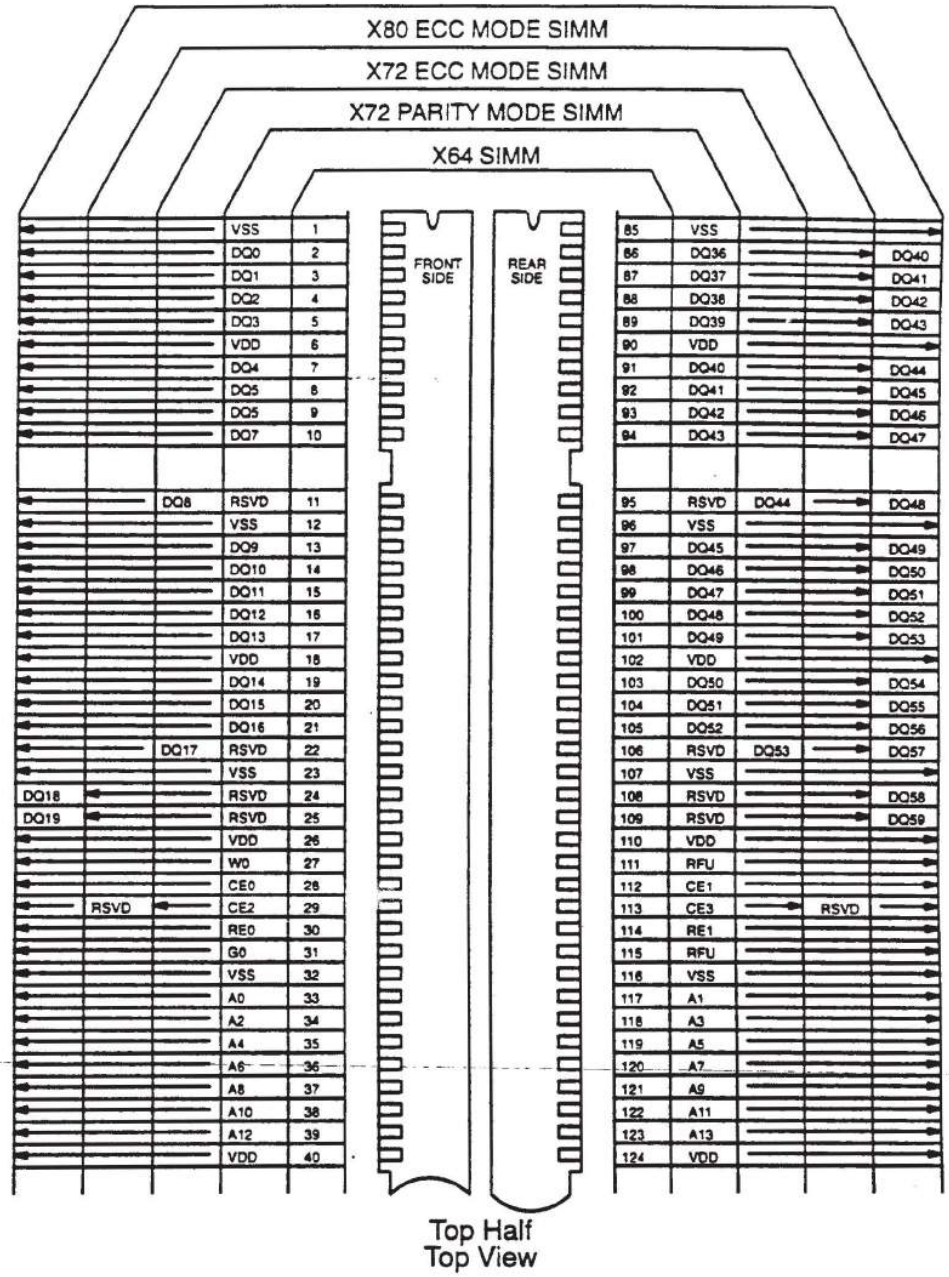


FIGURE 4–13 A
64, 72, or 80 BIT SIMM PINOUT, TOP HALF

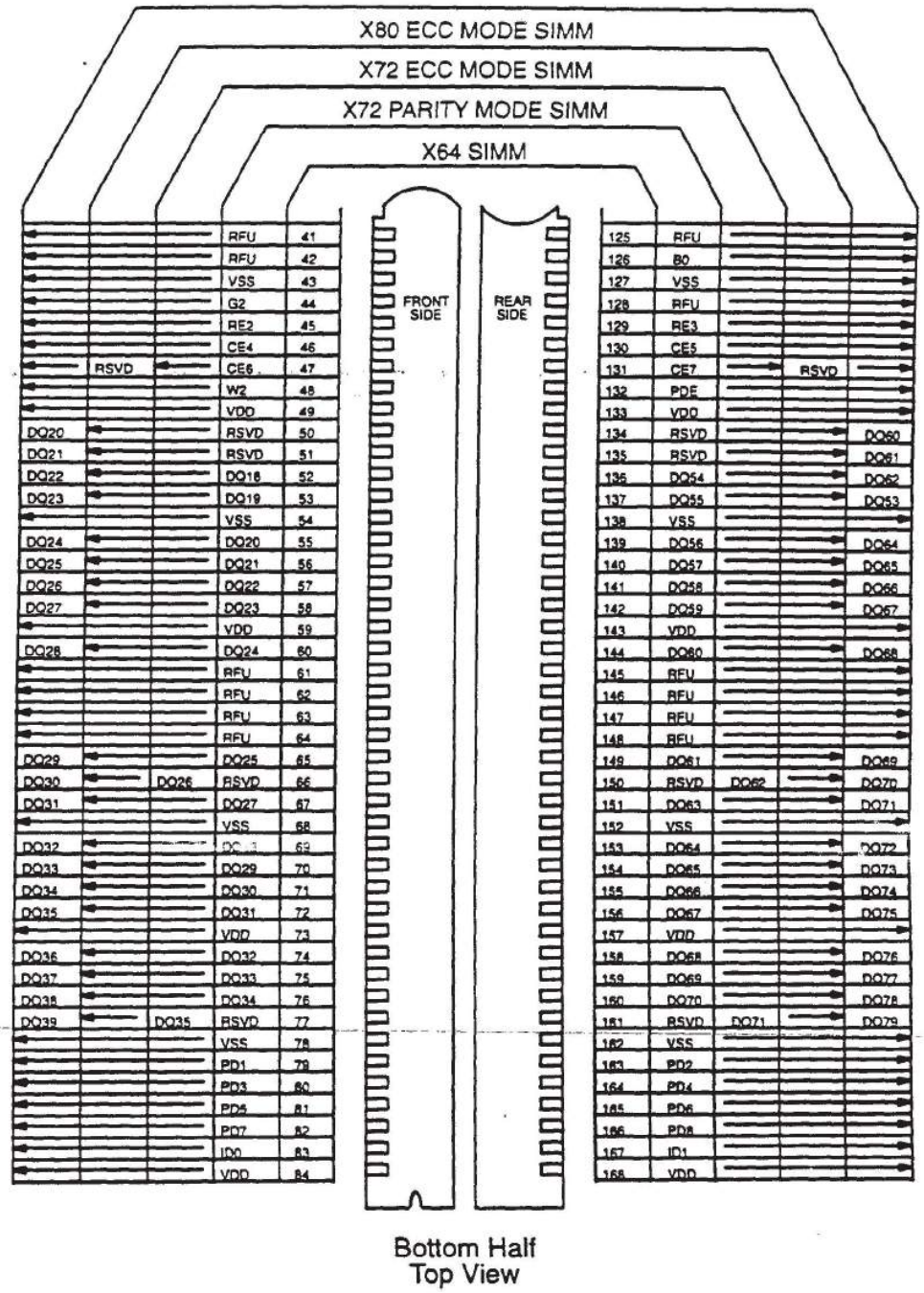


FIGURE 4–13 B
64, 72, or 80 BIT SIMM PINOUT, BOTTOM HALF

Release 4

PD BITS 5 4 3 2 1	MODULE CONFIGURATION (PARITY, ECC)	DRAM ORGANIZATION	RE ADDR.	CE ADDR.	REFRESH PERIOD (mS) NORMAL	SLOW
1 1 1 1 1	NO MODULE					
0 0 0 0 0	256K X 64/72, 72	256K X 16/18	9	9	8	64
0 0 0 0 1	512K X 64/72, 72	256K X 16/18	9	9	8	64
0 0 0 1 0	512K X 64/72, 72/80	512K X 8/9	10	9	16	128
0 0 0 1 1	1M X 64/72, 72/80	512K X 8/9	10	9	16	128
0 0 1 0 0	1M X 64/72, 72/80	1M X 1/4/16/18	10	10	16	128
0 0 1 0 1	2M X 64/72, 72/80	1M X 1/4/16/18	10	10	16	128
0 0 1 1 0	1M X 64/72, 72	1M X 16/18	12	8	64	256
0 1 0 0 0	2M X 64/72, 72	1M X 16/18	12	8	64	256
0 1 0 0 1	2M X 64/72, 72/80	2M X 8/9	11	10	32	256
0 1 0 1 0	4M X 64/72, 72/80	2M X 8/9	11	10	32	256
0 1 0 1 1	4M X 72	4M X 1/4/18	12**	11**	64	256
0 1 0 1 1	4M X 64, 72/80	4M X 4/16	12	10	64	256
0 1 1 0 0	8M X 64/72, 72	4M X 16/18	12	10	64	256
0 1 1 0 1	8M X 64/72, 72/80	8M X 8/9	12	11	64	256
0 1 1 1 0	16M X 64/72, 72/80	8M X 8/9	12	11	64	256
0 1 1 1 1	16M X 64/72, 72/80	16M X 4	13	11	128	512
1 0 0 0 0	16M X 72, 72	16M X 16/18	TBD*	TBD*	TBD*	TBD*
1 0 0 0 1	32M X 72, 72	16M X 16/18	TBD*	TBD*	TBD*	TBD*
1 0 0 1 0	32M X 64/72, 72/80	32M X 8/9	TBD*	TBD*	TBD*	TBD*
1 0 0 1 1	64M X 64/72, 72/80	32M X 8/9	TBD*	TBD*	TBD*	TBD*
1 0 1 0 0	64M X 64, 72/80	64M X 4	TBD*	TBD*	TBD*	TBD*
X 0 1 1 1	Expansion					TBD

Note 1) * These modules using 256M devices are for reference only and will be further defined in the future.
Note 2) 1 = NC or driven to VOH; 0 = VSS or driven to VOL.
Note 3) ** This addressing includes a redundant address to allow mixing of 12/10(X4) and 11/11(X1) DRAMs
PD Note: PD & ID terminals must each be pulled up through a resistor to VDD at the next higher level assembly. PDs will either be open (NC) or driven to VSS via on–board buffer circuits.
ID Note: IDs will either be open (NC) or connected directly to VSS without a buffer.

	PD7	PD6
SPEED (tRAC)	165	82
80 nS	0	1
70 nS	1	0
60 nS	1	1
50 nS	0	0
PD SPEED TABLE		

	PD8	ID0
CONFIGURATION	166	83
X64	1	0
X72 PARITY	1	1
X72 ECC	0	0
X80 ECC	0	1
DATA CONFIGURATION		

	ID1
REFRESH MODE	166
NORMAL	0
SELF–REFRESH	1
REFRESH MODE	

FIGURE 4–13 C

64, 72, or 80 BIT SIMM PRESENCE DETECT & CONFIGURATION TABLES

Release 4

64, 72, & 80 BIT DRAM SIMM CAPACITY IN M BYTE																				
Memory Device / SIMM Configuration	4M DRAM					16M DRAM					64M DRAM					256M DRAM				
	256K		512K		1M	1M		2M		4M	4M		8M		16M	16M		32M		64M
	X18	X16	X9	X8	X4	X18	X16	X9	X8	X4	X18	X16	X9	X8	X4	X18	X16	X9	X8	X4
256K X 64		4																		
256K X 72	4																			
256K X 72 (ECC)	4																			
256K X 80 (ECC)																				
512 X 64		8		8																
512K X 72	8		8																	
512K X 72 (ECC)	8		8	9																
512K X 80 (ECC)				10																
1M X 64				16	16		4													
1M X 72			16		18	4														
1M X 72 (ECC)			16	18	18	4														
1M X 80 (ECC)				20	20															
2M X 64							8		8											
2M X 72						8		8												
2M X 72 (ECC)						8		8	9											
2M X 80 (ECC)									10											
4M X 64									16	16		4								
4M X 72								16		18	4									
4M X 72 (ECC)								16	18	18	4									
4M X 80 (ECC)									20	20										
8M X 64												8		8						
8M X 72											8		8							
8M X 72 (ECC)											8		8	9						
8M X 80 (ECC)														10						
16M X 64														16	16		4			
16M X 72													16		18	4				
16M X 72 (ECC)													16	18	18	4				
16M X 80 (ECC)														20	20					
32M X 64																	8		8	
32M X 72																8		8		
32M X 72 (ECC)																8		8	9	
32M X 80 (ECC)																			10	
64M X 64																			16	16
64M X 72																		16		18
64M X 72 (ECC)																		16	18	18
64M X 80 (ECC)																			20	20

FIGURE 4–13 D
64, 72, & 80 BIT DRAM SIMM Capacity Table

Release 4

Jedec 0007833

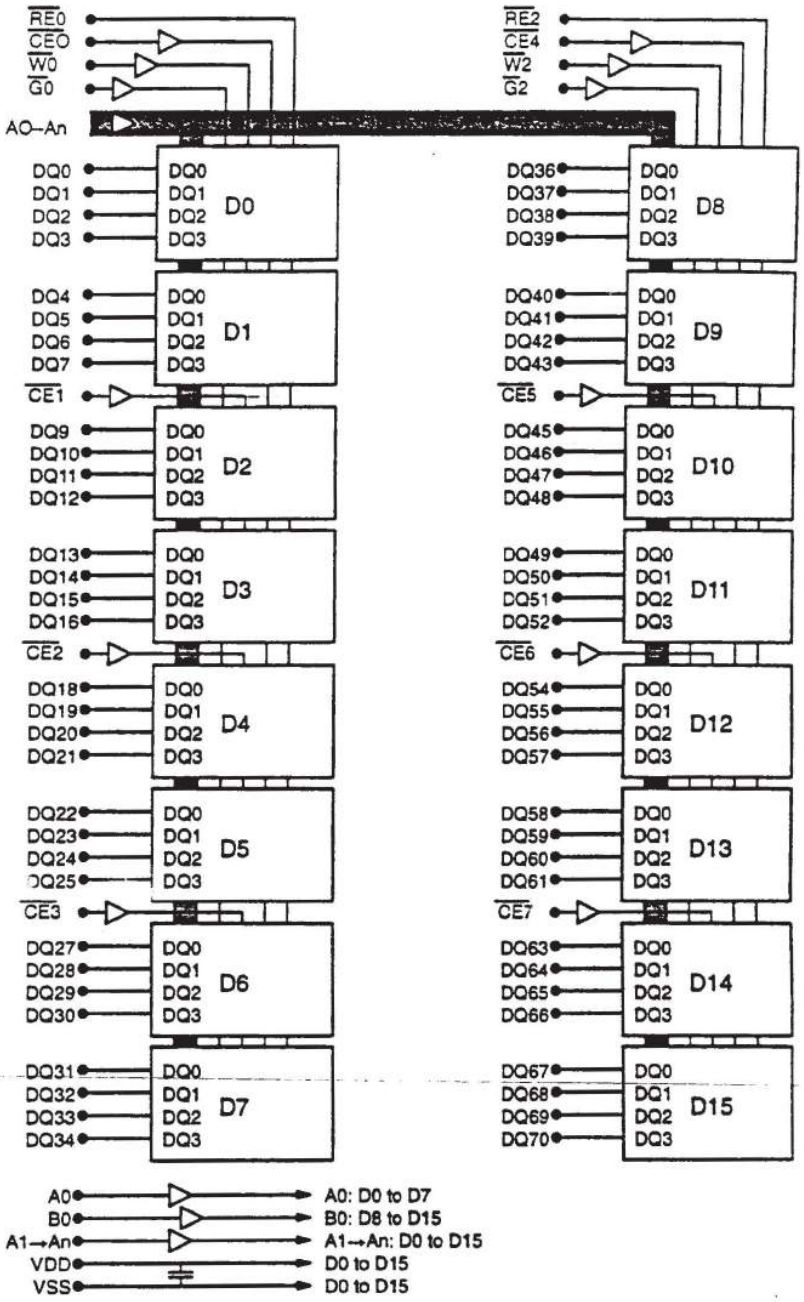


FIGURE 4–13 E

X64 DRAM SIMM, 1 bank with X4 DRAMs

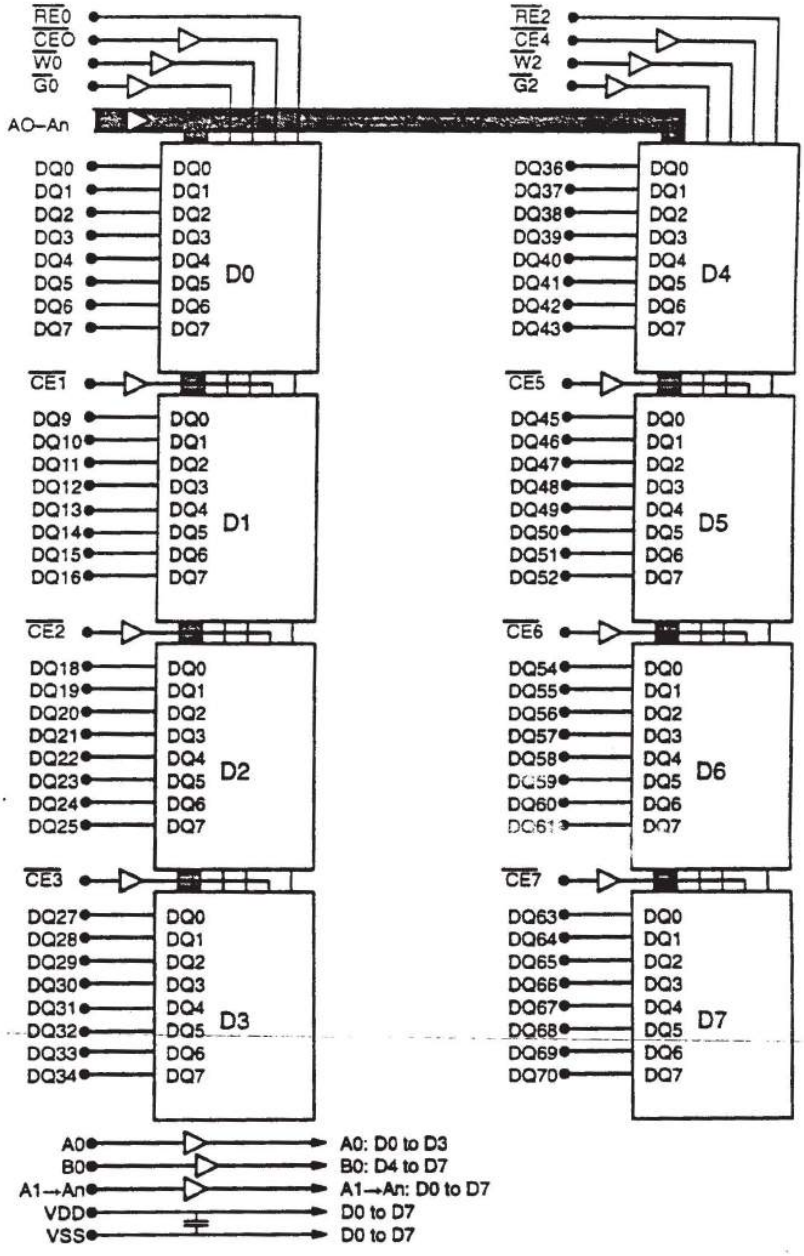


FIGURE 4–13 F
X64 DRAM SIMM, 1 bank with X8 DRAMs

Release 4

Jedec 0007835

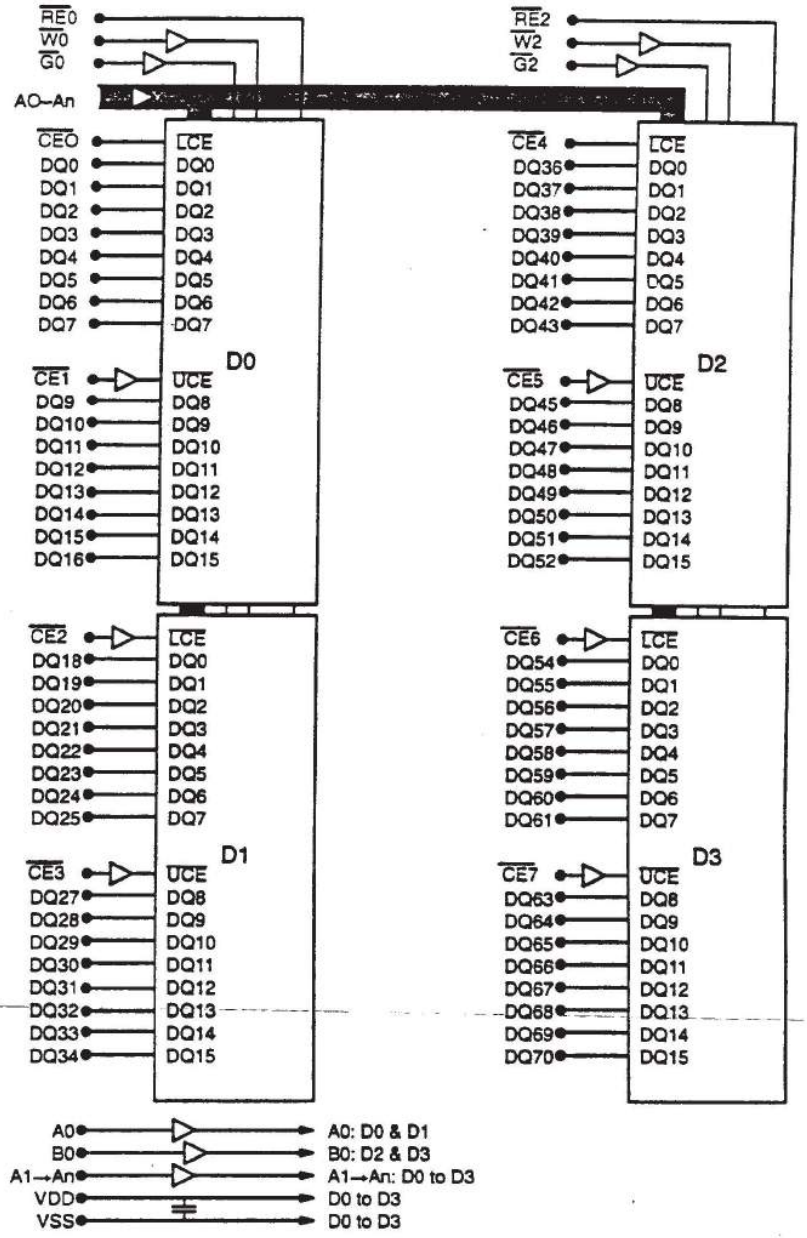


FIGURE 4–13 G

X64 DRAM SIMM, 1 bank with X16 DRAMs

Release 4

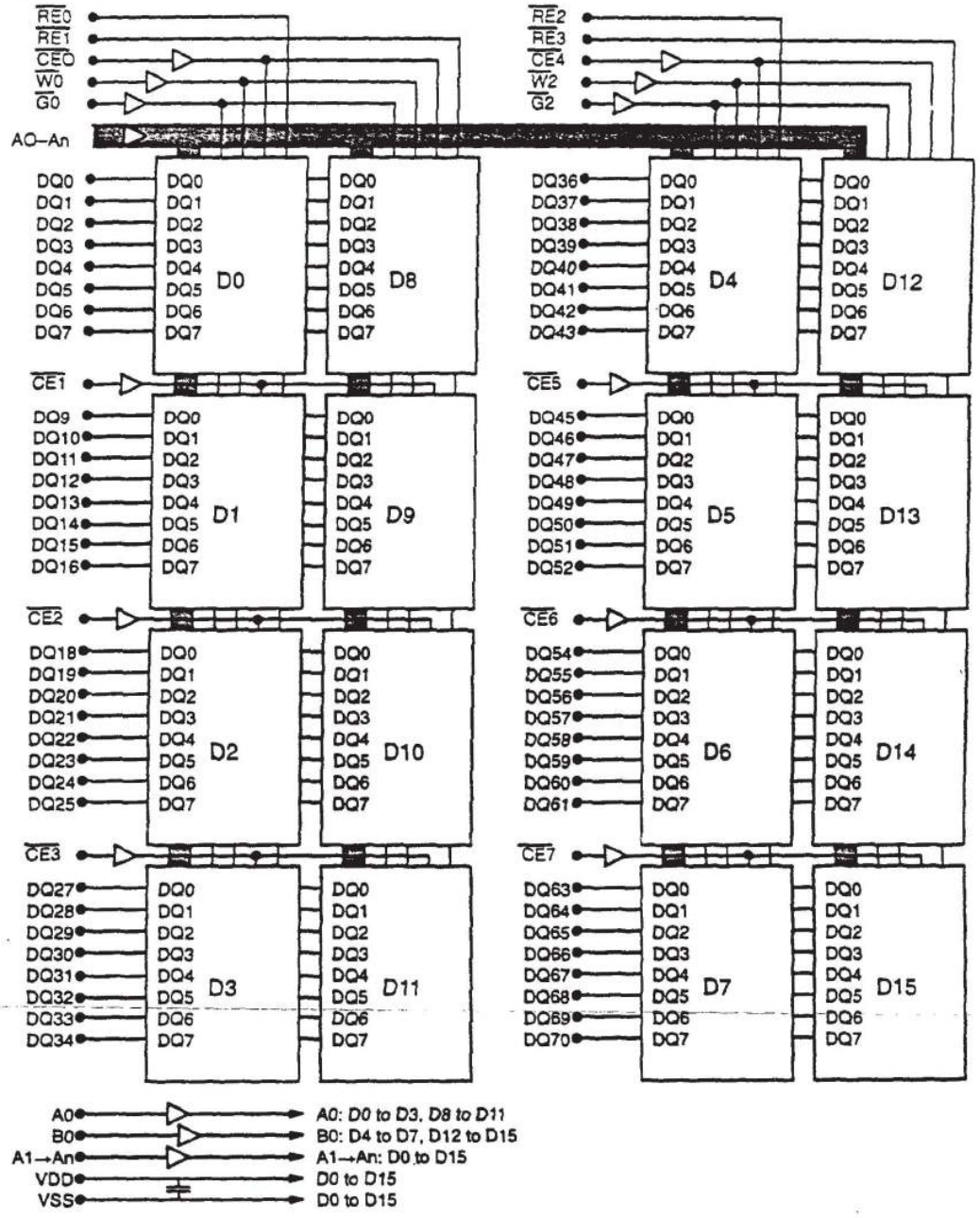


FIGURE 4–13 H
X64 DRAM SIMM, 2 banks with X8 DRAMs

Release 4

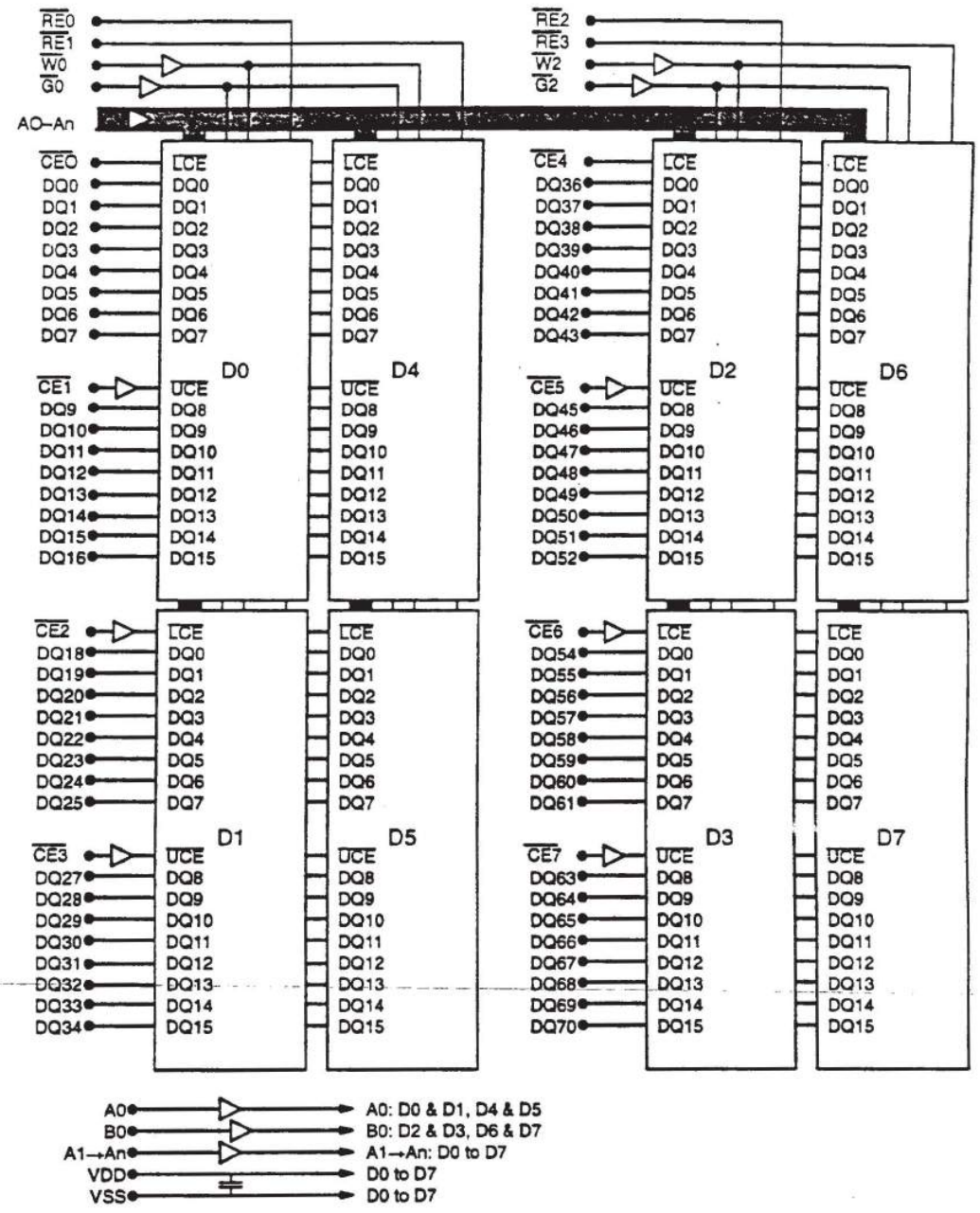


FIGURE 4–13 I

X64 DRAM SIMM, 2 banks with X16 DRAMs

Release 4

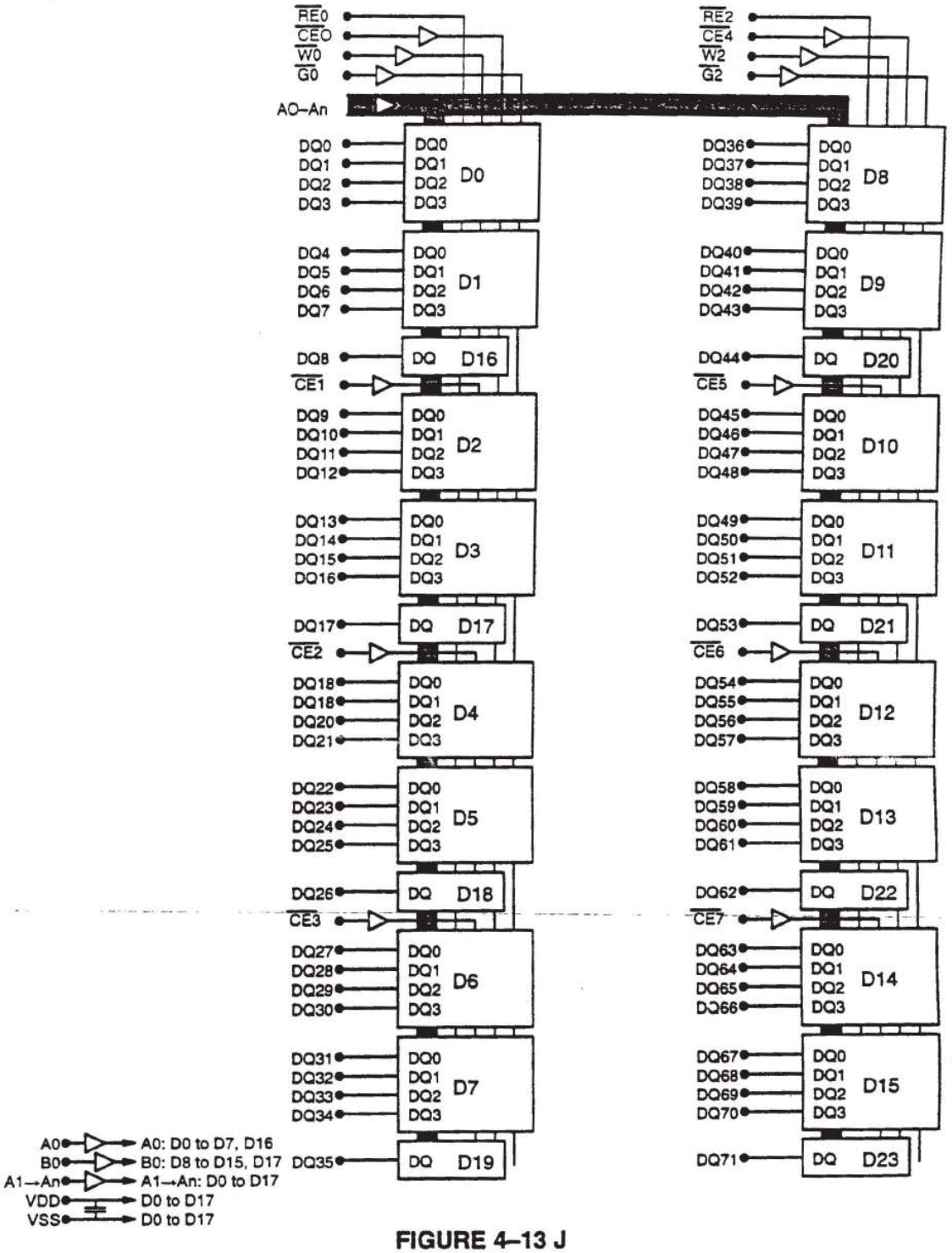


FIGURE 4–13 J

X72 (Parity mode) DRAM SIMM, 1 bank with X4 & X1 DRAMs

Release 4

Jedec 0007839

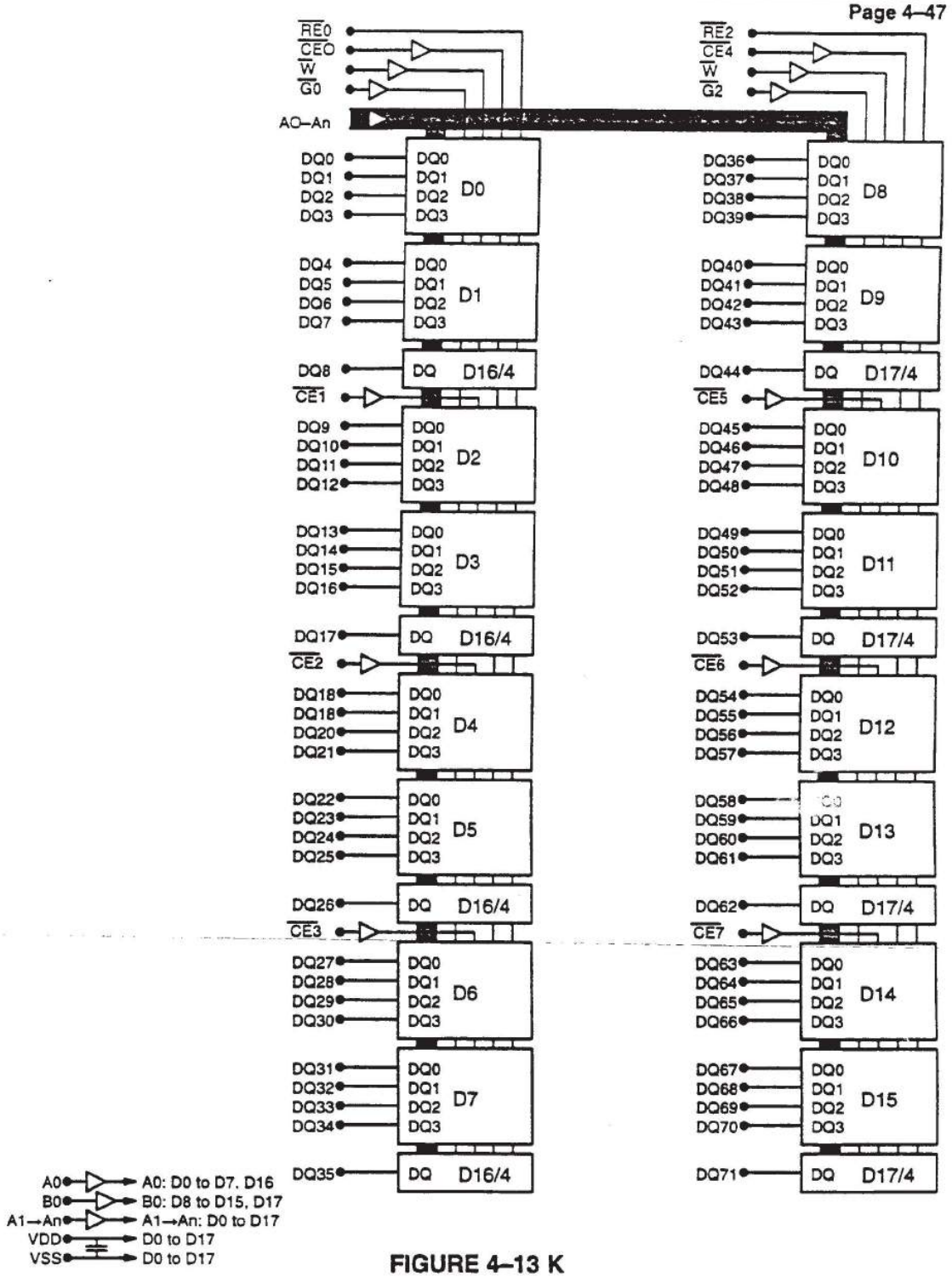


FIGURE 4–13 K

X72 (Parity mode) DRAM SIMM, 1 bank with X4 & X4 W/4 $\overline{CE}$ DRAMs

Release 4

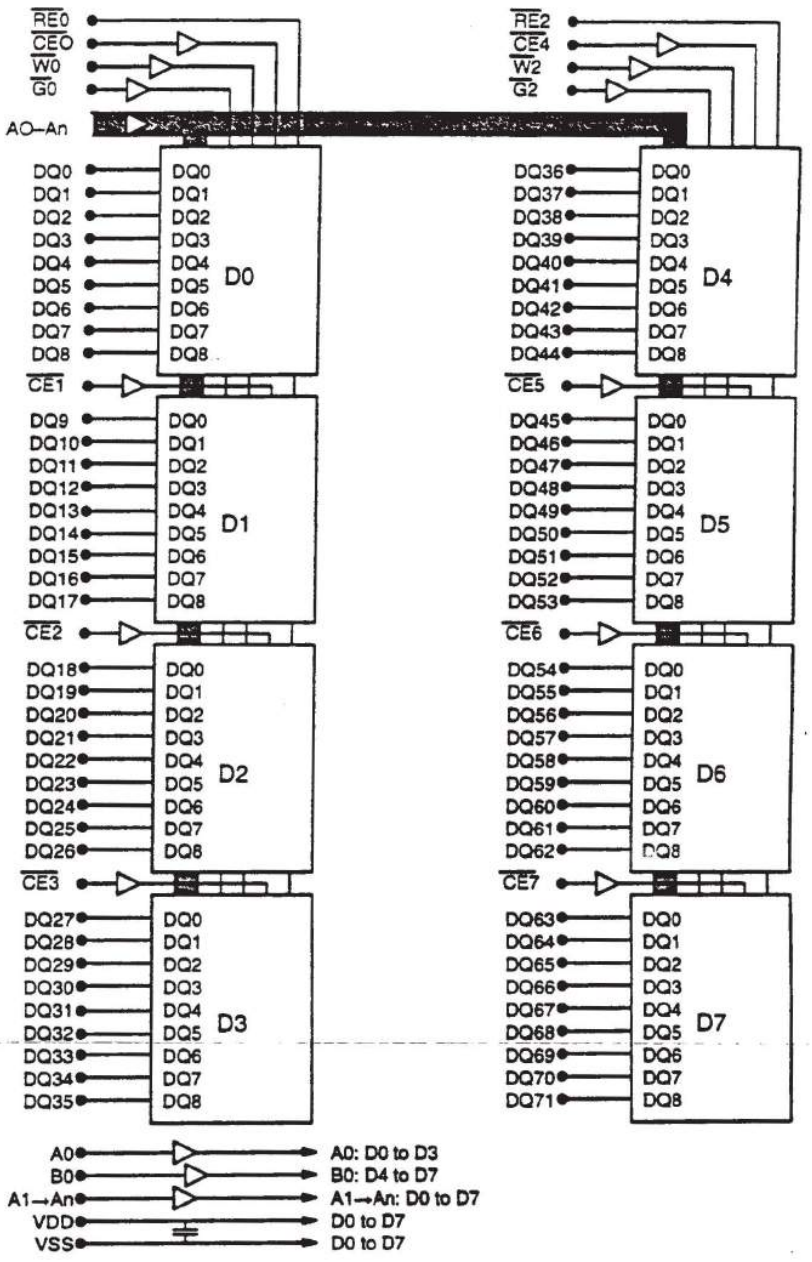


FIGURE 4–13 L
X72 (Parity mode) DRAM SIMM, 1 bank with X9 DRAMs

Release 4

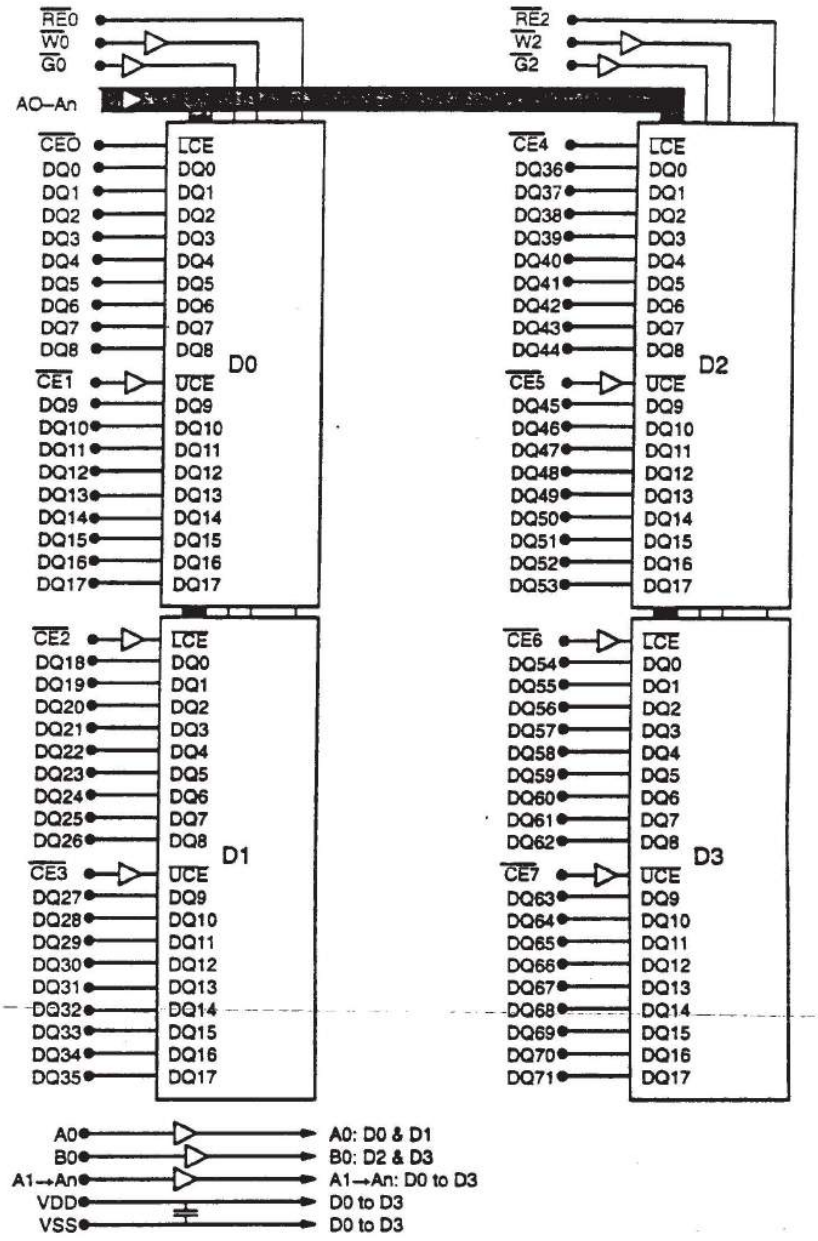


FIGURE 4–13 M

X72 (Parity mode) DRAM SIMM, 1 bank with X18 DRAMs

Release 4

Jedec 0007842

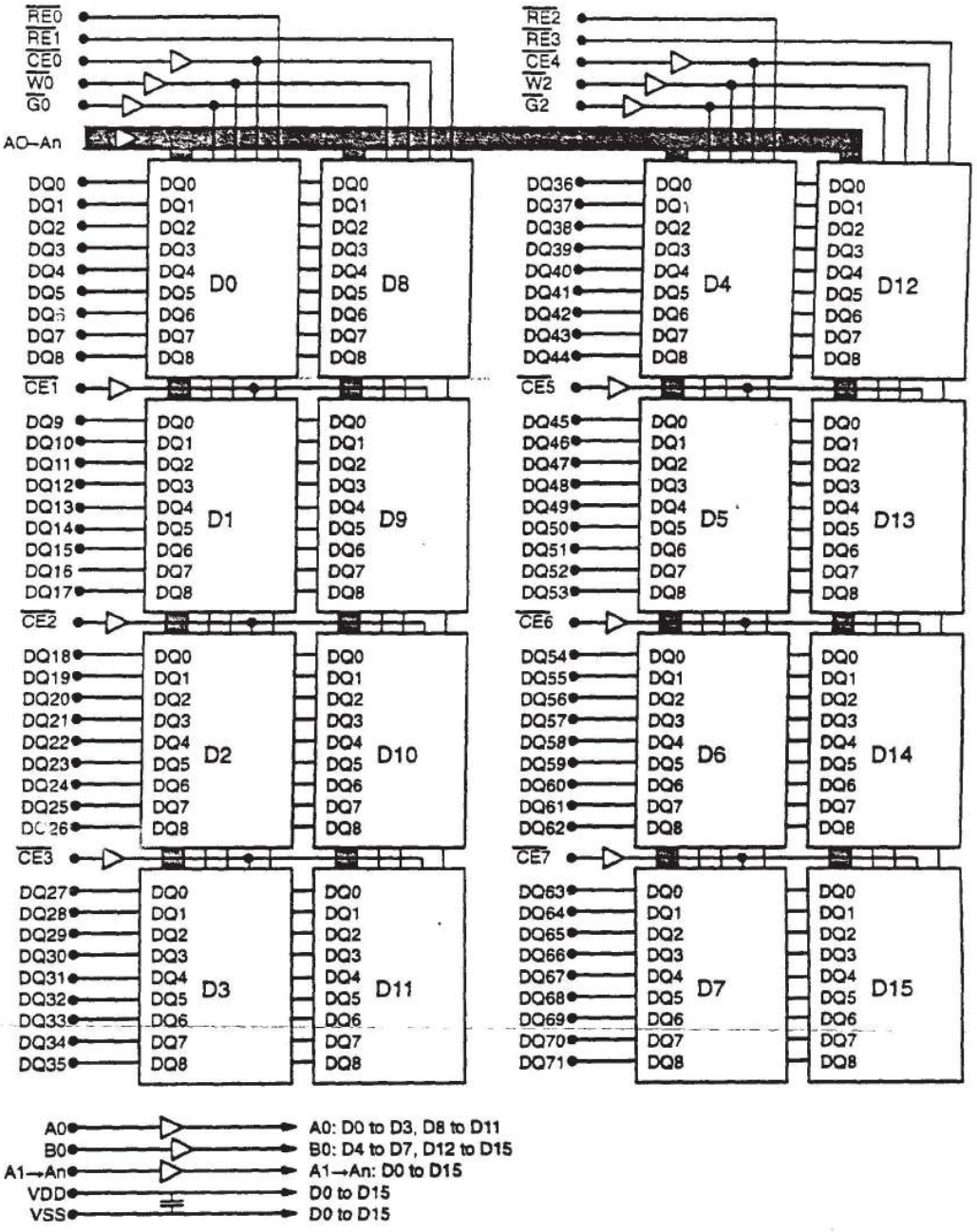


FIGURE 4–13 N

X72 (Parity mode) DRAM SIMM, 2 banks with X9 DRAMs

Release 4

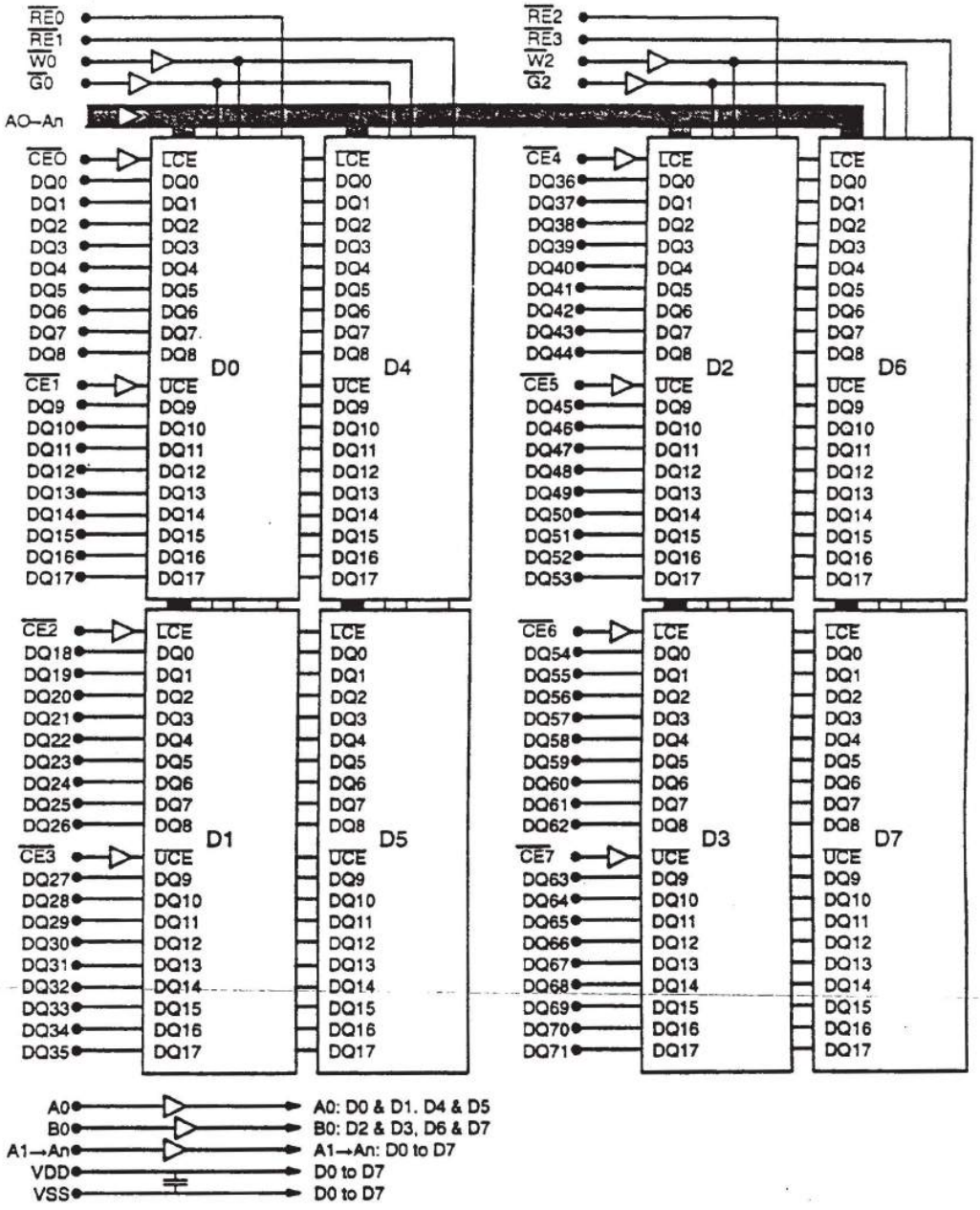


FIGURE 4–13 O

X72 (Parity mode) DRAM SIMM, 2 bank with X18 DRAMs

Release 4

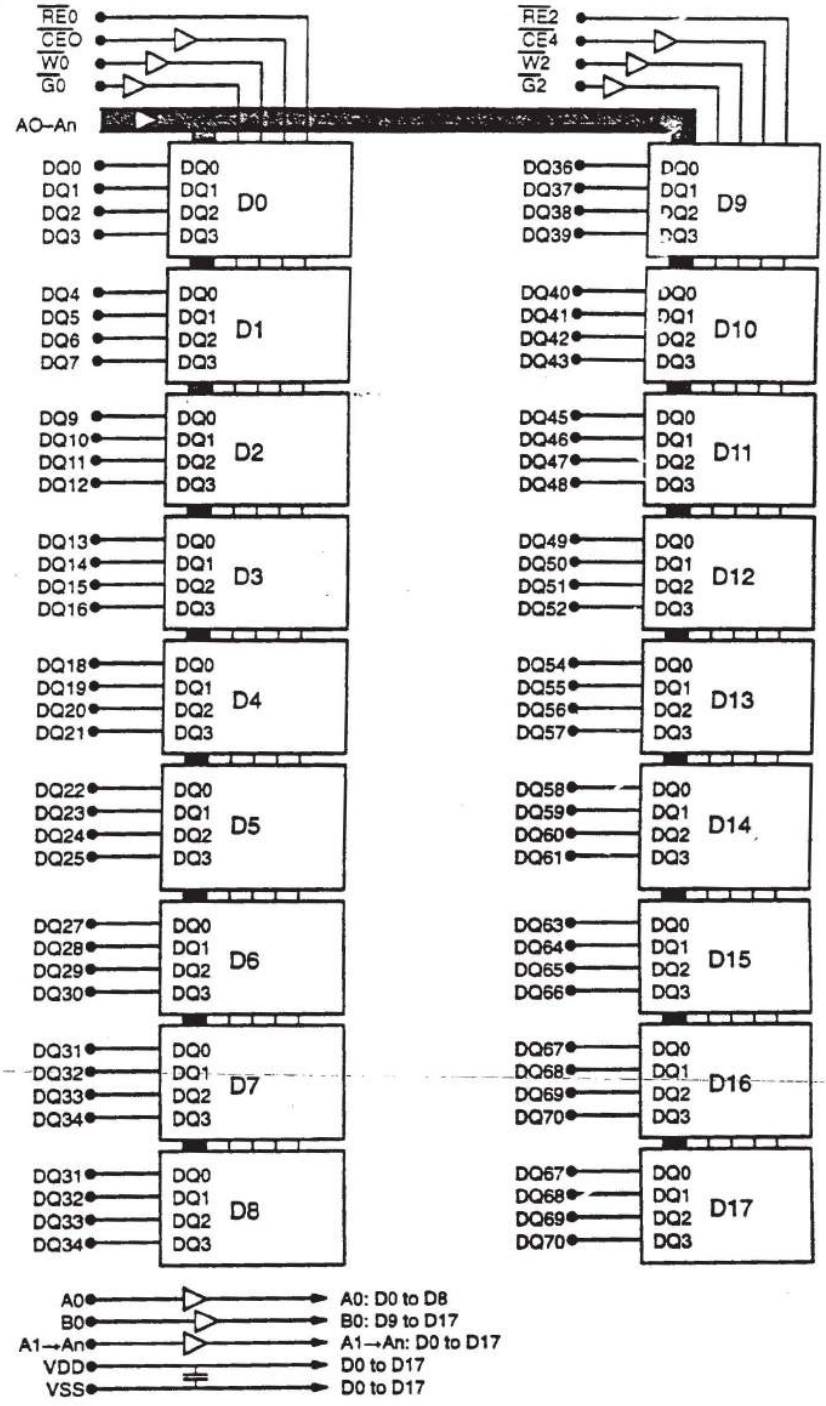


FIGURE 4–13 P
X 72 (ECC mode) DRAM SIMM, 1 bank with X4 DRAMs

Release 4

Jedec 0007845

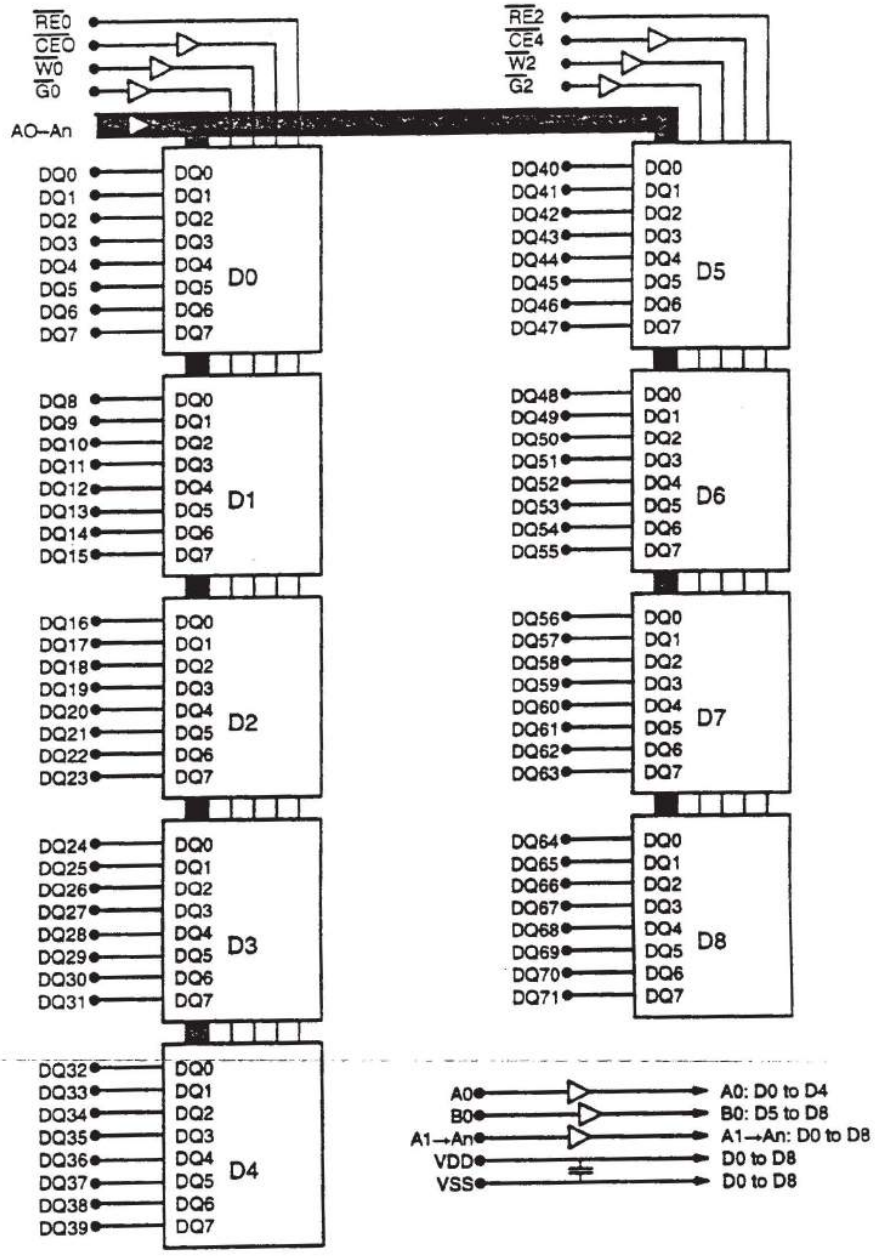


FIGURE 4–13 Q

X72 (ECC mode) DRAM SIMM, 1 bank with X8 DRAMs

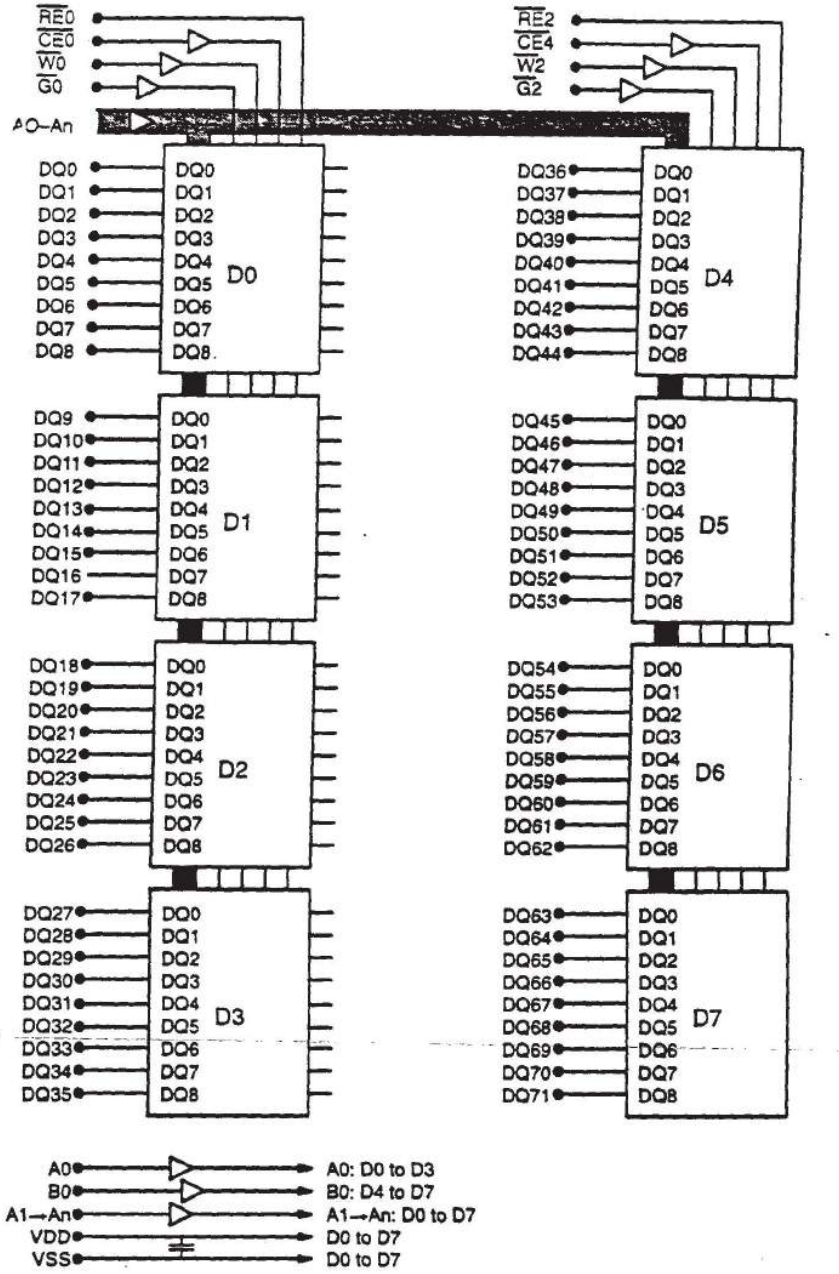


FIGURE 4–13 R

X72 (ECC mode) DRAM SIMM, 1 bank with X9 DRAMs

Release 4

Jedec 0007847

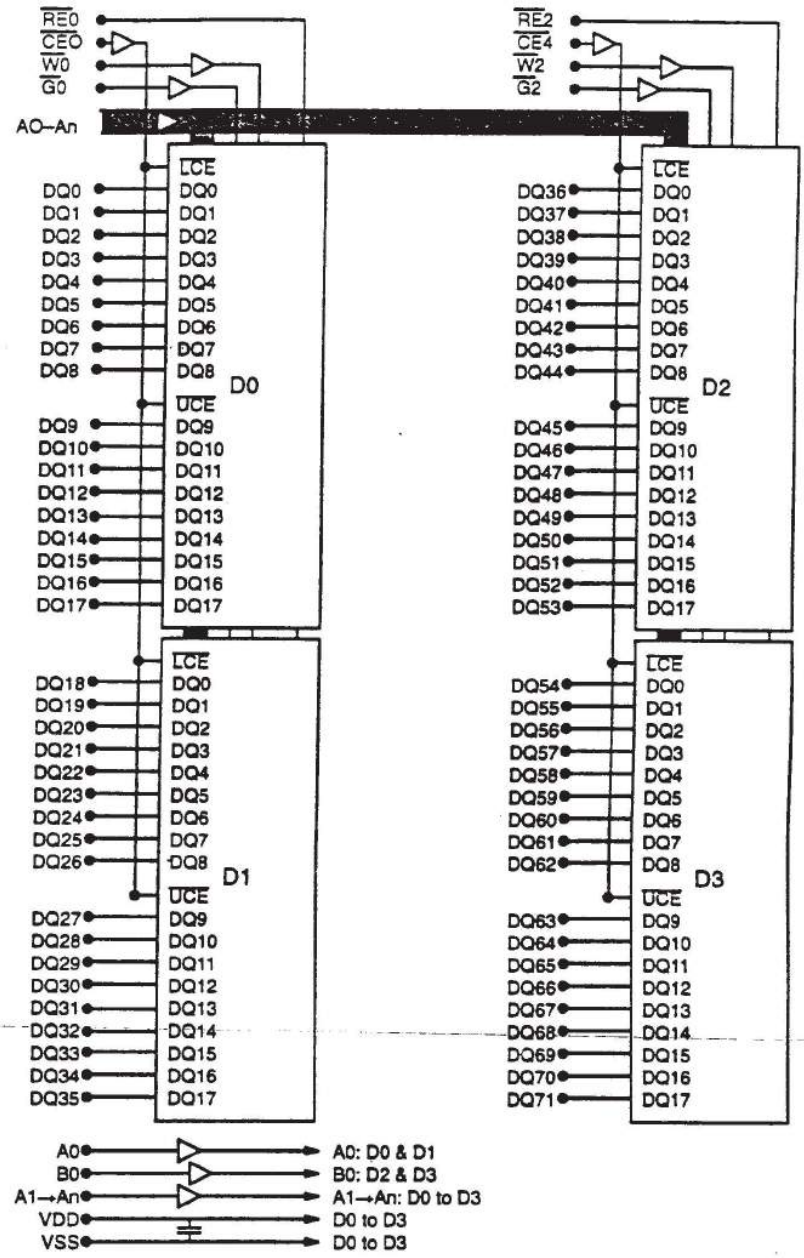


FIGURE 4–13 S

X72 (ECC mode) DRAM SIMM, 1 bank with X18 DRAMs

Release 4

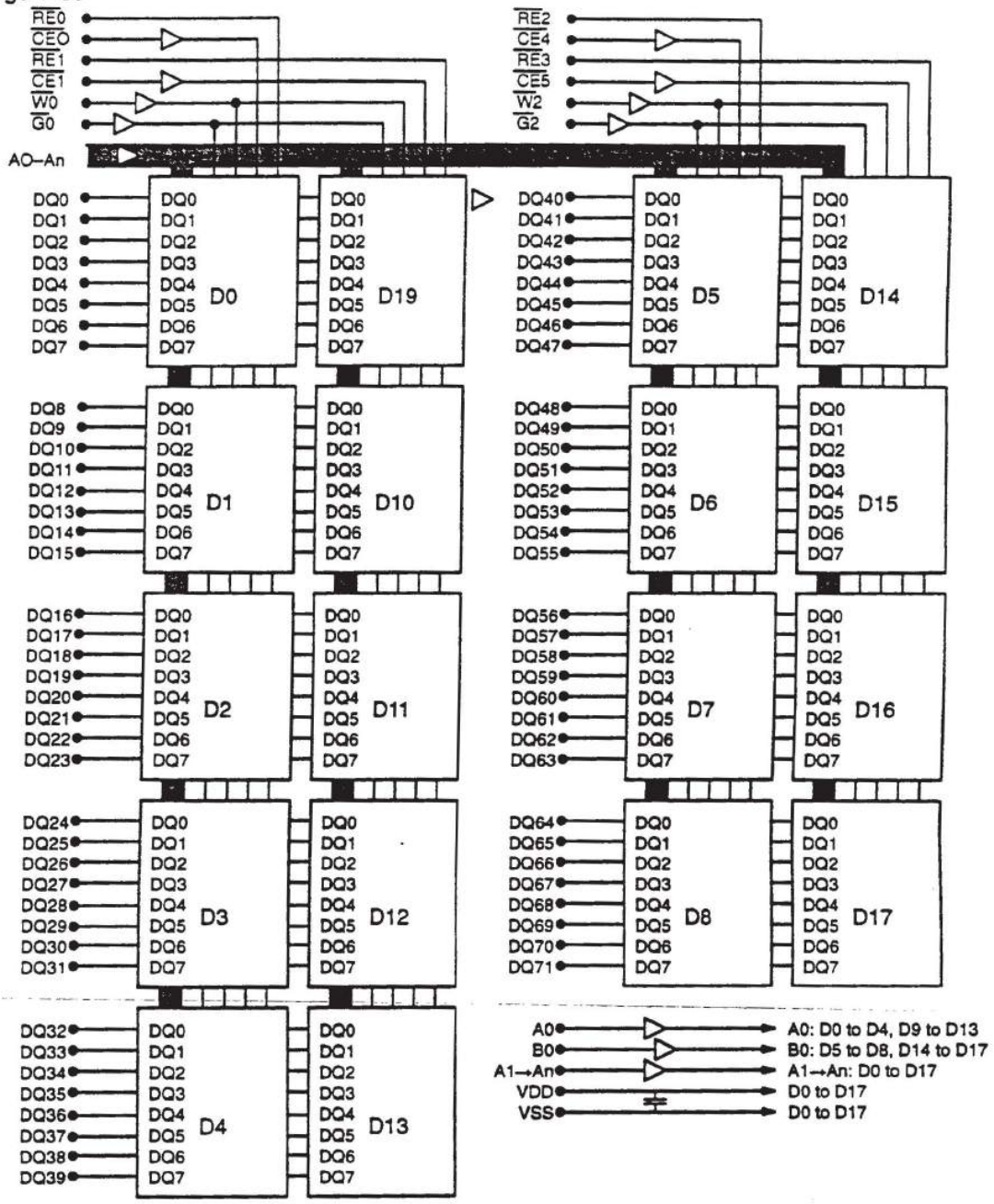


FIGURE 4–13 T

X72 (ECC mode) DRAM SIMM, 2 banks with X8 DRAMs

Release 4

Jedec 0007849

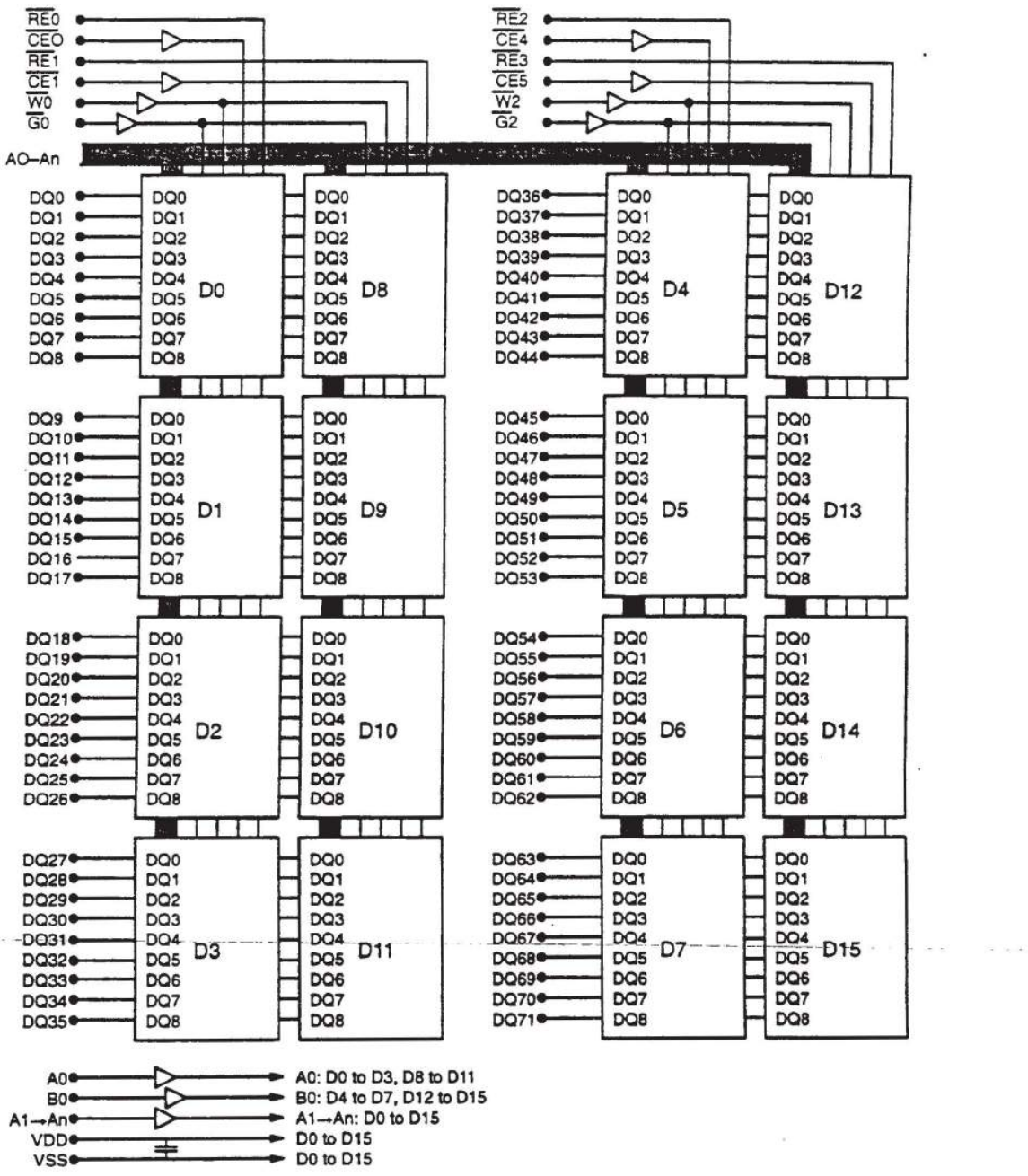


FIGURE 4–13 U

X72 (ECC mode) DRAM SIMM, 2 banks with X9 DRAMs

Release 4

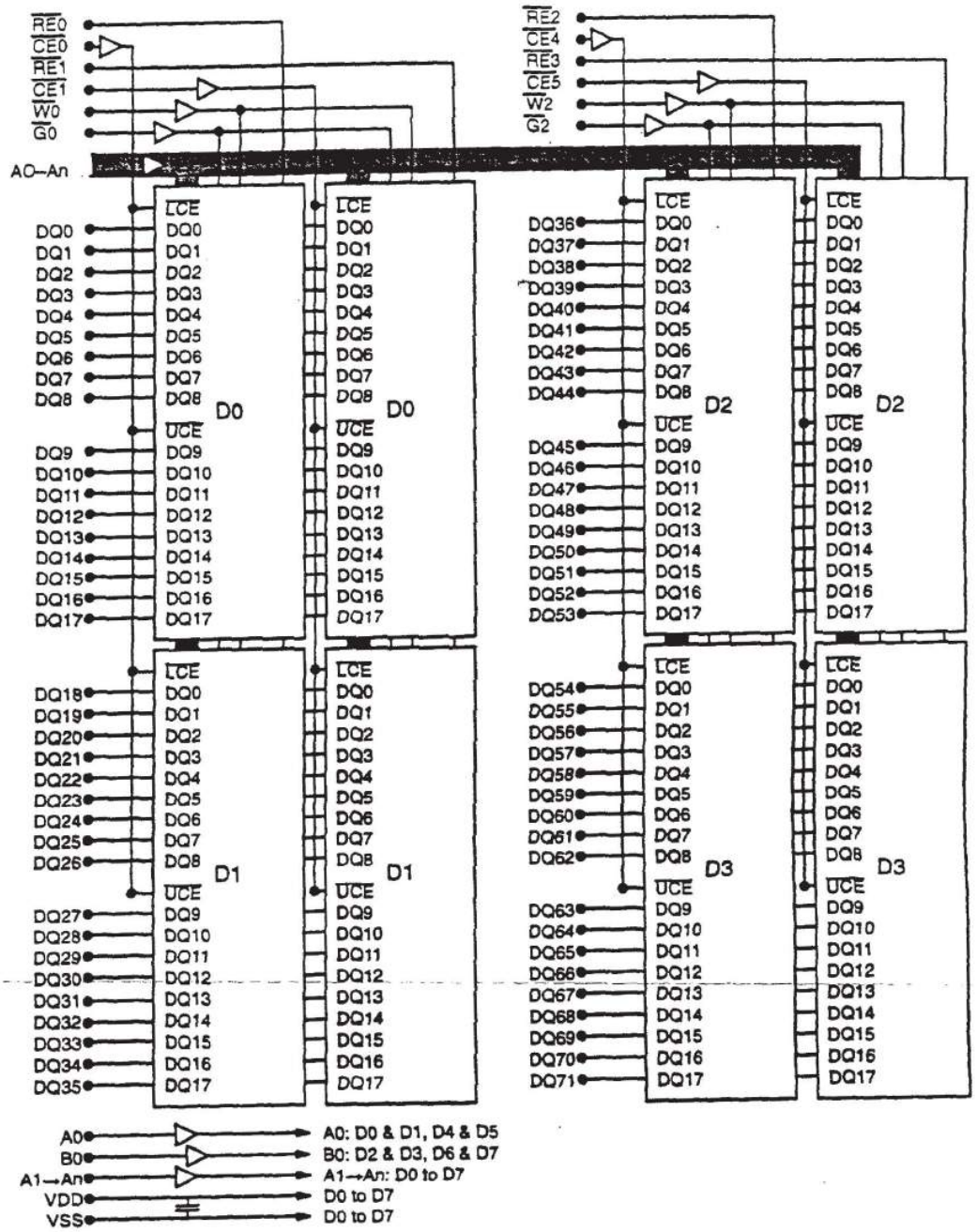


FIGURE 4–13 V

X72 (ECC mode) DRAM SIMM, 2 banks with X18 DRAMs

Release 4

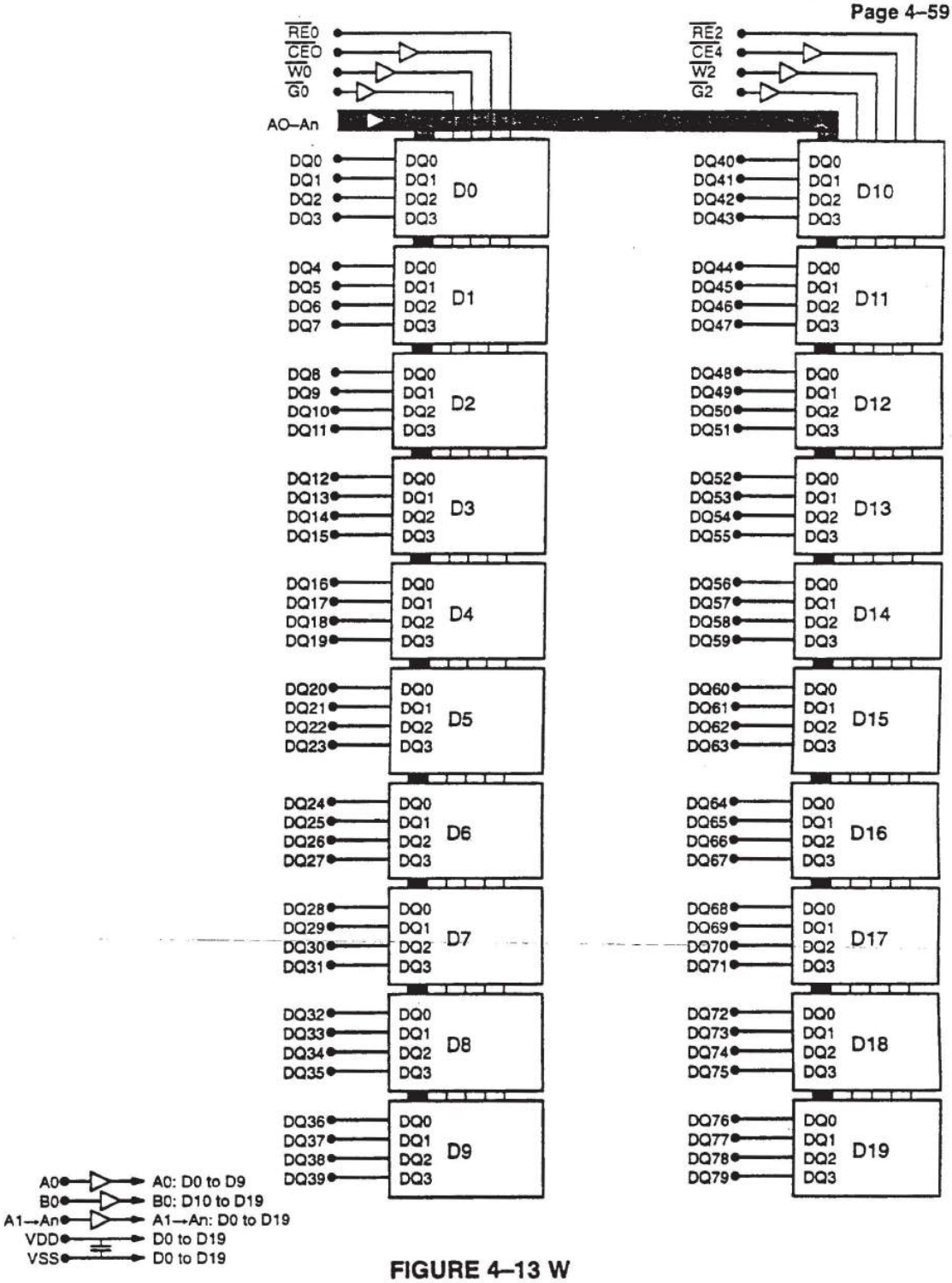


FIGURE 4–13 W

80 BIT (ECC mode) DRAM SIMM, 1 bank with X4 DRAMs

Release 4

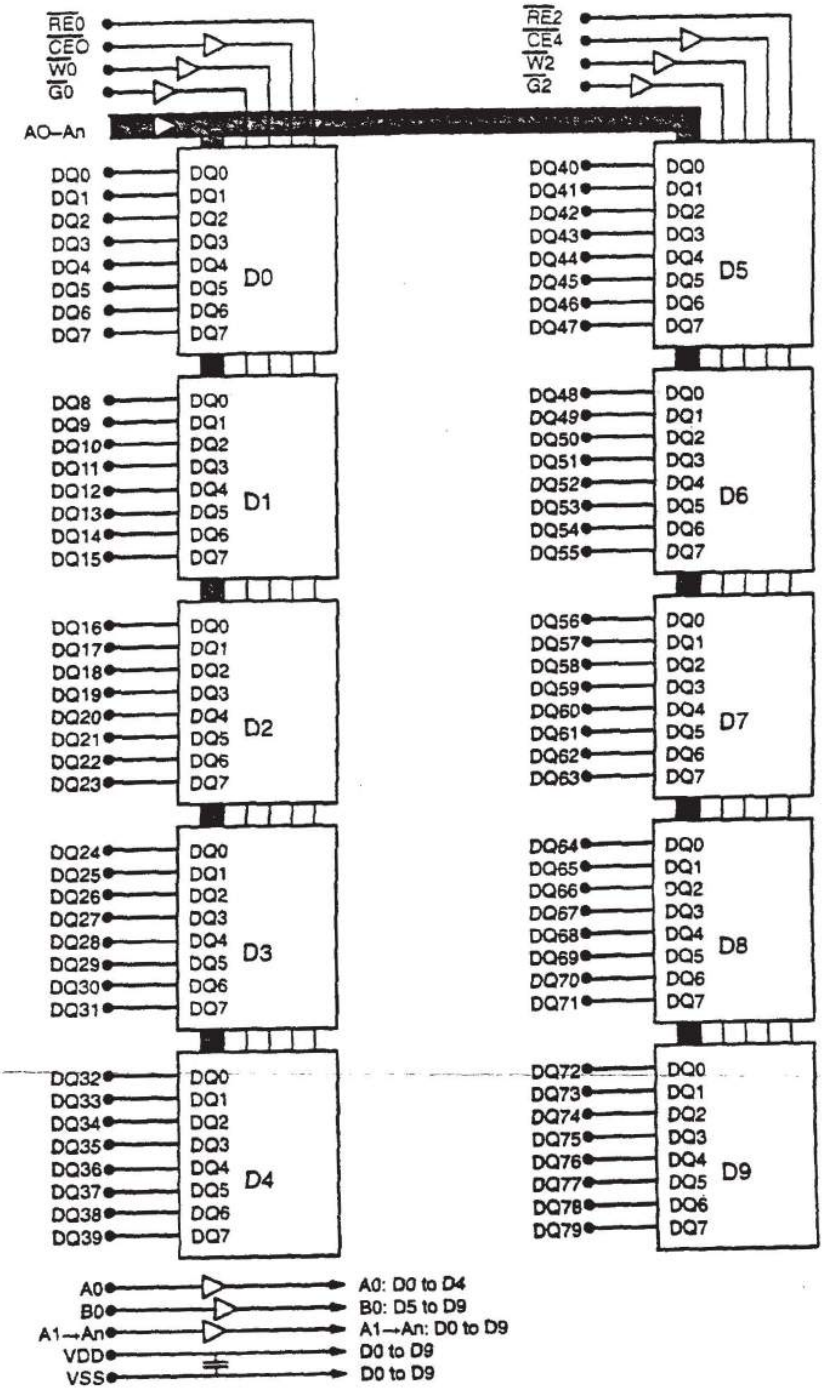


FIGURE 4–13 X

X80 (ECC mode) DRAM SIMM, 1 bank with X8 DRAMs

Release 4

Jedec 0007853

jx0056-174

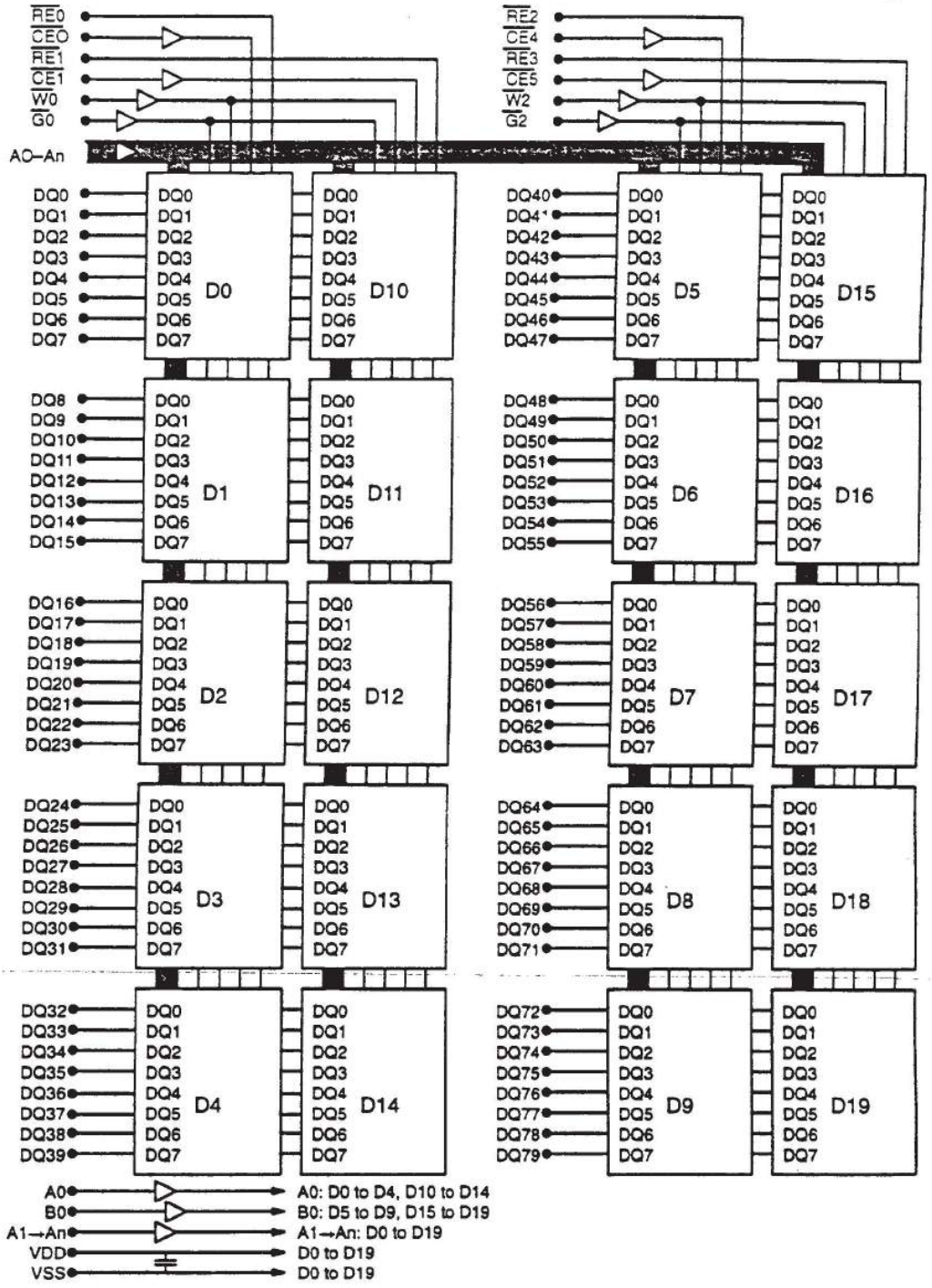


FIGURE 4–13 Y

X80 (ECC mode) DRAM SIMM, 2 banks with X8 DRAMs

Release 4

5 PROGRAMMABLE LOGIC AND ASIC DEVICES

The following standards define pinouts for Programmable Logic Devices (PLD) and Programmable Application Specific Devices (ASIC). These standards were all developed by the BIPOLAR Committee.

5.1 Pin Out Standards

5.1.1 PIN–OUT STANDARDS FOR PLD DIP TO SCC CONVERSION

This standard defines the pin–out conventions for converting a PLD in DIP to an SCC. Conversions are given for five different packages:

5.1.1.1 – 20 PIN DIP to 20 TERMINAL SCC, 0.350" BY 0.350", Fig. 5–1

5.1.1.2 – 24 PIN DIP to 28 TERMINAL SCC, 0.450" BY 0.450", Fig. 5–2

5.1.1.3 – 28 PIN DIP to 28 TERMINAL SCC, 0.450" BY 0.450", Fig. 5–2

5.1.1.4 – 24 PIN FUNCTIONS IN 28 PIN DIP & 28 TERMINAL SCC, Fig. 5–9

5.1.1.5 – 20 PIN FUNCTIONS IN 28 TERMINAL SCC AND 24 PIN DIP FOR HIGH SPEED OPERATION, Fig. 5–11

5.1.2 POWER PIN LOCATIONS FOR PLD and ASIC DEVICES

The following standards define the power pin locations for PLD and ASIC devices in a variety of packages.

5.1.2.1 – POWER PIN LOCATIONS FOR ECL PLD IN DIP

This standard defines the location of the power pins for ECL PLD devices in 24 PIN DIP. It is applicable to all currently available ECL families. The power pin locations are defined in Fig. 5–3.

5.1.2.2 – POWER PIN LOCATIONS FOR TTL PLD IN DIP and CC

This standard defines the location of the power pins for TTL PLD devices in 40 PIN DIP and 44 TERMINAL CC. It is applicable to all currently available TTL compatible families. The power pin locations are defined in Figures 5–4 & 5–5.

5.1.2.3 – POWER PIN LOCATIONS FOR TTL PROGRAMMABLE ASIC IN DIP and CC

This standard defines the location of the power pins for TTL compatible PROGRAMMABLE ASIC devices in 48 & 64 PIN DIP and 52, 64, & 84 TERMINAL CC. It is applicable to all currently available TTL compatible families. The power pin locations are defined in Figures 5–6 & 5–7.

5.1.2.4 – POWER PIN LOCATIONS FOR PLD IN 132 PIN QFP

This standard defines the POWER and GROUND connections for PLD devices in 132 Pin Quad Flat Pack packages. This standard is compatible with other standards for JEDEC Standards on packages with 40 through 84 pins. The power pin locations are defined in Figure 5–10.

5.1.3 Nomenclature for FPLD

This standard defines a compact nomenclature to be used to describe Field Programmable Logic Devices. The standard is applicable to all current and future devices, regardless of technology, density, and package. The details of the standard will be published as an addendum to EIA standard RS–428.

5.1.4 PLD Data Transfer Format

This standard defines a data transmission format to be used for transmitting data between a data preparation system and a device programmer that is used to program a PLD device.
The details of this standard are contained in JEDEC STANDARD #3–B published Nov. 1989.

5.1.5 PLD Standard OUTPUT LOADS

This standard defines a set of output loads providing various drive capabilities for PLD devices operating at either TTL or CMOS interface levels. A method is given whereby loads for other combinations of drive capabilities may be established. The details of this standard are shown in Figures 5–8A, B, C, & D.

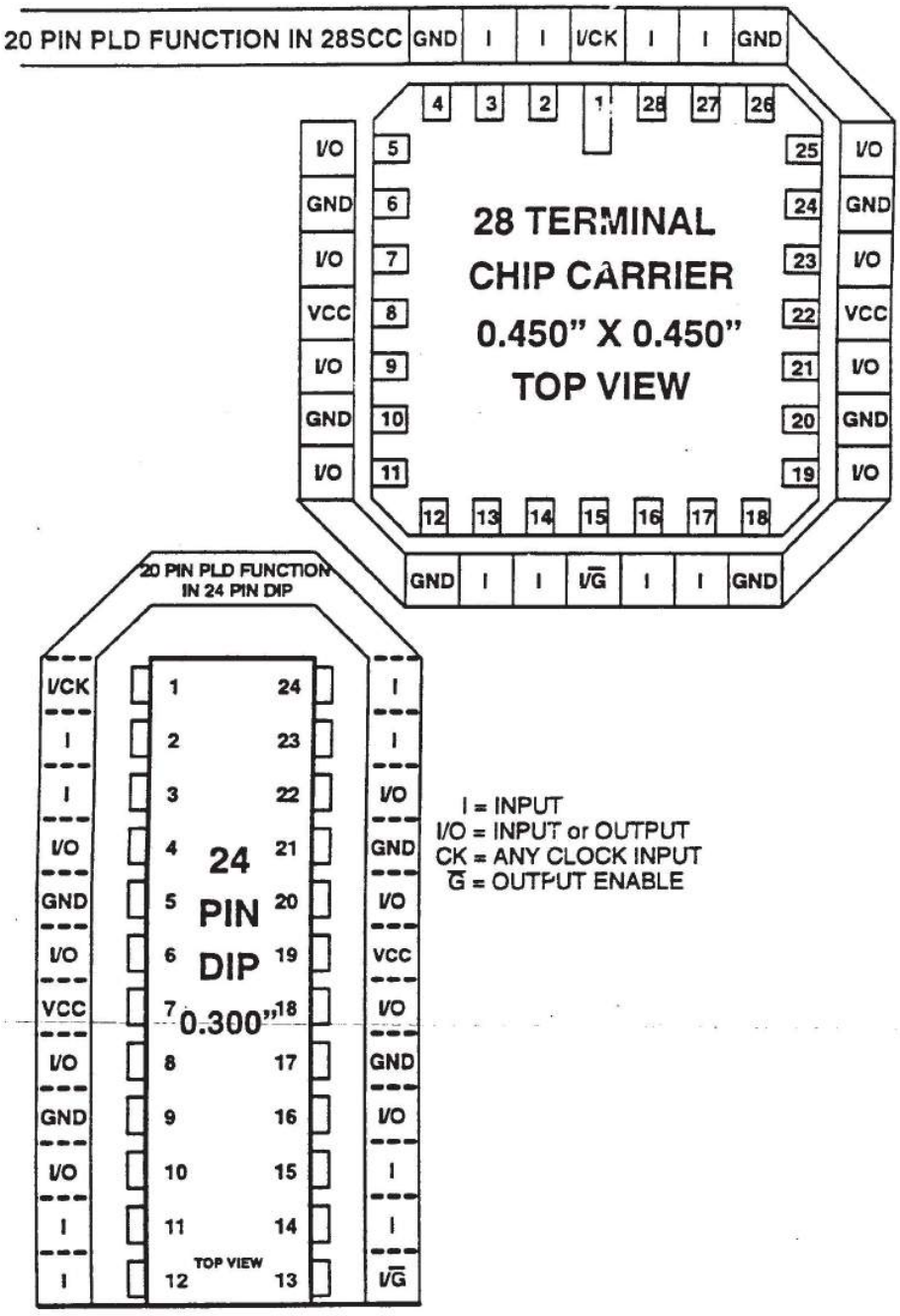


FIGURE 5–11
HIGH SPEED PINOUT FOR 20 PIN PLD FUNCTIONS

JESD 21-C, Release 4 Insertion Instructions

Instructions for adding Release 4 to JEDEC Standard 21-C.

Inclosed with this instruction sheet are new and replacement pages for JEDEC Standard 21-C. Those pages which contain new material are labeled "Release 4" at the bottom of the page. In some cases, there will be old material on the back of the sheet containing a Release 4 page. This old material will be labeled Release 1, Release 2, or Release 3 as there are no changes from the original release.

In the following 65 instructions, the material is arranged in 3 columns. The first column tells which sheet to remove from the 21-C binder. The second column tells which sheet to add to the binder. The third column gives an explanation of the reason for the change or addition.

	REMOVE	ADD	REASON
1	Remove Title Page;	Add replacement Title Page:	Contains revision Log for Standard.
2	Remove TOC, 7 sheets;	Add replacement TOC, 7 sheets;	Revised Table of Contents
3	Remove PP 2-1 to 2-6 and P 2-11/12	Add replacement 2-1 to 2-6 and 2-11/12	New terms added to Device Pin Names section. and package related terms section.
4	Remove P 3.4.1-3;	Add replacement P 3.4.1-3:	New items added.
5	Remove P 3.4.1-11	Add New P 3.4.1-11/12	Contains new Figure 3.4.1-8.
6	Remove P 3.4.2-3	Add replacement P 3.4.2-3	New item added.
7		Add new page P 3.4.2-11;	Contains new figure 3.4.2-7.
8	Remove P 3.7-1;	Add Replacement P 3.7-1:	New item added.
9		Add new P 3.7-3;	Contains new standard, Fig 3.7-1
10	Remove P 3.7.1-3;	Add replacement P 3.7.1-3:	Existing items modified.
11	Remove P 3.7.1-11/12	Add replacement P 3.7.1-11/12	New dimension table added to Fig. 3.7.1-7.
12	Remove P 3.7.1-13	Add new P 3.7.1-13;	New dimension table added fo Fig. 3.7.1-9.
13	Remove P 3.7.2-3	Add replacement P 3.7.2-3	Existing items modified.
14	Remove P 3.7.2-5/6	Add replacement P 3.7.2-5/6	New dimension table added to Fig. 3.7.2-2.
15	Remove P 3.7.2-7/8	Add Replacement P 3.7.2-7/8;	New dimension table added to Fig. 3.7.2-4.
16	Remove P 3.7.3-3/4	Add replacement P 3.7.3-3/4:	Existing items modified.
17	Remove P 3.7.3-15/16	Add replacement P 3.7.3-15/16	New dimension table added to Fig. 3.7.3-12.
18	Remove P 3.7.3-17/18	Add Replacement P 3.7.3-17/18	New dimension tables added to Figs. 3.7.3-13 & 3.7.3-14
19	Remove P 3.7.4-3/4	Add New P 3.7.4-3/4	Existing items modified.
20	Remove P 3.7.4-9/10	Add Replacement 3.7.4-9/10	New dimension table added to Figs 3.7.4-6 & 3.8.4-7.
21	Remove P. 3.7.4-11/12	Add new P 3.7.4-11/12	New dimension table added to Fig. 3.7.4-8.
22	Remove P 3.7.4-13/14	Add new P 3.7.4-13/14	Add dimension table added to Fig. 3.7.4-11.

23	Remove P 3.7.4-15/16	Add replacement P 3.7.4-15/16	New dimension tables added to Figs. 3.7.4-12 & 3.7.4-13
24	Remove P 3.7.5-3/4;	Add replacement P 3.7.5-3/4:	Existing items modified.
25	Remove P 3.7.5-9/10	Add New p 3.7.5-9/10;	Modify pinout of one device in Fig. 3.7.5-6.
26	Remove P 3.7.5-13/14	Add Replacement P 3.7.5-13/14	New dimension tables added to Figs. 3.7.5-9 & 3.7.5-10.
27	Remove P 3.7.5-21/22	Add replacement P 3.7.5-21/22	New dimension table added to Fig. 3.7.5-17.
28	Remove P 3.7.7-3	Add replacement P 3.7.7-3	New item added.
29		Add new P 3.7.7-11/12	Add new Standard.
30	Remove P 3.9.1-3/4	Add replacement P 3.9.1-3/4	Existing items modified, new item added.
31	Remove P 3.9.1-9/10;	Add replacement P 3.9.1-9/10;	Add new device & packages to Figs 3.9.1-5 & 3.9.1-6.
32	Remove P 3.9.1-13/14	Add replacement P 3.9.1-13/14	Fig. 3.9.1-10 modified.
33		Add new P 3.9.1-15	Add new Fig. 3.9.1-11.
34	Remove P 3.9.2-3/4	Add replacement P 3.9.2-3/4	Existing items modified, new standard added.
35	Remove P 3.9.2-7/8	Add Replacement P 3.9.2-7/8	Device and packages added to Fig. 3.9.2-4.
36	Remove P 3.9.2-9/10	Add replacement P 3.9.2-9/10	Patent note added to Fig 3.9.2-6.
37	Remove P 3.9.2-13/14	Add replacement P 3.9.2-13/14	Drawing modified, patent note added to Fig 3.9.2-10
38	Remove P 3.9.2-15/16	Add Replacement P 3.9.2-15/16	Modified Fig 3.9.2-11, add new standard, Fig. 3.9.2-12.
39	Remove P 3.9.3-3	Add replacement P 3.9.3-3;	Supplement existing standard.
40	Remove P 3.9.3-11	Add replacement P 3.9.3-11	Add new device to Fig. 3.9.3-7.
41	Remove P 3.9.4-3	Add replacement P 3.9.4-3;	Add new items.
42	Remove P 3.9.4-7/8	Add replacement P 3.9.4-7/8	Correct errors in original publication of Fig 3.9.4-3.
43	Remove P 3.9.4-9/10;	Add replacement P 3.9.4-9/10	Correct package error in Fig. 3.9.4-5.
44		Add new P 3.9.4-11;	Add new standard, Fig 3.9.4-7,A & B.
45		Add new P 3.9.4-13;	Add new standard, Fig. 3.9.4-8
46	Remove P. 3.9.5-5/6	Add replacement P 3.9.5-5/6;	Modify Fig. 3.9.5-1B to clarify standard.
47	Remove PP 3.9.5-7/8 and 3.9.5-9/10	Add replacement PP 3.9.5-7/8 and 3.9.5-9/10	Modify existing standard.
48	Remove P 3.10.4-11/12	Add replacement P 3.10.4-11/12	Correct error in original R3 timing diagram.
49		Insert divider for SDRAM section	New section 3-11 , SDRAM added.
50		Add new pages 3.11-1, 3.11.1-1, 3.11.2-1, 3.11.2-3, 3.11.3-1, . 3.11.3-3,3.11.5-1, 3.11.5-3, 3.11.5-5/6 to .11.5-17/18	New standards on SDRAMs, pinouts and features.

51	Remove PP 4-5/6 & 4-6B	Add replacement PP 4-5/6 & 4-6B/6C	Old standard supplemented, new standards added
52	Remove P 4-11/12	Add replacement P 4-11/12	New device added to existing standard.
53	Remove P 4-15/16	Add replacement P 4-15/16	New PD table in Fig. 4-6.
54	Remove PP 4-19/20, 4-21/22, & 4-23-24	Add replacement PP 4-19/20, 4-21/22, & 4-23/24	Modifiy PD table and correct Fig 4-8 block diagrams.
55	Remove P 4-25	Add replacement P 4-25/26 & new P 4-27/28	New standard Fig. 4-10.
56		Add new PP 4-29/30, 4-31/32, and 4-33/34	New Standard Fig 4-11
57		Add new P 4-35/36	New standard, Fig 4-12.
58		Add new pages 4-37/38 to 4-61	New standard
59	Remove P 5-1	Add replacement P 5-1	New item added.
60		Add new P 5-15	New standard added, Fig 5-11.

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