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United States Patent [19] Nagai

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[45] Date of Patent: **Sep. 5, 1995**

[54] SYNCHRONOUS DRAM HAVING INITIAL MODE SETTING CIRCUIT

[56] References Cited

U.S. PATENT DOCUMENTS

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[57] **ABSTRACT**

[21] Appl. No.: **307,420**

The initial mode setting circuit 30 has a circuit 31 for generating a reset pulse RST after detecting that the power source voltage VCC has reached a specified value when the power source voltage VCC starts up, and fuses 32 to 37, each one end of which is commonly connected to the output end of the reset signal generating circuit 31 and the other ends of which are connected to one of either the set input end S or the reset input end R of the flip flops 11 to 13. The fuses 32 to 37 are melted and cut off electrically or with a laser.

[22] Filed: **Sep. 19, 1994**

[30] **Foreign Application Priority Data**

Sep. 21, 1993 [JP] Japan 5-235225

[51] Int. Cl.⁶ **G11C 13/00**

[52] U.S. Cl. **365/233; 365/225.7;**
365/230.06

[58] Field of Search 365/233, 230.06, 225.7

7 Claims, 4 Drawing Sheets

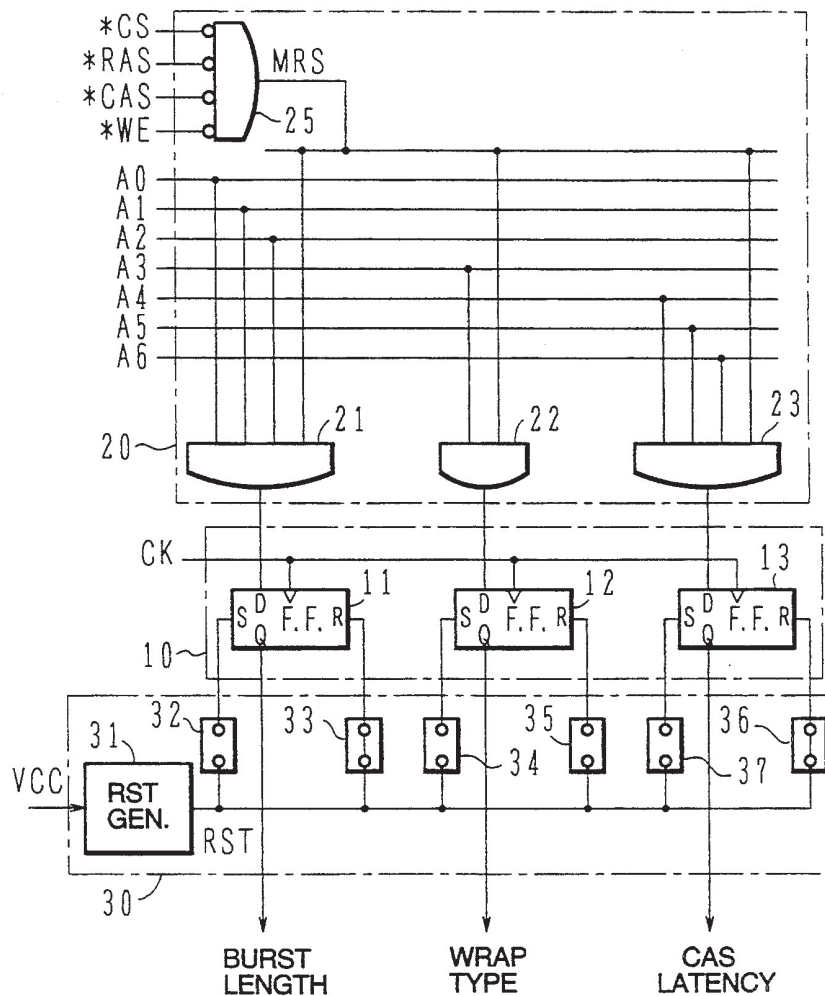


FIG. 1

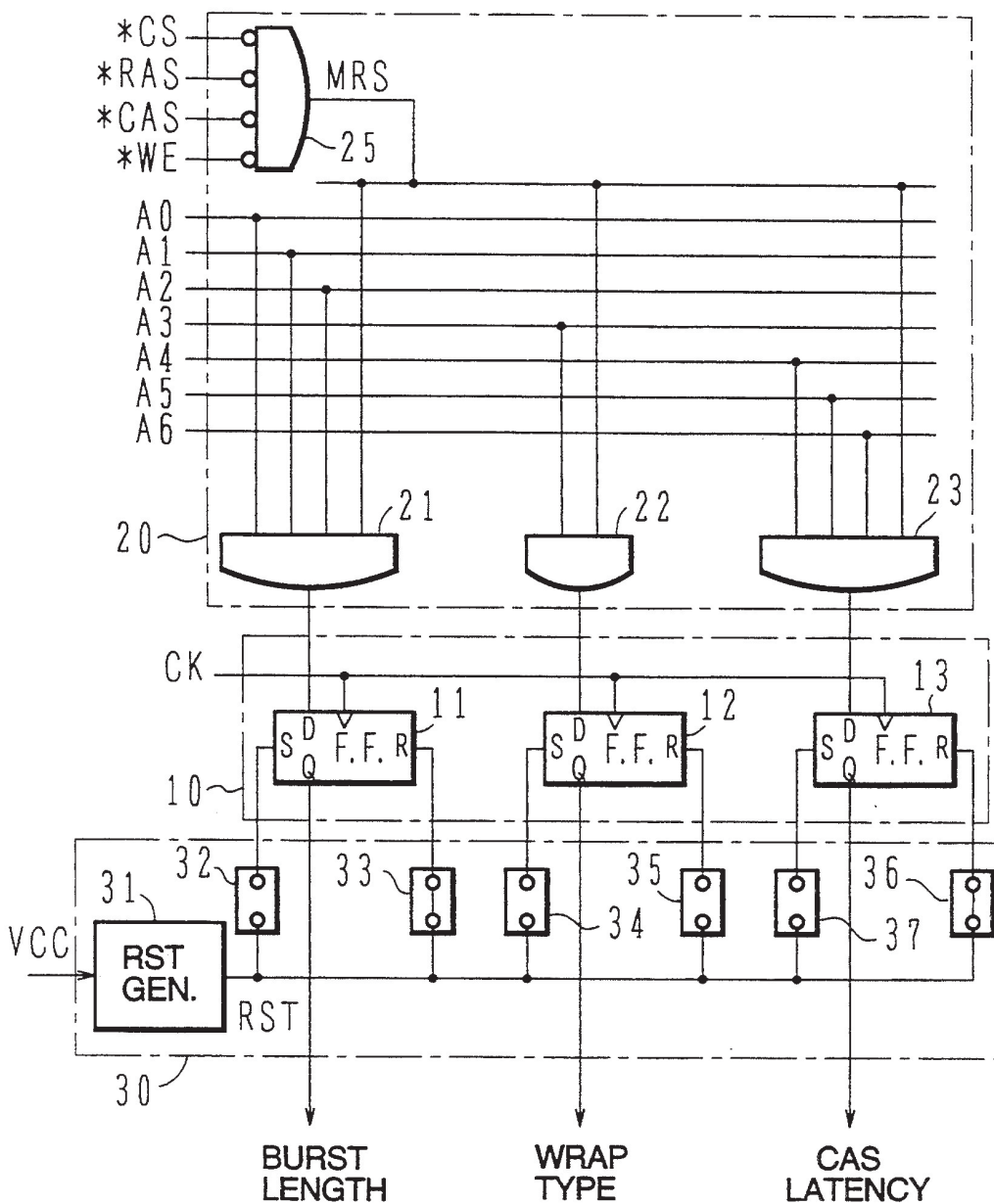


FIG. 2

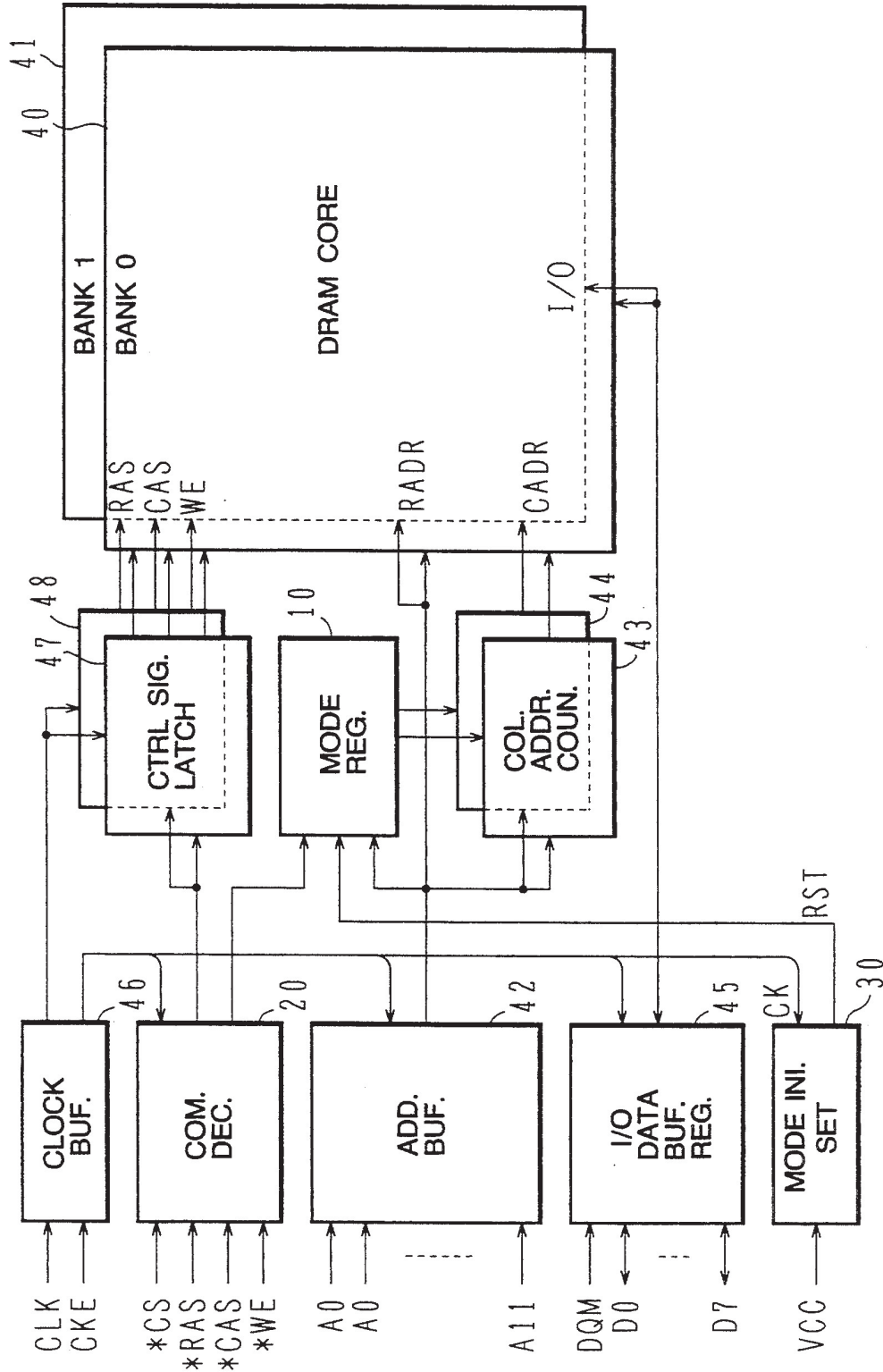


FIG.3A
(PRIOR ART)

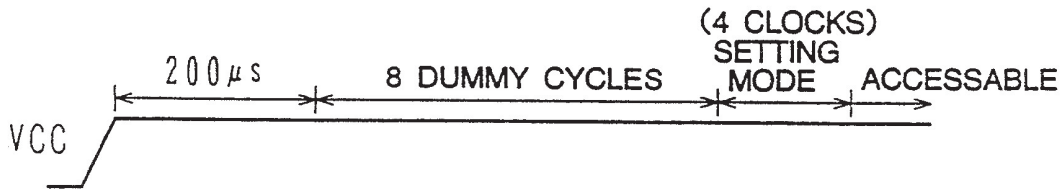


FIG.3B

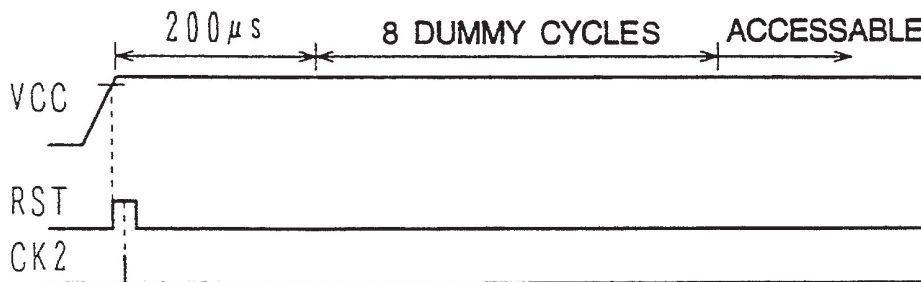
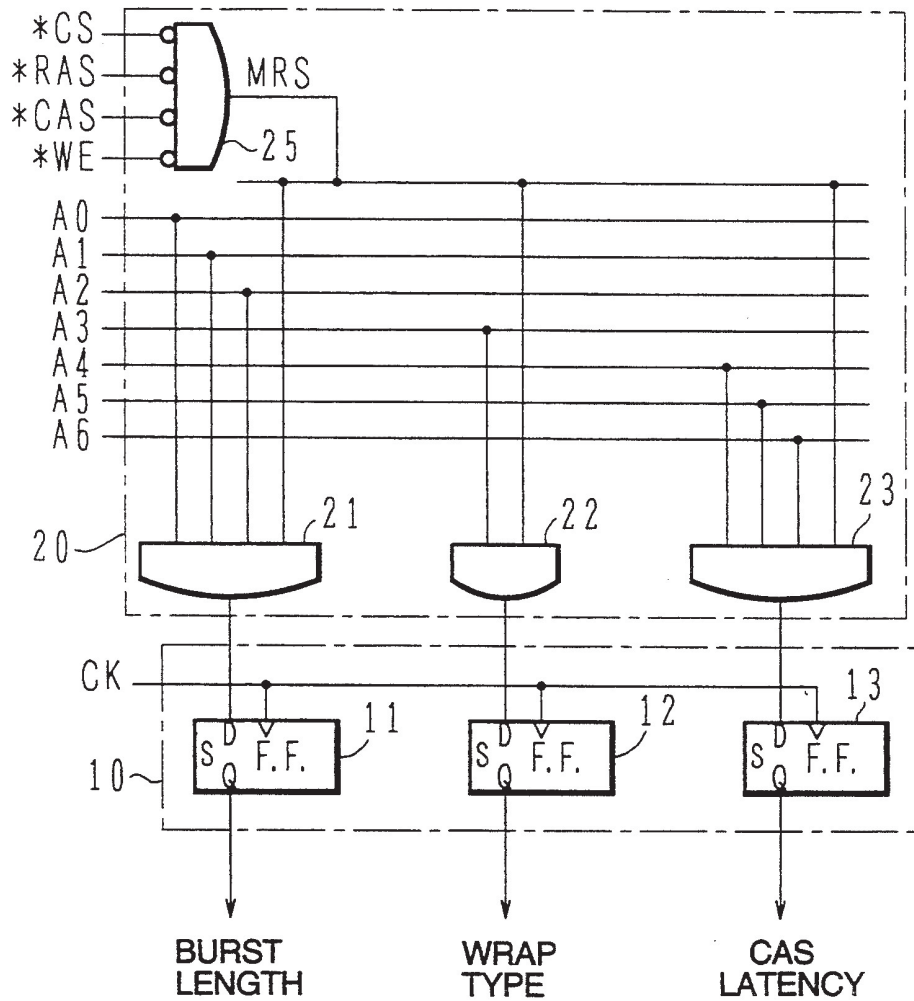


FIG. 4
(PRIOR ART)



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