US006243797B1

(12) **United States Patent**
Merritt

(10) **Patent No.: US 6,243,797 B1**
(45) **Date of Patent: *Jun. 5, 2001**

(54) **MULTIPLEXED SEMICONDUCTOR DATA TRANSFER ARRANGEMENT WITH TIMING SIGNAL GENERATOR**

(75) Inventor: **Todd A. Merritt**, Boise, ID (US)

(73) Assignee: **Micron Technlogy, Inc.**, Boise, ID (US)

(*) Notice: This patent issued on a continued prosecution application filed under 37 CFR 1.53(d), and is subject to the twenty year patent term provisions of 35 U.S.C. 154(a)(2).

Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **08/801,161**

(22) Filed: **Feb. 18, 1997**

(51) **Int. Cl.**[7] **G06F 12/00**
(52) **U.S. Cl.** **711/167**; 711/169; 711/157; 711/100; 711/168
(58) **Field of Search** 365/233, 230.08, 365/189.12; 711/104, 167, 100, 101, 102, 105, 111, 150, 154, 157, 168, 169

(56) **References Cited**

U.S. PATENT DOCUMENTS

4,961,169	*	10/1990	Matsumura et al.	365/189.12
4,985,643		1/1991	Proebsting	307/443
5,261,068	*	11/1993	Gaskins et al.	711/157
5,325,502		6/1994	McLaury	395/425
5,349,566		9/1994	Merritt et al.	365/233.5
5,384,750	*	1/1995	Lee	365/233
5,430,687	*	7/1995	Hung et al.	365/230.08
5,544,124	*	8/1996	Zagar et al.	365/230.08
5,587,961	*	12/1996	Wright et al.	365/233

OTHER PUBLICATIONS

"Micron 4 Meg X 4/2 Meg X 8 SDRAM", *Micron Synchronous DRAM Data Book*, Micron Technology, Inc., pp. 1–44, (Rev. Feb. 1997).

"Wave–pipelining: Is it Practical?",*1994 IEEE International Symposium on Circuits and Systems*, vol. 4 of 6 VLSI, pp. 163, (164 is blank, not included and 165–166, (May 30–Jun. 2, 1994).

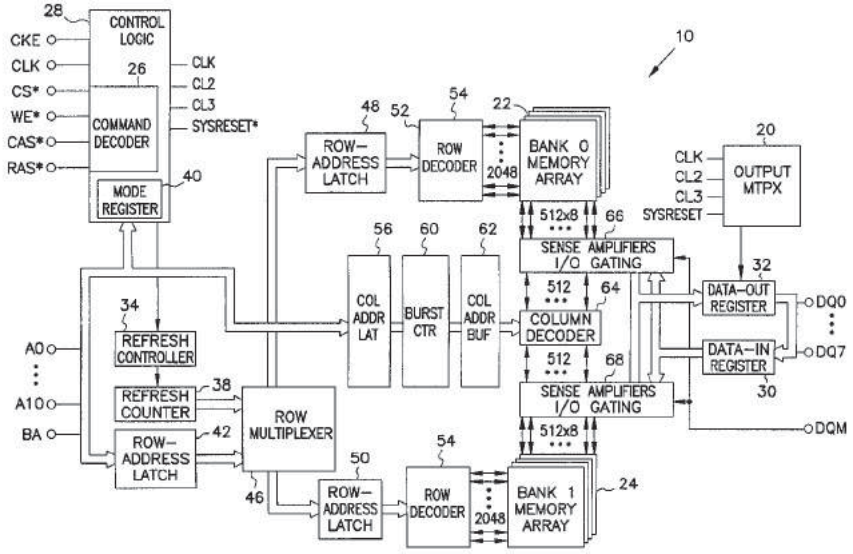
(List continued on next page.)

Primary Examiner—John W. Cabeca
Assistant Examiner—Matthew D. Anderson
(74) *Attorney, Agent, or Firm*—Schwegman, Lundberg, Woessner & Kluth, P.A.

(57) **ABSTRACT**

A multiplexing arrangement for transferring data retrieved from a memory array to data outputs of a semiconductor memory, including a multiplexing circuit that is responsive to latency select signals to cause data retrieved sequentially from the memory array to be loaded into and read from data latch circuits of a data output register in a sequence that establishes a known delay between the time that data is retrieved from the memory array and stored in the data output register and the time that the data is read from the data output register. The delay allows data to be held in the data output register when the data is available and to be passed to the data outputs of the memory when desired. Also described is a multi-phase timing signal generator that includes a multi-stage shift register connected for operation as a recirculating shift register, a drive circuit responsive to system clock pulses for advancing a bit pattern through the shift register, and an output circuit for logically combining signals provided at outputs of the shift register as the bit pattern is advanced through the shift register to produce sequential timing signals.

20 Claims, 7 Drawing Sheets



OTHER PUBLICATIONS

Fujiwara, et al., "A 200MHz 16Mbit Synchronous DRAM with Block Access Mode",*1994 Symposium on VLSI Circuits—Digest of Technical Papers*, IEEE Cat. No. 94Ch3434–8, pp. 79–80, (Jun. 9–11, 1994).

Takai, et al., "250 Mbyte/sec Synchronous DRAM Using a 3–Stage–Pipelined Architecture",*1993 Symposium on VLSI Circuits—Digest of Technical Paper*, IEEE Cat. No. 93 CH 3304–3, pp. 59–60, (May 19–21, 1993).

Wong, et al., "A Bipolar Population Counter Using Wave Pipelining to Achieve 2.5x Normal Clock Frequency",*1992 IEEE International Solid–State Circuits Conference—Digest of Technical Papers*, First Edition—IEEE Cat. No. 92CH3128–6, pp. 56–57, (Feb., 1992).

Yoo, et al., "A 150MHz 8–Banks 256M Synchronous DRAM with Wave Pipelining Methods",*1995 IEEE International Solid–State Circuits Conference*, ISSCC95/Session 14—Paper FA 14.4, pp. 250, (1995).

* cited by examiner

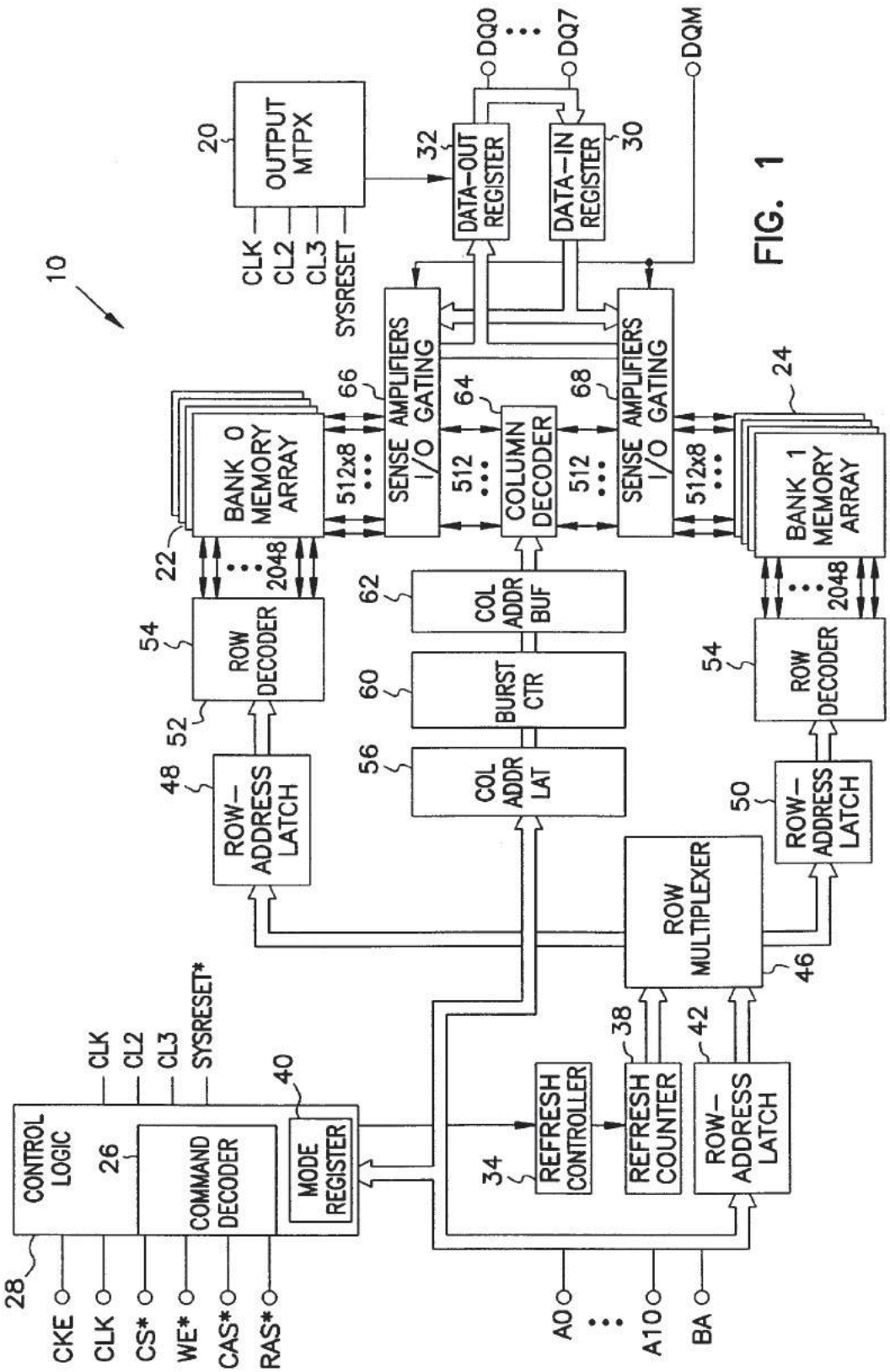


FIG. 1

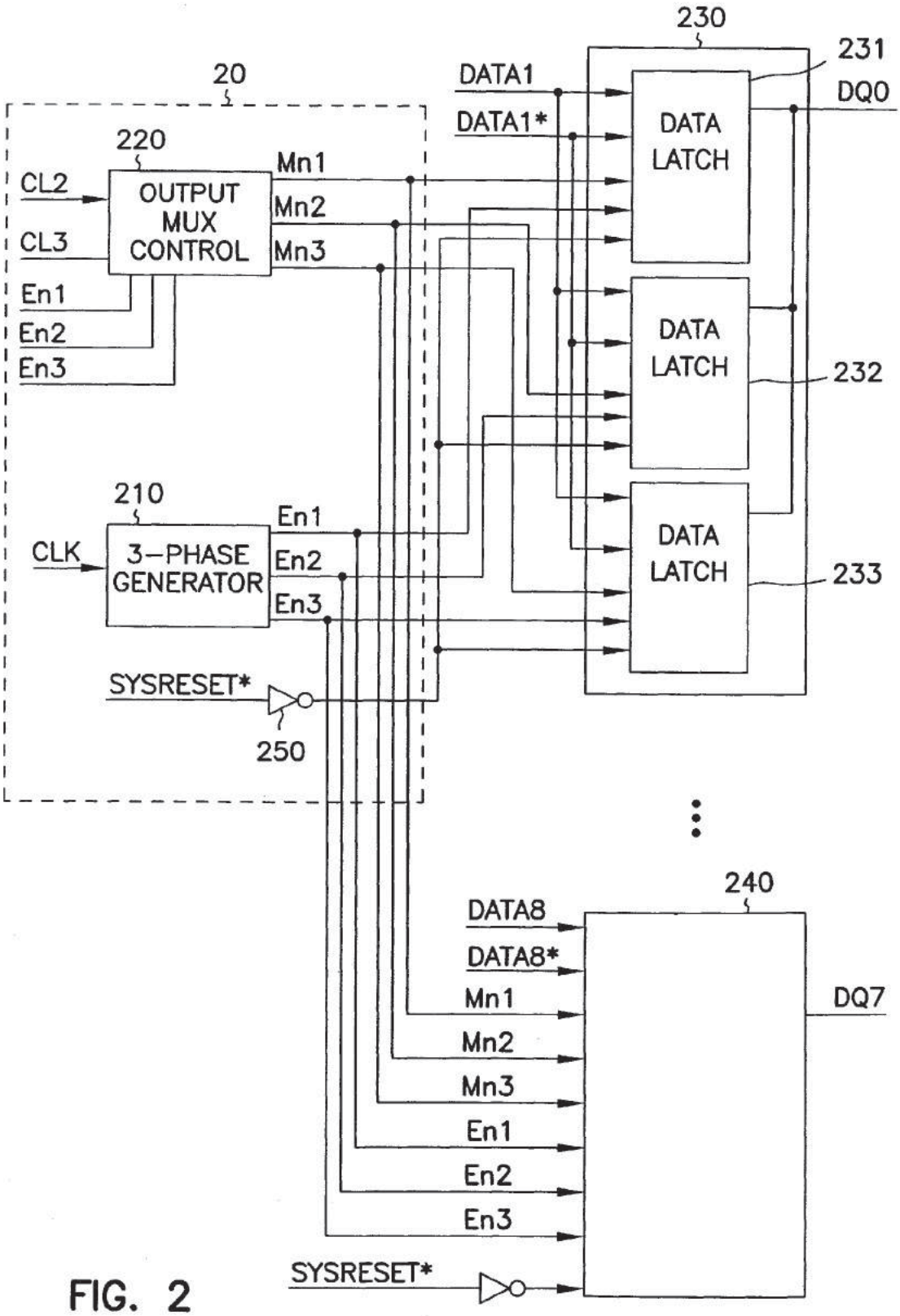


FIG. 2

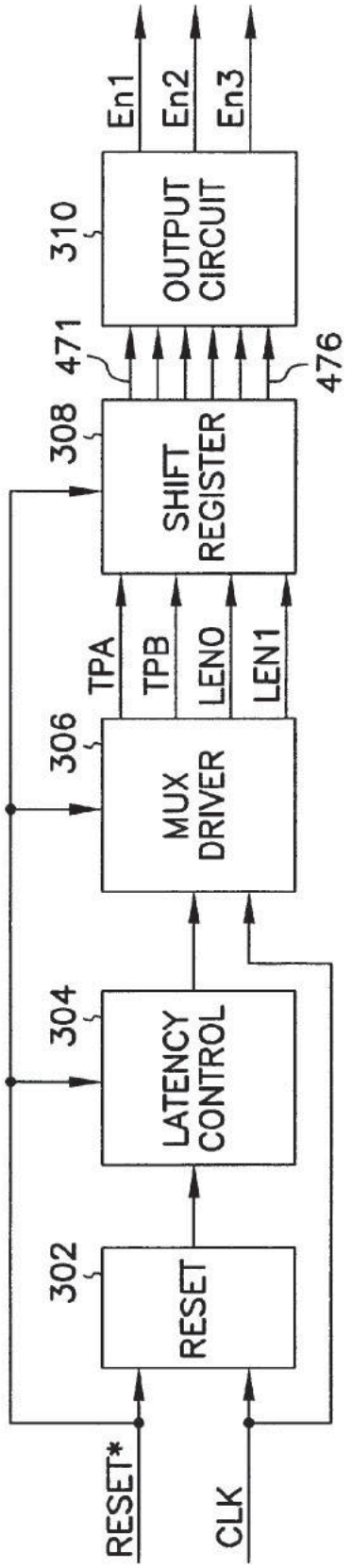


FIG. 3

DOCKET ALARM

Explore Litigation Insights

Docket Alarm provides insights to develop a more informed litigation strategy and the peace of mind of knowing you're on top of things.

Real-Time Litigation Alerts

Keep your litigation team up-to-date with **real-time alerts** and advanced team management tools built for the enterprise, all while greatly reducing PACER spend.

Our comprehensive service means we can handle Federal, State, and Administrative courts across the country.

Advanced Docket Research

With over 230 million records, Docket Alarm's cloud-native docket research platform finds what other services can't. Coverage includes Federal, State, plus PTAB, TTAB, ITC and NLRB decisions, all in one place.

Identify arguments that have been successful in the past with full text, pinpoint searching. Link to case law cited within any court document via Fastcase.

Analytics At Your Fingertips

Learn what happened the last time a particular judge, opposing counsel or company faced cases similar to yours.

Advanced out-of-the-box PTAB and TTAB analytics are always at your fingertips.

API

Docket Alarm offers a powerful API (application programming interface) to developers that want to integrate case filings into their apps.

LAW FIRMS
Build custom dashboards for your attorneys and clients with live data direct from the court.

Automate many repetitive legal tasks like conflict checks, document management, and marketing.

FINANCIAL INSTITUTIONS
Litigation and bankruptcy checks for companies and debtors.

E-DISCOVERY AND LEGAL VENDORS
Sync your system to PACER to automate legal marketing.