IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent of: Krause
US Patent No.: 6,157,589
Issue Date: December 5, 2000
Appl. Serial No.: 09/343,431

Title: DYNAMIC SEMICONDUCTOR MEMORY DEVICE AND METHOD FOR INITIALIZING A DYNAMIC SEMICONDUCTOR MEMORY DEVICE

Mail Stop Patent Board
Patent Trial and Appeal Board
U.S. Patent and Trademark Office
P.O. Box 1450
Alexandria, VA 22313-1450

DECLARATION OF VIVEK SUBRAMANIAN

I, Vivek Subramanian, declare as follows:

I. Introduction

1. I am making this declaration at the request of the Real Party in Interest (Kingston Technology Company, Inc.) in the matter of *Inter Partes* Review of U.S. Patent No. 6,157,589 ("the '589 patent").

2. I am being compensated for my work. My compensation does not depend on the outcome of this proceeding.

3. I have been asked to consider whether certain references disclose or render obvious the claims of the '589 Patent, either alone or in combination with each other.

4. I have been advised that a patent claim may be invalid as obvious if the differences between the subject matter patented and the prior art are such that the subject matter as a whole would have been obvious at the time of the invention to a person having ordinary skill in the art. I have also been advised that several factual inquiries underlie a determination of obviousness. These inquiries include the scope and content of the prior art, the level of ordinary skill in the field of the invention, the differences between the claimed invention and the prior art, and any objective evidence of non-obviousness.

5. I have been advised that objective evidence of non-obviousness directly attributable to the claimed invention, known as "secondary considerations of non-obviousness," may include commercial success, satisfaction of a long-felt but unsolved need, failure of others, copying, skepticism or disbelief before the invention, and unexpected results. I am not aware of any such objective evidence of non-obviousness that is directly attributable to the subject matter claimed in the '589 patent at this time.

6. In addition, I have been advised that the law requires a "common sense" approach of examining whether the claimed invention is obvious to a person skilled in the art. For example, I have been advised that combining familiar elements according to known methods is likely to be obvious when it does no more than yield predictable results. I have further been advised that this is especially true in

instances where there are a limited numbers of possible solutions to technical problems or challenges.

7. I have been informed that claims 11 and 12 of the '589 Patent are subject to this *inter partes* review.

II. Materials Reviewed

8. In forming the opinions, I express below, I considered my own knowledge of the art and at least the following references:

KINGSTON-1001	U.S. Patent No. 6,157,589 ('589 Patent)
KINGSTON-1002	File History of U.S. Patent No. 6,157,589
KINGSTON-1005	U.S. Patent No. 6,243,797 B1 ("Merritt")
KINGSTON-1006	U.S. Patent No. 5,448,528 ("Nagai")
KINGSTON-1007	JEDEC Standard 21-C Release 4
KINGSTON-1008	Plaintiff Polaris Innovations Limited's Preliminary Disclosure Of Asserted Claims And Infringement Contentions, Exhibit 1, Preliminary Infringement Claim Chart for U.S. Patent No. 6,157,589 ("589 Patent") *Polaris Innovations Ltd. v. Kingston Tech. Co., Inc.*, Case No. 8:16-cv-300-CJC (C.D. Cal. July 8, 2016)

III. Qualifications

9. I summarize my relevant knowledge and experience below. My Curriculum Vitae contains additional information and is attached as Exhibit 1004.

10. I received a B.S. in electrical engineering from Louisiana State University in 1994, an M.S. in electrical engineering from Stanford University in 1996, and a Ph.D. in electrical engineering from Stanford University in 1998.

11. I co-founded Matrix Semiconductor, Inc. in 1998 to develop high density memory technology.

12. I have been teaching in the Electrical Engineering and Computer Sciences Department at the University of California, Berkeley since 2000. I was an Assistant Professor from 2000 to 2005, an Associate Professor from 2005 to 2011, and a Professor from 2011 to the present.

13. I have been an adjunct professor at the Sunchon National University in Sunchon, Korea since 2009, leading research in printed electronics.

14. I have been an independent consultant in the semiconductor industry since 2000, focusing on memory technology, flexible electronics, and RFID technology.

15. I have published more than 200 technical papers in journals and at conferences.

16. I am a named inventor on over 40 U.S. Patents, many of which are in the field of memory design.

IV. Person of Ordinary Skill in the Art and State of The Art

17. In my opinion, a person of ordinary skill in the art as of the time of the '589 Patent would have a Master's degree in Electrical Engineering and at least 2 years'

experience working in the field of semiconductor memory design. I believe this to be a reasonable statement of the level of ordinary skill in the art for the patent and claims at issue. I also believe that I was one of ordinary skill in the art at the time the '589 Patent was filed.

18. The opinions that I provide in this declaration are consistent with the knowledge and experience of one of ordinary skill in the art at the priority date of the '589 Patent.

19. At the time of the '589 Patent's priority date, a standard initialization sequence was well known in the art, as specified in the JEDEC standard and as recognized in the specification of the '589 patent itself. *See* Ex. 1001 at 1:21-2:5 (describing JEDEC initialization sequence as prior art); *see also* Ex. 1007, JEDEC 21-C Standard at 115. It was further well known in the art that within this initialization sequence, at least 200 microseconds needed to elapse after powering on the DRAM in order to stabilize the electrical properties of the DRAM, including voltage. Moreover, those of ordinary skill in the art recognized that a DRAM control circuit could be used to carry out the JEDEC initialization sequence, by sending the various signals specified in the initialization sequence (such a reset signal, a clock enable signal, and a mode register set signal) such that the DRAM was ready for normal operation. *See* Ex. 1005 at Fig. 1; Ex. 1006 at Fig. 1.

DOCKET ALARM

Explore Litigation Insights

Docket Alarm provides insights to develop a more informed litigation strategy and the peace of mind of knowing you're on top of things.

Real-Time Litigation Alerts

Keep your litigation team up-to-date with **real-time alerts** and advanced team management tools built for the enterprise, all while greatly reducing PACER spend.

Our comprehensive service means we can handle Federal, State, and Administrative courts across the country.

Advanced Docket Research

With over 230 million records, Docket Alarm's cloud-native docket research platform finds what other services can't. Coverage includes Federal, State, plus PTAB, TTAB, ITC and NLRB decisions, all in one place.

Identify arguments that have been successful in the past with full text, pinpoint searching. Link to case law cited within any court document via Fastcase.

Analytics At Your Fingertips

Learn what happened the last time a particular judge, opposing counsel or company faced cases similar to yours.

Advanced out-of-the-box PTAB and TTAB analytics are always at your fingertips.

API

Docket Alarm offers a powerful API (application programming interface) to developers that want to integrate case filings into their apps.

LAW FIRMS
Build custom dashboards for your attorneys and clients with live data direct from the court.

Automate many repetitive legal tasks like conflict checks, document management, and marketing.

FINANCIAL INSTITUTIONS
Litigation and bankruptcy checks for companies and debtors.

E-DISCOVERY AND LEGAL VENDORS
Sync your system to PACER to automate legal marketing.