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Paper 9
Entered: May 2, 2017

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

KINGSTON TECHNOLOGY COMPANY, INC.,
Petitioner,

v.

POLARIS INNOVATIONS LTD.,
Patent Owner.

Case IPR2017-00238
Patent 6,157,589

Before SALLY C. MEDLEY, BARBARA A. PARVIS, and MATTHEW R. CLEMENTS, *Administrative Patent Judges*.

MEDLEY, *Administrative Patent Judge*.

DECISION
Denying Institution of *Inter Partes* Review
37 C.F.R. § 42.108

I. INTRODUCTION

Kingston Technology Company, Inc. ("Petitioner") filed a Petition for *inter partes* review of claims 11 and 12 of U.S. Patent No. 6,157,589 (Ex. 1001, "the '589 patent"). Paper 2 ("Pet."). Polaris Innovations Ltd. ("Patent Owner") filed a Preliminary Response. Paper 7 ("Prelim. Resp.").[1]

Institution of an *inter partes* review is authorized by statute when "the information presented in the petition . . . and any response . . . shows that there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition." 35 U.S.C. § 314(a); *see* 37 C.F.R. § 42.108. Upon consideration of the Petition and Preliminary Response, we conclude the information presented does not show there is a reasonable likelihood that Petitioner would prevail in establishing the unpatentability of claim 11 or claim 12 of the '589 Patent.

A. Related Matters

The parties state that the '589 Patent is the subject of a pending lawsuit in the Central District of California, i.e., *Polaris Innovations Ltd. v. Kingston Tech. Co.*, Case No. 8:16–cv-300 (C.D. Cal.). Pet. 2; Paper 4 (Patent Owner's Mandatory Notices), 1.

B. The '589 Patent

The '589 Patent is directed to a random access memory device (i.e., DRAM) having an initialization circuit which controls a switching-on operation of the semiconductor memory device and of its circuit

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[1] Subsequent to filing its Preliminary Response, Patent Owner filed a Motion for *pro hac vice* admission of Nathan Nobu Lowenstein. Paper 8. Because we do not institute trial, we *dismiss* the motion.

components. Ex. 1001, 1:9–13. Figure 1 of the '589 Patent is reproduced below.

Fig 1

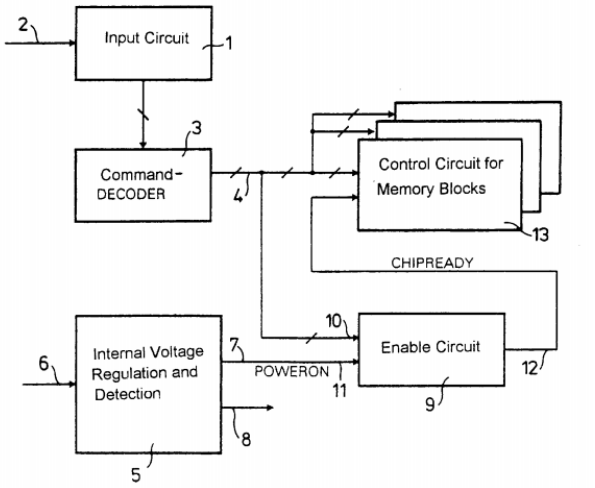

Figure 1 illustrates a schematic view of components of an initialization circuit that controls a switching-on operation of a semiconductor memory.

As shown in Figure 1 above, the initialization circuit has an input circuit 1, with input command and clock signals 2. *Id.* at 3:51–54. Input command and clock signals 2 are amplified and conditioned and then received by command decoder 3, whose output 4 includes PRE or PRECHARGE (preparation command for word line activation), ARF or AUTOREFRESH (refresh command), and MRS or MODE-REGISTER-SET (loading configuration register command). *Id.* at 3:54–61. The initialization circuit further has a circuit 5 for internal voltage regulation and/or detection, whose input 6 includes the external supply voltages that are externally applied to the semiconductor memory. *Id.* at 3:61–65. Circuit 5 has a first output 7 outputting a POWERON signal and a second output 8 supplying stabilized internal supply voltages. *Id.* at 3:65–67. In operation,

"circuit 5 supplies an active POWERUP signal if, after the POWERUP phase of the SDRAM memory, the internal supply voltages present at the output 8 have reached the values necessary for proper operation of the component." *Id.* at 4:4–8.

Figure 2 of the '589 Patent is reproduced below.

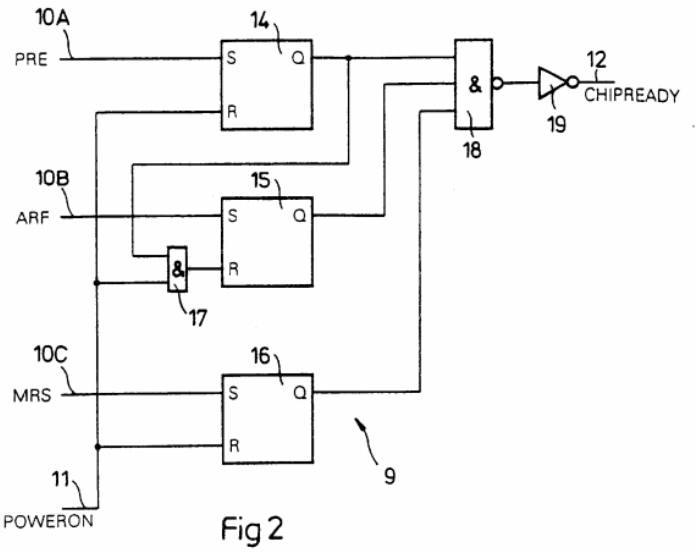

Fig 2

Figure 2 illustrates a circuit diagram of an enable circuit that supplies an enable signal (CHIPREADY).

Figure 2 above shows the details of the enable circuit 9. Enable circuit contains "three bistable multivibrator stages 14, 15 and 16 each having a set input S, a reset input R, and also an output Q." *Id.* at 4:25–28. An AND gate 17 is connected upstream of reset input R of multivibrator stage 15 and an AND gate 18 is connected downstream of outputs Q of multivibrator stages 14, 15, and 16. *Id.* at 4:25–31. The enable signal CHIPREADY is output at output 12 of inverter 19 and the enable signal CHIPREADY is active HIGH, i.e., activated when its voltage level is at a logic HIGH. The command signals PRE, ARF, MRS applied to respective set inputs S of 14, 15, and 16 are each active LOW. *Id.* at 4:31–40. The

supply voltage stable signal (POWERON) is applied to reset inputs R for multivibrator stages 14 and 16 and applied to input of AND gate 17 for multivibrator stage 15. *Id.* at 4:40–48.

In operation, activation of enable signal CHIPREADY at output 12 to logic HIGH is generated only when a predetermined chronological initialization sequence of command signals PRE, ARF, and MRS and activation of the POWERON signal to the logic level HIGH are detected. *Id.* at 4:48–55. "Only then are the control circuits 13 unlatched on account of the activation of the enable signal CHIPREADY; the control circuits 13 remaining latched prior to this." *Id.* at 4:55–58.

C. Illustrative Claim

Petitioner challenges independent claim 11 and dependent claim 12 which depends from claim 11. Independent claim 11, reproduced below, is illustrative of the claimed subject matter:

> 11. An improved method for initializing a dynamic semiconductor memory device of a random access type via an initialization circuit controlling a switching-on operation of the dynamic semiconductor memory device and of its circuit components, the improvement which comprises:
>
> supplying, via the initialization circuit, a supply voltage stable signal once a supply voltage has been stabilized after the switching-on operation of the dynamic semiconductor memory device; and
>
> supplying, via an enable circuit of the initialization circuit, an enable signal, the initialization circuit receiving the supply voltage stable signal and further command signals externally applied to the dynamic semiconductor memory device, after an identification of a predetermined proper initialization sequence of the further command signals the enable signal being generated and effecting an unlatching of a control

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