UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

APPLE INC.,
Petitioner,

v.

CALIFORNIA INSTITUTE OF TECHNOLOGY,
Patent Owner.

Case IPR2017-00219
Patent No. 7,116,710

DECLARATION OF DR. R. MICHAEL TANNER

I, Robert Michael Tanner, declare as follows:

I. QUALIFICATIONS

1. I am Chief Academic Counsel at the Association of Public and Land-grant Universities (APLU), in which position I have served since my retirement in 2015. I had previously served as APLU's Vice President for Academic Affairs and Chief Academic Officer since 2011.

2. Prior to my work at APLU, I taught as a professor of Computer Science and Electrical Engineering at the University of Illinois at Chicago and at the University of California, Santa Cruz. I also served in Vice Chancellor positions at both institutions, as well as other administrative roles. I have also been a visiting professor at institutions including the California Institute of Technology ("Caltech"), the Massachusetts Institute of Technology, and Stanford University, and I worked in the 1980's as a consultant to companies in the disk and telecommunication industry.

3. In 1981, I authored a paper titled "A Recursive Approach to Low Complexity Codes," in which I proposed a new method of graphically representing the constraint equations governing the codeword elements in sparse check matrix codes. This graphical representation, called a "Tanner graph," is named after me. My contributions to the field of coding have led me to be recognized as the founder of the subfield "codes on graphs."

4. My professional research interests have concentrated on topics involving information and communication theory, and on the theory of algorithms and computational complexity. Significant areas on which I have focused have included: a) development of highly efficient error-correcting codes that are amenable to decoding with ultra-concurrent iterative algorithms; and b) the theoretical and algorithmic reconciliation of block and convolutional codes.

5. I received a Ph.D. in Electrical Engineering with Specialization in Information Theory from Stanford in 1971. I also hold a Master's Degree from Stanford in Electrical Engineering and a Bachelor's Degree from Stanford in Electrical Engineering, which I received in 1967 and 1966, respectively.

6. A copy of my Curriculum Vitae, provided as Exhibit 2002, contains further details on my education, experience, publications, patents, and other qualifications to render an expert opinion in this matter.

II. SCOPE OF WORK

7. I was asked by counsel for Caltech in the case IPR2017-00219 to review U.S. Patent No. 7,116,710 ("the '710 patent") and related applications, including Provisional Application No. 60/205,095 ("the '095 provisional application"). I receive $400 per hour for my services. No part of my compensation is dependent on my opinions or on the outcome of this proceeding.

8. I was also asked by counsel for Caltech to review the papers "Analysis of Low Density Codes and Improved Designs Using Irregular Graphs," authored by Michael G. Luby et al. ("Luby," Ex. 1204) and "Coding Theorems for 'Turbo-Like' Codes" by Dariush Divsalar *et al* ("Divsalar," Ex. 1203).

9. I was further asked to provide my understanding of whether an irregular graph as discussed in Luby indicates that the underlying code includes irregular repetition of data elements.

10. Luby discloses decoding, but does not describe encoding. Luby does not disclose encoding involving repetition of information bits, much less encoding with irregular repetition as in the '710 patent claims. Divsalar discloses a coding scheme with regular repetition. As described in further detail below, a regular repeat-accumulate code as disclosed by Divsalar can be represented by an irregular graph, as defined by Luby, without any changes to the underlying code.

III. OVERVIEW OF IRREGULAR CODES IN LUBY AND IN THE '710 PATENT

11. The '710 patent discloses a serially-concatenated interleaved convolutional code with an outer code and an inner code. (Ex. 1201, Title, Abstract.) The outer code irregularly repeats bits in a data block, which are then scrambled by a permuter. (*Id*. at Abstract, 1:58-67.)

12. The specification of the '710 patent explains that the outer coder may be irregular, meaning that it could be a repeater that repeats the bits in a block a

particular number of times, and repeats bits in another block a different number of times. (*See id.* at 2:48-58.)

13. The scrambled, or interleaved, bits are then subjected to a second encoding, which includes one or more accumulators that perform modulo two addition. (*Id.* at 2:1-5, 2:65-3:17.)

14. Modulo two addition is an exclusive-or operation, often called XOR, and denoted with the symbol $\oplus$. The modulo-two addition of two bits is shown below:

A	**B**	**A⊕B**
0	0	0
0	1	1
1	0	1
1	1	0

15. As indicated above, the modulo-two addition of a value with itself is 0.

16. The '710 patent defines an accumulator as a block whose input block [x1, x2, … , xn] and output block [y1, . . . , yn] are related by the following formula:

$$y_1 = x_1$$

$$y_2 = x_1 \oplus x_2$$

$$y_3 = x_1 \oplus x_2 \oplus x_3$$

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