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12   **UNITED STATES DISTRICT COURT**

13   **CENTRAL DISTRICT OF CALIFORNIA**

14 THE CALIFORNIA INSTITUTE OF
   TECHNOLOGY,
15   Case No. 2:13-cv-07245-MRP-
                                            JEM
16   Plaintiff,

17   vs.   **JOINT CLAIM
                                            CONSTRUCTION AND
18 HUGHES COMMUNICATIONS INC.,   PREHEARING STATEMENT
   HUGHES NETWORK SYSTEMS LLC,   PURSUANT TO THE
   DISH NETWORK CORPORATION,   COURT'S AMENDED
19 DISH NETWORK LLC, and DISHNET   SCHEDULING ORDER
   SATELLITE BROADBAND LLC,   (DKT. NO. 47)
20
                    Defendant.
21
22   The Hon. Mariana R. Pfaelzer
                                            United States District Court Judge
23
24
                                            Hearing Date: July 9, 2014
25   Time: 1:30 p.m.
                                            Place: Courtroom 12
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1   Plaintiff The California Institute of Technology ("Caltech") and Defendants

2 Hughes Communications Inc., Hughes Network Systems LLC, DISH Network

3 Corporation, DISH Network LLC, and dishNET Satellite Broadband LLC

4 (collectively, "Hughes") hereby submit this Joint Claim Construction and

5 Prehearing Statement pursuant to the Court's Amended Scheduling Order (Dkt. No.

6 47).

7 **I.   AGREED CLAIM CONSTRUCTIONS**

8   The parties have reached agreement on the construction of the following

9 claim terms:

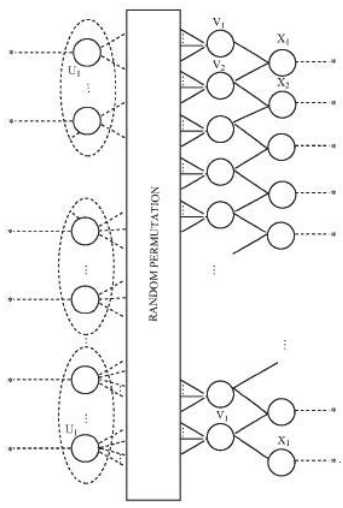| Claim Term(s)	Patent Claim(s)	Agreed Construction
"irregularly"	'710 patent, claim 15; '032 patent, claim 1	"a different number of times"
"interleaving" / "interleaver" / "scramble"	'710 patent, claims 1, 15, and 19	"changing the order of data elements" / "module that changes the order of data elements"
"sums of bits in subsets of the information bits" / "summing of bits in a subset of the information bits" / "adding additional subsets of information bits"	'781 patent, claims 6, 13, 20, 21, 22	"the result(s) of adding together two or more information bits from a subset of information bits" / "adding together two or more information bits from a subset of information bits"
"wherein two or more memory locations of the first set of memory locations are read by the permutation module different times from one another"	'833 patent, claims 1 and 8	"where two or more memory locations of the first set of memory locations are read by the permutation module a different number of times from one another"
"permutation module"	'833 patent, claims 1, 2, 3, 6 and 8	"a module that changes the order of data

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		elements"

If the parties reach agreement as to the constructions of additional terms at a later date, they will supplement the Joint Statement to reflect any such additional agreement.

II.   DISPUTED CLAIM CONSTRUCTIONS

The parties have identified the following terms as disputed, and respectfully request that they be construed by the Court:

Claim Term(s)	Patent Claim(s)	Caltech's Construction	Hughes's Construction
"repeat"	'710 patent, claims 1, 6, 11, 15,16, and 19	"re-use in forming a code"	"sequential duplication"
$$x_j = x_{j-1} + \sum_{i=1}^{a} v_{(j-1)(a+i)}$$	'032 claim 1	"The parity bit X_j is the sum of (a) the parity bit X_{j-1} and (b) the sum of a number, "a," of randomly chosen irregular repeats of the message bits"	This term is indefinite under 35 U.S.C. §112, ¶2. In the alternative, plain meaning.
	'032 patent, claims 11 and 18	The Tanner Graph shows the generation of parity bits (indicated by x_i) whose values are each determined by the constraints imposed by the check nodes (indicated by v_i) they are each connected to. Each check	This term is indefinite under 35 U.S.C. §112, ¶2. At a minimum, however, this limitation requires "at least three information bits, where each of the three information bits contributes to a

Claim Term(s)	Patent Claim(s)	Caltech's Construction	Hughes's Construction
		node is also randomly connected to message bits, where subsets of message bits are re-used a different number of times in forming the connections to check nodes; one subset will be re-used two times, one subset will be re-used three times, and at least one additional subset will be re-used more than three times. A check node imposes the constraint that the modulo-2 sum of all bits connected to it is "0."	different number of parity checks."
"transmitting" / "transmission"	'032 patent, claims 1, 8 and 10	"sending over a channel"	"sending over a physical channel"
"codeword"	'781 patent, claims 1-4, 11, 13-16, 19-21	"a discrete encoded sequence of data elements "	"a discrete sequence of data elements encoded for transmission"

Claim Term(s)	Patent Claim(s)	Caltech's Construction	Hughes's Construction
"combine"	'833 patent, claims 1, 2, 3, 8, 9, 10, and 13	"performing mod-2 addition or exclusive-OR sum and/or writing the sum to the second set of memory locations based on a corresponding index"	This term is indefinite under 35 U.S.C. §112, ¶2. In the alternative, plain meaning.

The parties respectfully reserve the right to amend, correct, or supplement their respective claim construction positions in response to any change of position by another party or for other good cause.

III.   ANTICIPATED LENGTH OF CLAIM CONSTRUCTION HEARING

The parties expect that the claim construction hearing will take three hours.

IV.   PROPOSED WITNESSES TO CALL

The parties do not intend to offer any live witness testimony at the claim construction hearing.

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