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Paper 77
Entered: December 27, 2018

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

APPLE INC.,
Petitioner,

v.

CALIFORNIA INSTITUTE OF TECHNOLOGY,
Patent Owner.

Case IPR2017-00210
Patent 7,116,710 B1

Before KEN B. BARRETT, TREVOR M. JEFFERSON, and JOHN A. HUDALLA, *Administrative Patent Judges*.

JEFFERSON, *Administrative Patent Judge*.

FINAL WRITTEN DECISION
35 U.S.C. § 318(a) and 37 C.F.R. § 42.73

I. INTRODUCTION

Petitioner, Apple, Inc. ("Apple"), filed a Petition (Paper 5, "Pet.") requesting an *inter partes* review of claims 1–8, 10–17, and 19–33 of U.S. Patent No. 7,116,710 B1 (Ex. 1001, "the '710 patent") pursuant to 35 U.S.C. §§ 311–319. Patent Owner, California Institute of Technology ("Caltech"), filed a Preliminary Response (Paper 17, "Prelim. Resp.") to the Petition.

We instituted an *inter partes* review on claims 1–8, 11–17, 19–22, and 24–33 of the '710 patent on certain grounds of unpatentability presented. (Paper 18, "Inst. Dec."). Caltech filed a Patent Owner Response (Paper 35, "PO Resp."), and Apple filed a Petitioner Reply (Paper 46, "Pet. Reply"). Caltech also filed a Sur-Reply (Paper 62, "PO Sur-Reply"), as was authorized by our Order of March 2, 2018 (Paper 55). An oral hearing was held on April 19, 2018, and a transcript of the hearing is included in the record. Paper 72 ("Tr.").

Apple filed a Declaration of James A. Davis, Ph.D. (Ex. 1006) with its Petition and a Declaration of Brendan Frey, Ph.D. (Ex. 1065) with its Reply. Caltech filed Declarations of Dr. Dariush Divsalar (Ex. 2031) and Dr. Michael Mitzenmacher (Ex. 2004) with its Response.

As authorized in our Order of February 10, 2018 (Paper 48), Patent Owner filed a motion for sanctions related to Petitioner's cross-examination of Patent Owner's witnesses, Dr. Mitzenmacher (Paper 50) and Dr. Divsalar, and Petitioner filed an opposition (Paper 52).

In light of the U.S. Supreme Court's decision in *SAS Institute, Inc. v. Iancu*, 138 S. Ct. 1348 (2018), we modified our Institution Decision to institute on all of the challenged claims and all of the grounds. Paper 69. Subsequently, the parties filed a joint motion to limit the Petitions to the

claims and grounds that were originally instituted. Paper 71. We granted their motion. Paper 73. As a result, the remaining instituted claims and grounds are the same as they had been at the time of the Institution Decision. *See id.* at 3.

The one-year period normally available to issue a Final Written Decision was extended under 37 C.F.R. § 42.100(c). Papers 74, 75, 1–2.

We have jurisdiction under 35 U.S.C. § 6. This decision is a Final Written Decision under 35 U.S.C. § 318(a) as to the patentability of claims 1–8, 11–17, 19–22, and 24–33 of the '710 patent. For the reasons discussed below, Petitioner has not demonstrated by a preponderance of the evidence that claims that claims 1–8, 11–17, 19–22, and 24–33 are unpatentable.

A. Related Proceedings

The parties indicate that the '710 patent was involved in the following active case, *Cal. Inst. of Tech. v. Broadcom Ltd.*, No. 2:16-cv-03714 (C.D. Cal. filed May 26, 2016), and in concluded cases, *Cal. Inst. of Tech. v. Hughes Commc'ns, Inc.*, No. 2:15-cv-01108 (C.D. Cal. filed Feb. 17, 2015); and *Cal. Inst. of Tech. v. Hughes Commc'ns, Inc.*, 2:13-cv-07245 (C.D. Cal. filed Oct. 1, 2013). Pet. 3, Paper 8, 2–3.

The parties also identify co-pending case IPR2017-00219, in which Apple filed a petition for *inter partes* review of the '710 patent. Pet. 3; Paper 8, 2–3. *Inter partes* review of the '710 patent was previously considered and denied in *Hughes Network Sys., LLC v. Cal. Inst. of Tech.*, IPR2015-00067 (PTAB April 27, 2015) (Paper 18) ("IPR2015-00067") and *Hughes Network Sys., LLC v. Cal. Inst. of Tech.*, IPR2015-00068 (PTAB

April 27, 2015) ("IPR2015-00068"). Finally, patents related to the '710 patent were challenged in IPR2015-00059, IPR2015-00060, IPR2015-00061, and IPR2015-00081. Pet. 3.

B. The '710 Patent

The '710 patent describes the serial concatenation of interleaved convolutional codes forming turbo-like codes. Ex. 1001, Title. It explains some of the prior art with reference to its Fig. 1, reproduced below.

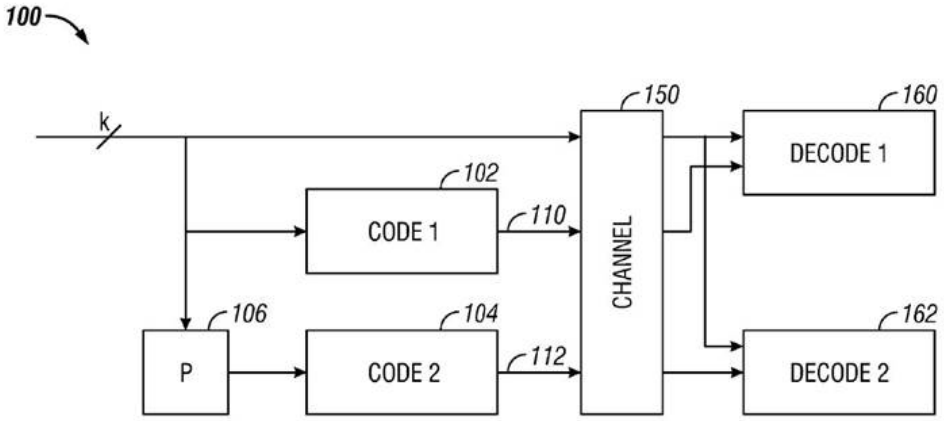

FIG. 1
(Prior Art)

Figure 1 is a schematic diagram of a prior "turbo code" system. *Id.* at 2:14–15. The '710 patent specification describes Figure 1 as follows:

> A standard turbo coder 100 is shown in FIG. 1. A block of k information bits is input directly to a first coder 102. A k bit interleaver 106 also receives the k bits and interleaves them prior to applying them to a second coder 104. The second coder produces an output that has more bits than its input, that is, it is a coder with rate that is less than 1. The coders 102,104 are typically recursive convolutional coders.
>
> Three different items are sent over the channel 150: the original k bits, first encoded bits 110, and second encoded bits 112. At the decoding end, two decoders are used: a first

> constituent decoder 160 and a second constituent decoder 162. Each receives both the original k bits, and one of the encoded portions 110, 112. Each decoder sends likelihood estimates of the decoded bits to the other decoders. The estimates are used to decode the uncoded information bits as corrupted by the noisy channel.

Id. at 1:38–53(emphasis omitted).

A coder 200, according to a first embodiment of the invention, is described with respect to Figure 2, reproduced below.

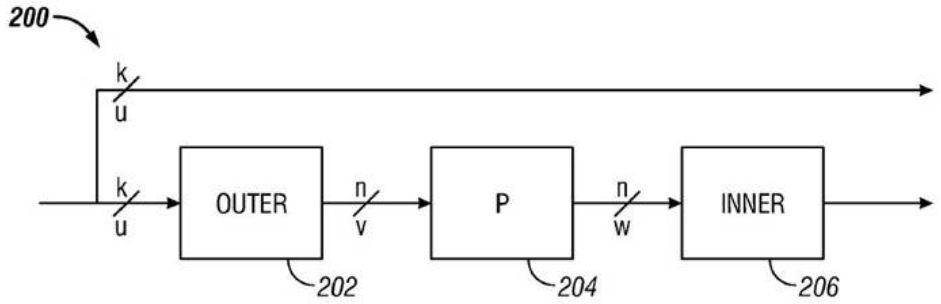

FIG. 2

Figure 2 of the '710 patent is a schematic diagram of coder 200. *Id.* at 2:16–17.

The specification states that "coder 200 may include an outer coder 202, an interleaver 204, and inner coder 206." *Id.* at 2:34–35. It further states as follows:

> The outer coder 202 receives uncoded data. The data may be partitioned into blocks of fixed size, say k bits. The outer coder may be an (n,k) binary linear block coder, where n>k. The coder accepts as input a block u of k data bits and produces an output block v of n data bits. The mathematical relationship between u and v is $v=T_0u$, where T_0 is an $n\times k$ matrix, and the rate[1] of the coder is k/n.

[1] The "rate" of an encoder refers to the ratio of the number of input bits to the number of resulting encoded output bits related to those input bits. *See* Pet. 9.

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