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(54) **SERIAL CONCATENATION OF INTERLEAVED CONVOLUTIONAL CODES FORMING TURBO-LIKE CODES**

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H04B 1/66 (2006.01)

(52) **U.S. Cl.** **375/240**; 375/262; 375/265; 375/341; 341/51; 341/102; 714/752

(58) **Field of Classification Search** 375/259, 375/262, 265, 285, 296, 341, 346, 348; 714/746, 714/752, 755, 756, 786, 792, 794, 795, 796; 341/51, 52, 56, 102, 103
See application file for complete search history.

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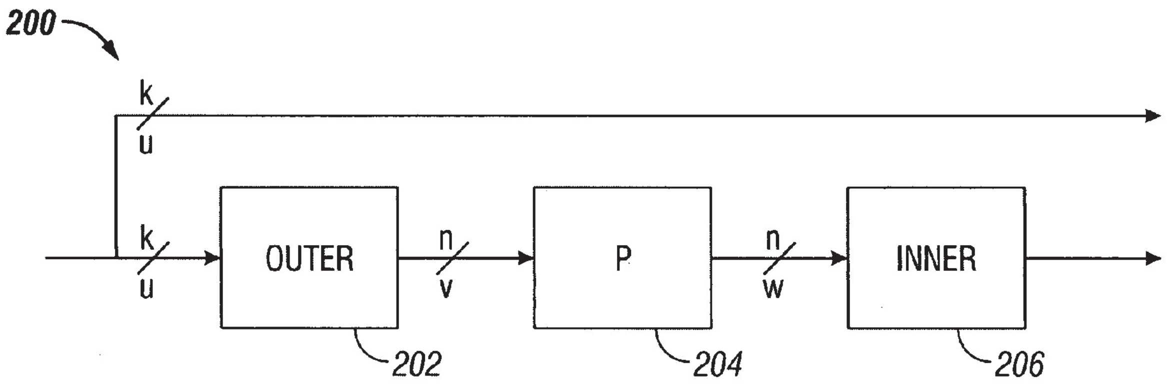
(57) **ABSTRACT**

A serial concatenated coder includes an outer coder and an inner coder. The outer coder irregularly repeats bits in a data block according to a degree profile and scrambles the repeated bits. The scrambled and repeated bits are input to an inner coder, which has a rate substantially close to one.

33 Claims, 5 Drawing Sheets



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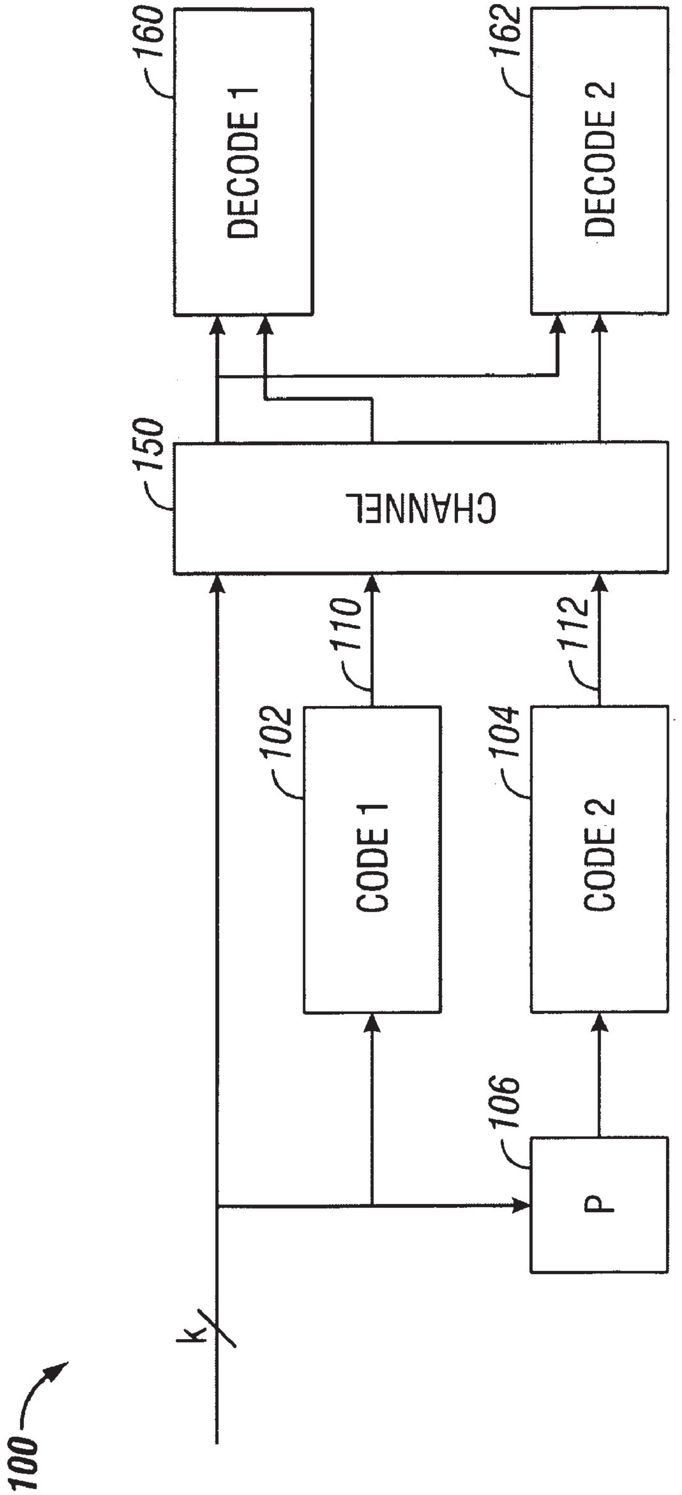

FIG. 1
(Prior Art)

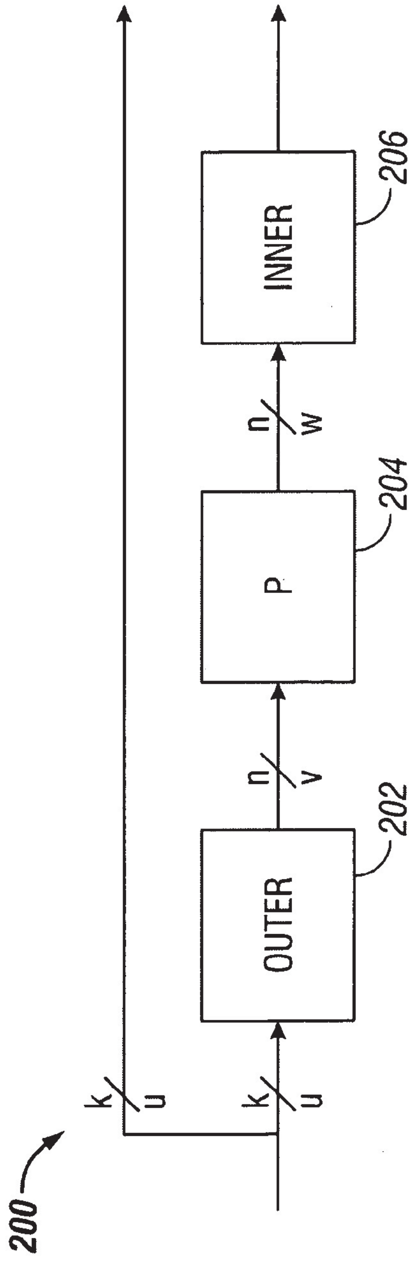

FIG. 2

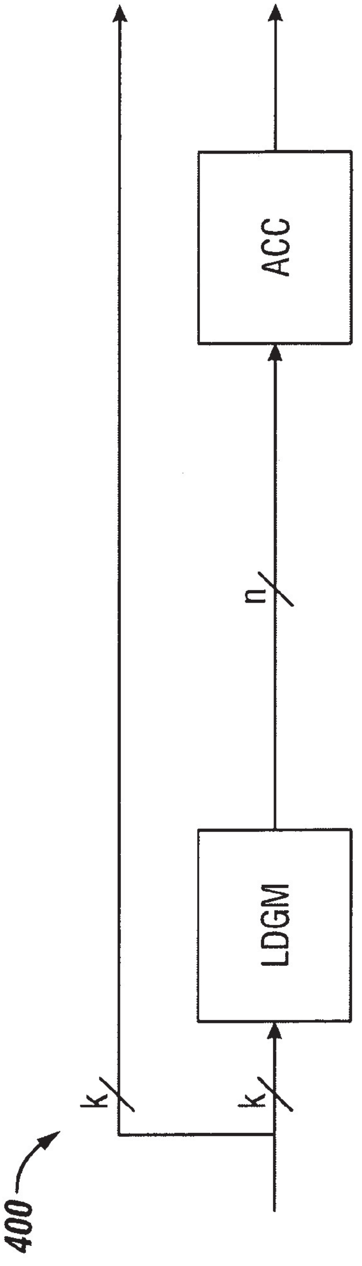

FIG. 4

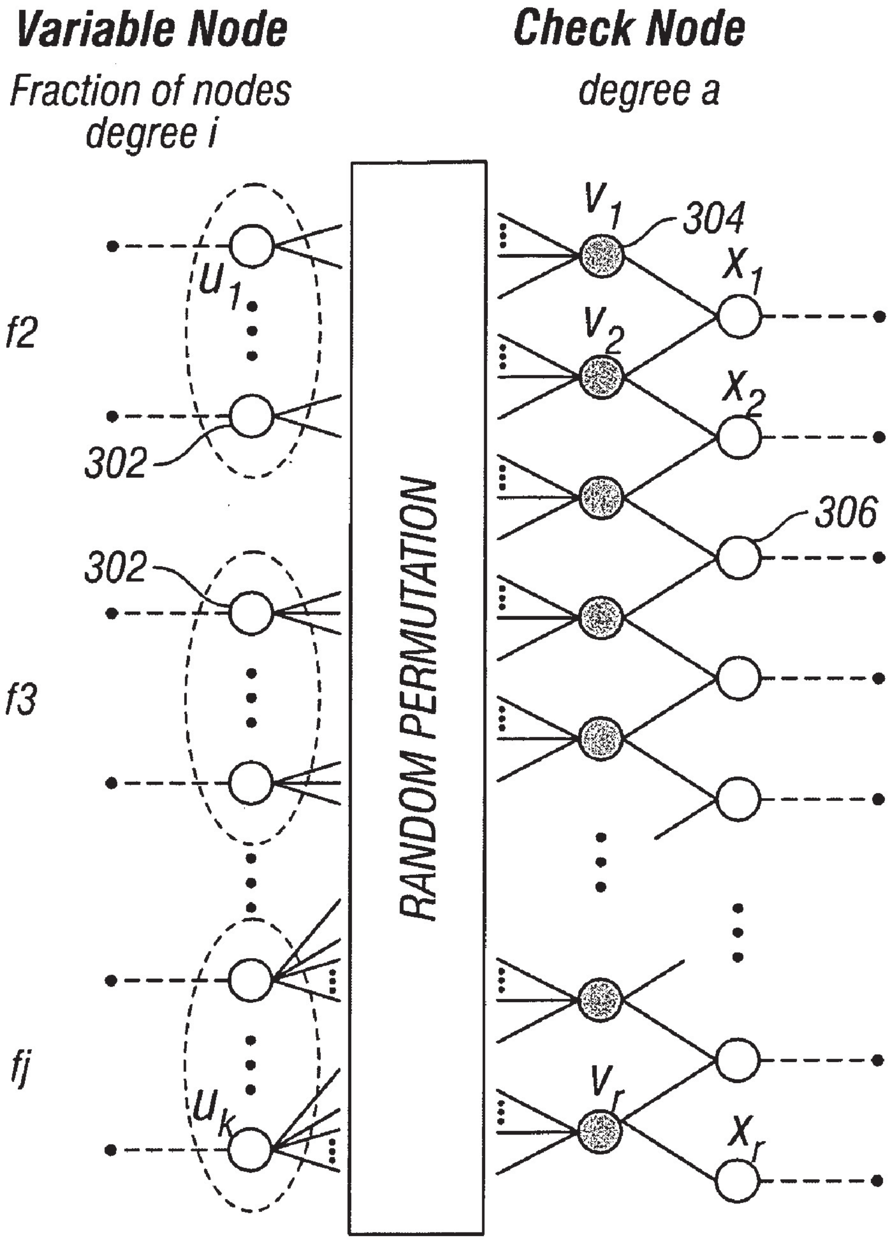
Variable Node
Fraction of nodes degree i
Check Node
degree a
RANDOM PERMUTATION
u_1
u_k
f2
f3
fj
302
302
v_1
v_2
v_r
304
x_1
x_2
x_r
306

FIG. 3

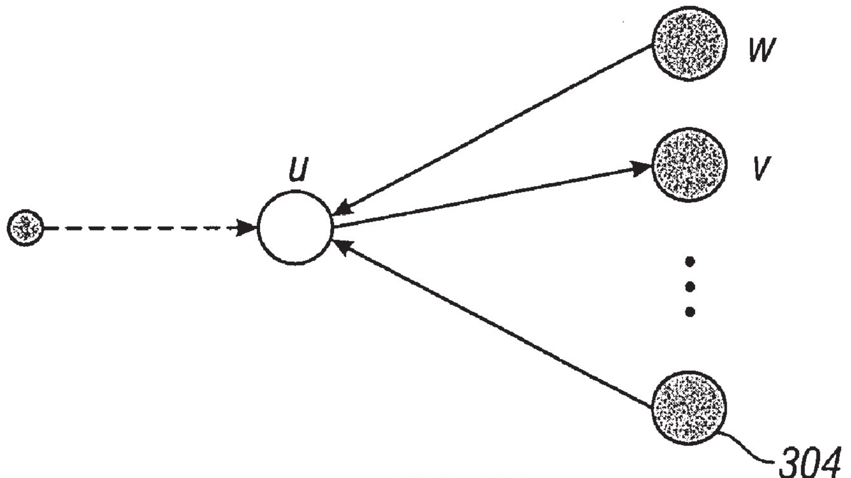

FIG. 5A

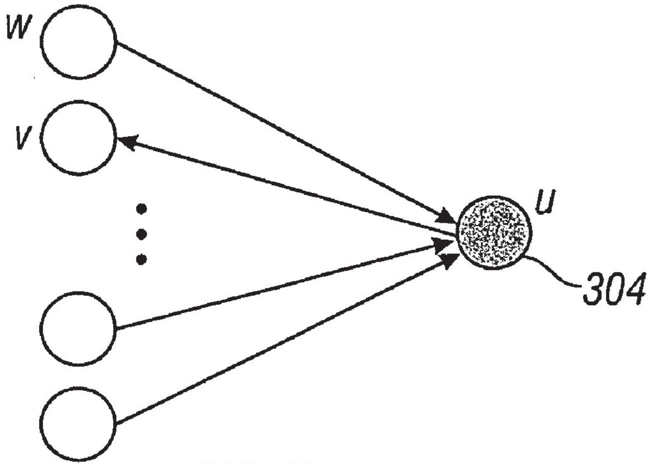

FIG. 5B

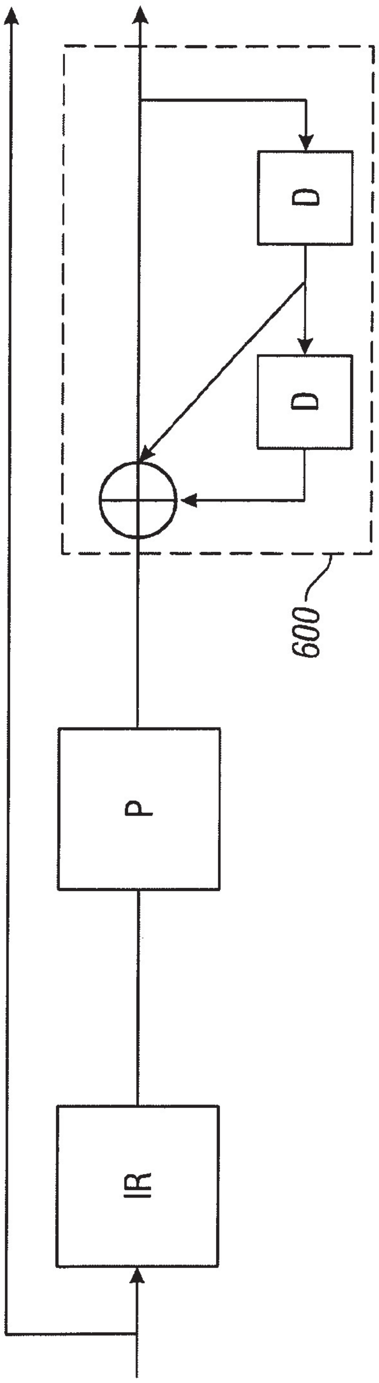

FIG. 6

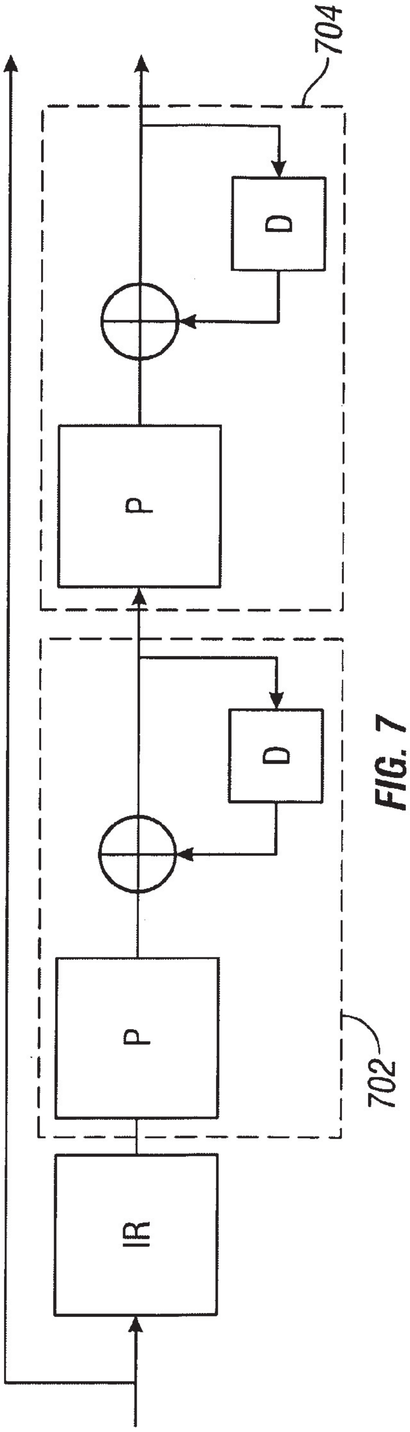

FIG. 7

SERIAL CONCATENATION OF INTERLEAVED CONVOLUTIONAL CODES FORMING TURBO-LIKE CODES

CROSS-REFERENCE TO RELATED APPLICATIONS

This application claims priority to U.S. Provisional Application Ser. No. 60/205,095, filed on May 18, 2000, and to U.S. application Ser. No. 09/922,852, filed on Aug. 18, 2000 and entitled Interleaved Serial Concatenation Forming Turbo-Like Codes.

GOVERNMENT LICENSE RIGHTS

The U.S. Government has a paid-up license in this invention and the right in limited circumstances to require the patent owner to license others on reasonable terms as provided for by the terms of Grant No. CCR-9804793 awarded by the National Science Foundation.

BACKGROUND

Properties of a channel affect the amount of data that can be handled by the channel. The so-called "Shannon limit" defines the theoretical limit of the amount of data that a channel can carry.

Different techniques have been used to increase the data rate that can be handled by a channel. "Near Shannon Limit Error-Correcting Coding and Decoding: Turbo Codes," by Berrou et al. ICC, pp 1064–1070, (1993), described a new "turbo code" technique that has revolutionized the field of error correcting codes. Turbo codes have sufficient randomness to allow reliable communication over the channel at a high data rate near capacity. However, they still retain sufficient structure to allow practical encoding and decoding algorithms. Still, the technique for encoding and decoding turbo codes can be relatively complex.

A standard turbo coder **100** is shown in FIG. **1**. A block of k information bits is input directly to a first coder **102**. A k bit interleaver **106** also receives the k bits and interleaves them prior to applying them to a second coder **104**. The second coder produces an output that has more bits than its input, that is, it is a coder with rate that is less than 1. The coders **102**, **104** are typically recursive convolutional coders.

Three different items are sent over the channel **150**: the original k bits, first encoded bits **110**, and second encoded bits **112**. At the decoding end, two decoders are used: a first constituent decoder **160** and a second constituent decoder **162**. Each receives both the original k bits, and one of the encoded portions **110**, **112**. Each decoder sends likelihood estimates of the decoded bits to the other decoders. The estimates are used to decode the uncoded information bits as corrupted by the noisy channel.

SUMMARY

A coding system according to an embodiment is configured to receive a portion of a signal to be encoded, for example, a data block including a fixed number of bits. The coding system includes an outer coder, which repeats and scrambles bits in the data block. The data block is apportioned into two or more sub-blocks, and bits in different sub-blocks are repeated a different number of times according to a selected degree profile. The outer coder may include a repeater with a variable rate and an interleaver. Alternatively, the outer coder may be a low-density generator matrix (LDGM) coder.

The repeated and scrambled bits are input to an inner coder that has a rate substantially close to one. The inner coder may include one or more accumulators that perform recursive modulo two addition operations on the input bit stream.

The encoded data output from the inner coder may be transmitted on a channel and decoded in linear time at a destination using iterative decoding techniques. The decoding techniques may be based on a Tanner graph representation of the code.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** is a schematic diagram of a prior "turbo code" system.

FIG. **2** is a schematic diagram of a coder according to an embodiment.

FIG. **3** is a Tanner graph for an irregular repeat and accumulate (IRA) coder.

FIG. **4** is a schematic diagram of an IRA coder according to an embodiment.

FIG. **5**A illustrates a message from a variable node to a check node on the Tanner graph of FIG. **3**.

FIG. **5**B illustrates a message from a check node to a variable node on the Tanner graph of FIG. **3**.

FIG. **6** is a schematic diagram of a coder according to an alternate embodiment.

FIG. **7** is a schematic diagram of a coder according to another alternate embodiment.

DETAILED DESCRIPTION

FIG. **2** illustrates a coder **200** according to an embodiment. The coder **200** may include an outer coder **202**, an interleaver **204**, and inner coder **206**. The coder may be used to format blocks of data for transmission, introducing redundancy into the stream of data to protect the data from loss due to transmission errors. The encoded data may then be decoded at a destination in linear time at rates that may approach the channel capacity.

The outer coder **202** receives the uncoded data. The data may be partitioned into blocks of fixed size, say k bits. The outer coder may be an (n,k) binary linear block coder, where n>k. The coder accepts as input a block u of k data bits and produces an output block v of n data bits. The mathematical relationship between u and v is $v=T_0u$, where T_0 is an n×k matrix, and the rate of the coder is k/n.

The rate of the coder may be irregular, that is, the value of T_0 is not constant, and may differ for sub-blocks of bits in the data block. In an embodiment, the outer coder **202** is a repeater that repeats the k bits in a block a number of times q to produce a block with n bits, where n=qk. Since the repeater has an irregular output, different bits in the block may be repeated a different number of times. For example, a fraction of the bits in the block may be repeated two times, a fraction of bits may be repeated three times, and the remainder of bits may be repeated four times. These fractions define a degree sequence, or degree profile, of the code.

The inner coder **206** may be a linear rate-1 coder, which means that the n-bit output block x can be written as $x=T_Iw$, where T_I is a nonsingular n×n matrix. The inner coder **210** can have a rate that is close to 1, e.g., within 50%, more preferably 10% and perhaps even more preferably within 1% of 1.

In an embodiment, the inner coder **206** is an accumulator, which produces outputs that are the modulo two (mod-2) partial sums of its inputs. The accumulator may be a truncated rate-1 recursive convolutional coder with the transfer function 1/(1+D). Such an accumulator may be considered a block coder whose input block $[x_1, \ldots, x_n]$ and output block $[y_1, \ldots, y_n]$ are related by the formula

$$y_1 = x_1$$

$$y_2 = x_1 \oplus x_2$$

$$y_3 = x_1 \oplus x_2 \oplus x_3$$

$$y_n = x_1 \oplus x_2 \oplus x_3 \oplus \ldots \oplus x_n.$$

where "⊕" denotes mod-2, or exclusive-OR (XOR), addition. An advantage of this system is that only mod-2 addition is necessary for the accumulator. The accumulator may be embodied using only XOR gates, which may simplify the design.

The bits output from the outer coder **202** are scrambled before they are input to the inner coder **206**. This scrambling may be performed by the interleaver **204**, which performs a pseudo-random permutation of an input block v, yielding an output block w having the same length as v.

The serial concatenation of the interleaved irregular repeat code and the accumulate code produces an irregular repeat and accumulate (IRA) code. An IRA code is a linear code, and as such, may be represented as a set of parity checks. The set of parity checks may be represented in a bipartite graph, called the Tanner graph, of the code. FIG. **3** shows a Tanner graph **300** of an IRA code with parameters $(f_1, \ldots, f_j; a)$, where $f_i \geqq 0$, $\Sigma_i f_i = 1$ and "a" is a positive integer. The Tanner graph includes two kinds of nodes: variable nodes (open circles) and check nodes (filled circles). There are k variable nodes **302** on the left, called information nodes. There are r variable nodes **306** on the right, called parity nodes. There are $r = (k\Sigma_i i f_i)/a$ check nodes **304** connected between the information nodes and the parity nodes. Each information node **302** is connected to a number of check nodes **304**. The fraction of information nodes connected to exactly i check nodes is f_i. For example, in the Tanner graph **300**, each of the f_2 information nodes are connected to two check nodes, corresponding to a repeat of q=2, and each of the f_3 information nodes are connected to three check nodes, corresponding to q=3.

Each check node **304** is connected to exactly "a" information nodes **302**. In FIG. **3**, a=3. These connections can be made in many ways, as indicated by the arbitrary permutation of the ra edges joining information nodes **302** and check nodes **304** in permutation block **310**. These connections correspond to the scrambling performed by the interleaver **204**.

In an alternate embodiment, the outer coder **202** may be a low-density generator matrix (LDGM) coder that performs an irregular repeat of the k bits in the block, as shown in FIG. **4**. As the name implies, an LDGM code has a sparse (low-density) generator matrix. The IRA code produced by the coder **400** is a serial concatenation of the LDGM code and the accumulator code. The interleaver **204** in FIG. **2** may be excluded due to the randomness already present in the structure of the LDGM code.

If the permutation performed in permutation block **310** is fixed, the Tanner graph represents a binary linear block code with k information bits $(u_1, \ldots, u_k)$ and r parity bits $(x_1, \ldots, x_r)$, as follows. Each of the information bits is associated with one of the information nodes **302**, and each of the parity bits is associated with one of the parity nodes **306**. The value of a parity bit is determined uniquely by the condition that the mod-2 sum of the values of the variable nodes connected to each of the check nodes **304** is zero. To see this, set $x_0 = 0$. Then if the values of the bits on the ra edges coming out the permutation box are $(v_1, \ldots, v_{ra})$, then we have the recursive formula

$$x_j = x_{j-1} + \sum_{i=1}^{\lambda} v_{(j-1)\lambda+i}$$

for j=1, 2, . . . , r. This is in effect the encoding algorithm.

Two types of IRA codes are represented in FIG. **3**, a nonsystematic version and a systematic version. The nonsystematic version is an (r,k) code, in which the codeword corresponding to the information bits $(u_1, \ldots, u_k)$ is $(x_1, \ldots, x_r)$. The systematic version is a (k+r, k) code, in which the codeword is $(u_1, \ldots, u_k; x_1, \ldots, x_r)$.

The rate of the nonsystematic code is

$$R_{nsys} = \frac{a}{\sum_i i f_i}$$

The rate of the systematic code is

$$R_{sys} = \frac{a}{a + \sum_i i f_i}$$

For example, regular repeat and accumulate (RA) codes can be considered nonsystematic IRA codes with a=1 and exactly one f_i equal to 1, say $f_q = 1$, and the rest zero, in which case R_{nsys} simplifies to R=1/q.

The IRA code may be represented using an alternate notation. Let λ_i be the fraction of edges between the information nodes **302** and the check nodes **304** that are adjacent to an information node of degree i, and let ρ_i be the fraction of such edges that are adjacent to a check node of degree i+2 (i.e., one that is adjacent to i information nodes). These edge fractions may be used to represent the IRA code rather than the corresponding node fractions. Define $\lambda(x) = \Sigma_i \lambda_i x^{i-1}$ and $\rho(x) = \Sigma_i \rho_i x^{i-1}$ to be the generating functions of these sequences. The pair (λ, ρ) is called a degree distribution. For $L(x) = \Sigma_i f_i x_i$,

$$f_i = \frac{\lambda_i / i}{\sum_j \lambda_j / j}$$

$$L(x) = \int_0^x \lambda(t)\,dt \Big/ \int_0^1 \lambda(t)\,dt$$

The rate of the systematic IRA code given by the degree distribution is given by

$$\text{Rate} = \left(1 + \frac{\sum_j \rho_j / j}{\sum_j \lambda_j / j}\right)^{-1}$$

"Belief propagation" on the Tanner Graph realization may be used to decode IRA codes. Roughly speaking, the belief propagation decoding technique allows the messages passed on an edge to represent posterior densities on the bit associated with the variable node. A probability density on a bit is a pair of non-negative real numbers p(0), p(1) satisfying p(0)+p(1)=1, where p(0) denotes the probability of the bit being 0, p(1) the probability of it being 1. Such a pair can be represented by its log likelihood ratio, m=log(p(0)/p(1)). The outgoing message from a variable node u to a check node v represents information about u, and a message from a check node u to a variable node v represents information about u, as shown in FIGS. **5**A and **5**B, respectively.

The outgoing message from a node u to a node v depends on the incoming messages from all neighbors w of u except v. If u is a variable message node, this outgoing message is

$$m(u \to v) = \sum_{w \neq v} m(w \to u) + m_0(u)$$

where $m_0(u)$ is the log-likelihood message associated with u. If u is a check node, the corresponding formula is

$$\tan h\frac{m(u \to v)}{2} = \prod_{w \neq v} \tan h\frac{m(w \to u)}{2}$$

Before decoding, the messages m(w→u) and m(u→v) are initialized to be zero, and $m_0(u)$ is initialized to be the log-likelihood ratio based on the channel received information. If the channel is memoryless, i.e., each channel output only relies on its input, and y is the output of the channel code bit u, then $m_0(i)=\log(p(u=0|y)/p(u=1|y))$. After this initialization, the decoding process may run in a fully parallel and local manner. In each iteration, every variable/check node receives messages from its neighbors, and sends back updated messages. Decoding is terminated after a fixed number of iterations or detecting that all the constraints are satisfied. Upon termination, the decoder outputs a decoded sequence based on the messages $m(u)=\Sigma w_m(w \to u)$.

Thus, on various channels, iterative decoding only differs in the initial messages $m_0(u)$. For example, consider three memoryless channel models: a binary erasure channel (BEC); a binary symmetric channel (BSC); and an additive white Gaussian noise (AGWN) channel.

In the BEC, there are two inputs and three outputs. When 0 is transmitted, the receiver can receive either 0 or an erasure E. An erasure E output means that the receiver does not know how to demodulate the output. Similarly, when 1 is transmitted, the receiver can receive either 1 or E. Thus, for the BEC, y∈{0, E, 1}, and

$$m_0(u) = \begin{cases} +\infty & \text{if } y = 0 \\ 0 & \text{if } y = E \\ -\infty & \text{if } y = 1 \end{cases}$$

In the BSC, there are two possible inputs (0,1) and two possible outputs (0, 1). The BSC is characterized by a set of conditional probabilities relating all possible outputs to possible inputs. Thus, for the BSC y∈{0, 1},

$$m_0(u) = \begin{cases} \log\frac{1-p}{p} & \text{if } y = 0 \\ -\log\frac{1-p}{p} & \text{if } y = 1 \end{cases}$$

and

In the AWGN, the discrete-time input symbols X take their values in a finite alphabet while channel output symbols Y can take any values along the real line. There is assumed to be no distortion or other effects other than the addition of white Gaussian noise. In an AWGN with a Binary Phase Shift Keying (BPSK) signaling which maps 0 to the symbol with amplitude $\sqrt{Es}$ and 1 to the symbol with amplitude $-\sqrt{Es}$, output y∈R, then

$$m_0(u)=4y\sqrt{E_s}/N_0$$

where $N_0/2$ is the noise power spectral density.

The selection of a degree profile for use in a particular transmission channel is a design parameter, which may be affected by various attributes of the channel. The criteria for selecting a particular degree profile may include, for example, the type of channel and the data rate on the channel. For example, Table 1 shows degree profiles that have been found to produce good results for an AWGN channel model.

TABLE 1

a	2	3	4
λ2	0.139025	0.078194	0.054485
λ3	0.2221555	0.128085	0.104315
λ5		0.160813	
λ6	0.638820	0.036178	0.126755
λ10			0.229816
λ11			0.016484
λ12		0.108828	
λ13		0.487902	
λ14			
λ16			
λ27			0.450302
λ28			0.017842
Rate	0.333364	0.333223	0.333218
σGA	1.1840	1.2415	1.2615
σ*	1.1981	1.2607	1.2780
(Eb/N0) * (dB)	0.190	−0.250	−0.371
S.L. (dB)	−0.4953	−0.4958	−0.4958

Table 1 shows degree profiles yielding codes of rate approximately ⅓ for the AWGN channel and with a=2, 3, 4. For each sequence, the Gaussian approximation noise threshold, the actual sum-product decoding threshold and the corresponding energy per bit (E_b)-noise power (N_0) ratio in dB are given. Also listed is the Shannon limit (S.L.).

As the parameter "a" is increased, the performance improves. For example, for a=4, the best code found has an iterative decoding threshold of $E_b/N_0=-0.371$ dB, which is only 0.12 dB above the Shannon limit.

The accumulator component of the coder may be replaced by a "double accumulator" **600** as shown in FIG. **6**. The double accumulator can be viewed as a truncated rate 1 convolutional coder with transfer function $1/(1+D+D^2)$.

Alternatively, a pair of accumulators may be the added, as shown in FIG. **7**. There are three component codes: the "outer" code **700**, the "middle" code **702**, and the "inner" code **704**. The outer code is an irregular repetition code, and the middle and inner codes are both accumulators.

IRA codes may be implemented in a variety of channels, including memoryless channels, such as the BEC, BSC, and AWGN, as well as channels having non-binary input, non-symmetric and fading channels, and/or channels with memory.

A number of embodiments have been described. Nevertheless, it will be understood that various modifications may be made without departing from the spirit and scope of the invention. Accordingly, other embodiments are within the scope of the following claims.

The invention claimed is:

1. A method of encoding a signal, comprising:

obtaining a block of data in the signal to be encoded;

partitioning said data block into a plurality of sub-blocks, each sub-block including a plurality of data elements;

first encoding the data block to from a first encoded data block, said first encoding including repeating the data elements in different sub-blocks a different number of times;

interleaving the repeated data elements in the first encoded data block; and

second encoding said first encoded data block using an encoder that has a rate close to one.

2. The method of claim **1**, wherein said second encoding is via a rate 1 linear transformation.

3. The method of claim **1**, wherein said first encoding is carried out by a first coder with a variable rate less than one, and said second encoding is carried out by a second coder with a rate substantially close to one.

4. The method of claim **3**, wherein the second coder comprises an accumulator.

5. The method of claim **4**, wherein the data elements comprises bits.

6. The method of claim **5**, wherein the first coder comprises a repeater operable to repeat different sub-blocks a different number of times in response to a selected degree profile.

7. The method of claim **4**, wherein the first coder comprises a low-density generator matrix coder and the second coder comprises an accumulator.

8. The method of claim **1**, wherein the second encoding uses a transfer function of $1/(1+D)$.

9. The method of claim **1**, wherein the second encoding uses a transfer function of $1/(1+D+D^2)$.

10. The method of claim **1**, wherein said second encoding utilizes two accumulators.

11. A method of encoding a signal, comprising:

receiving a block of data in the signal to be encoded, the data block including a plurality of bits;

first encoding the data block such that each bit in the data block is repeated and two or more of said plurality of bits are repeated a different number of times in order to form a first encoded data block; and

second encoding the first encoded data block in such a way that bits in the first encoded data block are accumulated.

12. The method of claim **11**, wherein the said second encoding is via a rate 1 linear transformation.

13. The method of claim **11**, wherein the first encoding is via a low-density generator matrix transformation.

14. The method of claim **11**, wherein the signal to be encoded comprises a plurality of data blocks of fixed size.

15. A coder comprising:

a first coder having an input configured to receive a stream of bits, said first coder operative to repeat said stream of bits irregularly and scramble the repeated bits; and

a second coder operative to further encode bits output from the first coder at a rate within 10% of one.

16. The coder of claim **15**, wherein the stream of bits includes a data block, and wherein the first coder is operative to apportion said data block into a plurality of sub-blocks and to repeat bits in each sub-block a number of times, wherein bits in different sub-blocks are repeated a different number of times.

17. The coder of claim **16**, wherein the second coder comprises a recursive convolutional encoder with a transfer function of $1/(1+D)$.

18. The coder of claim **16**, wherein the second coder comprises a recursive convolutional encoder with a transfer function of $1/(1+D+D^2)$.

19. The coder of claim **15**, wherein the first coder comprises a repeater having a variable rate and an interleaver.

20. The coder of claim **15**, wherein the first coder comprises a low-density generator matrix coder.

21. The coder of claim **15**, wherein the second coder comprises a rate 1 linear encoder.

22. The coder of claim **21**, wherein the second coder comprises an accumulator.

23. The coder of claim **22**, wherein the second coder further comprises a second accumulator.

24. The coder of claim **15**, wherein the second coder comprises a coder operative to further encode bits output from the first coder at a rate within 1% of one.

25. A coding system comprising:

a first coder having an input configured to receive a stream of bits, said first coder operative to repeat said stream of bits irregularly and scramble the repeated bits;

a second coder operative to further encode bits output from the first coder at a rate within 10% of one in order to form an encoded data stream; and

a decoder operative to receive the encoded data stream and decode the encoded data stream using an iterative decoding technique.

26. The coding system of claim **25**, wherein the first coder comprises a repeater operative to receive a data block including a plurality of bits from said stream of bits and to repeat bits in the data block a different number of times according to a selected degree profile.

27. The coding system of claim **26**, wherein the first coder comprises an interleaver.

28. The coding system of claim **25**, wherein the first coder comprises a low-density generator matrix coder.

29. The coding system of claim **25**, wherein the second coder comprises a rate 1 accumulator.

30. The coding system of claim **25**, wherein the decoder is operative to decode the encoded data stream using a posterior decoding techniques.

31. The coding system of claim **25**, wherein the decoder is operative to decode the encoded data stream based on a Tanner graph representation.

32. The coding system of claim **25**, wherein the decoder is operative to decode the encoded data stream in linear time.

33. The coding system of claim **25**, wherein the second coder comprises a coder operative to further encode bits output from the first coder at a rate within 1% of one.

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UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : 7,116,710 B1 Page 1 of 1
APPLICATION NO. : 09/861102
DATED : October 3, 2006
INVENTOR(S) : Hui Jin, Aamod Khandekar and Robert J. McEliece

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

At column **1**, line **8**, please amend the paragraph as follows:

This application claims the priority [[to]] of U.S. Provisional Application Ser. No. 60/205,095, filed on May 18, 2000, and [[to]] is a continuation-in-part of U.S. application Ser. No. 09/922,852, filed on Aug. 18, 2000 and entitled Interleaved Serial Concatenation Forming Turbo-Like Codes.

Signed and Sealed this

Twenty-second Day of July, 2008

Jon W. Dudas

JON W. DUDAS
Director of the United States Patent and Trademark Office