US005996059A

United States Patent [19]

Porten et al.

[11] Patent Number: 5,996,059

[45] Date of Patent: *Nov. 30, 1999

[54] **SYSTEM FOR MONITORING AN EXECUTION PIPELINE UTILIZING AN ADDRESS PIPELINE IN PARALLEL WITH THE EXECUTION PIPELINE**

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[73] Assignee: **National Semiconductor Corporation**, Santa Clara, Calif.

[*] Notice: This patent issued on a continued prosecution application filed under 37 CFR 1.53(d), and is subject to the twenty year patent term provisions of 35 U.S.C. 154(a)(2).

[21] Appl. No.: **08/886,520**

[22] Filed: **Jul. 1, 1997**

[51] **Int. Cl.**[6] **G06F 9/30**

[52] **U.S. Cl.** **712/200**; 712/42; 714/38

[58] **Field of Search** 395/376, 377, 395/800.41, 800.42; 712/200, 201, 41, 42; 714/38, 45

[56] **References Cited**

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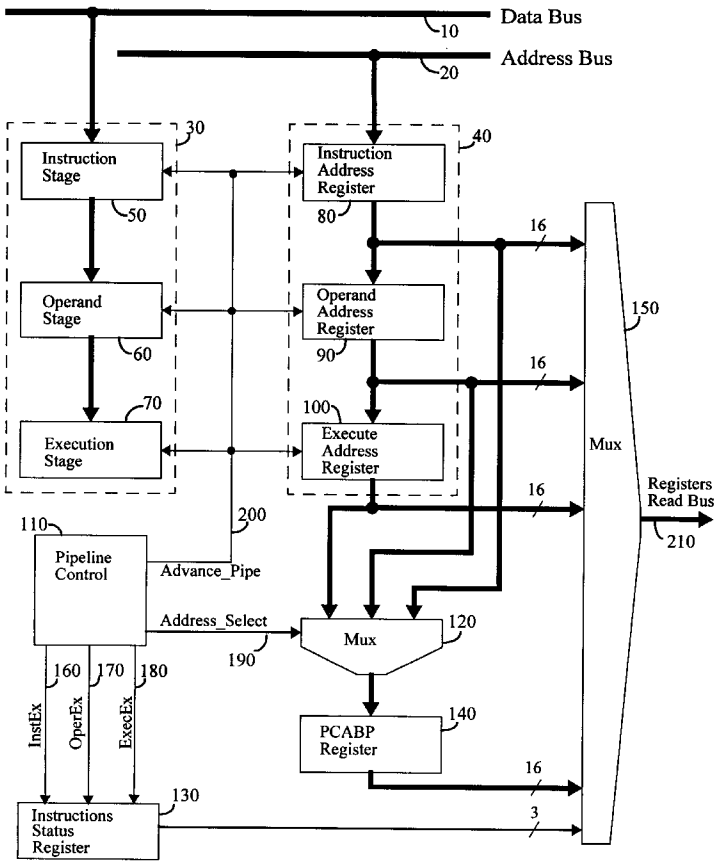
Primary Examiner—Richard L. Ellis

Attorney, Agent, or Firm—Limbach & Limbach, LLP

[57] **ABSTRACT**

An address pipeline includes a sequence of registers for storing the memory addresses of instructions currently being processed within the different stages of an execution pipeline. In parallel with the execution pipeline, the address pipeline advances the corresponding memory addresses as the instructions are advanced through the execution pipeline. Address pipelining allows the programmer of a pipelined processor to understand the otherwise hidden operation of a pipelined processor by giving the programmer means to track instructions through the pipeline. In addition, the address pipeline includes an instruction status register for indicating whether an instruction at any given stage of the pipeline has been executed and a program counter address breakpoint register for storing the address of the instruction that actually triggers a breakpoint.

17 Claims, 4 Drawing Sheets



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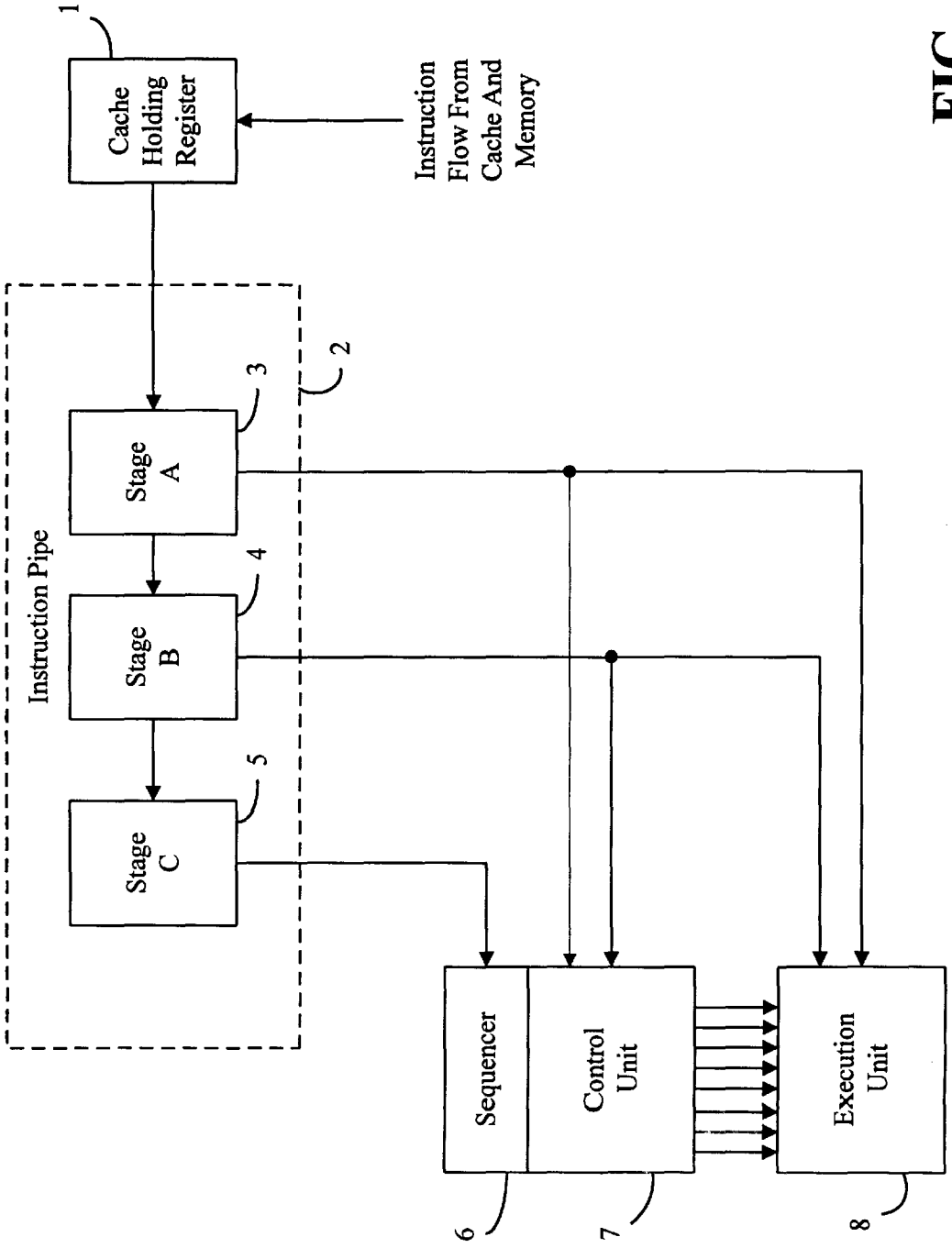

FIG. 1
(PRIOR ART)

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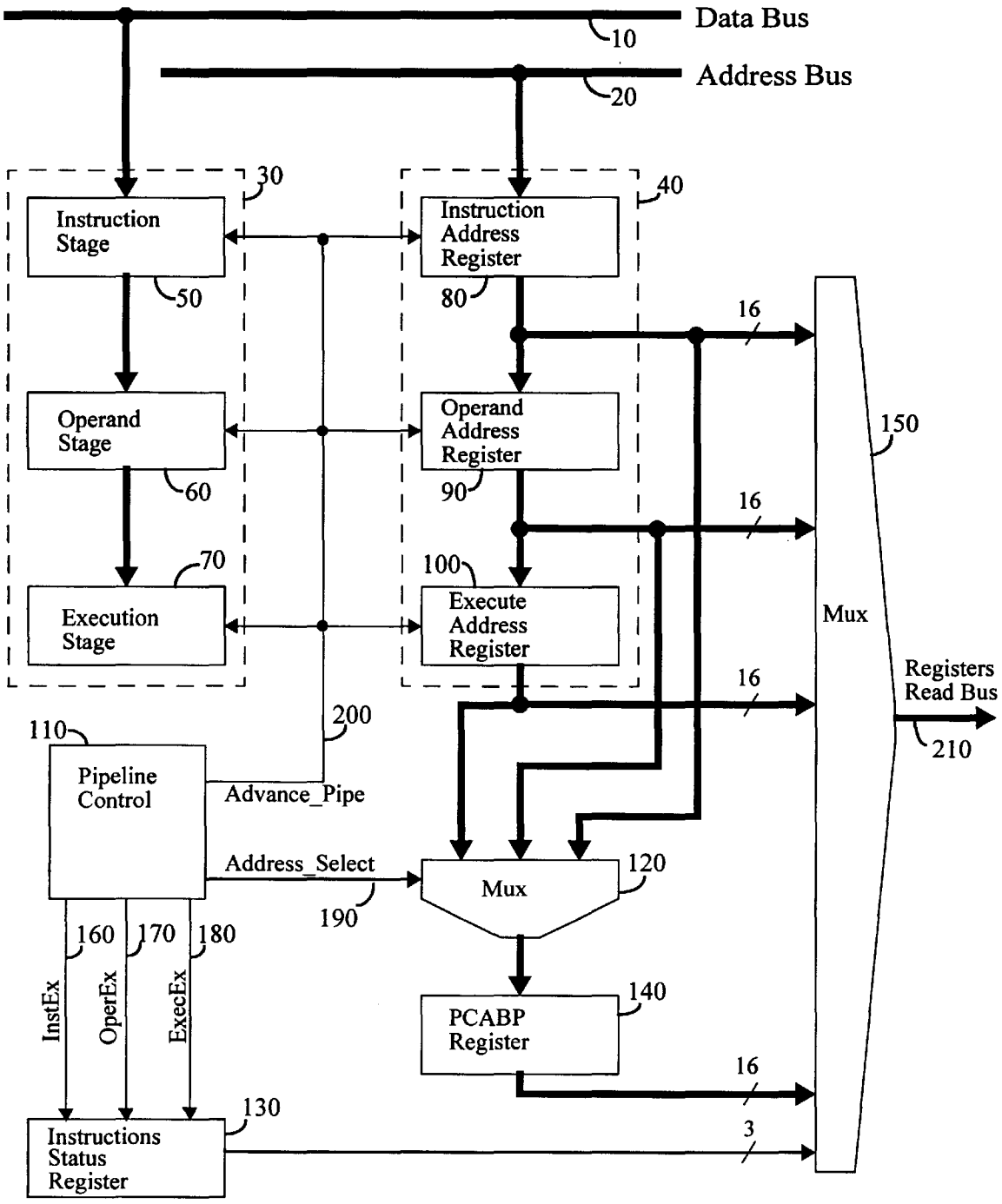

FIG. 2

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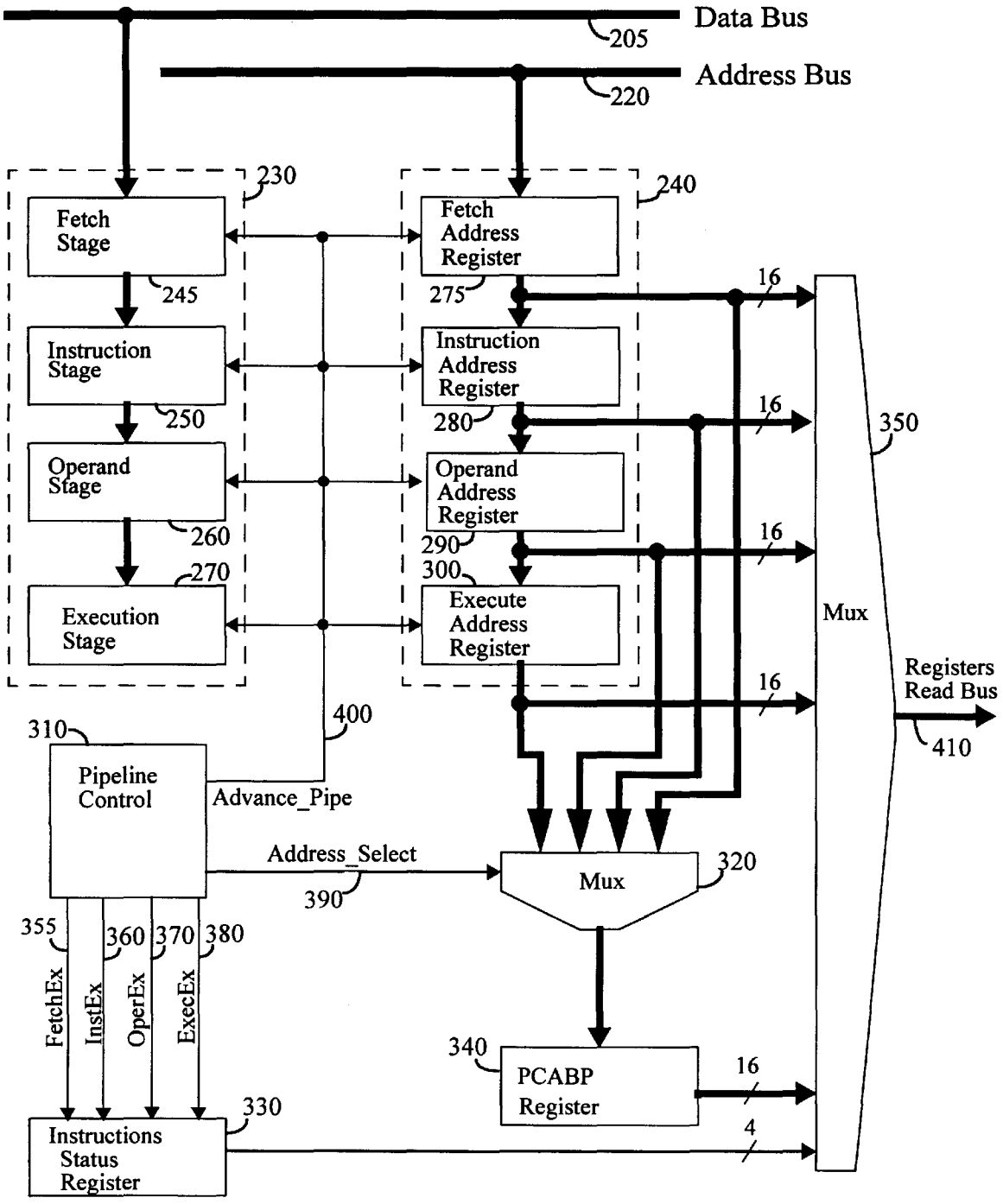

FIG. 3

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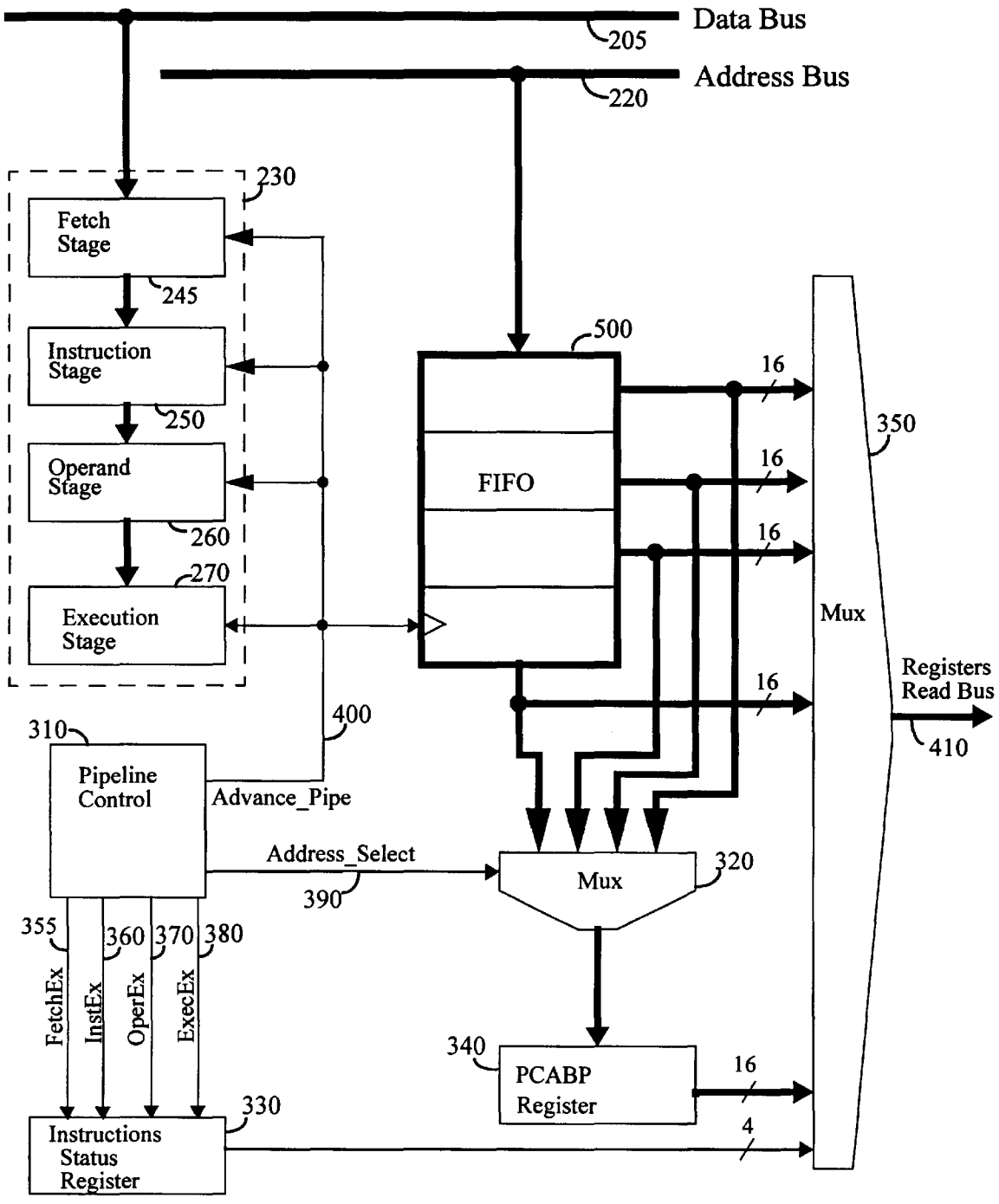

FIG. 4

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