UNITED STATES PATENT AND TRADEMARK OFFICE UNITED STATES DEPARTMENT OF United States Patent and Trademark of Address: COMMISSIONER FOR PATENTS P.O. Box 1450 Alexandria, Virginia 22313-1450 www.usplo.gov				
APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/467,092	08/24/2006	Michael Tasler	0256.0002.NPUS01	3038
69995 7590 09/28/2015 The Meola Firm, PLLC 2500 Westchester Avenue, Suite 210			EXAMINER LEE, CHUN KUAN	
Purchase, NY 1	10577		ART UNIT	PAPER NUMBER
			2181	
			MAIL DATE	DELIVERY MODE
			09/28/2015	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

PTOL-90A (Rev. 04/07)

Apple 1002 (Part 1 of 2) U.S. Pat. 9,189,437

Application No. Applicant(s) Corrected 11/467,092 TASLER, MICHAEL						
Notice of Allowability	Examiner Chun-Kuan Lee	Art Unit 2181	AIA (First Inventor to File) Status No			
The MAILING DATE of this communication apper All claims being allowable, PROSECUTION ON THE MERITS IS herewith (or previously mailed), a Notice of Allowance (PTOL-85) NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT R of the Office or upon petition by the applicant. See 37 CFR 1.313	(OR REMAINS) CLOSED in this ap or other appropriate communicatio IGHTS. This application is subject t	plication. If not n will be mailed	included in due course. THIS			
 Image: Market Ma	/were filed on					
 An election was made by the applicant in response to a rest requirement and election have been incorporated into this a 		the interview on	; the restriction			
benefit from the Patent Prosecution Highway program at a	3. The allowed claim(s) is/are <u>239 and 333-376 (renumbered as claims 1-45)</u> . As a result of the allowed claim(s), you may be eligible to benefit from the Patent Prosecution Highway program at a participating intellectual property office for the corresponding application. For more information, please see <u>http://www.uspto.gov/patents/init_events/pph/index.jsp</u> or send an inquiry to PPHfeedback@uspto.gov.					
 4. Acknowledgment is made of a claim for foreign priority under Certified copies: a) All b) □ Some *c) □ None of the: 1. Certified copies of the priority documents have 2. □ Certified copies of the priority documents have 3. □ Copies of the certified copies of the priority documents have 4. □ Certified copies of the priority documents have 5. □ Copies of the certified copies of the priority documents have 6. □ Copies of the certified copies of the priority documents have 7. □ Certified copies of the priority documents have 8. □ Copies of the certified copies of the priority documents have 8. □ Copies of the certified copies of the priority documents have 9. □ Certified copies of the certified copies of the priority documents have 9. □ Copies of the certified copies of the priority documents have 9. □ Certified copies of the certified copies of the priority documents have 	been received. been received in Application No		application from the			
Applicant has THREE MONTHS FROM THE "MAILING DATE" noted below. Failure to timely comply will result in ABANDONM THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.		complying with	the requirements			
5. CORRECTED DRAWINGS (as "replacement sheets") mus						
including changes required by the attached Examiner' Paper No./Mail Date	s Amendment / Comment or in the (Office action of				
Identifying indicia such as the application number (see 37 CFR 1 each sheet. Replacement sheet(s) should be labeled as such in t			(not the back) of			
 DEPOSIT OF and/or INFORMATION about the deposit of E attached Examiner's comment regarding REQUIREMENT FC 			he			
Attachment(s) 1. □ Notice of References Cited (PTO-892) 2. □ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date	5. ⊠ Examiner's Ameno 6. ⊠ Examiner's Staten 7. □ Other					
/Chun-Kuan Lee/ Primary Examiner, Art Unit 2181	tice of Allowability		r No./Mail Date 20150925			

DETAILED ACTION

I. EXAMINER'S AMENDMENTS

OPTIONS AVAILABLE TO THE APPLICANT

An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by **37 CFR § 1.312**. To ensure consideration of such an amendment, it **MUST** be submitted no later than the payment of the issue fee.

AUTHORIZATION FOR THE CORRECTIONS BY THE EXAMINER

Authorization for this examiner's amendment was given in a telephone interview with Anthony L. Meola, having Reg. No. 44,936, on 08/03/2015 and 09/24/2015. Accordingly, since a complete record of the interview has been incorporated in the instant examiner's amendment, no separate interview summary form is included in the instant office letter **MPEP § 713.04**.

CORRECTIONS MADE IN THE APPLICATION

The application has been amended as following:

IN THE CLAIMS:

The below described amendments to the claims are necessary to further clarify the claimed invention.

As per claim 239, claim 239 is amended as following:

"An analog data generating and processing device (ADGPD), comprising: an input/output (i/o) port;

.

a program memory;

a data storage memory;

a processor operatively interfaced with the i/o port, the program memory and the <u>data</u> storage memory;

wherein the processor is adapted to implement a data generation process by which analog data is acquired from each respective analog acquisition channel of a plurality of independent analog acquisition channels, the analog data from each respective channel is digitized, coupled into the processor, and is processed by the processor, and the processed and digitized analog data is stored in the data storage memory as at least one file of digitized analog data;

wherein the processor also is adapted to be involved in an automatic recognition process of a host computer in which, when the i/o port is operatively interfaced with a multi-purpose interface of the host computer, the processor executes at least one instruction set stored in the program memory and thereby causes at least one parameter identifying the analog data generating and processing device, independent of analog data source, as a digital storage device instead of as an analog data generating and processing device to be automatically sent through the i/o port and to the multipurpose interface of the computer (a) without requiring any end user to load any

software onto the computer at any time and (b) without requiring any end user to interact with the computer to set up a file system in the ADGPD at any time, wherein the at least one parameter is consistent with the ADGPD being responsive to commands issued from a customary device driver;

wherein the at least one parameter provides information to the computer about file transfer characteristics of the ADGPD; and

wherein the processor is further adapted to be involved in an automatic file transfer process in which, when the i/o port is operatively interfaced with the multipurpose interface of the computer, and after the at least one parameter has been sent from the i/o port to the multi-purpose interface of the computer, the processor executes at least one other instruction set stored in the program memory to thereby cause the at least one file of digitized analog data acquired from at least one of the plurality of analog acquisition channels to be transferred to the computer using <u>the customary</u> device driver for the digital storage device while causing the analog data generating and processing device to appear to the computer as if it were the digital storage device without requiring any user-loaded file transfer enabling software to be loaded on or installed in the computer at any <u>time.</u>"

As per claim 369, claim 369 is amended as following:

"The analog data generating and processing device of claim <u>239 further</u> <u>comprising an input connector having at least one BNC input</u> coupled to the processor

through a respective independently programmable amplifier, a multiplexer, and an analog to digital converter."

As per claim 370, claim 370 is amended as following:

"An analog data generating and processing device <u>(ADGPD)</u> for acquiring analog data and for communicating with a host computer comprising:

a program, memory;

a data storage memory;

a digital processor configured to interface to a multi-purpose interface of the host computer, the program memory, and the data storage memory;

an analog to digital converter operatively coupled to the digital processor and configured to acquire analog data from each respective analog acquisition channel of a plurality of analog acquisition channels, the analog to digital converter configured to convert the acquired analog data to digitized acquired analog data and to couple the digitized acquired analog data from the plurality of analog acquisition channels into the digital processor for processing by the digital processor;

the digital processor configured to automatically generate and transmit to the host computer via the multipurpose interface an identification parameter which identifies the analog data generating and processing device to the host computer as a digital storage device but which is different than an analog data generating and processing device and independent of analog data source, and the processor communicating with the host computer through the multi-purpose interface as if the analog data generating

and processing device were the digital storage device including transferring the digitized acquired analog data acquired from at least one of the analog acquisition channels. wherein the identification parameter is consistent with the ADGPD being responsive to commands issued from a customary device driver, using the customary device driver present for a digital storage device in the host computer without requiring the user to load the customary device driver; and

wherein the digital processor is configured to transmit to the host computer active commands through the multipurpose interface to access a system bus of the host computer to enable communication directly with other devices of the host computer while bypassing the host computer processor without requiring the user to load enabling software."

As per claim 372, claim 372 is amended as following:

"An analog data generating and processing device <u>(ADGPD)</u> for acquiring analog data and for communicating with a host computer which includes a manufacturer installed BIOS comprising:

a program memory;

a data storage memory;

a digital processor configured to interface to a multi-purpose interface of the host computer, the program memory, and the data storage memory;

an analog to digital converter operatively coupled to the digital processor and configured to simultaneously acquire analog data from each respective analog source of a plurality of analog sources on a respective one of a plurality of independent analog

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acquisition channels, the analog to digital converter configured to convert the acquired analog data to digitized acquired analog data and to couple the digitized acquired analog data into the digital processor for processing by the digital processor;

the digital processor configured to automatically generate and transmit to the host computer via the multipurpose interface an identification parameter which identifies the analog data generating and processing device to the host computer as a digital mass storage device but which is different than an analog data generating and processing device and independent of the analog sources, and the processor communicating with the host computer through the multi-purpose interface as if the analog data generating and processing device were the digital mass storage device including transferring the digitized analog data acquired from at least one of the analog sources, wherein the identification parameter is consistent with the ADGPD being responsive to commands issued from a customary device driver, using the customary device driver present in the BIOS of the host computer for the digital mass storage device driver."

As per claim 374, claim 374 is amended as following:

"An analog data generating and processing method for acquiring analog data and for communicating with a host computer comprising:

operatively interfacing an analog data device including a digital processor, a program memory and a data storage memory, to a multi-purpose interface of the host computer;

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acquiring analog data on each respective analog acquisition channel of a plurality of independent analog acquisition channels, converting the acquired analog data to digitized acquired analog data, and coupling the digitized acquired analog data into the digital processor for processing by the digital processor;

automatically generating and transmitting to the host computer via the multipurpose interface an identification parameter which identifies the analog data generating and processing device to the host computer as a digital storage device but which is different than an analog data device, and independent of analog data source, and the analog data generating and processing device communicating with the host computer through the multi-purpose interface as if the analog data generating and processing device were the digital storage device including transferring the digitized acquired analog data acquired from at least one of the analog acquisition channels, wherein the identification parameter is consistent with the ADGPD being responsive to commands issued from a customary device driver, using the customary device driver present for the customary digital storage device in the host computer without requiring the user to load the device driver."

II. ALLOWABLE SUBJECT MATTER

Claims 239 and 333-376 (renumbered as claims 1-45) are allowed.

The following is an **Examiner's Statement of Reasons for Allowance**, See MPEP 1302.14:

The primary reason for the allowance of the independent claims 239, 370, 372 and 374 (renumbered as claims 1, 39, 41 and 43) is the inclusion of the inventive concept for sending at least one parameter that is consistent with the portable peripheral device being responsive to commands issued from a customary driver for the file transferring of digitally converted analog data in combination with other recited claimed elements, **which is not found in the prior art of record.** Because claims 333-369, 371, 373, and 375-376 (renumbered as claims 2-38, 40, 42 and 44-45) depend directly or indirectly on claims independent claims 239, 370, 372 and 374 (renumbered as claims 1, 39, 41 and 43), these claims are considered allowable for at least the same reasons noted above.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

CONCLUSION

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chun-Kuan (Mike) Lee whose telephone number is (571) 272-0671. The examiner can normally be reached on 8AM to 5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Idriss Alrobaye can be reached on (571) 270-1023. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Chun-Kuan Lee/ Primary Examiner Art Unit 2181 September 25, 2015



UNITED STATES PATENT AND TRADEMARK OFFICE

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NOTICE OF ALLOWANCE AND FEE(S) DUE

69995 7590 09/17/2015 The Meola Firm, PLLC 2500 Westchester Avenue, Suite 210 Purchase, NY 10577

EXAMINER				
LEE, CHUN KUAN				
ART UNIT PAPER NUMBER				
2181				

DATE MAILED: 09/17/2015

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.	
11/467,092	08/24/2006	Michael Tasler	0256.0002.NPUS01	3038	

TITLE OF INVENTION: ANALOG DATA GENERATING AND PROCESSING DEVICE FOR USE WITH A PERSONAL COMPUTER

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	\$960	\$0	\$0	\$960	12/17/2015

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the ENTITY STATUS shown above. If the ENTITY STATUS is shown as SMALL or MICRO, verify whether entitlement to that entity status still applies.

If the ENTITY STATUS is the same as shown above, pay the TOTAL FEE(S) DUE shown above.

If the ENTITY STATUS is changed from that shown above, on PART B - FEE(S) TRANSMITTAL, complete section number 5 titled "Change in Entity Status (from status indicated above)".

For purposes of this notice, small entity fees are 1/2 the amount of undiscounted fees, and micro entity fees are 1/2 the amount of small entity fees.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

Page 1 of 3

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail Mail Stop ISSUE FEE Commissioner for Patents P.O. Box 1450 Alexandria, Virginia 22313-1450

or <u>Fax</u> (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

69995 7590 09/17/2015 The Meola Firm, PLLC 2500 Westchester Avenue, Suite 210 Purchase, NY 10577

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name
(Signature
(Date

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/467,092	08/24/2006	Michael Tasler	0256.0002.NPUS01	3038

TITLE OF INVENTION: ANALOG DATA GENERATING AND PROCESSING DEVICE FOR USE WITH A PERSONAL COMPUTER

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	\$960	\$0	\$0	\$960	12/17/2015

EXAMINER	ART UNIT	CLASS-SUBCLASS		
LEE, CHUN KUAN	2181	710-022000		
 Change of correspondence address or indication CFR 1.363). Change of correspondence address (or Cha Address form PTO/SB/122) attached. "Fee Address" indication (or "Fee Address" PTO/SB/47; Rev 03-02 or more recent) attache Number is required. ASSIGNEE NAME AND RESIDENCE DAT/ PLEASE NOTE: Unless an assignee is identi recordation as set forth in 37 CFR 3.11. Comp (A) NAME OF ASSIGNEE 	nge of Correspondence Indication form d. Use of a Customer A TO BE PRINTED ON 7	or agents OR, alternativ (2) The name of a singl registered attorney or a 2 registered patent attor listed, no name will be THE PATENT (print or typ data will appear on the part T a substitute for filing an	3 registered patent attorneys rely, e firm (having as a member a gent) and the names of up to neys or agents. If no name is printed.	1 2 3 id below, the document has been filed for
Please check the appropriate assignee category or	categories (will not be p	cinted on the patent):	Individual 🖵 Corporation or c	other private group entity 🖵 Government
 4a. The following fee(s) are submitted: Issue Fee Publication Fee (No small entity discount p Advance Order - # of Copies	ermitted)	 A check is enclosed. Payment by credit care The director is hereby 	se first reapply any previously d. Form PTO-2038 is attached. authorized to charge the requirec sit Account Number	paid issue fee shown above) d fee(s), any deficiency, or credits any (enclose an extra copy of this form).
 5. Change in Entity Status (from status indicated Applicant certifying micro entity status. See Applicant asserting small entity status. See Applicant changing to regular undiscounted 	e 37 CFR 1.29 37 CFR 1.27 I fee status.	<u>NOTE</u> : If the application to be a notification of loss <u>NOTE</u> : Checking this box entity status, as applicable	was previously under micro entil of entitlement to micro entity st s will be taken to be a notification 2.	(see forms PTO/SB/15A and 15B), issue ed at the risk of application abandonment. ty status, checking this box will be taken atus. n of loss of entitlement to small or micro
NOTE: This form must be signed in accordance w	vith 37 CFR 1.31 and 1.3	3. See 37 CFR 1.4 for signa	ture requirements and certificati	ons.
Authorized Signature				
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PTOL-85 Part B (10-13) Approved for use through 10/31/2013.

OMB 0651-0033 U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

UNITED STATES PATENT AND TRADEMARK OFFICE United States Patent and Trademark Office Address: COMMISSIONER FOR PATENTS P.O. Box 1450 Alexandria, Virginia 22313-1450 www.uspto.gov							
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69995 75	90 09/17/2015		EXAN	IINER			
The Meola Firm, 2500 Westchester			LEE, CHU	JN KUAN			
Purchase, NY 1057	,		ART UNIT	PAPER NUMBER			
			2181				
			DATE MAILED: 09/17/201	5			

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)

(Applications filed on or after May 29, 2000)

The Office has discontinued providing a Patent Term Adjustment (PTA) calculation with the Notice of Allowance.

Section 1(h)(2) of the AIA Technical Corrections Act amended 35 U.S.C. 154(b)(3)(B)(i) to eliminate the requirement that the Office provide a patent term adjustment determination with the notice of allowance. See Revisions to Patent Term Adjustment, 78 Fed. Reg. 19416, 19417 (Apr. 1, 2013). Therefore, the Office is no longer providing an initial patent term adjustment determination with the notice of allowance. The Office will continue to provide a patent term adjustment determination with the Issue Notification Letter that is mailed to applicant approximately three weeks prior to the issue date of the patent, and will include the patent term adjustment on the patent. Any request for reconsideration of the patent term adjustment determination (or reinstatement of patent term adjustment) should follow the process outlined in 37 CFR 1.705.

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

OMB Clearance and PRA Burden Statement for PTOL-85 Part B

The Paperwork Reduction Act (PRA) of 1995 requires Federal agencies to obtain Office of Management and Budget approval before requesting most types of information from the public. When OMB approves an agency request to collect information from the public, OMB (i) provides a valid OMB Control Number and expiration date for the agency to display on the instrument that will be used to collect the information and (ii) requires the agency to inform the public about the OMB Control Number's legal significance in accordance with 5 CFR 1320.5(b).

The information collected by PTOL-85 Part B is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450. Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

- 1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
- 2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
- 3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
- 4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
- 5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
- 6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
- 7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
- 8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
- 9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

	Applicatio 11/467,09	plication No.Applicant(s)/467,092TASLER, MICHAEL			
Notice of Allowability	Examiner Chun-Kua	r	Art Unit 2181	AIA (First Inventor to File) Status No	
The MAILING DATE of this communication app All claims being allowable, PROSECUTION ON THE MERITS IS herewith (or previously mailed), a Notice of Allowance (PTOL-85 NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT F of the Office or upon petition by the applicant. See 37 CFR 1.31	S (OR REMAI 5) or other app RIGHTS. This	NS) CLOSED in this app propriate communication s application is subject to	lication. If not will be mailed	t included in due course. THIS	
 Image: This communication is responsive to <u>06/01/2015</u>. Image: A declaration(s)/affidavit(s) under 37 CFR 1.130(b) was 	as/were filed o	on <u>.</u>			
2. An election was made by the applicant in response to a re- requirement and election have been incorporated into this		rement set forth during th	e interview or	n; the restriction	
 The allowed claim(s) is/are <u>239 and 333-376 (renumbered</u> benefit from the Patent Prosecution Highway program at For more information, please see <u>http://www.uspto.gov/pat</u> <u>PPHfeedback@uspto.gov</u>. 	t a participatin	g intellectual property off	ice for the cor		
4. Acknowledgment is made of a claim for foreign priority unc	der 35 U.S.C.	§ 119(a)-(d) or (f).			
Certified copies: a) ⊠ All b) □ Some *c) □ None of the:					
1. X Certified copies of the priority documents hav	ve been receiv	ved.			
2. 🗌 Certified copies of the priority documents hav	ve been receiv	ved in Application No.			
3. 🔲 Copies of the certified copies of the priority de	ocuments hav	ve been received in this n	ational stage	application from the	
International Bureau (PCT Rule 17.2(a)).					
* Certified copies not received:					
Applicant has THREE MONTHS FROM THE "MAILING DATE noted below. Failure to timely comply will result in ABANDON THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.			omplying with	the requirements	
5. CORRECTED DRAWINGS (as "replacement sheets") mu	ist be submitte	ed.			
including changes required by the attached Examiner Paper No./Mail Date	r's Amendmei	nt / Comment or in the Of	fice action of		
Identifying indicia such as the application number (see 37 CFR each sheet. Replacement sheet(s) should be labeled as such in				(not the back) of	
 DEPOSIT OF and/or INFORMATION about the deposit of attached Examiner's comment regarding REQUIREMENT F 	BIOLOGICAL FOR THE DEF	MATERIAL must be sub POSIT OF BIOLOGICAL	mitted. Note MATERIAL.	the	
 Attachment(s) 1. ☐ Notice of References Cited (PTO-892) 2. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date	6	5. 🛛 Examiner's Amendn 5. 🖾 Examiner's Stateme 7. 🔲 Other			
/Chun-Kuan Lee/ Primary Examiner, Art Unit 2181					
U.S. Patent and Trademark Office PTOL-37 (Rev. 08-13)	otice of Allowa	ability	Part of Pape	er No./Mail Date 20150803	

DETAILED ACTION

I. EXAMINER'S AMENDMENTS

OPTIONS AVAILABLE TO THE APPLICANT

An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by **37 CFR § 1.312**. To ensure consideration of such an amendment, it **MUST** be submitted no later than the payment of the issue fee.

AUTHORIZATION FOR THE CORRECTIONS BY THE EXAMINER

Authorization for this examiner's amendment was given in a telephone interview with Anthony L. Meola, having Reg. No. 44,936, on 08/03/2015. Accordingly, since a complete record of the interview has been incorporated in the instant examiner's amendment, no separate interview summary form is included in the instant office letter **MPEP § 713.04**.

CORRECTIONS MADE IN THE APPLICATION

The application has been amended as following:

IN THE CLAIMS:

The below described amendments to the claims are necessary to further clarify the claimed invention.

As per claim 239, claim 239 is amended as following:

"An analog data generating and processing device (ADGPD), comprising:

an input/output (i/o) port;

a program memory;

a data storage memory;

a processor operatively interfaced with the i/o port, the program memory and the <u>data</u> storage memory;

wherein the processor is adapted to implement a data generation process by which analog data is acquired from each respective analog acquisition channel of a plurality of independent analog acquisition channels, the analog data from each respective channel is digitized, coupled into the processor, and is processed by the processor, and the processed and digitized analog data is stored in the data storage memory as at least one file of digitized analog data;

wherein the processor also is adapted to be involved in an automatic recognition process of a host computer in which, when the i/o port is operatively interfaced with a multi-purpose interface of the host computer, the processor executes at least one instruction set stored in the program memory and thereby causes at least one parameter identifying the analog data generating and processing device, independent of analog data source, as a digital storage device instead of as an analog data generating and processing device to be automatically sent through the i/o port and to the multipurpose interface of the computer (a) without requiring any end user to load any software onto the computer at any time and (b) without requiring any end user to

interact with the computer to set up a file system in the ADGPD at any time, wherein the at least one parameter is consistent with the ADGPD being responsive to commands issued from a customary device driver;

wherein the at least one parameter provides information to the computer about file transfer characteristics of the ADGPD; and

wherein the processor is further adapted to be involved in an automatic file transfer process in which, when the i/o port is operatively interfaced with the multipurpose interface of the computer, and after the at least one parameter has been sent from the i/o port to the multi-purpose interface of the computer, the processor executes at least one other instruction set stored in the program memory to thereby cause the at least one file of digitized analog data acquired from at least one of the plurality of analog acquisition channels to be transferred to the computer using <u>the customary</u> device driver for the digital storage device while causing the analog data generating and processing device to appear to the computer as if it were the digital storage device without requiring any user-loaded file transfer enabling software to be loaded on or installed in the computer at any <u>time.</u>"

As per claim 370, claim 370 is amended as following:

"An analog data generating and processing device <u>(ADGPD)</u> for acquiring analog data and for communicating with a host computer comprising:

a program, memory;

a data storage memory;

Page 4

a digital processor configured to interface to a multi-purpose interface of the host computer, the program memory, and the data storage memory;

an analog to digital converter operatively coupled to the digital processor and configured to acquire analog data from each respective analog acquisition channel of a plurality of analog acquisition channels, the analog to digital converter configured to convert the acquired analog data to digitized acquired analog data and to couple the digitized acquired analog data from the plurality of analog acquisition channels into the digital processor for processing by the digital processor;

the digital processor configured to automatically generate and transmit to the host computer via the multipurpose interface an identification parameter which identifies the analog data generating and processing device to the host computer as a digital storage device but which is different than an analog data generating and processing device and independent of analog data source, and the processor communicating with the host computer through the multi-purpose interface as if the analog data generating and processing device were the digital storage device including transferring the digitized acquired analog data acquired from at least one of the analog acquisition channels, wherein the identification parameter is consistent with the ADGPD being responsive to commands issued from a customary device driver, using the customary device driver present for a digital storage device in the host computer without requiring the user to load the customary device driver; and

wherein the digital processor is configured to transmit to the host computer active commands through the multipurpose interface to access a system bus of the host

computer to enable communication directly with other devices of the host computer while bypassing the host computer processor without requiring the user to load enabling software."

As per claim 372, claim 372 is amended as following:

"An analog data generating and processing device <u>(ADGPD)</u> for acquiring analog data and for communicating with a host computer which includes a manufacturer installed BIOS comprising:

a program memory;

a data storage memory;

a digital processor configured to interface to a multi-purpose interface of the host computer, the program memory, and the data storage memory;

an analog to digital converter operatively coupled to the digital processor and configured to simultaneously acquire analog data from each respective analog source of a plurality of analog sources on a respective one of a plurality of independent analog acquisition channels, the analog to digital converter configured to convert the acquired analog data to digitized acquired analog data and to couple the digitized acquired analog data into the digital processor for processing by the digital processor;

the digital processor configured to automatically generate and transmit to the host computer via the multipurpose interface an identification parameter which identifies the analog data generating and processing device to the host computer as a digital mass storage device but which is different than an analog data generating and processing device and independent of the analog sources, and the processor

communicating with the host computer through the multi-purpose interface as if the analog data generating and processing device were the digital mass storage device including transferring the digitized analog data acquired from at least one of the analog sources, wherein the identification parameter is consistent with the ADGPD being responsive to commands issued from a customary device driver, using the customary device driver present in the BIOS of the host computer for the digital mass storage device driver."

As per claim 374, claim 374 is amended as following:

"An analog data generating and processing method for acquiring analog data and for communicating with a host computer comprising:

operatively interfacing an analog data device including a digital processor, a program memory and a data storage memory, to a multi-purpose interface of the host computer;

acquiring analog data on each respective analog acquisition channel of a plurality of independent analog acquisition channels, converting the acquired analog data to digitized acquired analog data, and coupling the digitized acquired analog data into the digital processor for processing by the digital processor;

automatically generating and transmitting to the host computer via the multipurpose interface an identification parameter which identifies the analog data generating and processing device to the host computer as a digital storage device but which is different than an analog data device, and independent of analog data source,

and the analog data generating and processing device communicating with the host computer through the multi-purpose interface as if the analog data generating and processing device were the digital storage device including transferring the digitized acquired analog data acquired from at least one of the analog acquisition channels, wherein the identification parameter is consistent with the ADGPD being responsive to commands issued from a customary device driver, using the customary device driver present for the customary digital storage device in the host computer without requiring the user to load the device driver."

II. ALLOWABLE SUBJECT MATTER

Claims 239 and 333-376 (renumbered as claims 1-45) are allowed.

The following is an **Examiner's Statement of Reasons for Allowance**, See MPEP 1302.14:

The primary reason for the allowance of the independent claims 239, 370, 372 and 374 (renumbered as claims 1, 39, 41 and 43) is the inclusion of the inventive concept for sending at least one parameter that is consistent with the portable peripheral device being responsive to commands issued from a customary driver for the file transferring of digitally converted analog data in combination with other recited claimed elements, **which is not found in the prior art of record.** Because claims 333-369, 371, 373, and 375-376 (renumbered as claims 2-38, 40, 42 and 44-45) depend Application/Control Number: 11/467,092Page 9Art Unit: 2181directly or indirectly on claims independent claims 239, 370, 372 and 374 (renumberedas claims 1, 39, 41 and 43), these claims are considered allowable for at least the same

reasons noted above.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

CONCLUSION

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chun-Kuan (Mike) Lee whose telephone number is (571) 272-0671. The examiner can normally be reached on 8AM to 5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Idriss Alrobaye can be reached on (571) 270-1023. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Chun-Kuan Lee/ Primary Examiner Art Unit 2181 September 10, 2015

	ED STATES PATENT	AND TRADEMARK OFFICE	UNITED STATES DEPAR United States Patent and Address: COMMISSIONER F P.O. Box 1450 Alexandria, Virginia 22: www.uspto.gov	FOR PATENTS
APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/467,092	08/24/2006	Michael Tasler	0256.0002.NPUS01	3038
69995 The Meola Firm	7590 06/01/2015	EXAMINER		
	ter Avenue, Suite 210	LEE, CHUN KUAN		
			ART UNIT	PAPER NUMBER
			2181	
			MAIL DATE	DELIVERY MODE
			06/01/2015	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

Ex parte MICHAEL TASLER

Appeal 2013-000397 Application 11/467,092 Technology Center 2100

Before ELENI MANTIS MERCADER, CARL W. WHITEHEAD JR. and BETH Z. SHAW, *Administrative Patent Judges*.

WHITEHEAD JR., Administrative Patent Judge.

DECISION ON APPEAL¹

STATEMENT OF THE CASE

Appellant is appealing the final rejection of claims 239 and 333–376 under 35 U.S.C. § 134(a). Appeal Brief 5. We have jurisdiction under 35 U.S.C. § 6(b) (2012).

We reverse.

Introduction

"The present invention relates to the transfer of data and in particular to interface devices for communication between a computer or host device and a data transmit/receive device from which data is to be acquired or with which two-way communication is to take place." Specification [2].

¹ An Oral Hearing was held on April 16, 2015.

Representative Claim (disputed limitations emphasized)

239. An analog data generating and processing device (ADGPD),

comprising:

an input/output (i/o) port;

a program memory;

a data storage memory;

a processor operatively interfaced with the i/o port, the program memory and the ata [sic] storage memory;

wherein the processor is adapted to implement a data generation process by which analog data is acquired from each respective analog acquisition channel of a plurality of independent analog acquisition channels, the analog data from each respective channel is digitized, coupled into the processor, and is processed by the processor, and the processed and digitized analog data is stored in the data storage memory as at least one file of digitized analog data;

wherein the processor also is adapted to be involved in an automatic recognition process of a host computer in which, when the i/o port is operatively interfaced with a multi-purpose interface of the host computer, the processor executes at least one instruction set stored in the

program memory and thereby causes at least one parameter identifying the analog data generating and processing device, independent of analog data source, as a digital storage device instead of as an analog data generating and processing device to be automatically' sent through the i/o port and to the multipurpose interface of the computer (a) without requiring any end user to load any software onto the computer at any time and (b) without requiring any end user to interact with the computer to set up a file system in the ADGPD at any time;

wherein the at least one parameter provides information to the computer about file transfer characteristics of the ADGPD; and

wherein the processor is further adapted to be involved in an automatic file transfer process in which, when the i/o port is operatively interfaced with the multi-purpose interface of the computer, and after the at least one parameter has been sent from the i/o port to the multipurpose interface of the computer, the processor executes at least one other instruction set stored in the program memory to thereby cause the at least one file of digitized analog data acquired from at least one of the plurality of analog acquisition channels to be transferred to the computer using a device driver for the digital storage device while causing the analog data generating and processing device to appear to the computer as if it were the digital storage device without

requiring any user-loaded file transfer enabling software to be loaded on or installed in the computer at any time; [sic].

Rejections on Appeal

Claims 239, 333–339, 341–362, 364–367 and 369–376 stand rejected as being unpatentable under 35 U.S.C. § 103(a) over Hashimoto (US Patent Number 6,111,604; issued August 29, 2000), Smith, (US Patent Number 5,634,075; issued May 27, 1997), Ristelhueber (Robert Ristelhueber, *Plug and play is almost here*, ELECTRONIC BUSINESS BUYER, vol. 29, no. 5, pg. 43, May 1994), and Shinohara (US Patent Number 5,742,934; issued April 21, 1998). Answer 6–33.

Claims 340 and 368 stand rejected as being unpatentable under 35 U.S.C. § 103(a) over Hashimoto, Smith, Ristelhueber, Shinohara and Endo (US Patent Number 4,652,928; issued March 24, 1987). Answer 33–34.

Claim 363 stands rejected as being unpatentable under 35 U.S.C. § 103(a) over Hashimoto, Smith, Ristelhueber, Shinohara and Roberts (US Patent Number 5,576,757; issued November 19, 1996). Answer 35.

ANALYSIS

Rather than reiterate the arguments of Appellant and the Examiner, we refer to the Appeal Brief (filed May 7, 2012), the Answer (mailed July 25, 2012) and the Reply Brief (filed September 25, 2012) for the respective

Appeal 2013-000397 Application 11/467,092

details. We have considered in this decision only those arguments Appellant timely raised in the Briefs.

Appellants argue the Examiner failed to establish a prima facie case of obviousness because the Ristelhueber reference is non-technical magazine article that generally describes the coming of Plug and Play. Appeal Brief

22.

The Examiner finds:

<u>Ristelhueber</u> did conceive the idea for the need to allow "users to simply insert a card or peripheral into a desktop system and have it start running immediately, without a lot of fussing and fuming" (on page 1) such as "reliving the end user of any need to fumble with floppy disks and user manuals to get the device up and running" (on page 2, 5th paragraph); therefore, the Plug and Play protocol enable[s] the user to simply insert/install the peripheral device into the desktop system and use the peripheral device immediately without fumbling with floppy disks to install the proper device driver.

Answer 57.

Appellants argue Ristelhueber does not provide an enabling disclosure about how the peripheral components are attached and recognized in a Plug and Play protocol. Appeal Brief 22–23. We find Appellant's arguments persuasive because we agree that Ristelhueber fails to discuss or even mention device drivers or what consequently occurs once the peripheral components are connected. *See* Appeal Brief 23. Ristelhueber discloses the idea of a Plug and Play protocol but fails to disclose the technical knowledge that would enable one of ordinary skill in the art to duplicate or modify the Plug and Play protocol. Therefore, we reverse the Examiner's obviousness rejections of claims 239, and claims 333–376 for the same reasons.

4

Appeal 2013-000397 Application 11/467,092

DECISION

The Examiner's 35 U.S.C. § 103(a) rejections of claims 239 and 333-

376 are reversed.

<u>REVERSED</u>

ELD

	ed States Patent a	and Trademark Office	UNITED STATES DEPAR United States Patent and Address: COMMISSIONER F P.O. Box 1450 Alexandria, Virginia 223 www.uspto.gov	Trademark Office OR PATENTS
APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/467,092	08/24/2006	Michael Tasler	31436/43993	3038
24628 Husch Blackwe	7590 07/19/2011	EXAMINER		
Husch Blackwe	ell Sanders LLP Welsh & F	LEE, CHUN KUAN		
120 S RIVERSIDE PLAZA 22ND FLOOR CHICAGO, IL 60606			ART UNIT	PAPER NUMBER
			2181	
			MAIL DATE	DELIVERY MODE
			07/19/2011	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

	Application No.	Applicant(s)				
	11/467,092	TASLER, MICHAEL				
Office Action Summary	Examiner	Art Unit				
	Chun-Kuan Lee	2181				
The MAILING DATE of this communication appears on the cover sheet with the correspondence address Period for Reply						
 A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>3</u> MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION. Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication. If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication. Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b). 						
Status						
1) Responsive to communication(s) filed on <u>10 M</u>	l <u>ay 2011</u> .					
2a)⊠ This action is FINAL . 2b)□ This	action is non-final.					
3) Since this application is in condition for allowar	nce except for formal matters, pro	osecution as to the merits is				
closed in accordance with the practice under E	<i>Ex parte Quayle</i> , 1935 C.D. 11, 4	53 O.G. 213.				
Disposition of Claims						
 4) Claim(s) <u>239 and 333-374</u> is/are pending in the application. 4a) Of the above claim(s) is/are withdrawn from consideration. 5) Claim(s) is/are allowed. 6) Claim(s) <u>239 and 333-374</u> is/are rejected. 7) Claim(s) is/are objected to. 8) Claim(s) are subject to restriction and/or election requirement. 						
Application Papers						
 9) The specification is objected to by the Examiner. 10) The drawing(s) filed on <u>8/24/2006 & 8/31/2009</u> is/are: a) accepted or b) objected to by the Examiner. Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a). Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d). 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152. 						
Priority under 35 U.S.C. § 119						
 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f). a) All b) Some * c) None of: Certified copies of the priority documents have been received. Certified copies of the priority documents have been received in Application No 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)). * See the attached detailed Office action for a list of the certified copies not received. 						
Attachment(s) 1) Notice of References Cited (PTO-892) 2) Notice of Draftsperson's Patent Drawing Review (PTO-948) 3) Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date 03/10/2011. U.S. Patent and Trademark Office PTOL-326 (Rev. 08-06)	4) X Interview Summary Paper No(s)/Mail D 5) Notice of Informal F 6) Other:	ate. <u>20110714</u> .				

033

DETAILED ACTION

RESPONSE TO ARGUMENTS

1. Applicant's arguments filed 05/10/2011 have been fully considered but they are not persuasive. Currently claims 1-238 and 240-332 are cancelled; and claims 239 and 333-374 are pending for examination.

2. In response to applicant's plurality of arguments with regard to the independent claims 239, 370, 372, and 374 rejected under 35 U.S.C. 103(a) that the resulting combination of the references does not teach/suggest applicant's inventive concept because of the following:

- <u>Hashimoto</u> discloses only the image data on one channel coupled into the processor and processed by the processor, and does not disclose the claimed analog data from a plurality of independent analog acquisition channels coupled into and processed by the processor;
- <u>Hashimoto</u> does not describe an automatic recognition process of the host computer as now claimed because <u>Hashimoto</u> merely describes a process for detection by the camera of an active connection by monitoring for a signal from the interface, and not the recognition process claimed which is a process in which the host computer recognizes the attached ADGPD and the ADGPD processor automatically sends mis-identifying information to the host computer;

- the Office Action also asserts that the <u>Hashimoto</u> digital camera CPU controls the digital camera to be recognized by the PC where the camera needs to be recognized by the PC so the PC knows how to properly communicate with the camera; however, no such recognition control is disclosed in <u>Hashimoto</u>; further, at the time of the <u>Hashimoto</u> disclosure, the user would load software and input information into the host computer to identify the camera and there was no requirement for the camera CPU to be involved in a recognition process;
- none of the other cited references disclose a processor in the peripheral device involved in the claimed automatic recognition process which automatically sends an identification parameter to the host computer because host computer in <u>Smith's</u> Plug and Play functionality assigns an identifying number rather than the peripheral processor automatically sending identification information; therefore <u>Smith</u> do not disclose automatic sending of identification (i.e. <u>Smith</u> discloses a host computer resource allocation process concerned with allocation of the resources of the host computer to avoid conflicts between resources within the host and not device recognition process), <u>Smith</u> does not mention of identification information being read or sent and <u>Smith</u> does not even mention a peripheral processor automatically providing identification information to the host computer;
- <u>Smith</u> also does not describe a peripheral having a processor involved in the Plug and Play process;

- indicating that the ROM BIOS of the computer loads the device driver does not teach or relate in any way to the ADGPD processor automatically sending identifying information;
- the loading of the device driver occurs after the peripheral device has been assigned resources and activated, and requires that a device driver then be provided; therefore, the Plug and Play functionality of <u>Smith</u> is also contrary to the claim feature calling for not requiring any user-loaded file transfer enabling software to be installed in the computer at any time, and this would include any special software driver;
- <u>Smith</u> expressly teaches the contrary, that a device driver must be loaded once the peripherals have been set up and host computer resources assigned (see e.g., Smith, Fig. 2, ref. 126 and Col. 4 lines 32-33);
- Plug and Play functionality of <u>Smith</u> is functionality which is primarily located in the host computer not the peripheral;
- <u>Ristelhueber</u> do not describes a peripheral device having an automatic recognition process without requiring any end user to load any software on the computer at anytime because <u>Ristelhueber</u> is a non-technical buyer magazine article which generically describes a coming Plug and Play standard with an enthusiastic description of the future ("In about a year the key standard and specifications will be in place to make PnP a reality", p. 1, paragraph 3); thus, <u>Ristelhueber</u> is not enabling prior art; <u>Ristelhueber</u> is not describing recognizing what peripheral is attached, only whether there is a peripheral attached to the

port; further, there is no enabling disclosure of how such recognition would one day be implemented; the description in <u>Ristelhueber</u> is just an over enthusiastic prediction of the hoped for goals for PnP, which is to detect when a new device is attached (i.e. identifying presence not what it is), configure the host computer resources to accommodate it, and then activate the device; however,

<u>Ristelhueber</u> nowhere discusses or even mentions device drivers, or what will happen after a device is configured and activated and as discussed herein, the <u>Smith</u> reference and the PnP Standards Specification make clear that a device driver is still needed after the peripheral has been detected, assigned resources and activated in accordance with Plug and Play; furthermore, there is no teaching in <u>Ristelhueber</u> to relieve the user from having to load a device driver, there is no mention of a processor on the peripheral, and there is no mention of the need or lack of need for user loaded software on the host computer;

- the environment and functionality, and the problems to be resolved in <u>Shinohara</u> are completely different to <u>Hashimoto</u>; therefore, it would not be obvious to combine the <u>Shinohara</u>'s flash disk drive features with <u>Hashimoto</u> because of these fundamental differences; <u>Shinohara</u> does not teach or even mention that there is no need for user interaction to set up a file system, or that the device is not identified as an analog data generating and processing device and is identified instead as a digital mass storage device; <u>Shinohara</u> is merely a mass storage device acting as a mass storage device; further, the data structure set up would require software on the host computer to perform these set-up functions; thus, additional software must be added to the host computer to set up the data structure for the flash drive; further, since <u>Shinohara</u> is merely a hard disk emulator connected to a computer, it cannot cause an acquired file of digitized analog data acquired from a analog source to be transferred (i.e., there is only digital data stored by the host computer); and the teaching of <u>Shinohara</u> does not suggest to one of ordinary skill in the art the operation and identification of an analog generating and processing device as an entirely different type of device, i.e. a mass storage device, and does not suggest a device which sends an identifying parameter to the host computer identifying the device as a device of dramatically different type than what it actually is;

<u>Shinohara</u> merely describes an approach to extending the life of the flash memory in a flash disk drive, and there is no mention of device drivers or no mention of not needing to load file transfer enabling software by <u>Shinohara</u>; nowhere in <u>Shinohara</u> is there any mention of transferring a file of digitized analog data (<u>Shinohara</u> is a disk driver, as such, it cannot acquire and digitize analog data and therefore cannot transfer it), or any data, without requiring any user loaded file transfer enabling software; rather, the detailed description cited calls for the host computer to perform unique file management functions (Col. 4, lines 34-49) which would require data transfer software in the host computer to set up the disk emulation; further, there is no teaching or mention of the disclosed disk emulator being able to transfer data without data-transfer

software loaded on the host computer; thus, Shinohara does not teach the feature of transferring digitized analog data without requiring any user loaded file transfer enabling software; the Office Action also asserts that combining the flash memory device of Shinohara with the Plug and Play functionality of the other references such as Smith, teaches this feature; however, as discussed above, Plug and Play is concerned with allocation of the resources of the host computer to avoid conflicts between resources within the host computer; the Plug and Play process thus does not eliminate the need to supply a driver but rather calls for loading the driver after the system resources are allocated and the devices activated; the Plug and Play standard does not address device drivers other than the fact that one is needed. (Plug and Play Specification p. 1 Abstract: "However, user interface issues for installation of device drivers are not addressed";) thus, even with Plug and Play, a device specific driver is still needed for each peripheral installed in the Plug and Play computer system in order for the peripheral's processor to execute an instruction to automatically transfer a file of digitized analog data to the computer from the peripheral device; this is clearly demonstrated by the Smith reference and the Plug and Play Specification document; thus, neither Shinohara nor the Plug and Play functionality disclosed in the other cited references teach data transfer without a user loaded driver;

- the device described in <u>Shinohara</u> is merely a memory for storage of digital data by a host computer and for retrieval of that data by the host computer, and thus

is not suitable for receiving analog data from a source independent of the host computer nor for transferring acquiring digitized analog data to a host computer; further, Shinohara does not teach transferring the acquired analog data while causing the analog data generating and processing device to appear to the computer as a digital storage device, as claimed; the Shinohara device has one port that merely receives and stores digital data from the computer and allows that same computer to retrieve that stored data through the same port; the claimed invention has two separate ports providing input of analog data on one port and subsequent transfer of digitized analog data to a computer on another port; thus, the disk memory emulation of <u>Shinohara</u> is dramatically different from the claimed invention and not compatible with or combinable with Hashimoto to obtain the claimed invention; stated another way, at most Shinohara merely teaches that a digital memory device having a single read/write port such as a flash memory, may be configured to emulate another digital memory device; this does not teach and is not related to an analog data acquisition device having both an analog input and a host computer interface port which can emulate a hard disk; thus, the combination of Shinohara with the other references does not teach or suggest the claimed automatic file transfer of acquired digitized analog data without requiring user loaded file transfer enabling software; indeed, there is nothing to suggest the advantage of not requiring user loaded file transfer enabling software in any device, let alone in an analog data acquisition device;

- <u>Hashimoto</u> and <u>Smith</u> are incompatible and cannot be properly combined, because <u>Hashimoto</u> describes checks a switch 110 which is manually set by the camera user, to determine whether it is in the transmit mode or is in a receive mode and <u>Smith</u> describes a Plug and Play process which requires the host computer to read and write data between the PnP peripheral device and the host computer; and
- combination of <u>Hashimoto</u> and <u>Shinohara</u> is also improper because <u>Hashimoto</u> describes an electronic camera while <u>Shinohara</u> describes a flash disk drive; and <u>Hashimoto</u> operates in a transmit only mode or a receive only mode selected by the user with a mode selection switch and <u>Shinohara</u>'s flash disk requires the host computer to read and write (i.e. <u>Hashimoto</u>'s one way communication would prevent two way exchange);

applicant's arguments have fully been considered, but are not found to be persuasive.

The examiner respectfully disagrees; and please note that applicant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.,* 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

To further clarify the examiner's position, first of all, based on the interview dated 07/12/2011, applicant's inventive concept corresponds to the functionality of "... single analog sensing device with multiple parallel channels for acquiring analog data through

the multiple parallel channels, wherein the single analog sensing device is connected to a digital device, such as a host, and the digital device (host) recognizing the connected single analog sensing device as a digital device, such as a hard drive (e.g. digital storage device) or printer; and when the single analog sensing device is connected to the digital device (host) for transferring the acquired analog data to the digital device (host), the digital device (host) use a corresponding digital device driver, such as hard drive driver, for communicating with the single analog sensing device, as the digital device (host) thinks that the connected single analog sensing device is the hard drive (digital device) ...," wherein the examiner relied on the references as following for the teaching of applicant's invention:

<u>Hashimoto</u> teaches single analog sensing device (e.g. digital camera peripheral device) with multiple parallel channels (e.g. channel for audio and channel for image) for acquiring analog data (e.g. audio and image) through the multiple parallel channels, wherein the single analog sensing device is connected to a digital device, such as a host, and the digital device (host) recognizing the connected single analog sensing device (e.g. host need to recognize the connected peripheral device in order to know how to communicate with the connected peripheral device); and the single analog sensing device is connected to the digital device (host) for transferring the acquired analog data (e.g. audio data and image data) to the digital device (host), and for communicating with the single analog sensing device (Fig. 1A-1B; Fig. 8; Fig. 11-12; Fig. 14-15; col. 1, II. 35-57; col. 3, I. 43 to col. 4, I. 57; col. 5, II. 43-57; col. 6, I. 16 to col. 9, I. 17; col. 9, I. 46 to col. 11, I. 42 and col. 12, I. 16 to col. 14, I. 14), wherein the digital

camera acquire analog image data and analog audio data and store them into the flash memory card, and when the digital camera is connect to the host computer, the digitized image and audio data is then transferred from the flash memory card to the host computer.

<u>Smith</u> teaches plug and play functionality for a peripheral device connected to a host computer, wherein the host would recognize the connected peripheral device (Fig. 2-5; col. 1, II. 9-22; col. 2, I. 40 to col. 3, I. 59; col. 4, II. 5-34 and col. 6, II. 63-62).

<u>Ristelhueber</u> teaches plug and play functionality without user loading software (e.g. plug and play of a peripheral device by having a user to simply insert a peripheral into a desktop system and have it start running immediately, as the PnP computer will automatically identify any new hardware installed and configure the new hardware, and relieving the end user of any need to fumble with floppy disks and user manuals to get the device up and running; therefore, the peripheral device is connected and operational without requiring any end user to load any software/device driver on the computer at anytime) (pages 1-3).

Shinohara teaches a host recognizing the connected single analog sensing device as a digital device, such as a hard drive (e.g. hard disk drive emulation) and using a corresponding digital device driver, such as hard drive driver, as the digital device (host) thinks that the connected single analog sensing device is the hard drive (digital device) (col. 1, II. 48-60 and col. 3, I. 33 to col. 4, I. 49), by combining the hard disk drive emulation of the flash memory card into <u>Hashimoto</u>'s digital camera peripheral device's flash memory card having the image data and audio data that is to

be transferred to the host, the resulting combination of the references further teaches the above feature as the digital camera transfers the flash memory card's image data and audio data to the host via hard disk drive emulation by the flash memory card.

Therefore, the resulting combination of the references does teach the core of applicant's invention as following: the digital camera peripheral device having the flash memory card that receives and maintains the analog image data and the analog audio data; the digital camera peripheral device is then connected to the host, wherein the host views the connected digital camera peripheral device to be the hard disk drive as the flash memory card is emulating as the hard disk drive for transferring the image data and the audio data from the flash memory card to the host computer (e.g. the digital camera peripheral device acquires the analog image and audio data while causing the digital camera peripheral device appear/be identified to the computer as an emulating hard disk drive/digital storage device).

Hashimoto does disclose a plurality of independent analog acquisition channels (e.g. channel for image and channel for audio) coupled into and processed by the processor (Fig. 1A-1B; Fig. 8; Fig. 11-12; Fig. 14-15; col. 1, II. 27-57; col. 3, I. 43 to col. 4, I. 67; col. 5, II. 43-57; col. 6, I. 16 to col. 9, I. 17; col. 9, I. 46 to col. 11, I. 42; and col. 12, I. 16 to col. 14, I. 14).

The claimed feature associated with "recognition process claimed which is a process in which the host computer recognizes the attached ADGPD and the ADGPD processor automatically sends mis-identifying information to the host" is not taught by <u>Hashimoto</u> along, as argued by the applicant; instead, it is taught by the combined

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teaching of <u>Hashimoto</u>, <u>Smith</u>, <u>Ristelhueber : "Plug and play is almost here"</u> and Shinohara.

As <u>Hashimoto</u> does disclose the digital camera communicating with the PC; therefore, it would be required for the PC to recognize the connected device in order for the PC to know how to properly communicate with the connected device. The examiner is not certain where <u>Hashimoto</u> disclosures that the user would load software and input information into the host computer to identify the camera and there was no requirement for the camera CPU to be involved in a recognition process; therefore, is unable to properly respond to applicant's remark/argument.

Base on applicant's clarification during the interviews dated 10/06/2010 and 07/12/2011, it is the examiner's best understanding that the claimed feature of "automatic sending of identification," "identification information being read or sent," "a peripheral processor automatically providing identification information to the host computer," and "the ADGPD processor automatically sending identifying information" are process that corresponds to the functionality of recognizing the connected analog device as the hard drive (digital device), and as explained in detail above, the resulting combination of the references does teach/suggest recognizing the connected analog device as the hard drive (digital device); furthermore, applicant's arguments presented in the preceding remarks, dated 09/24/2010, also recognized the loading the driver for the connected peripheral device and identifying the resources needed by the peripheral device; therefore, in order to load the appropriate device driver (or identify the resources needed), the plug and play process need to recognize the connected peripheral device

to be able to pick/select the appropriate device driver, because if the device driver is inappropriate, then operation would not permitted.

The examiner is relying on the combined teaching of <u>Hashimoto</u>, <u>Smith</u>, <u>Ristelhueber : "Plug and play is almost here"</u> and <u>Shinohara</u>, not <u>Smith</u> along, for the teaching of a peripheral having a processor involved in the Plug and Play process.

The examiner is not fully clear where in <u>Smith</u> indicated the requirement of userloaded file transfer enabling software to be installed in the computer at any time, therefore, the examiner is unable to properly answer applicant's argument.

<u>Smith</u>'s loading of the device driver is not contrary to "automatic recognition," because <u>Smith</u>'s loading of the device driver is similar to applicant's loading of the corresponding device driver, such as the digital device driver, as explained by the applicant during the interviews dated 10/06/2010 and 07/12/2011.

Plug and Play functionality is not functionality which is primarily located in the host computer instead of the peripheral, Plug and Play functionality is a protocol that both the host and the peripheral device must conform to so that the peripheral device can be plug into the host and directly start playing/utilizing the connected peripheral device; and to further clarify, it is <u>Smith</u>'s invention that is primarily located in the host computer not the peripheral, not Plug and Play functionality/protocol (Fig. 2-5; col. 1, II. 9-22; col. 2, I. 40 to col. 3, I. 8; col. 3, II. 22-27; col. 3, II. 53-59; col. 4, II. 5-34; col. 6, II. 63-62).

<u>Ristelhueber</u> is clearly technically related the Plug and Play protocol and as the applicant indicated, it is prior art; wherein the Plug and Play functionality/protocol is

clearly enabled by <u>Smith</u> and Plug and Play Standard, and the examiner relied on Ristelhueber because Ristelhueber provided a clear description that is easily understood regarding how Plug and Play functions; and Ristelhueber does describe recognizing of what peripheral is attached because after the peripheral device is connected to the host, the host need to recognize what peripheral device is attached in order for the host to know what device driver is to be loaded for the connected peripheral device; additionally, applicant's arguments also suggest that the host device recognize the connected peripheral device because in order for the host to identify "the resources needed by the peripheral device" the host would need to know what that connected peripheral device is (on page 21 of applicant's arguments); therefore, Plug and Play functionality will recognize the new hardware and configure hardware to relieve the user of the need to fumble with floppy disks (e.g. looking for the device driver on the floppy disks) and user manuals to get the device up and running; therefore, by combining <u>Ristelhueber</u> with the other references, the resulting combination of the references does teach/suggest the automatic recognition process corresponds to Plug and Play by the user simply inserting a peripheral into the desktop and having it start running immediately, as the PnP computer will automatically identify any new hardware installed and configure the new hardware, and relieving the end user of any need to fumble with floppy disks and user manuals to get the device up and running. To further clarify, <u>Ristelhueber</u> does teach/suggest that the plug and play functionality relieve the user from having to load a device driver and lack of need for user loaded software on the host computer, because the installation of a peripheral device without Plug and Play

functionality would need the end user of to fumble with floppy disks (e.g. looking for the device driver on the floppy disks) and user manuals to get the device up and running; and the examiner is relying on the other references, and not on <u>Ristelhueber</u>, for the teaching/suggesting regarding the claimed feature of "a processor on the peripheral"; and as discussed above, Plug and Play functionality for loading of a device driver is similar to applicant's loading of the corresponding device driver, such as the digital device driver, as explained by the applicant during the interviews dated 10/06/2010 and 07/12/2011 (Ristelhueber, pages 1-3).

Shinohara's hard disk drive emulation is compatible with <u>Hashimoto</u>, as the examiner is combining <u>Shinohara</u>'s hard disk drive emulation by the flash memory card into <u>Hashimoto</u>'s flash memory card; with regard to the claimed features for "no need for user interaction to set up a file system" and "device is not identified as an analog data generating and processing device and is identified instead as a digital mass storage device," the examiner is not relying on <u>Shinohara</u> along, as the examiner is relying on the combination of <u>Shinohara</u> with the other prior art references; therefore, by combining the hard drive emulation into <u>Hashimoto</u>'s flash memory card, the resulting combination of the references does teach/suggest when the analog device is connected to the host for transferring data from the analog device's flash memory card, the host will recognize the connected analog device as a hard disk drive via the flash memory card to the host; and by combining the Plug and Play functionality with the hard disk drive emulation, additional software would not need to be added to the host computer to set

up the data structure for the flash drive; to further clarify, the examiner is relying on the combination of the references, not on <u>Shinohara</u> along, for the teaching of claimed features associated with operation and identification of an analog generating and processing device as an entirely different type of device and device which sends an identifying parameter to the host computer identifying the device as a device of dramatically different type than what it actually is (e.g. the analog device's flash memory card implementing hard disk emulation for data transferring to the host; therefore, the host recognizes the connected analog device as the hard disk) (<u>Shinohara</u>, col. 1, II. 48-60; and col. 3, I. 56 to col. 4, I. 49).

The examiner is relying on the combination of the references, not on <u>Shinohara</u> along, for the teaching of the claimed features associated with "device drivers," "not needing to load file transfer enabling software," "transferring a file of digitized analog data without requiring any user loaded file transfer enabling software," and "disk emulator being able to transfer data without data-transfer software loaded on the host computer;" and as discussed above, the combination of the references does teach/suggest Plug and Play functionality eliminates the need to supply a driver by the end user as the loading the driver after the system resources are allocated and the devices activated is done by the host; and also discussed in detail above, the Plug and Play functionality for loading of a device driver is similar to applicant's loading of the corresponding device driver, such as the digital device driver, as explained by the applicant during the interviews dated 10/06/2010 and 07/12/2011; therefore, the

combination of the references does teach/suggest "data transfer without a user loaded driver" via the Plug and Play functionality.

Shinohara's memory is suitable for receiving analog data from a source independent of the host computer and for transferring acquiring digitized analog data to a host computer because Shinohara's memory is a flash memory card and Hashimoto does teach/suggest that flash memory card is suitable for receiving analog data from a source independent of the host computer and for transferring acquiring digitized analog data to a host computer; as discussed above, the examiner is relying on the combination of the references, not on Shinohara along, for the teaching of the claimed features associated with "transferring the acquired analog data while causing the analog data generating and processing device to appear to the computer as a digital storage device," "has two separate ports providing input of analog data on one port and subsequent transfer of digitized analog data to a computer on another port," "an analog data acquisition device having both an analog input and a host computer interface port which can emulate a hard disk," and "automatic file transfer of acquired digitized analog data without requiring user loaded file transfer enabling software"; as also previously discussed, Shinohara's hard disk drive emulation by the flash memory card is not dramatically different because the examiner is combining <u>Shinohara</u>'s hard disk drive emulation by the flash memory card into <u>Hashimoto</u>'s flash memory card (i.e. both Shinohara and Hashimoto include the same flash memory card).

<u>Hashimoto</u> is compatible with other references because, base on the assumption that applicant's analysis of <u>Hashimoto</u> is correct, <u>Hashimoto</u> is not limited to one way

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communication, as <u>Hashimoto</u> does have two way exchange via a switch; to further clarify, the combination of the references would teach/suggest two way exchange via switch (e.g. electrical switch control by host) for implementing Plug and Play functionality or the combination of the references is not limited to DTR signaling and two way exchange take place without the need of the switch for implementing the Plug and Play functionality; additionally, as discussed above, <u>Hashimoto</u> and <u>Shinohara</u> are compatible as both have the corresponding flash memory card.

3. In response to applicant's arguments with regard to the claim 333, 370 and 375 rejected under 35 U.S.C. 103(a) that the combination of the references does not teach/suggest the claimed feature "transferring data from the digital camera directly to the hard disks of the host computer while bypassing the host computer processor" because none of the references even mention direct transfer bypassing the processor; applicant's arguments have fully been considered, but are not found to be persuasive.

The examiner respectfully disagrees, because as the combination of the references does teach/suggest the inventive concept for the instant application as discussed in detail above, the combination of the references does further teach/suggest the direct transfer bypassing the processor as data is transferred from the digital camera directly to the hard disk drive device of the computer; to further clarify, as the connected analog device is recognized as a hard disk drive, the hard disk drive on the host can directly communicate with the connected analog device via the hard disk drive emulation for transferring the data from the analog device's flash memory card to the

host's hard disk drive (e.g. communication between hard disk drives) (<u>Hashimoto</u>, Fig. 1A-1B; Fig. 8; Fig. 11-12; Fig. 14-15; col. 1, II. 27-57; col. 3, I. 43 to col. 4, I. 67; col. 5, II. 43-57; col. 6, I. 16 to col. 9, I. 17; col. 9, I. 46 to col. 11, I. 42; col. 12, I. 16 to col. 14, I. 14; <u>Smith</u>, Fig. 2-5; col. 1, II. 9-22; col. 2, I. 40 to col. 3, I. 8; col. 3, II. 22-27; col. 3, II. 53-59; col. 4, II. 5-34; col. 6, II. 63-62; <u>Ristelhueber</u>, pages 1-3; and <u>Shinohara</u>, col. 1, II. 48-60; col. 3, I. 56 to col. 4, I. 49).

4. In response to applicant's arguments with regard to the claims 334 and 372 rejected under 35 U.S.C. 103(a) that the combination of the references does not teach/suggest the claimed feature "call a driver which is part of the manufacturer installed BIOS to enable data transfer between the device and the host"; applicant's arguments have fully been considered, but are not found to be persuasive.

The examiner respectfully disagrees, because Plug and Play protocol calls a driver which is part of the manufacturer installed BIOS; therefore the data transfer between the device and the host requires to call the driver for the device, wherein the driver is part of the manufacturer installed BIOS (<u>Hashimoto</u>, Fig. 1A-1B; Fig. 8; Fig. 11-12; Fig. 14-15; col. 1, II. 27-57; col. 3, I. 43 to col. 4, I. 67; col. 5, II. 43-57; col. 6, I. 16 to col. 9, I. 17; col. 9, I. 46 to col. 11, I. 42; col. 12, I. 16 to col. 14, I. 14; <u>Smith</u>, Fig. 2-5; col. 1, II. 9-22; col. 2, I. 40 to col. 3, I. 8; col. 3, II. 22-27; col. 3, II. 53-59; col. 4, II. 5-34; col. 6, II. 63-62; <u>Ristelhueber</u>, pages 1-3; and <u>Shinohara</u>, col. 1, II. 48-60; col. 3, I. 56 to col. 4, I. 49).

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5. In response to applicant's argument that the examiner's conclusion of obviousness is based upon improper hindsight reasoning, it must be recognized that any judgment on obviousness is in a sense necessarily a reconstruction based upon hindsight reasoning. But so long as it takes into account only knowledge which was within the level of ordinary skill at the time the claimed invention was made, and does not include knowledge gleaned only from the applicant's disclosure, such a reconstruction is proper. See *In re McLaughlin*, 443 F.2d 1392, 170 USPQ 209 (CCPA 1971).

I. INTERVIEW SUMMARY

6. The interview mainly focused on getting a clear understand of applicant's claimed invention, wherein the examiner requested the applicant to clarify how applicant's inventive concept should be characterized, as applicant's indicated in applicant's response, dated 05/10/2011, that the applicant's disagree with the examiner's recharacterization of applicant's claimed invention, and the applicant in response, provided the following explanation:

Applicant indicated that the inventive concept for the instant application is the claims, and concede that the following is how the invention concept is functioning:

Single analog sensing device with multiple parallel channels for acquiring analog data through the multiple parallel channels, wherein the single analog sensing device is connected to a digital device, such as a host, and the digital device (host) recognizing the connected single analog sensing device as a digital device, such as a hard drive

(e.g. digital storage device) or printer; and when the single analog sensing device is connected to the digital device (host) for transferring the acquired analog data to the digital device (host), the digital device (host) use a corresponding digital device driver, such as hard drive driver, for communicating with the single analog sensing device, as the digital device (host) thinks that the connected single analog sensing device is the hard drive (digital device).

Additionally, because the utilization of digital device driver (hard drive driver) by the host (digital device), end user loading of any software onto the computer at any time and end user interaction with the computer to set up a file system is not required, as the host (digital device) thinks that the connected single analog sensing device is the hard drive (digital device), and the hard drive driver (digital device driver) is part of the host, that is the host already have the needed digital device driver (hard disk driver).

The examiner then inquired the applicant, base on the applicant's best knowledge, if there is anything out there that has an analog device with multiple parallel channels conventionally? And applicant responded that, at the time when this application was filed, applicant thinks multi-channel analog device exists.

II. REJECTIONS BASED ON PRIOR ART

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the

invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 239, 333-339, 341-345, 346-362, 364-367 and 369-376 are rejected under 35 U.S.C. 103(a) as being unpatentable over <u>Hashimoto et al.</u> (US Patent 6,111,604) in view of <u>Smith et al.</u> (US Patent 5,634,075), <u>Ristelhueber : "Plug and play</u> is almost here" and <u>Shinohara</u> (US Patent 5,742,934).

8. As per claim 239, <u>Hashimoto</u> teaches an analog data generating and processing device (ADGPD), comprising:

an input/output (i/o) port (Fig. 1A-1B; Fig. 8; col. 1, II. 35-57; col. 3, I. 43 to col. 4, I. 67; col. 5, II. 43-57; col. 6, I. 16 to col. 9, I. 17; col. 10, I. 41 to col. 11, I. 42 and col. 12, I. 16 to col. 13, I. 14), as the digital camera system have the corresponding i/o port for connecting to the PC (Fig. 8, ref. 29);

a program memory (Fig. 9, ref. 52, 54-55 and col. 8, l. 48 to col. 9, l. 17);

a data storage memory (Fig. 8, ref. 16; Fig. 10; col. 6, l. 16 to col. 8, l. 47 and col.

9, ll. 18-45);

a processor (Fig. 8, ref. 11, 23) operatively interfaced with the i/o port, the program memory (Fig. 9, ref. 52, 54-55) and the data storage memory (Fig. 8, ref. 16) (Fig. 8; Fig. 9; col. 6, l. 16 to col. 9, l. 17 and col. 10, l. 41 to col. 11, l. 42);

wherein the processor is adapted to implement a data generation process by which analog data (e.g. audio and visual analog data) is acquired from each respective analog acquisition channel of a plurality of independent analog acquisition channels (e.g. channel for audio analog data and channel for visual analog data), the analog data

from each respective channel is digitized (e.g. via analog to digital converter), coupled into the processor, and is processed by the processor, and the processed and digitized analog data is stored in the data storage memory (Fig. 8, ref. 16 and Fig. 10) as at least one file of digitized analog data (Fig. 12) (Fig. 1A-1B; Fig. 8; Fig. 11-12; Fig. 14-15; col. 1, II. 35-57; col. 3, I. 43 to col. 4, I. 57; col. 5, II. 43-57; col. 6, I. 16 to col. 9, I. 17 and col. 9, I. 46 to col. 10, I. 16);

wherein the processor also is adapted to be involved in an automatic recognition process in which, when the i/o port is operatively interfaced with a multi-purpose interface of a host computer, the processor executes at least one instruction set stored in the program memory; and wherein the processor is further adapted to be involved in an automatic file transfer process in which, when the i/o port is operatively interfaced with the multi-purpose interface of the computer, the processor executes at least one other instruction set stored in the program memory to thereby cause the at least one file of digitized analog data acquired from at least one of the plurality of analog acquisition channels to be transferred to the computer (Fig. 9; Fig. 11-12; Fig. 14-15; col. 1, II. 27-57; col. 6, I. 16 to col. 9, I. 17; col. 9, I. 46 to col. 11, I. 42 and col. 12, I. 16 to col. 14, I. 14), wherein the digital camera's CPU (Fig. 8, ref. 23) control the operation of the digital camera for the data transferring after the digital camera is connected to and recognized by the PC, and as the digital camera's CPU control any function of the digital camera, the digital camera's CPU further controls the digital camera to be recognized by the PC; wherein the digital camera needs to be recognized by the PC in order for the PC to

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know what peripheral device is connected such that the PC knows how to properly communicate with the connected peripheral device.

<u>Hashimoto</u> does not teach the ADGPD comprising: automatic recognition process of a host computer; causes at least one parameter identifying the analog data generating and processing device, independent of analog data source, as a digital storage device instead of as an analog data generating and processing device to be automatically sent through the i/o port and to the multi-purpose interface of the computer (a) without requiring any end user to load any software onto the computer at any time and (b) without requiring any end user to interact with the computer to set up a file system in the ADGPD at any time;

wherein the at least one parameter provides information to the computer about file transfer characteristics of the ADGPD; and

data transferring, after the at least one parameter has been sent from the i/o port to the multi-purpose interface of the computer, using a device driver for the digital storage device while causing the analog data generating and processing device to appear to the computer as if it were the digital storage device without requiring any user-loaded file transfer enabling software to be loaded on or installed in the computer at any time.

<u>Smith</u> teaches a system and a method comprising: automatic recognition process of a host computer, wherein at least one parameter (e.g. parameter signifying that the peripheral device has the ability communicate in accordance to the at least one

software driver) to be automatically sent through the i/o port and to the multi-purpose interface of the host computer (Fig. 2-5; col. 1, II. 9-22; col. 2, I. 40 to col. 3, I. 59; col. 4, II. 5-34 and col. 6, II. 63-62), by combining the plug-and-play functionality with <u>Hashimoto</u>'s automatic recognition process, the resulting combination further teaches the automatic recognition process corresponding to configuring plug and play system utilizing ROM BIOS by having the operating system load the device driver after the peripheral device is coupled to the PC for installation.

It would have been obvious for one of ordinary skill in this art, at the time of invention was made to include <u>Smith</u>'s plug and play functionality into <u>Hashimoto</u>'s automatic recognition process for the benefit of simplifying the installation of the peripheral device for the user as the peripheral device may be installed without the need for the user to install software or configure the peripheral device (<u>Smith</u>, col. 2, II. 40-67 and col. 5, II. 41-51 and col. 6, II. 63-65) to obtain the invention as specified in claim 239.

Hashimoto and Smith do not teach the ADGPD comprising: identifying the analog data generating and processing device, independent of analog data source, as a digital storage device instead of as an analog data generating and processing device (a) without ... load any software onto the computer at any time and (b) without requiring any end user to interact with the computer to set up a file system in the ADGPD at any time;

wherein the at least one parameter provides information to the computer about file transfer characteristics of the ADGPD; and

data transferring, after the at least one parameter has been sent from the i/o port to the multi-purpose interface of the computer, using a device driver for the digital storage device while causing the analog data generating and processing device to appear to the computer as if it were the digital storage device without requiring any user-loaded file transfer enabling software to be loaded on or installed in the computer at any time.

<u>Ristelhueber</u> teaches a system and a method comprising a peripheral device having an automatic recognition process without requiring any end user to load any software onto the computer at any time (pages 1-3), wherein the resulting combination of the references further teaches the above automatic recognition process corresponds to plug and play of a peripheral device by having a user to simply insert a peripheral into a desktop system and have it start running immediately, as the PnP computer will automatically identify any new hardware installed and configure the new hardware, and relieving the end user of any need to fumble with floppy disks and user manuals to get the device up and running; therefore, the installation of the peripheral device is accomplished without any type of software/driver being loaded by the user.

It would have been obvious for one of ordinary skill in this art, at the time of invention was made to include <u>Ristelhueber</u>'s alleviating user loading software/driver into <u>Hashimoto</u> and <u>Smith</u>'s plug-and-play processor, not only is such implementation well known to be in accord with the plug-and-play standard, but also for the benefit of

Application/Control Number: 11/467,092Page 28Art Unit: 2181simplifying the end user's PC upgrading and reducing cost for the computing industry(Ristelhueber, page 2, 3rd paragraph) to obtain the invention as specified in claim 239.

<u>Hashimoto</u>, <u>Smith</u> and <u>Ristelhueber</u> do not expressly teach the ADGPD comprising: identifying the analog data generating and processing device, independent of analog data source, as a digital storage device instead of as an analog data generating and processing device without requiring any end user to interact with the computer to set up a file system in the ADGPD at any time;

wherein the at least one parameter provides information to the computer about file transfer characteristics of the ADGPD; and

data transferring, after the at least one parameter has been sent from the i/o port to the multi-purpose interface of the computer, using a device driver for the digital storage device while causing the analog data generating and processing device to appear to the computer as if it were the digital storage device without requiring any user-loaded file transfer enabling software to be loaded on or installed in the computer at any time.

Shinohara teaches a system and a method comprising:

identifying the analog data generating and processing device, independent of analog data source, as a digital storage device instead of as an analog data generating and processing device without requiring any end user to interact with the computer to set up a file system in the ADGPD at any time (col. 1, II. 48-60 and col. 3, I. 33 to col. 4, I. 49), by combining the flash memory card emulating of a mass storage device (e.g.

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hard disk drive) with <u>Hashimoto</u>, <u>Smith</u>, <u>Kerigan</u> and <u>Ristelhueber</u>'s plug-and-play digital camera device having the processor and the flash memory card for data transferring with the host computer, the resulting combination of the references further teaches the above claimed feature, which is in accordance to the applicant's disclosure of the core novelty for the instant invention as disclosed by the applicant during the interview dated 10/06/2010;

wherein the at least one parameter provides information to the computer about file transfer characteristics (e.g. associated emulating hard disk drive data transferring characteristics) of the ADGPD (col. 1, II. 48-60 and col. 3, I. 33 to col. 4, I. 49), by combining the flash memory card emulating a mass storage device (e.g. hard disk drive) with <u>Hashimoto</u>, <u>Smith</u>, <u>Kerigan</u> and <u>Ristelhueber</u>'s plug-and-play digital camera device having the processor and the flash memory card for data transferring with the host computer, the resulting combination of the references further teaches the above claimed feature, which is in accordance to the applicant's disclosure of the core novelty for the instant invention as disclosed by the applicant during the interview dated 10/06/2010; and

data transferring, after the at least one parameter has been sent from the i/o port to the multi-purpose interface of the computer, using a device driver (e.g. hard disk drive device driver) for the digital storage device while causing the analog data generating and processing device to appear to the computer as if it were the digital storage device (e.g. hard disk drive) without requiring any user-loaded file transfer enabling software to be loaded on or installed in the computer at any time (col. 1, II. 48-60 and col. 3, I. 33 to

col. 4, I. 49), by combining the flash memory card emulating a mass storage device (e.g. hard disk drive) with <u>Hashimoto</u>, <u>Smith</u>, <u>Kerigan</u> and <u>Ristelhueber</u>'s plug-and-play digital camera device having the processor and the flash memory card for data transferring with the host computer, the resulting combination of the references further teaches the above claimed feature, which is in accordance to the applicant's disclosure of the core novelty for the instant invention as disclosed by the applicant during the interview dated 10/06/2010.

It would have been obvious for one of ordinary skill in this art, at the time of invention was made to include <u>Shinohara</u>'s hard disk drive emulation into <u>Hashimoto</u>, <u>Smith</u>, <u>Kerigan</u> and <u>Ristelhueber</u>'s plug-and-play processor for reading data from the memory card for the benefit of expanding the lifetime usage of the memory card (<u>Shinohara</u>, col. 2, II. 7-8) to obtain the invention as specified in claim 239.

9. As per claim 333, <u>Hashimoto</u>, <u>Smith</u>, <u>Ristelhueber</u> and <u>Shinohara</u> teach all the of limitations claim 239 as discussed above, where <u>Hashimoto</u>, <u>Smith</u>, <u>Ristelhueber</u> and <u>Shinohara</u> further teach the ADGPD comprising wherein the processor is configured to transmit to the computer active commands through the multi-purpose interface to access a system bus of the computer to enable communication directly with other devices of the computer while bypassing the computer processor (<u>Hashimoto</u>, Fig. 1A-1B; Fig. 8; Fig. 11-12; Fig. 14-15; col. 1, II. 27-57; col. 3, I. 43 to col. 4, I. 67; col. 5, II. 43-57; col. 6, I. 16 to col. 9, I. 17; col. 9, I. 46 to col. 11, I. 42; col. 12, I. 16 to col. 14, I. 14; <u>Smith</u>, Fig. 2-5; col. 1, II. 9-22; col. 2, I. 40 to col. 3, I. 8; col. 3, II. 22-27; col. 3, II. 53-

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59; col. 4, II. 5-34; col. 6, II. 63-62; <u>Ristelhueber</u>, pages 1-3; and <u>Shinohara</u>, col. 1, II. 48-60; col. 3, I. 56 to col. 4, I. 49), as the resulting combination of the references does teach/suggest the heart/core of applicant's invention, it would have been obvious for the resulting combination of the references to further teach the transferring of data from the digital camera directly to the hard disk drive device of the computer.

10. As per claim 334, <u>Hashimoto, Smith, Ristelhueber</u> and <u>Shinohara</u> teach all the of limitations claim 239 as discussed above, where <u>Hashimoto, Smith, Ristelhueber</u> and <u>Shinohara</u> further teach the ADGPD comprising wherein the at least one parameter identifies the analog data generating and processing device as a hard disk drive (e.g. hard disk emulation) and wherein data transfer between the analog data generating and processing device as a hard disk driver program which is matched to the host computer is enabled by a hard disk driver program which is matched to the host computer and part of a manufacturer installed BIOS of the host computer (<u>Hashimoto</u>, Fig. 1A-1B; Fig. 8; Fig. 11-12; Fig. 14-15; col. 1, II. 27-57; col. 3, I. 43 to col. 4, I. 67; col. 5, II. 43-57; col. 6, I. 16 to col. 9, I. 17; col. 9, I. 46 to col. 11, I. 42; col. 12, I. 16 to col. 14, I. 14; <u>Smith</u>, Fig. 2-5; col. 1, II. 9-22; col. 2, I. 40 to col. 3, I. 8; col. 3, II. 22-27; col. 3, II. 53-59; col. 4, II. 5-34; col. 6, II. 63-62; <u>Ristelhueber</u>, pages 1-3; and <u>Shinohara</u>, col. 1, II. 48-60; col. 3, I. 56 to col. 4, I. 49).

11. As per claim 335, <u>Hashimoto</u>, <u>Smith</u>, <u>Ristelhueber</u> and <u>Shinohara</u> teach all the of limitations claim 239 as discussed above, where <u>Hashimoto</u>, <u>Smith</u>, <u>Ristelhueber</u> and <u>Shinohara</u> further teach the ADGPD further comprising at least one additional analog

data generating and processing device coupled to the computer in parallel and each analog data generating and processing device attached to a difference analog data source (<u>Hashimoto</u>, Fig. 1A-1B; Fig. 8; Fig. 11-12; Fig. 14-15; col. 1, II. 27-57; col. 3, I. 43 to col. 4, I. 67; col. 5, II. 43-57; col. 6, I. 16 to col. 9, I. 17; col. 9, I. 46 to col. 11, I. 42; col. 12, I. 16 to col. 14, I. 14; <u>Smith</u>, Fig. 2-5; col. 1, II. 9-22; col. 2, I. 40 to col. 3, I. 8; col. 3, II. 22-27; col. 3, II. 53-59; col. 4, II. 5-34; col. 6, II. 63-62; <u>Ristelhueber</u>, pages 1-3; and <u>Shinohara</u>, col. 1, II. 48-60; col. 3, I. 56 to col. 4, I. 49), as the resulting combination of the references does teach/suggest the heart/core of applicant's invention, it would have been obvious for the resulting combination of the references to further teach more than one peripheral device (e.g. digital camera) is connected to the computer.

12. As per claim 336, <u>Hashimoto</u>, <u>Smith</u>, <u>Ristelhueber</u> and <u>Shinohara</u> teach all the of limitations claim 239 as discussed above, where <u>Hashimoto</u>, <u>Smith</u>, <u>Ristelhueber</u> and <u>Shinohara</u> further teach the ADGPD comprising wherein processor is configured to format the digitized analog data into blocks of data with block sizes suitable for a hard disk of the computer (<u>Hashimoto</u>, Fig. 1A-1B; Fig. 8; Fig. 11-12; Fig. 14-15; col. 1, II. 27-57; col. 3, I. 43 to col. 4, I. 67; col. 5, II. 43-57; col. 6, I. 16 to col. 9, I. 17; col. 9, I. 46 to col. 11, I. 42; col. 12, I. 16 to col. 14, I. 14; <u>Smith</u>, Fig. 2-5; col. 1, II. 9-22; col. 2, I. 40 to col. 3, I. 8; col. 3, II. 22-27; col. 3, II. 53-59; col. 4, II. 5-34; col. 6, II. 63-62; <u>Ristelhueber</u>, pages 1-3; and <u>Shinohara</u>, col. 1, II. 48-60; col. 3, I. 56 to col. 4, I. 49), as the digital camera is emulating the hard disk drive, data being transferred from the digital camera is hard disk drive data, suitable for the computer's hard disk.

13. As per claim 337, <u>Hashimoto</u>, <u>Smith</u>, <u>Ristelhueber</u> and <u>Shinohara</u> teach all the of limitations claim 239 as discussed above, where <u>Hashimoto</u>, <u>Smith</u>, <u>Ristelhueber</u> and <u>Shinohara</u> further teach the ADGPD further comprising a data buffer coupled to the processor to permit independence of time of data acquisition and data transfer to the host computer (<u>Hashimoto</u>, Fig. 1A-1B; Fig. 8; Fig. 11-12; Fig. 14-15; col. 1, II. 27-57; col. 3, I. 43 to col. 4, I. 67; col. 5, II. 43-57; col. 6, I. 16 to col. 9, I. 17; col. 9, I. 46 to col. 11, I. 42; col. 12, I. 16 to col. 14, I. 14; <u>Smith</u>, Fig. 2-5; col. 1, II. 9-22; col. 2, I. 40 to col. 3, I. 8; col. 3, II. 22-27; col. 3, II. 53-59; col. 4, II. 5-34; col. 6, II. 63-62; <u>Ristelhueber</u>, pages 1-3; and <u>Shinohara</u>, col. 1, II. 48-60; col. 3, I. 56 to col. 4, I. 49), as the resulting combination of the references does teach/suggest the heart/core of applicant's invention, it would have been obvious for the resulting combination of the references to further teach above the data buffer architecture.

14. As per claim 338, <u>Hashimoto</u>, <u>Smith</u>, <u>Ristelhueber</u> and <u>Shinohara</u> teach all the of limitations claim 239 as discussed above, where <u>Hashimoto</u>, <u>Smith</u>, <u>Ristelhueber</u> and <u>Shinohara</u> further teach the ADGPD comprising wherein each of the plurality of analog acquisition channels are independently programmable and further comprise a plurality of corresponding sample and hold amplifiers for simultaneous sampling on the plurality of analog acquisition channels to permit simultaneous analog data acquisition from a plurality of respective analog data sources (<u>Hashimoto</u>, Fig. 1A-1B; Fig. 8; Fig. 11-12; Fig. 14-15; col. 1, II. 27-57; col. 3, I. 43 to col. 4, I. 67; col. 5, II. 43-57; col. 6, I. 16 to col.

9, I. 17; col. 9, I. 46 to col. 11, I. 42; col. 12, I. 16 to col. 14, I. 14; <u>Smith</u>, Fig. 2-5; col. 1,
II. 9-22; col. 2, I. 40 to col. 3, I. 8; col. 3, II. 22-27; col. 3, II. 53-59; col. 4, II. 5-34; col. 6, II.
63-62; <u>Ristelhueber</u>, pages 1-3; and <u>Shinohara</u>, col. 1, II. 48-60; col. 3, I. 56 to col. 4, I.
49), as the resulting combination of the references does teach/suggest the heart/core of applicant's invention, it would have been obvious for the resulting combination of the references to further teach the above claimed feature as the audio and image data are simultaneously captured in order for proper generating the corresponding video data.

15. As per claim 339, <u>Hashimoto, Smith, Ristelhueber</u> and <u>Shinohara</u> teach all the of limitations claim 233 as discussed above, where <u>Hashimoto, Smith, Ristelhueber</u> and <u>Shinohara</u> further teach the ADGPD comprising wherein the active commands initiate active access to write data directly to a hard drive in the host computer independent of the host computer central processor (<u>Hashimoto</u>, Fig. 1A-1B; Fig. 8; Fig. 11-12; Fig. 14-15; col. 1, II. 27-57; col. 3, I. 43 to col. 4, I. 67; col. 5, II. 43-57; col. 6, I. 16 to col. 9, I. 17; col. 9, I. 46 to col. 11, I. 42; col. 12, I. 16 to col. 14, I. 14; <u>Smith</u>, Fig. 2-5; col. 1, II. 9-22; col. 2, I. 40 to col. 3, I. 8; col. 3, II. 22-27; col. 3, II. 53-59; col. 4, II. 5-34; col. 6, II. 63-62; <u>Ristelhueber</u>, pages 1-3; and <u>Shinohara</u>, col. 1, II. 48-60; col. 3, I. 56 to col. 4, I. 49), as the resulting combination of the references does teach/suggest the heart/core of applicant's invention, it would have been obvious for the resulting combination of the references to further teach the transferring of data from the digital camera directly to the hard disk drive device of the computer.

16. As per claim 341, <u>Hashimoto</u>, <u>Smith</u>, <u>Ristelhueber</u> and <u>Shinohara</u> teach all the of limitations claim 239 as discussed above, where <u>Hashimoto</u>, <u>Smith</u>, <u>Ristelhueber</u> and <u>Shinohara</u> further teach the ADGPD comprising wherein the analog data generating and processing device is attached directly to at least one analog source (<u>Hashimoto</u>, Fig. 1A-1B; Fig. 8; Fig. 11-12; Fig. 14-15; col. 1, II. 27-57; col. 3, I. 43 to col. 4, I. 67; col. 5, II. 43-57; col. 6, I. 16 to col. 9, I. 17; col. 9, I. 46 to col. 11, I. 42; col. 12, I. 16 to col. 14, I. 14; <u>Smith</u>, Fig. 2-5; col. 1, II. 9-22; col. 2, I. 40 to col. 3, I. 8; col. 3, II. 22-27; col. 3, II. 53-59; col. 4, II. 5-34; col. 6, II. 63-62; <u>Ristelhueber</u>, pages 1-3; and <u>Shinohara</u>, col. 1, II. 48-60; col. 3, I. 56 to col. 4, I. 49).

17. As per claim 342, <u>Hashimoto</u>, <u>Smith</u>, <u>Ristelhueber</u> and <u>Shinohara</u> teach all the of limitations claim 239 as discussed above, where <u>Hashimoto</u>, <u>Smith</u>, <u>Ristelhueber</u> and <u>Shinohara</u> further teach the ADGPD comprising wherein the analog data generating and processing device is a stand alone device (<u>Hashimoto</u>, Fig. 1A-1B; Fig. 8; Fig. 11-12; Fig. 14-15; col. 1, II. 27-57; col. 3, I. 43 to col. 4, I. 67; col. 5, II. 43-57; col. 6, I. 16 to col. 9, I. 17; col. 9, I. 46 to col. 11, I. 42; col. 12, I. 16 to col. 14, I. 14; <u>Smith</u>, Fig. 2-5; col. 1, II. 9-22; col. 2, I. 40 to col. 3, I. 8; col. 3, II. 22-27; col. 3, II. 53-59; col. 4, II. 5-34; col. 6, II. 63-62; <u>Ristelhueber</u>, pages 1-3; and <u>Shinohara</u>, col. 1, II. 48-60; col. 3, I. 56 to col. 4, I. 49).

18. As per claim 343, <u>Hashimoto</u>, <u>Smith</u>, <u>Ristelhueber</u> and <u>Shinohara</u> teach all the of limitations claim 239 as discussed above, where <u>Hashimoto</u>, <u>Smith</u>, <u>Ristelhueber</u> and

<u>Shinohara</u> further teach the ADGPD comprising wherein the input/output port further comprises a SCSI interface circuit (<u>Hashimoto</u>, Fig. 1A-1B; Fig. 8; Fig. 11-12; Fig. 14-15; col. 1, II. 27-57; col. 3, I. 43 to col. 4, I. 67; col. 5, II. 43-57; col. 6, I. 16 to col. 9, I. 17; col. 9, I. 46 to col. 11, I. 42; col. 12, I. 16 to col. 14, I. 14; <u>Smith</u>, Fig. 2-5; col. 1, II. 9-22; col. 2, I. 40 to col. 3, I. 8; col. 3, II. 22-27; col. 3, II. 53-59; col. 4, II. 5-34; col. 6, II. 63-62; <u>Ristelhueber</u>, pages 1-3; and <u>Shinohara</u>, col. 1, II. 48-60; col. 3, I. 56 to col. 4, I. 49).

19. As per claim 344, <u>Hashimoto</u>, <u>Smith</u>, <u>Ristelhueber</u> and <u>Shinohara</u> teach all the of limitations claim 335 as discussed above, where <u>Hashimoto</u>, <u>Smith</u>, <u>Ristelhueber</u> and <u>Shinohara</u> further teach the ADGPD comprising wherein as least some of the analog data sources are analog data sources of different types (<u>Hashimoto</u>, Fig. 1A-1B; Fig. 8; Fig. 11-12; Fig. 14-15; col. 1, II. 27-57; col. 3, I. 43 to col. 4, I. 67; col. 5, II. 43-57; col. 6, I. 16 to col. 9, I. 17; col. 9, I. 46 to col. 11, I. 42; col. 12, I. 16 to col. 14, I. 14; <u>Smith</u>, Fig. 2-5; col. 1, II. 9-22; col. 2, I. 40 to col. 3, I. 8; col. 3, II. 22-27; col. 3, II. 53-59; col. 4, II. 5-34; col. 6, II. 63-62; <u>Ristelhueber</u>, pages 1-3; and <u>Shinohara</u>, col. 1, II. 48-60; col. 3, I. 56 to col. 4, I. 49).

20. As per claim 345, <u>Hashimoto</u>, <u>Smith</u>, <u>Ristelhueber</u> and <u>Shinohara</u> teach all the of limitations claim 239 as discussed above, where <u>Hashimoto</u>, <u>Smith</u>, <u>Ristelhueber</u> and <u>Shinohara</u> further teach the ADGPD comprising wherein the analog data generating and processing device processor interprets a read command from the host computer as a data transfer command to initiate transfer of digitized analog data from the analog

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acquisition channels to the host computer (<u>Hashimoto</u>, Fig. 1A-1B; Fig. 8; Fig. 11-12; Fig. 14-15; col. 1, II. 27-57; col. 3, I. 43 to col. 4, I. 67; col. 5, II. 43-57; col. 6, I. 16 to col. 9, I. 17; col. 9, I. 46 to col. 11, I. 42; col. 12, I. 16 to col. 14, I. 14; <u>Smith</u>, Fig. 2-5; col. 1, II. 9-22; col. 2, I. 40 to col. 3, I. 8; col. 3, II. 22-27; col. 3, II. 53-59; col. 4, II. 5-34; col. 6, II. 63-62; <u>Ristelhueber</u>, pages 1-3; and <u>Shinohara</u>, col. 1, II. 48-60; col. 3, I. 56 to col. 4, I. 49), wherein the resulting combination of the references is functionally equivalent to the above claimed features for transferring data to the host computer.

21. As per claim 346, <u>Hashimoto</u>, <u>Smith</u>, <u>Ristelhueber</u> and <u>Shinohara</u> teach all the of limitations claim 239 as discussed above, where <u>Hashimoto</u>, <u>Smith</u>, <u>Ristelhueber</u> and <u>Shinohara</u> further teach the ADGPD comprising wherein the analog data generating and processing device is adapted to be interfaced with the multi-purpose interface of the computer by means of a cable (<u>Hashimoto</u>, Fig. 1A-1B; Fig. 8; Fig. 11-12; Fig. 14-15; col. 1, II. 27-57; col. 3, I. 43 to col. 4, I. 67; col. 5, II. 43-57; col. 6, I. 16 to col. 9, I. 17; col. 9, I. 46 to col. 11, I. 42; col. 12, I. 16 to col. 14, I. 14; <u>Smith</u>, Fig. 2-5; col. 1, II. 9-22; col. 2, I. 40 to col. 3, I. 8; col. 3, II. 22-27; col. 3, II. 53-59; col. 4, II. 5-34; col. 6, II. 63-62; <u>Ristelhueber</u>, pages 1-3; and <u>Shinohara</u>, col. 1, II. 48-60; col. 3, I. 56 to col. 4, I. 49).

22. As per claim 347, <u>Hashimoto</u>, <u>Smith</u>, <u>Ristelhueber</u> and <u>Shinohara</u> teach all the of limitations claim 239 as discussed above, where <u>Hashimoto</u>, <u>Smith</u>, <u>Ristelhueber</u> and <u>Shinohara</u> further teach the ADGPD comprising wherein at least one of the analog sources is a sensor that is operatively interfaced with the analog data generating and

processing device and that is designed to generate the analog data (<u>Hashimoto</u>, Fig. 1A-1B; Fig. 8; Fig. 11-12; Fig. 14-15; col. 1, II. 27-57; col. 3, I. 43 to col. 4, I. 67; col. 5, II. 43-57; col. 6, I. 16 to col. 9, I. 17; col. 9, I. 46 to col. 11, I. 42; col. 12, I. 16 to col. 14, I. 14; <u>Smith</u>, Fig. 2-5; col. 1, II. 9-22; col. 2, I. 40 to col. 3, I. 8; col. 3, II. 22-27; col. 3, II. 53-59; col. 4, II. 5-34; col. 6, II. 63-62; <u>Ristelhueber</u>, pages 1-3; and <u>Shinohara</u>, col. 1, II. 48-60; col. 3, I. 56 to col. 4, I. 49).

23. As per claim 348, Hashimoto, Smith, Ristelhueber and Shinohara teach all the of limitations claim 239 as discussed above, where Hashimoto, Smith, Ristelhueber and Shinohara further teach the ADGPD comprising wherein the processor is configured to transmit to the computer active commands through the multipurpose interface to access a system bus of the computer to enable communication directly with other devices of the computer while bypassing the computer processor without requiring the user to load enabling software (Hashimoto, Fig. 1A-1B; Fig. 8; Fig. 11-12; Fig. 14-15; col. 1, II. 27-57; col. 3, l. 43 to col. 4, l. 67; col. 5, ll. 43-57; col. 6, l. 16 to col. 9, l. 17; col. 9, l. 46 to col. 11, l. 42; col. 12, l. 16 to col. 14, l. 14; Smith, Fig. 2-5; col. 1, ll. 9-22; col. 2, l. 40 to col. 3, I. 8; col. 3, II. 22-27; col. 3, II. 53-59; col. 4, II. 5-34; col. 6, II. 63-62; Ristelhueber, pages 1-3; and Shinohara, col. 1, II. 48-60; col. 3, I. 56 to col. 4, I. 49), as the resulting combination of the references does teach/suggest the heart/core of applicant's invention, it would have been obvious for the resulting combination of the references to further teach the transferring of data from the digital camera directly to the hard disk drive device of the computer via the system bus of the computer.

24. As per claim 349, <u>Hashimoto</u>, <u>Smith</u>, <u>Ristelhueber</u> and <u>Shinohara</u> teach all the of limitations claim 239 as discussed above, where <u>Hashimoto</u>, <u>Smith</u>, <u>Ristelhueber</u> and <u>Shinohara</u> further teach the ADGPD comprising wherein the plurality of analog acquisition channels are independently programmable (<u>Hashimoto</u>, Fig. 1A-1B; Fig. 8; Fig. 11-12; Fig. 14-15; col. 1, II. 27-57; col. 3, I. 43 to col. 4, I. 67; col. 5, II. 43-57; col. 6, I. 16 to col. 9, I. 17; col. 9, I. 46 to col. 11, I. 42; col. 12, I. 16 to col. 14, I. 14; <u>Smith</u>, Fig. 2-5; col. 1, II. 9-22; col. 2, I. 40 to col. 3, I. 8; col. 3, II. 22-27; col. 3, II. 53-59; col. 4, II. 5-34; col. 6, II. 63-62; <u>Ristelhueber</u>, pages 1-3; and <u>Shinohara</u>, col. 1, II. 48-60; col. 3, I. 56 to col. 4, I. 49), as the resulting combination of the references does teach/suggest the heart/core of applicant's invention, it would have been obvious for the resulting combination of the references.

25. As per claim 350, <u>Hashimoto</u>, <u>Smith</u>, <u>Ristelhueber</u> and <u>Shinohara</u> teach all the of limitations claim 239 as discussed above, where <u>Hashimoto</u>, <u>Smith</u>, <u>Ristelhueber</u> and <u>Shinohara</u> further teach the ADGPD comprising wherein at least one analog source is designed to receive data from a host device (<u>Hashimoto</u>, Fig. 1A-1B; Fig. 8; Fig. 11-12; Fig. 14-15; col. 1, II. 27-57; col. 3, I. 43 to col. 4, I. 67; col. 5, II. 43-57; col. 6, I. 16 to col. 9, I. 17; col. 9, I. 46 to col. 11, I. 42; col. 12, I. 16 to col. 14, I. 14; <u>Smith</u>, Fig. 2-5; col. 1, II. 9-22; col. 2, I. 40 to col. 3, I. 8; col. 3, II. 22-27; col. 3, II. 53-59; col. 4, II. 5-34; col. 6, II. 63-62; <u>Ristelhueber</u>, pages 1-3; and <u>Shinohara</u>, col. 1, II. 48-60; col. 3, I. 56 to col. 4, I. 49), as the resulting combination of the references does teach/suggest the heart/core of

applicant's invention, it would have been obvious for the resulting combination of the references to further teach the host device receiving audiovisual information from the camera and communicating to the camera by updating control program to control the sensor.

26. As per claim 351, <u>Hashimoto</u>, <u>Smith</u>, <u>Ristelhueber</u> and <u>Shinohara</u> teach all the of limitations claim 239 as discussed above, where <u>Hashimoto</u>, <u>Smith</u>, <u>Ristelhueber</u> and <u>Shinohara</u> further teach the ADGPD comprising wherein at least one analog source comprises a multimeter that is operatively interfaced with the analog data generating and processing device and that is designed to generate the analog data (<u>Hashimoto</u>, Fig. 1A-1B; Fig. 8; Fig. 11-12; Fig. 14-15; col. 1, II. 27-57; col. 3, I. 43 to col. 4, I. 67; col. 5, II. 43-57; col. 6, I. 16 to col. 9, I. 17; col. 9, I. 46 to col. 11, I. 42; col. 12, I. 16 to col. 14, I. 14; <u>Smith</u>, Fig. 2-5; col. 1, II. 9-22; col. 2, I. 40 to col. 3, I. 8; col. 3, II. 22-27; col. 3, II. 53-59; col. 4, II. 5-34; col. 6, II. 63-62; <u>Ristelhueber</u>, pages 1-3; and <u>Shinohara</u>, col. 1, II. 48-60; col. 3, I. 56 to col. 4, I. 49), as the resulting combination of the references does teach/suggest the heart/core of applicant's invention, it would have been obvious for the resulting combination of the references to further implement the heart/core of applicant's invention in an alternative embodiment on the multimeter, as the multimeter, like the digital camera, is a portable stand along peripheral device.

27. As per claim 352, <u>Hashimoto</u>, <u>Smith</u>, <u>Ristelhueber</u> and <u>Shinohara</u> teach all the of limitations claim 239 as discussed above, where <u>Hashimoto</u>, <u>Smith</u>, <u>Ristelhueber</u> and

<u>Shinohara</u> further teach the ADGPD comprising wherein the at least one parameter is consistent with the analog data generating and processing device being responsive to a SCSI inquiry command (<u>Hashimoto</u>, Fig. 1A-1B; Fig. 8; Fig. 11-12; Fig. 14-15; col. 1, II. 27-57; col. 3, I. 43 to col. 4, I. 67; col. 5, II. 43-57; col. 6, I. 16 to col. 9, I. 17; col. 9, I. 46 to col. 11, I. 42; col. 12, I. 16 to col. 14, I. 14; <u>Smith</u>, Fig. 2-5; col. 1, II. 9-22; col. 2, I. 40 to col. 3, I. 8; col. 3, II. 22-27; col. 3, II. 53-59; col. 4, II. 5-34; col. 6, II. 63-62; <u>Ristelhueber</u>, pages 1-3; and <u>Shinohara</u>, col. 1, II. 48-60; col. 3, I. 56 to col. 4, I. 49).

28. As per claim 353, <u>Hashimoto</u>, <u>Smith</u>, <u>Ristelhueber</u> and <u>Shinohara</u> teach all the of limitations claim 239 as discussed above, where <u>Hashimoto</u>, <u>Smith</u>, <u>Ristelhueber</u> and <u>Shinohara</u> further teach the ADGPD comprising wherein the at least one parameter identifies the analog data generating and processing device as a digital mass storage device (<u>Hashimoto</u>, Fig. 1A-1B; Fig. 8; Fig. 11-12; Fig. 14-15; col. 1, II. 27-57; col. 3, I. 43 to col. 4, I. 67; col. 5, II. 43-57; col. 6, I. 16 to col. 9, I. 17; col. 9, I. 46 to col. 11, I. 42; col. 12, I. 16 to col. 14, I. 14; <u>Smith</u>, Fig. 2-5; col. 1, II. 9-22; col. 2, I. 40 to col. 3, I. 8; col. 3, II. 22-27; col. 3, II. 53-59; col. 4, II. 5-34; col. 6, II. 63-62; <u>Ristelhueber</u>, pages 1-3; and <u>Shinohara</u>, col. 1, II. 48-60; col. 3, I. 56 to col. 4, I. 49).

29. As per claim 354, <u>Hashimoto</u>, <u>Smith</u>, <u>Ristelhueber</u> and <u>Shinohara</u> teach all the of limitations claim 239 as discussed above, where <u>Hashimoto</u>, <u>Smith</u>, <u>Ristelhueber</u> and <u>Shinohara</u> further teach the ADGPD comprising wherein the processor is configured to, when the processor is operatively interfaced with the multi-purpose interface of the

computer and after the at least one parameter has been sent to the multi-purpose interface of the computer, execute at least one set of computer code stored in program memory and thereby cause analog data generating and processing device file system information to be automatically sent to the multipurpose interface without requiring any end user to interact with the computer to set up a file system in the analog data generating and processing device at any time (Hashimoto, Fig. 1A-1B; Fig. 8; Fig. 11-12; Fig. 14-15; col. 1, II. 27-57; col. 3, I. 43 to col. 4, I. 67; col. 5, II. 43-57; col. 6, I. 16 to col. 9, I. 17; col. 9, I. 46 to col. 11, I. 42; col. 12, I. 16 to col. 14, I. 14; <u>Smith</u>, Fig. 2-5; col. 1, II. 9-22; col. 2, I. 40 to col. 3, I. 8; col. 3, II. 22-27; col. 3, II. 53-59; col. 4, II. 5-34; col. 6, II. 63-62; <u>Ristelhueber</u>, pages 1-3; and <u>Shinohara</u>, col. 1, II. 48-60; col. 3, I. 56 to col. 4, I. 49).

30. As per claim 355, <u>Hashimoto</u>, <u>Smith</u>, <u>Ristelhueber</u> and <u>Shinohara</u> teach all the of limitations claim 254 as discussed above, where <u>Hashimoto</u>, <u>Smith</u>, <u>Ristelhueber</u> and <u>Shinohara</u> further teach the ADGPD comprising wherein the analog data generating and processing device file system information comprises at least one indication of a file system type that is used to store the at least one file of digitized analog data in the data storage memory (<u>Hashimoto</u>, Fig. 1A-1B; Fig. 8; Fig. 11-12; Fig. 14-15; col. 1, II. 27-57; col. 3, I. 43 to col. 4, I. 67; col. 5, II. 43-57; col. 6, I. 16 to col. 9, I. 17; col. 9, I. 46 to col. 11, I. 42; col. 12, I. 16 to col. 14, I. 14; <u>Smith</u>, Fig. 2-5; col. 1, II. 9-22; col. 2, I. 40 to col. 3, I. 8; col. 3, II. 22-27; col. 3, II. 53-59; col. 4, II. 5-34; col. 6, II. 63-62; <u>Ristelhueber</u>, pages 1-3; and <u>Shinohara</u>, col. 1, II. 48-60; col. 3, I. 56 to col. 4, I. 49), as the type of file

system corresponds to the plug-and-play ADGPD having the memory card emulating as the hard disk drive for data transferring after the plug-and-play ADGPD is connected to the PC.

31. As per claim 356, <u>Hashimoto</u>, <u>Smith</u>, <u>Ristelhueber</u> and <u>Shinohara</u> teach all the of limitations claim 239 as discussed above, where <u>Hashimoto</u>, <u>Smith</u>, <u>Ristelhueber</u> and <u>Shinohara</u> further teach the ADGPD comprising wherein the at least one parameter is consistent with the analog data generating and processing device being a digital mass storage device other than a magnetic floppy disk drive (<u>Hashimoto</u>, Fig. 1A-1B; Fig. 8; Fig. 11-12; Fig. 14-15; col. 1, II. 27-57; col. 3, I. 43 to col. 4, I. 67; col. 5, II. 43-57; col. 6, I. 16 to col. 9, I. 17; col. 9, I. 46 to col. 11, I. 42; col. 12, I. 16 to col. 14, I. 14; <u>Smith</u>, Fig. 2-5; col. 1, II. 9-22; col. 2, I. 40 to col. 3, I. 8; col. 3, II. 22-27; col. 3, II. 53-59; col. 4, II. 5-34; col. 6, II. 63-62; <u>Ristelhueber</u>, pages 1-3; and <u>Shinohara</u>, col. 1, II. 48-60; col. 3, I. 56 to col. 4, I. 49).

32. As per claim 357, <u>Hashimoto</u>, <u>Smith</u>, <u>Ristelhueber</u> and <u>Shinohara</u> teach all the of limitations claim 239 as discussed above, where <u>Hashimoto</u>, <u>Smith</u>, <u>Ristelhueber</u> and <u>Shinohara</u> further teach the ADGPD comprising wherein the processor is configured to cause, after the at least one parameter has been sent to the multipurpose interface, file allocation table information to be sent to the multipurpose interface, wherein the processor is configured to cause a virtual boot sequence to be sent to the multipurpose interface which includes at least information that is representative of a number of

sectors of a storage disk, and wherein the file allocation table information includes at least a start location of a file allocation table (<u>Hashimoto</u>, Fig. 1A-1B; Fig. 8; Fig. 11-12; Fig. 14-15; col. 1, II. 27-57; col. 3, I. 43 to col. 4, I. 67; col. 5, II. 43-57; col. 6, I. 16 to col. 9, I. 17; col. 9, I. 46 to col. 11, I. 42; col. 12, I. 16 to col. 14, I. 14; <u>Smith</u>, Fig. 2-5; col. 1, II. 9-22; col. 2, I. 40 to col. 3, I. 8; col. 3, II. 22-27; col. 3, II. 53-59; col. 4, II. 5-34; col. 6, II. 63-62; <u>Ristelhueber</u>, pages 1-3; and <u>Shinohara</u>, col. 1, II. 48-60; col. 3, I. 56 to col. 4, I. 49), wherein the transferring of the parameter, the file allocation table information and the virtual boot sequence corresponds to the plug-and-play ADGPD having the memory card emulating as the hard disk drive for data transferring after the plug-and-play ADGPD is connected to the PC.

33. As per claim 358, <u>Hashimoto</u>, <u>Smith</u>, <u>Ristelhueber</u> and <u>Shinohara</u> teach all the of limitations claim 357 as discussed above, where <u>Hashimoto</u>, <u>Smith</u>, <u>Ristelhueber</u> and <u>Shinohara</u> further teach the ADGPD further comprising the processor configured to implement a process to acquire digital data from at least one digital source (<u>Hashimoto</u>, Fig. 1A-1B; Fig. 8; Fig. 11-12; Fig. 14-15; col. 1, II. 27-57; col. 3, I. 43 to col. 4, I. 67; col. 5, II. 43-57; col. 6, I. 16 to col. 9, I. 17; col. 9, I. 46 to col. 11, I. 42; col. 12, I. 16 to col. 14, I. 14; <u>Smith</u>, Fig. 2-5; col. 1, II. 9-22; col. 2, I. 40 to col. 3, I. 8; col. 3, II. 22-27; col. 3, II. 53-59; col. 4, II. 5-34; col. 6, II. 63-62; <u>Ristelhueber</u>, pages 1-3; and <u>Shinohara</u>, col. 1, II. 48-60; col. 3, I. 56 to col. 4, I. 49), as the resulting combination of the references does teach/suggest the heart/core of applicant's invention, it would have been obvious for the

resulting combination of the references to further teach acquiring the digital data from the digital source (e.g. digital data from memory card or I/O card).

34. As per claim 359, <u>Hashimoto</u>, <u>Smith</u>, <u>Ristelhueber</u> and <u>Shinohara</u> teach all the of limitations claim 239 as discussed above, where <u>Hashimoto</u>, <u>Smith</u>, <u>Ristelhueber</u> and <u>Shinohara</u> further teach the ADGPD comprising wherein the processor comprises a single digital signal processor (<u>Hashimoto</u>, Fig. 1A-1B; Fig. 8; Fig. 11-12; Fig. 14-15; col. 1, II. 27-57; col. 3, I. 43 to col. 4, I. 67; col. 5, II. 43-57; col. 6, I. 16 to col. 9, I. 17; col. 9, I. 46 to col. 11, I. 42; col. 12, I. 16 to col. 14, I. 14; <u>Smith</u>, Fig. 2-5; col. 1, II. 9-22; col. 2, I. 40 to col. 3, I. 8; col. 3, II. 22-27; col. 3, II. 53-59; col. 4, II. 5-34; col. 6, II. 63-62; <u>Ristelhueber</u>, pages 1-3; and <u>Shinohara</u>, col. 1, II. 48-60; col. 3, I. 56 to col. 4, I. 49).

35. As per claim 360, <u>Hashimoto</u>, <u>Smith</u>, <u>Ristelhueber</u> and <u>Shinohara</u> teach all the of limitations claim 239 as discussed above, where <u>Hashimoto</u>, <u>Smith</u>, <u>Ristelhueber</u> and <u>Shinohara</u> further teach the ADGPD comprising wherein the processor is configured to initiate a process by which digitized analog data are directly transferred to an input/output device (e.g. I/O card) (<u>Hashimoto</u>, Fig. 1A-1B; Fig. 8; Fig. 11-12; Fig. 14-15; col. 1, II. 27-57; col. 3, I. 43 to col. 4, I. 67; col. 5, II. 43-57; col. 6, I. 16 to col. 9, I. 17; col. 9, I. 46 to col. 11, I. 42; col. 12, I. 16 to col. 14, I. 14; <u>Smith</u>, Fig. 2-5; col. 1, II. 9-22; col. 2, I. 40 to col. 3, I. 8; col. 3, II. 22-27; col. 3, II. 53-59; col. 4, II. 5-34; col. 6, II. 63-62; <u>Ristelhueber</u>, pages 1-3; and <u>Shinohara</u>, col. 1, II. 48-60; col. 3, I. 56 to col. 4, I. 49).

36. As per claim 361, <u>Hashimoto</u>, <u>Smith</u>, <u>Ristelhueber</u> and <u>Shinohara</u> teach all the of limitations claim 239 as discussed above, where <u>Hashimoto</u>, <u>Smith</u>, <u>Ristelhueber</u> and <u>Shinohara</u> further teach the ADGPD comprising wherein the processor is configured to allow an aspect of operation (e.g. updating control program) of the analog data generating and processing device other than the transfer of at least some of the digitized analog data from the data storage memory to the multi-purpose interface to be controlled by means of an external computer (<u>Hashimoto</u>, Fig. 1A-1B; Fig. 8; Fig. 11-12; Fig. 14-15; col. 1, II. 27-57; col. 3, I. 43 to col. 4, I. 67; col. 5, II. 43-57; col. 6, I. 16 to col. 9, I. 17; col. 9, I. 46 to col. 11, I. 42; col. 12, I. 16 to col. 14, I. 14; <u>Smith</u>, Fig. 2-5; col. 1, II. 9-22; col. 2, I. 40 to col. 3, I. 8; col. 3, II. 22-27; col. 3, II. 53-59; col. 4, II. 5-34; col. 6, II. 63-62; <u>Ristelhueber</u>, pages 1-3; and <u>Shinohara</u>, col. 1, II. 48-60; col. 3, I. 56 to col. 4, I. 49), as the PC directly update the control program in the ADGPD.

37. As per claim 362, <u>Hashimoto</u>, <u>Smith</u>, <u>Ristelhueber</u> and <u>Shinohara</u> teach all the of limitations claim 239 as discussed above, where <u>Hashimoto</u>, <u>Smith</u>, <u>Ristelhueber</u> and <u>Shinohara</u> further teach the ADGPD comprising wherein the analog data generating and processing device comprises at least a portion of a medical device (<u>Hashimoto</u>, Fig. 1A-1B; Fig. 8; Fig. 11-12; Fig. 14-15; col. 1, II. 27-57; col. 3, I. 43 to col. 4, I. 67; col. 5, II. 43-57; col. 6, I. 16 to col. 9, I. 17; col. 9, I. 46 to col. 11, I. 42; col. 12, I. 16 to col. 14, I. 14; <u>Smith</u>, Fig. 2-5; col. 1, II. 9-22; col. 2, I. 40 to col. 3, I. 8; col. 3, II. 22-27; col. 3, II. 53-59; col. 4, II. 5-34; col. 6, II. 63-62; <u>Ristelhueber</u>, pages 1-3; and <u>Shinohara</u>, col. 1, II. 48-60; col. 3, I. 56 to col. 4, I. 49), such as pictures taken for medical use.

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38. As per claim 364, <u>Hashimoto, Smith, Ristelhueber</u> and <u>Shinohara</u> teach all the of limitations claim 239 as discussed above, where <u>Hashimoto, Smith, Ristelhueber</u> and <u>Shinohara</u> further teach the ADGPD comprising wherein the analog data generation and automatic file transfer at least partially overlap in time (<u>Hashimoto</u>, Fig. 1A-1B; Fig. 8; Fig. 11-12; Fig. 14-15; col. 1, II. 27-57; col. 3, I. 43 to col. 4, I. 67; col. 5, II. 43-57; col. 6, I. 16 to col. 9, I. 17; col. 9, I. 46 to col. 11, I. 42; col. 12, I. 16 to col. 14, I. 14; <u>Smith</u>, Fig. 2-5; col. 1, II. 9-22; col. 2, I. 40 to col. 3, I. 8; col. 3, II. 22-27; col. 3, II. 53-59; col. 4, II. 5-34; col. 6, II. 63-62; <u>Ristelhueber</u>, pages 1-3; and <u>Shinohara</u>, col. 1, II. 48-60; col. 3, I. 56 to col. 4, I. 49), as the resulting combination of the references does teach/suggest the heart/core of applicant's invention, it would have been obvious for the resulting combination of the references to further teach after the first analog data is generated and being transferred, the second analog data is being generated (e.g. generating the second analog data while transferring of the first analog data).

39. As per claim 365, <u>Hashimoto</u>, <u>Smith</u>, <u>Ristelhueber</u> and <u>Shinohara</u> teach all the of limitations claim 239 as discussed above, where <u>Hashimoto</u>, <u>Smith</u>, <u>Ristelhueber</u> and <u>Shinohara</u> further teach the ADGPD comprising wherein at least one analog source is coupled to the analog data generating and processing device and is designed for either one-way or two-way communication (<u>Hashimoto</u>, Fig. 1A-1B; Fig. 8; Fig. 11-12; Fig. 14-15; col. 1, II. 27-57; col. 3, I. 43 to col. 4, I. 67; col. 5, II. 43-57; col. 6, I. 16 to col. 9, I. 17; col. 9, I. 46 to col. 11, I. 42; col. 12, I. 16 to col. 14, I. 14; <u>Smith</u>, Fig. 2-5; col. 1, II. 9-22;

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 col. 2, l. 40 to col. 3, l. 8; col. 3, ll. 22-27; col. 3, ll. 53-59; col. 4, ll. 5-34; col. 6, ll. 63-62;

<u>Ristelhueber</u>, pages 1-3; and <u>Shinohara</u>, col. 1, II. 48-60; col. 3, I. 56 to col. 4, I. 49).

40. As per claim 366, <u>Hashimoto, Smith, Ristelhueber</u> and <u>Shinohara</u> teach all the of limitations claim 239 as discussed above, where <u>Hashimoto, Smith, Ristelhueber</u> and <u>Shinohara</u> further teach the ADGPD comprising wherein the analog data generating and processing device is designed so that the at least one aspect of operation is controlled by means of a configuration file which includes specification of a volume of analog data to be acquired by specifying a measurement time (<u>Hashimoto</u>, Fig. 1A-1B; Fig. 8; Fig. 11-12; Fig. 14-15; col. 1, II. 27-57; col. 3, I. 43 to col. 4, I. 67; col. 5, II. 43-57; col. 6, I. 16 to col. 9, I. 17; col. 9, I. 46 to col. 11, I. 42; col. 12, I. 16 to col. 14, I. 14; <u>Smith</u>, Fig. 2-5; col. 6, II. 63-62; <u>Ristelhueber</u>, pages 1-3; and <u>Shinohara</u>, col. 1, II. 48-60; col. 3, I. 56 to col. 4, I. 49) as the resulting combination of the references does teach/suggest the heart/core of applicant's invention, it would have been obvious for the resulting combination of the references to further teach the configuration file.

41. As per claim 367, <u>Hashimoto</u>, <u>Smith</u>, <u>Ristelhueber</u> and <u>Shinohara</u> teach all the of limitations claim 239 as discussed above, where <u>Hashimoto</u>, <u>Smith</u>, <u>Ristelhueber</u> and <u>Shinohara</u> further teach the ADGPD comprising wherein the analog data generating and processing device is designed to be responsive to a test unit ready command (<u>Hashimoto</u>, Fig. 1A-1B; Fig. 8; Fig. 11-12; Fig. 14-15; col. 1, II. 27-57; col. 3, I. 43 to col.

4, I. 67; col. 5, II. 43-57; col. 6, I. 16 to col. 9, I. 17; col. 9, I. 46 to col. 11, I. 42; col. 12, I. 16 to col. 14, I. 14; <u>Smith</u>, Fig. 2-5; col. 1, II. 9-22; col. 2, I. 40 to col. 3, I. 8; col. 3, II. 22-27; col. 3, II. 53-59; col. 4, II. 5-34; col. 6, II. 63-62; <u>Ristelhueber</u>, pages 1-3; and <u>Shinohara</u>, col. 1, II. 48-60; col. 3, I. 56 to col. 4, I. 49).

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42. As per claim 369, Hashimoto, Smith, Ristelhueber and Shinohara teach all the of limitations claim 268 as discussed above, where Hashimoto, Smith, Ristelhueber and Shinohara further teach the ADGPD comprising wherein the input connector comprises a plurality of BNC inputs each coupled to the processor through a respective independently programmable amplifier, a multiplexer, and an analog to digital converter (<u>Hashimoto</u>, Fig. 1A-1B; Fig. 8; Fig. 11-12; Fig. 14-15; col. 1, II. 27-57; col. 3, I. 43 to col. 4, l. 67; col. 5, ll. 43-57; col. 6, l. 16 to col. 9, l. 17; col. 9, l. 46 to col. 11, l. 42; col. 12, l. 16 to col. 14, I. 14; Smith, Fig. 2-5; col. 1, II. 9-22; col. 2, I. 40 to col. 3, I. 8; col. 3, II. 22-27; col. 3, II. 53-59; col. 4, II. 5-34; col. 6, II. 63-62; Ristelhueber, pages 1-3; and Shinohara, col. 1, II. 48-60; col. 3, I. 56 to col. 4, I. 49), as the resulting combination of the references does teach/suggest the heart/core of applicant's invention, it would have been obvious for the resulting combination of the references to further implement the heart/core of applicant's invention in an alternative embodiment on a device having the plurality of BNC inputs each coupled to the processor through the respective independently programmable amplifier, the multiplexer, and the analog to digital converter.

43. As per claims 370-376, as claims 370-376 are claiming the same invention as claims 239, 333-339, 341-344, 346-362, 364-367 and 369, the examiner will reject claims 370-376 base on the same rational as the rejection for claims 239, 333-339, 341-344, 346-362, 364-367 and 369.

44. Claims 340 and 368 are rejected under 35 U.S.C. 103(a) as being unpatentable over <u>Hashimoto et al.</u> (US Patent 6,111,604) in view of <u>Hashimoto et al.</u> (US Patent 6,111,604) in view of <u>Smith et al.</u> (US Patent 5,634,075), <u>Ristelhueber : "Plug and play is almost here"</u> and <u>Shinohara</u> (US Patent 5,742,934) as applied to claim 239 above, and further in view of <u>Endo et</u> <u>al.</u> (US Patent 4,652,928).

<u>Hashimoto</u>, <u>Smith</u>, <u>Ristelhueber</u> and <u>Shinohara</u> teach all the limitations of claim 239 as discussed above, wherein <u>Hashimoto</u> further teaches the ADGPD comprising wherein the analog data generating and processing device configured to allow at least one analog source (<u>Hashimoto</u>, Fig. 8, ref. 1, 6, 9) to be attached thereto (<u>Hashimoto</u>, Fig. 8).

Hashimoto, Smith, Ristelhueber and Shinohara do not expressly teach the ADGPD comprising:

configured to allow at least one analog source to be detached therefrom;

the analog data generating and processing device is designed so that a user can attach at least one analog source thereto or detach the at least one analog source therefrom;

the respective independent analog acquisition channels are coupled to an input connector for detachably connecting to a plurality of analog sources.

Endo teaches the ADGPD (e.g. digital camera) comprising:

configured to allow at least one analog source to be detached therefrom (col. 1, ll. 18-25 and col. 13, ll. 57-58), by combining the coupling and de-coupling of the CCD with <u>Hashimoto</u>, <u>Smith</u>, <u>Ristelhueber</u> and <u>Shinohara</u>'s sensor coupled to the analog data generating and processing device, the resulting combination of the references further teaches the above claimed feature;

the analog data generating and processing device is designed so that a user can attach at least one analog source thereto or detach the at least one analog source therefrom (col. 1, II. 18-25 and col. 13, II. 57-58), by combining the coupling and de-coupling of the CCD with <u>Hashimoto, Smith, Ristelhueber</u> and <u>Shinohara</u>'s sensor coupled to the analog data generating and processing device, the resulting combination of the references further teaches the above claimed feature; and

the respective independent analog acquisition channels are coupled to an input connector for detachably connecting to a plurality of analog sources (col. 1, II. 18-25 and col. 13, II. 57-58), by combining the coupling and de-coupling of the CCD with <u>Hashimoto</u>, <u>Smith</u>, <u>Ristelhueber</u> and <u>Shinohara</u>'s sensor coupled to the analog data generating and processing device, the resulting combination of the references further teaches the above claimed feature.

It would have been obvious for one of ordinary skill in this art, at the time of invention was made to include <u>Endo</u>'s interchangeable sensor into <u>Hashimoto</u>, <u>Smith</u>, <u>Ristelhueber</u> and <u>Shinohara</u>'s sensor coupled to the processor for the benefit of adaptively increase the resolution of the camera to obtaining a better quality image (<u>Endo</u>, col. 1, II. 18-20) to obtain the invention as specified in claims 340 and 368.

45. Claim 363 is rejected under 35 U.S.C. 103(a) as being unpatentable over <u>Hashimoto et</u> <u>al.</u> (US Patent 6,111,604) in view of <u>Smith et al.</u> (US Patent 5,634,075), <u>Ristelhueber : "Plug</u> <u>and play is almost here"</u> and <u>Shinohara</u> (US Patent 5,742,934) as applied to claim 329 above, and further in view of <u>Roberts et al.</u> (US Patent 5,576,757).

Hashimoto, Smith, Ristelhueber and Shinohara teach all the limitations of claim 329 as discussed above, wherein Hashimoto further teaches the ADGPD comprising wherein the digitized analog data is processed by the processor (Hashimoto, Fig. 1A-1B; Fig. 8; Fig. 11-12; Fig. 14-15; col. 1, II. 27-57; col. 3, I. 43 to col. 4, I. 67; col. 5, II. 43-57; col. 6, I. 16 to col. 9, I. 17; col. 9, I. 46 to col. 11, I. 42; col. 12, I. 16 to col. 14, I. 14).

<u>Hashimoto</u>, <u>Smith</u>, <u>Ristelhueber</u> and <u>Shinohara</u> do not expressly teach the ADGPD comprising performing a fast Fourier transform.

<u>Roberts</u> teaches a system and a method comprising an electronic still camera processing data by being subject to a fast Fourier transform (Abstract and col. 9, I. 60 to col. 10, I. 7).

It would have been obvious for one of ordinary skill in this art, at the time of invention was made to include <u>Roberts</u>'s fast Fourier transform into <u>Hashimoto</u>, <u>Smith</u>, <u>Ristelhueber</u> and <u>Shinohara</u>'s ADGPD for the benefit of having an easier computation for image processing while providing a reasonable visual fidelity (<u>Roberts</u>, col. 10, II. 1-3) to obtain the invention as specified in claim 363.

III. CLOSING COMMENTS

<u>Conclusion</u>

a. STATUS OF CLAIMS IN THE APPLICATION

The following is a summary of the treatment and status of all claims in the application as recommended by **M.P.E.P. 707.07(i)**:

a(1) CLAIMS REJECTED IN THE APPLICATION

Per the instant office action, claims 239 and 333-376 have received a first action on the merits and is subject of a first action non-final.

b. DIRECTION OF FUTURE CORRESPONDENCES

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chun-Kuan (Mike) Lee whose telephone number is (571) 272-0671. The examiner can normally be reached on 8AM to 5PM.

IMPORTANT NOTE

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Alford Kindred can be reached on (571) 272-4037. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Chun-Kuan Lee/ Primary Examiner Art Unit 2181 July 18, 2011

112384

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of: Michael Tasler

Application No.: 11/467,092

Filed: August 24, 2006

Confirmation No.: 3038

Examiner: C. K. Lee

Art Unit: 2181

For: ANALOG DATA GENERATING AND PROCESSING DEVICE HAVING A MULTI-USE AUTOMATIC PROCESSOR (as amended)

AMENDMENT

MS Amendment Commissioner for Patents P.O. Box 1450 Alexandria, VA 22313-1450

Dear Sir:

In response to the Office Action mailed November 10, 2010, please amend the application

as follows:

Claims:

1-238. (cancelled).

239. (currently amended) An analog data generating and processing device (ADGPD), comprising:

an input/output (i/o) port;

a program memory;

a data storage memory;

a processor operatively interfaced with the i/o port, the program memory and the data storage memory;

wherein the processor is adapted to implement a data generation process by which analog data is acquired from each respective analog acquisition channel of a plurality of independent analog acquisition channels, the analog data <u>from each respective channel is</u> <u>digitized, coupled into the processor, and</u> is processed <u>by the processor and digitized</u>, and the processed and digitized analog data is stored in the data storage memory as at least one file of digitized analog data;

wherein the processor also is adapted to be involved in an automatic recognition process <u>of a host computer</u> in which, when the i/o port is operatively interfaced with a multipurpose interface of <u>athe host</u> computer, the processor executes at least one instruction set stored in the program memory and thereby causes at least one parameter identifying the analog data generating and processing device, independent of analog data source, as a digital storage device instead of as an analog data generating and processing device to be automatically sent through the i/o port and to the multi-purpose interface of the computer (a) without requiring any end user to

load any software onto the computer at any time and (b) without requiring any end user to interact with the computer to set up a file system in the ADGPD at any time;

wherein the at least one parameter provides information to the computer about file transfer characteristics of the ADGPD; and

wherein the processor is further adapted to be involved in an automatic file transfer process in which, when the i/o port is operatively interfaced with the multi-purpose interface of the computer, and after the at least one parameter has been sent from the i/o port to the multipurpose interface of the computer, the processor executes at least one other instruction set stored in the program memory to thereby cause the at least one file of digitized analog data acquired from at least one of the plurality of analog acquisition channels to be transferred to the computer using a device driver for the digital storage device while causing the analog data generating and processing device to appear to the computer as if it were a<u>the</u> digital storage device without requiring any user-loaded file transfer enabling software to be loaded on or installed in the computer at any time;

240. – 332. (cancelled).

333. (previously presented) The analog data generating and processing device of claim 239 wherein the processor is configured to transmit to the computer active commands through the multi-purpose interface to access a system bus of the computer to enable communication directly with other devices of the computer while bypassing the computer processor.

334. (currently amended) The analog data generating and processing device of claim 239 wherein the at least one parameter identifies the analog data generating and processing device as a hard disk drive and wherein data transfer between the analog data generating and processing device and the host computer is enabled by a hard disk driver program which is matched to the

host computer and part of a manufacturer installed BIOS of the host computer.

335. (previously presented) The analog data generating and processing device of claim 239 further comprising at least one additional analog data generating and processing device coupled to the computer in parallel and each analog data generating and processing device attached to a difference analog data source.

336. (previously presented) The analog data generating and processing device of claim 239 wherein processor is configured to format the digitized analog data into blocks of data with block sizes suitable for a hard disk of the computer.

337. (previously presented) The analog data generating and processing device of claim 239 further comprising a data buffer coupled to the processor to permit independence of time of data acquisition and data transfer to the host computer.

338. (previously presented) The analog data generating and processing device of claim 239 wherein each of the plurality of analog acquisition channels are independently programmable and further comprise a plurality of corresponding sample and hold amplifiers for simultaneous sampling on the plurality of analog acquisition channels to permit simultaneous analog data acquisition from a plurality of respective analog data sources.

339. (previously presented) The analog data generating and processing device of claim 333 wherein the active commands initiate active access to write data directly to a hard drive in the host computer independent of the host computer central processor.

340. (previously presented) The analog data generating and processing device of claim 239 is configured to allow at least one analog source to be attached thereto and detached therefrom.

341. (previously presented) The analog data generating and processing device of

claim 239, wherein the analog data generating and processing device is attached directly to at least one analog source.

342. (previously presented) The analog data generating and processing device of claim 239, wherein the analog data generating and processing device is a stand alone device.

343. (previously presented) The analog data generating and processing device of claim 239, wherein the input/output port further comprises a SCSI interface circuit.

344. (previously presented) The analog data generating and processing device of claim 335, wherein as least some of the analog data sources are analog data sources of different types.

345. (currently amended) The analog data generating and processing device of claim 239, wherein the analog data generating and processing device is designed so that a user can attach at least one analog source thereto or detach the at least one analog source therefrom processor interprets a read command from the host computer as a data transfer command to initiate transfer of digitized analog data from the analog acquisition channels to the host computer.

346. (previously presented) The analog data generating and processing device of claim 239, wherein the analog data generating and processing device is adapted to be interfaced with the multi-purpose interface of the computer by means of a cable.

347. (previously presented) The analog data generating and processing device of claim 239, wherein at least one of the analog sources is a sensor that is operatively interfaced with the analog data generating and processing device and that is designed to generate the analog data.

348. (previously presented) The analog data generating and processing device of claim 239 wherein the processor is configured to transmit to the computer active commands

through the multipurpose interface to access a system bus of the computer to enable communication directly with other devices of the computer while bypassing the computer processor without requiring the user to load enabling software.

349. (previously presented) The analog data generating and processing device of claim 239, wherein the plurality of analog acquisition channels are independently programmable.

350. (previously presented) The analog data generating and processing device of claim 239, wherein at least one analog source is designed to receive data from a host device.

351. (previously presented) The analog data generating and processing device of claim 239 wherein at least one analog source comprises a multimeter that is operatively interfaced with the analog data generating and processing device and that is designed to generate the analog data.

352. (previously presented) The analog data generating and processing device of claim 239, wherein the at least one parameter is consistent with the analog data generating and processing device being responsive to a SCSI inquiry command.

353. (previously presented) The analog data generating and processing device of claim 239, wherein the at least one parameter identifies the analog data generating and processing device as a digital mass storage device.

354. (previously presented) The analog data generating and processing device of claim 239, wherein the processor is configured to, when the processor is operatively interfaced with the multi-purpose interface of the computer and after the at least one parameter has been sent to the multi-purpose interface of the computer, execute at least one set of computer code stored in program memory and thereby cause analog data generating and processing device file system information to be automatically sent to the multipurpose

interface without requiring any end user to interact with the computer to set up a file system in the analog data generating and processing device at any time.

355. (previously presented) The analog data generating and processing device of claim 354, wherein the analog data generating and processing device file system information comprises at least one indication of a file system type that is used to store the at least one file of digitized analog data in the data storage memory.

356. (previously presented) The analog data generating and processing device of claim 239, wherein the at least one parameter is consistent with the analog data generating and processing device being a digital mass storage device other than a magnetic floppy disk drive.

357. (previously presented) The analog data generating and processing device of claim 239,

wherein the processor is configured to cause, after the at least one parameter has been sent to the multipurpose interface, file allocation table information to be sent to the multipurpose interface,

wherein the processor is configured to cause a virtual boot sequence to be sent to the multipurpose interface which includes at least information that is representative of a number of sectors of a storage disk, and

wherein the file allocation table information includes at least a start location of a file allocation table.

358. (previously presented) The analog data generating and processing device of claim 357, further comprising the processor configured to implement a process to acquire digital data from at least one digital source.

359. (previously presented) The analog data generating and processing device of

claim 239, wherein the processor comprises a single digital signal processor.

360. (previously presented) The analog data generating and processing device of claim 239, wherein the processor is configured to initiate a process by which digitized analog data are directly transferred to an input/output device.

361. (previously presented) The analog data generating and processing device of claim 239, wherein the processor is configured to allow an aspect of operation of the analog data generating and processing device other than the transfer of at least some of the digitized analog data from the data storage memory to the multi-purpose interface to be controlled by means of an external computer.

362. (previously presented) The analog data generating and processing device of claim 239, wherein the analog data generating and processing device comprises at least a portion of a medical device.

363. (previously presented) The analog data generating and processing device of claim 239, wherein the digitized analog data is processed by the processor performing a fast Fourier transform.

364. (previously presented) The analog data generating and processing device of claim 239, wherein the analog data generation and automatic file transfer at least partially overlap in time.

365. (previously presented) The analog data generating and processing device of claim 239 wherein at least one analog source is coupled to the analog data generating and processing device and is designed for either one-way or two-way communication.

366. (currently amended) The analog data generating and processing device of claim 239, wherein the analog data generating and processing device is designed so that the at least one aspect of operation is controlled by means of a configuration file <u>which</u>

includes specification of a volume of analog data to be acquired by specifying a measurement time.

367. (previously presented) The analog data generating and processing device of claim 239, wherein the analog data generating and processing device is designed to be responsive to a test unit ready command.

368. (previously presented) The analog data generating and processing device of claim 239 wherein the respective independent analog acquisition channels are coupled to an input connector for detachably connecting to a plurality of analog sources.

369. (previously presented) The analog data generating and processing device of claim 268 wherein the input connector comprises a plurality of BNC inputs each coupled to the processor through a respective independently programmable amplifier, a multiplexer, and an analog to digital converter.

370. (currently amended) An analog data generating and processing device for acquiring analog data and for communicating with a host computer comprising:

a program memory;

a data storage memory;

a digital processor configured to interface to a multi-purpose interface of the host computer, the program memory, and the data storage memory;

an analog to digital converter operatively coupled to the digital processor and configured to acquire analog data from each respective analog acquisition channel of a plurality of analog acquisition channels, the analog to digital converter configured to convert the acquired analog data to digitized acquired analog data and to couple the digitized acquired analog data to <u>from the</u> <u>plurality of analog acquisition channels into</u> the digital processor <u>under control of for processing by</u> the digital processor;

the digital processor configured to automatically generate and transmit to the host computer via the multipurpose interface an identification parameter which identifies the analog data generating and processing device to the host computer as a digital storage device but which is different than an analog data generating and processing device and independent of analog data source, and the processor communicating with the host computer through the multi-purpose interface as if the analog data generating and processing device were the digital storage device including transferring the digitized acquired analog data acquired from at least one of the analog acquisition channels, using a device driver present for a digital storage device in the host computer without requiring the user to load the device driver; and

wherein the digital processor is configured to transmit to the host computer active commands through the multipurpose interface to access a system bus of the host computer to enable communication directly with other devices of the host computer while bypassing the host computer processor without requiring the user to load enabling software.

371. (previously presented) The analog data generating and processing device of claim 370, wherein the plurality of analog acquisition channels are independently programmable and further comprising a plurality of corresponding sample and hold amplifiers configured to simultaneously sample the plurality of analog acquisition channels.

372. (currently amended) An analog data generating and processing device for acquiring analog data and for communicating with a host computer <u>which includes a</u> manufacturer installed BIOS comprising:

a program memory;

a data storage memory;

a digital processor configured to interface to a multi-purpose interface of the host computer, the program memory, and the data storage memory;

an analog to digital converter operatively coupled to the digital processor and configured to simultaneously acquire analog data from each respective analog source of a plurality of analog sources on a respective one of a plurality of independent analog acquisition channels, the analog to digital converter configured to convert the acquired analog data to digitized acquired analog data and to couple the digitized acquired analog data to the digital processor under control of for processing by the digital processor;

the digital processor configured to automatically generate and transmit to the host computer via the multipurpose interface an identification parameter which identifies the analog data generating and processing device to the host computer as a digital mass storage device whichis customary in host computers but which is different than an analog data generating and processing device and independent of the analog sources, and the processor communicating with the host computer through the multi-purpose interface as if the analog data generating and processing device were the digital mass storage device including transferring the digitized analog data acquired from at least one of the analog sources, using a device driver present in the BIOS of the host computer for the digital mass storage device in the host computer without requiring the user to load the device driver.

373. (previously presented) The analog data generating and processing device of claim 372, wherein the digital processor is configured to transmit to the host computer active commands through the multipurpose interface to access a system bus of the host computer to enable communication directly with other devices of the host computer while bypassing the host computer processor without requiring the user to load enabling software.

374. (currently amended) An analog data generating and processing method for acquiring analog data and for communicating with a host computer comprising:

operatively interfacing an analog data device including a digital processor, a program

memory and a data storage memory, to a multi-purpose interface of the host computer;

acquiring analog data on each respective analog acquisition channel of a plurality of independent analog acquisition channels, converting the acquired analog data to digitized acquired analog data, and coupling the digitized acquired analog data to the digital processor under control of for processing by the digital processor;

automatically generating and transmitting to the host computer via the multipurpose interface an identification parameter which identifies the analog data generating and processing device to the host computer as a digital storage device but which is different than an analog data device, and independent of analog data source, and the analog data generating and processing device communicating with the host computer through the multi-purpose interface as if the analog data generating and processing device were the digital storage device including transferring the digitized acquired analog data acquired from at least one of the analog acquisition channels, using a device driver present for a digital storage device in the host computer without requiring the user to load the device driver.

375. (currently amended) The analog data generating and processing method of claim 375<u>374</u>, further comprising transmitting to the host computer, from the analog device, active commands through the multipurpose interface to access a system bus of the host computer to enable communication directly with other devices of the host computer while bypassing the host computer processor without requiring the user to load enabling software.

376. (previously presented) The analog data generating and processing method of claim 374 wherein the plurality of analog acquisition channels are independently programmable and further comprising a plurality of corresponding sample and hold amplifiers configured to simultaneously sample a plurality of the plurality of analog acquisition channels.

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REMARKS

Reconsideration and further examination of the subject patent application in view of the present Amendment and the following Remarks is respectfully requested. Claims 1-238 were previously cancelled, and claims 239 and claims 333-376 are pending. Claims 239 and 375 have been objected to for informalities. Claims 239, 333-339, 341-344, 346-362, 364-367, and 369-376 have been rejected under 35 U.S.C.§103(a) as being unpatentable over Hashimoto (U.S. Pat. No. 6,111,604), Smith (U.S. Pat. No. 5,634,075), Ristelhueber ("Plug and Play is almost here"), and Shinohara (U.S. Pat. No. 5,742,934). Claims 340, 345 and 368 have been rejected under 35 U.S.C. §103(a) as being unpatentable over Hashimoto, Smith, Ristelhueber and Shinohara, and further in view of Endo (U.S. Pat. No. 4,652,928), and Claim 363 have been rejected under 35 U.S.C. §103(a) as being unpatentable over Hashimoto, Smith, Ristelhueber, and Shinohara and further in view of Roberts (U.S. Pat. No. 5,576,757). Claims 239, 334, 345, 366, 370, 372 and 374 have been amended. After careful review of the claims and references, it is believed that the claims are in allowable form and a Notice of Allowance if respectfully requested.

Claim 239 has been objected to for unclear antecedent in the phrase "as if it were a digital storage device..." Claim 239 has been amended to read "...the digital storage device..." as suggested by the Examiner. Claim 375 has been objected to for the phrase "...method of claim 375..." and has been amended to "...method of Claim 374..." as suggested by the Examiner. Applicant submits that these claims are now in allowable form.

Independent claims 239, 370, 372 and 374 have been amended to clarify that data from a plurality of analog acquisition channels is coupled into the processor (see, e.g. Fig.2 and

specification p.16, paragraph 0040) and processed by the processor, and that the automatic recognition process is a process of the host computer recognizing a peripheral. Claims 334 and 372 have been amended to call for a driver in the BIOS used to enable data transfer (see, e.g. specification p.7, paragraph 0017). Claim 345 has been amended to call for the processor to interpret a read command as a data transfer command to initiate transfer from the analog channels to the host (see, e.g. specification p.10, paragraph 0025, lines 8-12). Claim 366 has been amended to call for specification of a volume of data (see, e.g. specification p.10, paragraph 0026, lines 1-5).

At the Examiner's request, a telephone interview was conducted on October 6, 2010 in which the claims in general were discussed. An interview summary by the Examiner has been submitted with the Office Action. Applicant respectfully disagrees with the summary of the interview particularly the characterization of the claims. The summary states that Applicant indicated that the claims can be associated with a digital camera, and that one example of Applicant's invention would be a medical device, and another example is a multimeter. However, Applicant would like to clarify that these are examples of how the invention as set out in most of the claims may be applied. The only claim with a multimeter limitation is Claim 351, the only claim with a medical device limitation is claim 363, and there are no claims having an express camera limitation, although the claims may cover use in a camera. In addition, the summary states that agreement was reached that "the core of Applicant's invention is a device that receives and stores analog data (e.g. acquiring data); the device is then connected to a host computer, wherein the host computer views the connected device as a digital storage device for transferring the acquired data to a host computer." Applicant respectfully disagrees. Applicant did not and does not agree with the above-quoted

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characterization of the claims. It is Applicant's position that the claims as they are set out define the invention, not the Examiner's recharacterization of the claims. Thus, Applicant respectfully requests that each claim of this application be examined as written and as a whole.

It is respectfully submitted that, the claims as presented are distinguishable over any combination of the cited references Hashimoto, Smith, Ristelhueber, Shinohara, Endo and Roberts. As such, it is respectfully submitted that the claims 239 and 333-376 are patentably distinguishable over all prior art of record.

The Office Action rejected claims 239, 333-339, 341-344, 346-362, 364-367 and 369-376 as obvious based on the combination of Hashimoto, Smith, Ristelhueber and Shinohara. The Office Action asserts (Office Action, p. 15) that Hashimoto discloses a processor implemented data generation process by which analog data is acquired from each independent analog acquisition channel and the analog data is processed, digitized and stored. However, the claims as amended call for the acquired analog data from each channel to be coupled into the processor and processed by the processor. Hashimoto discloses only the image data on one channel coupled into the processor and processed by the processor. The audio is coupled to an audio data compression/expansion circuit 3 which processes the data and stores it in a FIFO circuit 13 (See, e.g. Hashimoto, Col. 6, lines 18-39). Thus, Hashimoto does not disclose the claimed analog data from a plurality of independent analog acquisition channels coupled into and processed by the processor.

The Office Action also asserts that Hashimoto teaches an automatic recognition process in which the processor executes at least one instruction set. However, Hashimoto does not describe an automatic recognition process of the host computer as now claimed. Rather,

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Hashimoto describes a camera circuit in which a processor 23 in the camera detects proper connection to a host circuit interface by monitoring the data terminal ready (DTR) signal of the RS-232 connection or another signal of similar function of another user selected communications protocol (Hashimoto, Col. 10, lines 44-65; Fig. 4). When the signal from the communication interface is detected, a communication algorithm is set up in the camera to prepare the camera to transmit or receive information. Then the camera system detects whether a switch on the camera has been set to transmit or to receive to determine whether to transmit image data or receive data (Hashimoto, Col. 15, lines 3-16). Thus, Hashimoto merely describes a process for detection by the camera of an active connection by monitoring for a signal from the interface. This detection process is not the recognition process claimed which is a process in which the host computer recognizes the attached ADGPD and the ADGPD processor automatically sends mis-identifying information to the host computer. Hashimoto merely describes a process of the peripheral which detects a proper connection to an interface, which is the opposite of a process by the host to identify a peripheral. There is no description anywhere in Hashimoto of an automatic recognition process of a host. Further, there is no description anywhere in Hashimoto of any process that sends an identification parameter to the host computer, as claimed.

The Office Action also asserts that the Hashimoto digital camera CPU controls the digital camera to be recognized by the PC where the camera needs to be recognized by the PC so the PC knows how to properly communicate with the camera. However, no such recognition control is disclosed in Hashimoto. Further, at the time of the Hashimoto disclosure, the user would load software and input information into the host computer to identify the camera. There was no requirement for the camera CPU to be involved in a recognition process.

Similarly, none of the other cited references disclose a processor in the peripheral device involved in the claimed automatic recognition process which automatically sends an identification parameter to the host computer. The Office Action concedes that Hashimoto does not teach identification information identifying the ADGPD as a digital storage device being automatically sent as claimed, but asserts that Smith teaches an automatic recognition process wherein at least one parameter signifying ability to communicate in accordance with at least one software driver is automatically sent through the i/o port in figs. 2-5, and Col. 1-4, and Col. 6; and further asserts that by combining Hashimoto's automatic recognition process with Smith's Plug and Play functionality (Plug and Play refers to ISA PnP system bus technology referred to in both the Smith and Ristelhueber references) the combination further teaches the automatic recognition utilizing a ROM BIOS by having the operating system load the device driver after the device is coupled to the PC (Office Action, p. 17). However, not only does Hashimoto not disclose automatic recognition as discussed above, but Smith also fails to disclose automatic recognition and automatically sending identification information. Smith describes Plug and Play systems as requiring the Plug and Play host computer to assign a "handle" (I.D. number) to each peripheral card and then the host computer reads resource data from the peripheral (see, e.g. Col. 4, lines 26-34; Col. 3, lines 41-59). Thus, the host computer in Smith assigns an identifying number rather than the peripheral processor automatically sending identification information. Then the host computer reads resource data from the peripheral (Smith, Col. 4, lines 26-28: "the operating system will isolate each PnP device assign a "handle" (number) to each card, and read the resource data from that card"). There is no description of automatic sending of identification data. The Plug and Play process described in Smith or any other of the references is not concerned with recognizing the device. It is not a

device recognition process, rather it is a host computer resource allocation process concerned with allocation of the resources of the host computer to avoid conflicts between resources within the host. The host computer after supplying an I.D. merely performs a process of reading resource data and then allocating its resources to accommodate all the peripherals attached to it. There is no mention of identification information being read or sent. The cited passages of Smith do not even mention a peripheral processor automatically providing identification information to the host computer. Instead, the host computer initiates a "read" function to obtain resource data from the peripheral.

Smith also does not describe a peripheral having a processor involved in the Plug and Play process. The only Plug and Play peripheral device circuitry in Smith is shown in Figs. 6, 7, and 9 which show a circuit made up of registers, flips flops, etc. to allow the peripheral to configure upon power up to operate in legacy mode or plug or play mode. There is no peripheral processor described involved in automatic recognition of the peripheral by the host.

The Office Action further asserts that the combination of the Plug and Play functionality of Smith with Hashimoto's automatic recognition process results in teaching an automatic recognition process corresponding to configuring a Plug and Play system utilizing the ROM BIOS by having the operating system load the device driver after the peripheral device is coupled to the host PC for installation. However, saying that the ROM BIOS of the computer loads the device driver does not teach or relate in any way to the ADGPD processor automatically sending identifying information. Further, the loading of the device driver occurs after the peripheral device has been assigned resources and activated, and requires that a device driver then be provided. Thus, the Plug and Play functionality of Smith is also contrary to the claim feature calling for not requiring any user-loaded file transfer enabling software to be

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installed in the computer at any time, and this would include any special software driver.

The Office Action also suggests that the combination of Smith's Plug and Play functionality into Hashimoto's "automatic recognition" would be obvious to one of ordinary skill in the art because it would simplify the installation for the user without the need to install software or configure the peripheral devices. However, as we have seen, Smith expressly teaches the contrary, that a device driver must be loaded once the peripherals have been set up and host computer resources assigned (see e.g., Smith, Fig. 2, ref. 126 and Col. 4 lines 32-33).

Further, the Plug and Play functionality of Smith is functionality which is primarily located in the host computer not the peripheral. The Plug and Play compatibility as implemented in the peripheral in Smith is merely a set of logic gates and registers (not a processor) to give the peripheral compatibility with the Plug and Play functionality of the host computer. Plug and Play functionality calls for the host computer to configure its resources according to the needs of all the peripherals attached to it and thus primarily concerns software or firmware supplied functions located in the host computer. Thus, it would not make sense to one skilled in the art to put these Plug and Play functions into the peripheral device which would have no use for them. The peripheral device is only going to connect to a host computer and thus does not need to allocate its resources to handle multiple Plug and Play devices. In addition, as discussed above, neither Hashimoto nor Smith teach automatically sending identification information.

The Office Action concedes that Hashimoto and Smith do not teach indentifying the ADGPD as a digital storage device instead of as an analog data device without the end user loading software at anytime as claimed but asserts that Ristelhueber describes a peripheral device having an automatic recognition process without requiring any end user to load any

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software on the computer at anytime at page 1-3 (Office Action, p. 19). Ristelhueber, however, is a non-technical buyer magazine article which generically describes a coming Plug and Play standard with an enthusiastic description of the future ("In about a year the key standard and specifications will be in place to make PnP a reality", p. 1, paragraph 3). Thus, Ristelhueber is not enabling prior art. Ristelhueber is relied upon for disclosure of Plug and Play functionality. The Office Action appears to rely on vague predictions in Ristelhueber regarding recognition of new hardware, and configuring of hardware to relieve the user of the need to fumble with floppy disks and user manuals to get the device up and running. However, when read in context these phrases are predicting PnP will recognize that a new device is connected. The author is not describing recognizing what peripheral is attached, only whether there is a peripheral attached to the port. Further, there is no enabling disclosure of how such recognition would one day be implemented. The description in Ristelhueber is just an over enthusiastic prediction of the hoped for goals for PnP, which is to detect when a new device is attached (i.e. identifying presence not what it is), configure the host computer resources to accommodate it, and then activate the device. However, Ristelhueber nowhere discusses or even mentions device drivers, or what will happen after a device is configured and activated. As discussed herein, the Smith reference and the PnP Standards Specification make clear that a device driver is still needed after the peripheral has been detected, assigned resources and activated in accordance with Plug and Play.

The Office Action further asserts with regard to Ristelhueber that the combination of references teaches the claimed automatic recognition process corresponds to Plug and Play by the user simply inserting a peripheral into the desktop and having it start running immediately. However, as discussed above, there is no disclosure of this in the cited references. Further,

there is no teaching in Ristelhueber of the processor of the peripheral (i.e. the ADGPD) automatically sending identification information to the computer, or of anything done or not done by a processor of a Plug and Play peripheral device. Ristelhueber merely describes the host computer determining the presence of a peripheral device, identifying the resources needed by the peripheral device and configuring its hardware thereby relieving the user from having to do so. There is no teaching in Ristelhueber to relieve the user from having to load a device driver. There is no mention of a processor on the peripheral, and no mention of the need or lack of need for user loaded software on the host computer. Thus, Ristelhueber does not disclose this claimed feature. Rather, Ristelhueber merely broadly describes future Plug and Play hopes without discussing device driver software for proper functioning of the peripheral after it is activated. As discussed above, the Plug and Play still requires loading a device driver after the peripheral device has been activated using a Plug and Play process. Thus, Ristelhueber does not teach a peripheral device which doesn't require an end user to load software onto the computer at anytime and none of the other cited references teach this feature. Therefore, all pending claims are distinguishable over the cited references on this ground as well.

The Office Action also concedes that Hashimoto, Smith and Ristelhueber do not teach the claimed identifying the analog data generating and processing device as a digital storage device instead of as an analog data generating and processing device without requiring any end user to interact with the computer to set up a file system at any time. However, the Office Action asserts (Office Action, p. 19-20) that Shinohara discloses this feature at Col 1, lines 48-60, and Col 3, lines 3 to Col 4, line 49. Shinohara describes a flash disk drive which couples only to a host computer to allow the host computer to send data for storage and retrieve the data

stored by the host computer. This is entirely different from the claimed analog data generating and processing device which acquires analog data from analog sources through a first port, and provides for transfer of the digitized analog data to a separate host computer through a second port. Therefore, the environment and functionality, and the problems to be resolved are completely different, and it would thus not be obvious to combine the Shinohara flash disk drive features with Hashimoto, and because of these fundamental differences, Shinohara is not compatible with Hashimoto. Moreover, the combination (even if considered somehow together) still would not end up meeting the terms of the claims. Shinohara merely describes how the host computer sends data and sets up the data structure in the flash disk drive but does not teach or even mention that there is no need for user interaction to set up a file system, or that the device is not identified as an analog data generating and processing device and is identified instead as a digital mass storage device. Shinohara is merely a mass storage device acting as a mass storage device. Further, the data structure set up would require software on the host computer to perform these set-up functions. Thus, additional software must be added to the host computer to set up the data structure for the flash drive. Further, since Shinohara is merely a hard disk emulator connected to a computer, it cannot cause an acquired file of digitized analog data acquired from a analog source to be transferred (i.e., there is only digital data stored by the host computer).

Since Hashimoto, Smith, Kerigan, and Ristelhueber do not teach the automatic identification process identifying an analog generating and processing device as a digital storage device or doing so without requiring any end user to interact with the computer to set up a file system in the ADGPD, and Shinohara also does not teach this feature, all pending claims are distinguishable over the cited references.

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Further, none of the references disclose a device which acquires and processes analog data but operates and identifies itself as a digital storage device. Shinohara discloses a mass storage device (i.e. a flash memory) which operates as a mass storage device. This teaching of Shinohara does not suggest to one of ordinary skill in the art the operation and identification of an analog generating and processing device as an entirely different type of device, i.e. a mass storage device, and does not suggest a device which sends an identifying parameter to the host computer identifying the device as a device of dramatically different type than what it actually is. Thus the claims are further distinguishable over the cited references for this reason in addition to the reasons discussed herein above.

The Office Action further asserts that Shinohara teaches a system and a method comprising data transferring using a device driver for the digital storage device while causing the ADGPD to appear to the computer as if it were a digital storage device without requiring any user-loaded file transfer enabling software to be loaded on or installed in the computer at anytime at Col. 1 lines 48-60 and Col. 3, line 33 to Col. 4, line 49 (Office Action, p. 21). The Office Action alleges that by combining the emulation of a mass storage device of Shinohara with the data transferring Plug and Play functionality of the combined other references, the resulting combination would teach this feature.

However, this is not the case because Shinohara merely describes an approach to extending the life of the flash memory in a flash disk drive. Shinohara at the cited Col. 1, line 48-60 merely describes a flash disk memory which can erase and write data in a unit sector of a flash memory to emulate a hard disk, where the host computer erases and writes a sector designated by the host computer so an address conversion table is not needed and also describes a disk operating system. There is no mention of device drivers, no mention of not needing to

load file transfer enabling software. Similarly Col. 3, line 33 to Col. 4, line 49 of Shinohara merely describe details of the flash disk which can cause the flash memory to last for a longer time using an address conversion table. However, nowhere in Shinohara is there any mention of transferring a file of digitized analog data (Shinohara is a disk driver, as such, it cannot acquire and digitize analog data and therefore cannot transfer it), or any data, without requiring any user loaded file transfer enabling software. Rather, the detailed description cited calls for the host computer to perform unique file management functions (Col. 4, lines 34-49) which would require data transfer software in the host computer to set up the disk emulation. Further, there is no teaching or mention of the disclosed disk emulator being able to transfer data without data-transfer software loaded on the host computer. The Shinohara reference is devoid of any such teaching. Thus, Shinohara does not teach the feature of transferring digitized analog data without requiring any user loaded file transfer enabling software.

The Office Action also asserts that combining the flash memory device of Shinohara with the Plug and Play functionality of the other references such as Smith, teaches this feature. However, as discussed above, Plug and Play is concerned with allocation of the resources of the host computer to avoid conflicts between resources within the host computer. In Plug and Play, the host computer reads the resource requirements from each attached peripheral, such resources as i/o addresses, interrupts levels, and DMA channels, (see, Smith, Col. 3, lines 1-4; also see Plug and Play ISA Specification, Version 1.0a, May 5, 1994 ("Plug and Play Specification") p.1, abstract, line 5, and lines 9-11). The computer then assigns to each peripheral device the necessary resources so as to avoid resource conflicts (see Smith, Col. 4, lines 25-32; and Plug and Play Spec. p.1, lines 11-12). Once the host computer has assigned its resources and activated the device, an appropriate device driver must then be loaded to permit

operation. As described in Smith, Col. 4, lines 26-33 in a PnP (Plug and Play) system:

"...the operating system will isolate each PNP device, assign a 'handle' (number) to each card, and read the resource data from that card. Once each card had been isolated, assigned a handle and read, the operating system software will arbitrate system resources for all PNP devices. Conflict-free resources may then be assigned and the devices activated. Finally, appropriate device drivers may be loaded and the system thus configured."

Also see Plug and Play Spec. p.1, Abstract, and Smith, Col. 3, lines 52-59. The Plug and Play process thus does not eliminate the need to supply a driver but rather calls for loading the driver after the system resources are allocated and the devices activated. The Plug and Play standard does not address device drivers other than the fact that one is needed. (Plug and Play Specification p. 1 Abstract: "However, user interface issues for installation of device drivers are not addressed".) Thus, even with Plug and Play, a device specific driver is still needed for each peripheral installed in the Plug and Play computer system in order for the peripheral's processor to execute an instruction to automatically transfer a file of digitized analog data to the computer from the peripheral device. This is clearly demonstrated by the Smith reference and the Plug and Play Specification document. Thus, neither Shinohara nor the Plug and Play functionality disclosed in the other cited references teach data transfer without a user loaded driver.

Moreover, the device described in Shinohara is merely a memory for storage of digital data by a host computer and for retrieval of that data by the host computer, and thus is not suitable for receiving analog data from a source independent of the host computer nor for transferring acquired digitized analog data to a host computer. Further, Shinohara does not teach transferring the acquired analog data while causing the analog data generating and processing device to appear to the computer as a digital storage device, as claimed. The

Shinohara device has one port that merely receives and stores digital data from the computer and allows that same computer to retrieve that stored data through the same port. The claimed invention has two separate ports providing input of analog data on one port and subsequent transfer of digitized analog data to a computer on another port. Thus, the disk memory emulation of Shinohara is dramatically different from the claimed invention and not compatible with or combinable with Hashimoto to obtain the claimed invention.

Stated another way, at most Shinohara merely teaches that a digital memory device having a single read/write port such as a flash memory, may be configured to emulate another digital memory device. This does not teach and is not related to an analog data acquisition device having both an analog input and a host computer interface port which can emulate a hard disk. Thus, the combination of Shinohara with the other references does not teach or suggest the claimed automatic file transfer of acquired digitized analog data without requiring user loaded file transfer enabling software. Indeed, there is nothing to suggest the advantage of not requiring user loaded file transfer enabling software in any device, let alone in an analog data acquisition device.

Accordingly, it is respectfully submitted that all the pending claims are distinguishable over the cited references because none of the references teaches the claimed transfer of a file of acquired digitized analog data by an analog generating and processing device while appearing to be a digital mass storage device without loading file transfer enabling software. That is, even if all the references could somehow be combined (which they cannot, as explained hereinafter), the result would still not meet the combined limitations of the claims.

The Office Action asserts with regard to claim 333, and apparently claims 370 and 375 that Hashimoto, Ristelhueber and Shinohara teach transferring data from the digital camera

directly to the hard disks of the host computer while bypassing the host computer processor. However, all the cited passages of Hashimoto describe a camera system but none even mention direct transfer bypassing the processor. The cited portion (p.1-3) of Ristelhueber discusses future Plug and Play in general regarding peripheral installation but does not address data transfer from peripheral to host at all. The cited portions of Shinohara concern flash memory but do not describe or even mention direct data transfer from a peripheral to the host hard disk bypassing the host's processor, as claimed. Since none of the references describe or in any way concerns this feature, the combination fails to render the claim obvious. Therefore, Claims 333, 370 and 375 are believed to be further distinguishable over the cited references.

Claims 334 and 372 have been amended to call for a driver which is part of the manufacturer installed BIOS to enable data transfer between the device and the host. None of the cited references disclose this feature. Therefore, claims 334 and 372-373 are believed to be further distinguishable over the references for this reason.

In addition to the lack of disclosure of the claimed feature discussed hereinabove, Hashimoto and Smith are incompatible and cannot be properly combined. As previously discussed, Hashimoto detects that it is properly connected to a host computer interface by monitoring for a DTR signal. Until the DTR signal is detected the power to the communication circuitry is turned off or in standby mode (Hashimoto, Col. 12, lines 62 to Col. 13, lines 8). After detecting the proper connection and activating the communication circuitry, Hashimoto checks a switch 110 which is manually set by the camera user, to determine whether it is in the transmit mode or is in a receive mode. (Hashimoto, Fig. 14, Ref. No. 308; Col. 10, lines 51-54 and Col. 11, lines 7-13). Thus, at any point in time, the Hashimoto camera is enabled to only transmit, or only receive; it is not enabled to do both. The user must manually switch between

modes. Smith, however, describes a Plug and Play process which requires the host computer to read resource data from the PnP peripheral device (see e.g. Smith, Col. 3, lines 41-43; Col. 4, lines 25-28). This read function requires the peripheral to receive a read request, which would include an address, and then requires the peripheral to transmit the resource data to the host computer. Thus, Smith's Plug and Play (and PnP in general) cannot be added to Hashimoto because the Hashimoto camera cannot both transmit and receive data at any one moment. If the mode switch in the Hashimoto camera is in the transmit position, then the camera would not be able to receive the read request and address, and if the mode switch is in the receive position, the camera would not be able to transmit the resource data. Thus, Hashimoto and Smith, are incompatible and cannot properly be combined. This is also true of Plug and Play in general.

The combination of Hashimoto and Shinohara is also improper. Hashimoto describes an electronic camera while Shinohara describes a flash disk drive. The Office Action combines Shinohara with Hashimoto by converting the Hashimoto camera to a disk drive emulator, thereby dramatically changing the fundamental structure, operation, and purpose of Hashimoto. Shinohara is merely a digital memory device having a single port to receive digital data from a computer for storage and to allow the same computer to retrieve that data through the same port. In other words, Shinohara merely teaches that a single port digital memory device can be configured to emulate a hard disk. This does not teach or suggest an analog data acquisition device having both an analog input and a separate host computer interface port emulating a hard disk. It is a huge inventive step to go from a digital mass storage device emulating a digital mass storage device to an analog device emulating a digital mass storage device. Thus, the combination requires improper hindsight based on the teachings of the instant application and therefore, Hashimoto and Shinohara cannot be properly combined.

In addition, as discussed above, Hashimoto operates in a transmit only mode or a receive only mode selected by the user with a mode selection switch. However, to function properly the Shinohara flash disk requires the host computer to read data from it. This is incompatible with Hashimoto one way communication, because the read function requires that the flash memory receive a read request with the address or sectors of the data requested, followed by an immediate transmission of the data. Hashimoto's one way communication would prevent this two way exchange. Thus, Shinohara is incompatible and not properly combinable with Hashimoto for this reason as well.

In view of the foregoing, applicant submits that claims 239, and 333-376 are not obvious over Hashimoto in view of the combined teachings of Smith, Ristelhueber, Roberts, Endo, and Shinohara. Accordingly, applicant respectfully submit that the instant application is in condition for allowance, and a Notice of Allowance is respectfully requested. Should the Examiner be of the opinion that a telephone conference would expedite prosecution of the subject application, the Primary Examiner is respectfully requested to call the undersigned at the below-listed number.

The Commissioner is hereby authorized to charge any additional fee which may be required for this application under 37 C.F.R. §§ 1.16-1.18, including but not limited to the extension of time fee, RCE fee, petition fee, extra claims fee, the issue fee, or credit any overpayment, to Deposit Account No. 23-0920. Should no proper amount be enclosed herewith, as by a check being in the wrong amount, unsigned, post-dated, otherwise improper or informal, or even entirely missing, the Commissioner is authorized to charge the unpaid amount to Deposit Account No. 23-0920.

Respectfully submitted,

HUSCH BLACKWELL LLP

<u>Le</u> By: James A. Scheer Registration No. 29,434

Dated: May 10, 2011

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		Application No.	Applicant(s)
Office Action Summary		11/467,092	TASLER, MICHAEL
		Examiner	Art Unit
		Chun-Kuan Lee	2181
The MAILING DATE of this communication appears on the cover sheet with the correspondence address Period for Reply			
 A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>3</u> MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION. Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication. If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication. Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b). 			
Status			
1)🖂	Responsive to communication(s) filed on 24 Sector	eptember 2010.	
2a)	This action is FINAL . 2b) This	action is non-final.	
3)	Since this application is in condition for allowar	nce except for formal matters, pro	osecution as to the merits is
closed in accordance with the practice under Ex parte Quayle, 1935 C.D. 11, 453 O.G. 213.			
Disposition of Claims			
4)⊠ Claim(s) <u>239 and 333-374</u> is/are pending in the application.			
4a) Of the above claim(s) is/are withdrawn from consideration.			
5) Claim(s) is/are allowed.			
6)⊠ Claim(s) <u>239 and 333-374</u> is/are rejected.			
7) Claim(s) is/are objected to.			
8) Claim(s) are subject to restriction and/or election requirement.			
Application Papers			
9) The specification is objected to by the Examiner.			
10)⊠ The drawing(s) filed on <u>8/24/2006 & 8/31/2009</u> is/are: a)⊠ accepted or b)⊡ objected to by the Examiner.			
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).			
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).			
11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.			
Priority under 35 U.S.C. § 119			
12)⊠ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f). a)⊠ All b)⊡ Some * c)⊡ None of:			
1. Certified copies of the priority documents have been received.			
2. ☐ Certified copies of the priority documents have been received in Application No			
3. Copies of the certified copies of the priority documents have been received in Application No			
application from the International Bureau (PCT Rule 17.2(a)).			
* 9	* See the attached detailed Office action for a list of the certified copies not received.		
Attachment(s)			
Attachment(s) 1) Notice of References Cited (PTO-892) 4) Interview Summary (PTO-413)			
	e of Draftsperson's Patent Drawing Review (PTO-948)	Paper No(s)/Mail Da	ate. <u>20101102</u> .
3) Infor	mation Disclosure Statement(s) (PTO/SB/08)	5) Notice of Informal F	Patent Application
Paper No(s)/Mail Date 6) Other:			
PTOL-326 (F		tion Summary Pa	art of Paper No./Mail Date 20101102

Continuation Sheet (PTOL-326)

Application No. 11467092

DETAILED ACTION

CONTINUED EXAMINATION UNDER 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 09/24/2010 has been entered.

RESPONSE TO ARGUMENTS

2. Applicant's arguments filed 09/24/2010 have been fully considered but they are not persuasive. Currently claims 1-238 and 240-332 are cancelled, and claims 239 and 333-374 are pending for examination.

3. In response to applicant's plurality of arguments with regard to the independent claims 239, 370, 372 and 374 rejected under 35 U.S.C. 103(a), wherein the plurality of arguments corresponds to that the resulting combination of the references does not teach/suggest applicant's invention because of the following:

- the combination of the references does not teach/suggest the claimed feature corresponding to "... analog data is acquired on a plurality of respective independent analog acquisition channels ... the identifying parameter identifies the analog data

generating and processing device as a digital storage device instead of as an the analog data generating and processing device ..."

- <u>Shinohara</u> does not teach device drivers, do not need to load file transfer enabling software, or transferring a file of digitized analog data without requiring any user loaded file transfer enabling software; instead <u>Shinohara</u> does teach the host computer to perform unique file management functions (Col. 4, lines 34-49) which would require data transfer software in the host computer to set up the disk emulation;

- Plug and Play is concerned only with allocation of the resources of the host computer to avoid conflicts between resources within the host computer; thus, the Plug and Play process does not need to recognize the peripheral, it only needs to determine what resources of the host computer the peripheral needs;

- <u>Plug and Play Spec.</u> p. 1, Abstract, and <u>Smith</u>, Col. 3, lines 52-59 does not eliminate the need to supply a driver but rather calls for loading the driver after the system resources are allocated and the devices activated; and the Plug and Play standard does not address device drivers other than the fact that one is needed. (Plug and Play Specification p. 1 Abstract: "However, user interface issues for installation of device drivers are not addressed".);

- <u>Shinohara</u> is merely a memory for storage of digital data by a host computer and for retrieval of that data by the host computer, and thus is not suitable for neither receiving analog data from a source independent of the host computer nor for transferring acquired digitized analog data to a host computer;

- <u>Shinohara</u> does not teach transferring the acquired analog data while causing the analog data generating and processing device to appear to the computer as a digital storage device;

- <u>Shinohara</u>'s device has one port that merely receives and stores digital data from the computer and allows that same computer to retrieve that stored data through the same port (i.e. not two separate ports providing input of analog data on one port and subsequent transfer of digitized analog data to a computer on another port);

- there is nothing to suggest the advantage of not requiring user loaded file transfer enabling software in any device, let alone in an analog data acquisition device;

- <u>Hashimoto</u> does not describe an automatic recognition process or the processor automatically sending an identification parameter;

- there is no description anywhere in <u>Hashimoto</u> of any process that sends an identification parameter to the host computer, automatically or otherwise;

- none of the other references disclose a processor in the peripheral device in an automatic recognition process which automatically sends an identification parameter to the host computer;

 not only does <u>Hashimoto</u> not disclose automatic recognition as discussed above, but <u>Smith</u> also fails to disclose automatic recognition and automatically sending identification information;

- the Plug and Play process described in <u>Smith</u> or any other of the references is not concerned with recognizing the device, as it is not a device recognition process, rather it is a host computer resource allocation process;

- <u>Smith</u> also does not describe a peripheral having a processor involved in the Plug and Play process;

- the ROM BIOS of the computer loads the device driver does not teach or relate in any way to the ADGPD processor automatically sending identifying information, as the loading of the device driver occurs after the peripheral device has been assigned resources and activated, and requires that a device driver then be provided;

- the Plug and Play functionality of <u>Smith</u> is functionality which is primarily located in the host computer not the peripheral;

- <u>Kerigan</u>, <u>Ristelhueber</u> or <u>Shinohara</u> does not disclose a processor of the peripheral device in an automatic recognition process which automatically sends an identification parameter to the host computer, as <u>Kerigan</u> merely describes a digital display interface with no disclosure of a peripheral processor, or of the processor automatically sending identification information in an automatic identification process; <u>Ristelhueber</u> provides a very generic description of Plug and Play, but does not disclose a processor of a peripheral in an automatic recognition process or the processor automatically sending identification information; and <u>Shinohara</u> merely describes a flash disk drive and thus also does not mention a processor of the peripheral device involved in an automatic recognition process or the processor automatically sending an identification process or the processor automatically sending an identification process or the processor automatic recognition process or the peripheral device involved in an automatic recognition process or automatically sending an identification process or the processor automatically sending an identification process or the processor automatically sending an identification process or the processor automatically sending an

- <u>Ristelhueber</u> does not describe a peripheral device having an automatic recognition process without requiring any end user to load any software on the computer at anytime;

- there is no teaching of the processor of the peripheral (i.e. the ADGPD) automatically sending identification information to the computer, or of anything done or not done by a processor of a Plug and Play peripheral device; it merely describes the host computer determining the presence of a peripheral device, identifying the resources needed by the peripheral device and configuring its hardware thereby relieving the user from having to do so;

- <u>Ristelhueber</u> to relieve the user from having to load a device driver, and there is no mention of a processor on the peripheral, and no mention of the need or lack of need for user loaded software on the host computer;

- all the claims similarly call for the processor in an automatic recognition process to automatically send identification information which identifies the analog data generating and processing device as a digital storage device instead of as an analog data generating and processing device without requiring any end user to interact with the computer to set up a file system at any time;

- the environment and functionality of <u>Shinohara</u>, and the problems to be resolved are completely different, and it would thus not be obvious to combine the <u>Shinohara</u> flash disk drive features with the other references;

- <u>Shinohara</u> does not teach that there is no need for user interaction to set up a file system or that an analog data generating and processing device is identified instead as a digital mass storage device; <u>Shinohara</u> is merely a mass storage device being a mass storage device; and further, the data structure set up would require software on the host computer to perform these set-up functions;

- none of the references disclose a device which acquires and processes analog data but operates and identifies itself as a digital storage device;

- <u>Hashimoto</u> and <u>Smith</u> are incompatible and cannot be properly combined, because <u>Hashimoto</u> describes checks a switch 110 which is manually set by the camera user, to determine whether it is in the transmit mode or is in a receive mode and <u>Smith</u> describes a Plug and Play process which requires the host computer to read and write data between the PnP peripheral device and the host computer;

- combination of Hashimoto and Shinohara is also improper because <u>Hashimoto</u> describes an electronic camera while <u>Shinohara</u> describes a flash disk drive; and <u>Hashimoto</u> operates in a transmit only mode or a receive only mode selected by the user with a mode selection switch and <u>Shinohara</u>'s flash disk requires the host computer to read and write (i.e. <u>Hashimoto</u>'s one way communication would prevent two way exchange);

- the combination requires hindsight assumptions about the disclosures in the references; and

- there is no disclosure by <u>Hashimoto</u> of automatic file transfer of digitized acquired analog data to a host computer without requiring user-loaded file transfer software; applicant's arguments have fully been considered, but are not found to be persuasive.

The examiner respectfully disagrees, and please note that applicant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references.

See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986); and also please note that it must be recognized that any judgment on obviousness is in a sense necessarily a reconstruction based upon hindsight reasoning. But so long as it takes into account only knowledge which was within the level of ordinary skill at the time the claimed invention was made, and does not include knowledge gleaned only from the applicant's disclosure, such a reconstruction is proper. See *In re McLaughlin*, 443 F.2d 1392, 170 USPQ 209 (CCPA 1971).

To further clarify the examiner's position, first of all, based on the interview dated 10/06/2010, the core of applicant's invention is "... a device that receives and stores analog data (e.g. acquiring data); the device is then connected to a host computer, wherein the host computer views the connected device as a digital storage device for transferring the acquired data to the host computer ...," wherein the examiner relied on the references as following for the teaching of applicant's invention:

<u>Hashimoto</u> teaches a device (e.g. digital camera peripheral device) that receives and stores analog data (e.g. acquiring data); the device is then connected to a host computer for transferring the acquired data to the host computer (Fig. 1A-1B; Fig. 8; Fig. 11-12; Fig. 14-15; col. 1, II. 35-57; col. 3, I. 43 to col. 4, I. 57; col. 5, II. 43-57; col. 6, I. 16 to col. 9, I. 17; col. 9, I. 46 to col. 11, I. 42 and col. 12, I. 16 to col. 14, I. 14), wherein the digital camera acquire image and audio data and store them into the flash memory card, and when the digital camera is connect to the host computer, the image and audio data is then transferred from the flash memory card to the host computer (e.g. the digital

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camera having two separate ports providing input of the analog image and audio data on one port and subsequent transfer of digitized analog data to the computer on another port).

Smith teaches plug and play functionality for a peripheral device connected to a host computer (Fig. 2-5; col. 1, II. 9-22; col. 2, I. 40 to col. 3, I. 59; col. 4, II. 5-34 and col. 6, II. 63-62).

<u>Ristelhueber</u> teaches plug and play functionality without user loading software (e.g. plug and play of a peripheral device by having a user to simply insert a peripheral into a desktop system and have it start running immediately, as the PnP computer will automatically identify any new hardware installed and configure the new hardware, and relieving the end user of any need to fumble with floppy disks and user manuals to get the device up and running; therefore, the peripheral device is connected and operational without requiring any end user to load any software/device driver on the computer at anytime) (pages 1-3).

Shinohara teaches a host computer views the connected device as a digital storage device (e.g. hard disk drive emulation) (col. 1, II. 48-60 and col. 3, I. 33 to col. 4, I. 49), by combining the hard disk drive emulation of the flash memory card into <u>Hashimoto</u>'s digital camera peripheral device's flash memory card storing the image and audio data, the resulting combination of the references further teaches the above feature of applicant's invention; furthermore, <u>Shinohara</u>'s teaching corresponds to the flash memory card and the examiner is combining <u>Shinohara</u>'s teaching into <u>Hashimoto</u>'s flash memory card within the digital camera peripheral device; therefore,

the environment and functionality of <u>Shinohara</u>'s teaching is suitable combined into <u>Hashimoto</u>'s flash memory card; and no where in <u>Shinohara</u> teaches that the user need to load the data transfer software.

Therefore, the resulting combination of the references does teach the core of applicant's invention as following: the digital camera peripheral device having the flash memory card that receives and stores the analog image and audio data; the digital camera peripheral device is then connected to the host computer, wherein the host computer views the connected digital camera peripheral device to be the flash memory card emulating as the hard disk drive for transferring the analog image and audio data from the flash memory card to the host computer (e.g. the digital camera peripheral device acquires the analog image and audio data while causing the digital camera peripheral device appear/be identified to the computer as an emulating hard disk drive/digital storage device).

<u>Hashimoto</u> further does teaches analog data is acquired on a plurality of respective independent analog acquisition channels (e.g. channel for acquiring image data and channel for acquiring audio data); and the combination of the references does teach/suggest "... the identifying parameter identifies the analog data generating and processing device as a digital storage device instead of as an the analog data generating and processing device …" as the combination of the references does teach plug and play of the digital camera peripheral device for hard disk drive emulation by the digital camera peripheral device's flash memory card as discussed in detail above.

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Furthermore, in applicant's arguments, applicant stated that the references disclose the loading the driver for the connected peripheral device and identifying the resources needed by the peripheral device; therefore, in order to load the appropriate device driver (or identify the resources needed), the plug and play process need to recognize the connected peripheral device to be able to pick/select the appropriate device driver, because if the device driver is inappropriate, then operation would not permitted.

And one of the advantage for combing the references with <u>Ristelhueber</u>'s teaching corresponding to the plug and play functionality without user loading software is that a user can simply insert a peripheral into a desktop system and have it start running immediately; and as <u>Ristelhueber</u> relieves the user from having to load a device driver, the user do not need to load software on the host computer (<u>Ristelhueber</u>, pages 1-3).

And the combination of the references does teach/suggest the claimed features corresponding to "an automatic recognition process," "the processor automatically sending an identification parameter," "sends an identification parameter to the host computer," "a processor in the peripheral device in an automatic recognition process which automatically sends an identification parameter to the host computer," "a processor on the peripheral," "the processor in an automatic recognition process to automatically send identification information which identifies the analog data generating and processing device as a digital storage device instead of as an analog data generating and processing device without requiring any end user to interact with the

computer to set up a file system at any time," "do not need for user interaction to set up a file system or that an analog data generating and processing device is identified instead as a digital mass storage device," "automatic file transfer of digitized acquired analog data to a host computer without requiring user-loaded file transfer software," and "peripheral device having the plug and play functionality" because applicant's invention is reflected in the above claimed features, and as discussed in detail above, the combination of the references does teach/suggest applicant's invention; therefore, the combination of the references does teach/suggest the above claimed features.

Additionally, <u>Hashimoto</u> does teach a peripheral having a processor (Fig. 8, ref. 11, 23) involved in the recognition process, and when combining <u>Hashimoto</u>'s teaching with the Plug and Play functionality as taught by <u>Smith</u>, <u>Ristelhueber</u>, and <u>Shinohara</u>, the resulting combination of the references does teach the peripheral having the processor involved in the Plug and Play process; wherein <u>Smith</u>'s requirement that a device driver be provided (loaded) (e.g. ROM BIOS) is consistent with the applicant's loading of the driver (e.g. during the interview on April 2nd 2008, applicant explained "... driver of the claimed invention may be located in the BIOS of the computer ..."; and <u>Hashimoto</u> is compatible with other references because, base on the assumption that applicant's analysis of <u>Hashimoto</u> is correct, <u>Hashimoto</u> is not limited to one way communication, as <u>Hashimoto</u> does have two way exchange via a switch.

I. INTERVIEW SUMMARY

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4. The interview mainly focused on getting a clear understanding of the heart of applicant's invention, and in response to the examiner's inquiry regarding the heart of applicant's invention, applicant explained that the invention is what is reflected in the claim language (e.g. corresponding to an analog data generating and processing device (ADFPD)); the examiner then requested for further clarification, wherein the applicant provided the following explanation:

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The applicant indicated that the current claims are not currently claiming a digital camera, but the claims can be associated with a digital camera; and a real world example of applicant's invention would be a medical device with a number of analog sensors sensing biomedical data, wherein the sensed biomedical data are collected (e.g. collecting analog data) and transferred to a host computer (e.g. transferring data to the computer while the computer thinks the connected medical device is a hard disk or some kind of digital storage device); furthermore, the applicant explained that another example of applicant's invention is a multimeter, wherein the multimeter is taking measurements (e.g. collecting analog data) from circuits, and the measurements are then transferred to a host computer (e.g. transferring data to the computer thinks the connected multimeter is a hard disk or some kind of digital storage device). In summary, the <u>core of applicant's invention</u> is <u>a device that receives and</u> stores analog data (e.g. acquiring data); the device is then connected to a host <u>computer views the connected device as a digital storage device for transferring the acquired data to the host computer</u>.

5. Claims 239 and 375 are objected to because of the following informalities:

in claim 239, "... as if it were a digital storage device without requiring any userloaded file transfer enabling software to be loaded ..." should be replaced with -... as if it were <u>the</u> digital storage device without requiring any user-loaded file transfer enabling software to be loaded ...-; and

in claim 375, line 1, "... method of claim 375 ..." should be replaced with -...

method of claim 374 ...-.

Please note that the request for the replacements as stated above is for the

purpose to improve the clarity of the claim language. Appropriate correction is required.

III. REJECTIONS BASED ON PRIOR ART

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 239, 333-339, 341-344, 346-362, 364-367 and 369-376 are rejected

under 35 U.S.C. 103(a) as being unpatentable over Hashimoto et al. (US Patent

6,111,604) in view of Smith et al. (US Patent 5,634,075), Ristelhueber : "Plug and play

is almost here" and Shinohara (US Patent 5,742,934).

7. As per claim 239, <u>Hashimoto</u> teaches an analog data generating and processing device (ADGPD), comprising:

an input/output (i/o) port (Fig. 1A-1B; Fig. 8; col. 1, II. 35-57; col. 3, I. 43 to col. 4, I. 67; col. 5, II. 43-57; col. 6, I. 16 to col. 9, I. 17; col. 10, I. 41 to col. 11, I. 42 and col. 12, I. 16 to col. 13, I. 14), as the digital camera system have the corresponding i/o port for connecting to the PC (Fig. 8, ref. 29);

a program memory (Fig. 9, ref. 52, 54-55 and col. 8, l. 48 to col. 9, l. 17);

a data storage memory (Fig. 8, ref. 16; Fig. 10; col. 6, l. 16 to col. 8, l. 47 and col. 9, ll. 18-45);

a processor (Fig. 8, ref. 11, 23) operatively interfaced with the i/o port, the program memory (Fig. 9, ref. 52, 54-55) and the data storage memory (Fig. 8, ref. 16) (Fig. 8; Fig. 9; col. 6, l. 16 to col. 9, l. 17 and col. 10, l. 41 to col. 11, l. 42);

wherein the processor is adapted to implement a data generation process by which analog data (e.g. audio and visual analog data) is acquired from each respective analog acquisition channel of a plurality of independent analog acquisition channels (e.g. channel for audio analog data and channel for visual analog data), the analog data is processed and digitized (e.g. via analog to digital converter), and the processed and digitized analog data is stored in the data storage memory (Fig. 8, ref. 16 and Fig. 10) as at least one file of digitized analog data (Fig. 12) (Fig. 1A-1B; Fig. 8; Fig. 11-12; Fig. 14-15; col. 1, II. 35-57; col. 3, I. 43 to col. 4, I. 57; col. 5, II. 43-57; col. 6, I. 16 to col. 9, I. 17 and col. 9, I. 46 to col. 10, I. 16);

wherein the processor also is adapted to be involved in an automatic recognition process in which, when the i/o port is operatively interfaced with a multi-purpose interface of a computer, the processor executes at least one instruction set stored in the program memory; and wherein the processor is further adapted to be involved in an automatic file transfer process in which, when the i/o port is operatively interfaced with the multi-purpose interface of the computer, the processor executes at least one other instruction set stored in the program memory to thereby cause the at least one file of digitized analog data acquired from at least one of the plurality of analog acquisition channels to be transferred to the computer (Fig. 9; Fig. 11-12; Fig. 14-15; col. 1, II. 27-57; col. 6, l. 16 to col. 9, l. 17; col. 9, l. 46 to col. 11, l. 42 and col. 12, l. 16 to col. 14, l. 14), wherein the digital camera's CPU (Fig. 8, ref. 23) control the operation of the digital camera for the data transferring after the digital camera is connected to and recognized by the PC, and as the digital camera's CPU control any function of the digital camera, the digital camera's CPU further controls the digital camera to be recognized by the PC; wherein the digital camera needs to be recognized by the PC in order for the PC to know what peripheral device is connected such that the PC knows how to properly communicate with the connected peripheral device.

<u>Hashimoto</u> does not teach the ADGPD comprising: causes at least one parameter identifying the analog data generating and processing device, independent of analog data source, as a digital storage device instead of as an analog data generating and processing device to be automatically sent through the i/o port and to the multi-

purpose interface of the computer (a) without requiring any end user to load any software onto the computer at any time and (b) without requiring any end user to interact with the computer to set up a file system in the ADGPD at any time;

wherein the at least one parameter provides information to the computer about file transfer characteristics of the ADGPD; and

data transferring, after the at least one parameter has been sent from the i/o port to the multi-purpose interface of the computer, using a device driver for the digital storage device while causing the analog data generating and processing device to appear to the computer as if it were the digital storage device without requiring any user-loaded file transfer enabling software to be loaded on or installed in the computer at any time.

Smith teaches a system and a method comprising: automatic recognition process wherein at least one parameter (e.g. parameter signifying that the peripheral device has the ability communicate in accordance to the at least one software driver) to be automatically sent through the i/o port and to the multi-purpose interface of the computer (Fig. 2-5; col. 1, II. 9-22; col. 2, I. 40 to col. 3, I. 59; col. 4, II. 5-34 and col. 6, II. 63-62), by combining the plug-and-play functionality with <u>Hashimoto</u>'s automatic recognition process, the resulting combination further teaches the automatic recognition process corresponding to configuring plug and play system utilizing ROM BIOS by having the operating system load the device driver after the peripheral device is coupled to the PC for installation.

It would have been obvious for one of ordinary skill in this art, at the time of invention was made to include <u>Smith</u>'s plug and play functionality into <u>Hashimoto</u>'s automatic recognition process for the benefit of simplifying the installation of the peripheral device for the user as the peripheral device may be installed without the need for the user to install software or configure the peripheral device (<u>Smith</u>, col. 2, II. 40-67 and col. 5, II. 41-51 and col. 6, II. 63-65) to obtain the invention as specified in claim 239.

<u>Hashimoto</u> and <u>Smith</u> do not teach the ADGPD comprising: identifying the analog data generating and processing device, independent of analog data source, as a digital storage device instead of as an analog data generating and processing device (a) without ... load any software onto the computer at any time and (b) without requiring any end user to interact with the computer to set up a file system in the ADGPD at any time;

wherein the at least one parameter provides information to the computer about file transfer characteristics of the ADGPD; and

data transferring, after the at least one parameter has been sent from the i/o port to the multi-purpose interface of the computer, using a device driver for the digital storage device while causing the analog data generating and processing device to appear to the computer as if it were the digital storage device without requiring any user-loaded file transfer enabling software to be loaded on or installed in the computer at any time.

<u>Ristelhueber</u> teaches a system and a method comprising a peripheral device having an automatic recognition process without requiring any end user to load any software onto the computer at any time (pages 1-3), wherein the resulting combination of the references further teaches the above automatic recognition process corresponds to plug and play of a peripheral device by having a user to simply insert a peripheral into a desktop system and have it start running immediately, as the PnP computer will automatically identify any new hardware installed and configure the new hardware, and relieving the end user of any need to fumble with floppy disks and user manuals to get the device up and running; therefore, the installation of the peripheral device is accomplished without any type of software/driver being loaded by the user.

It would have been obvious for one of ordinary skill in this art, at the time of invention was made to include <u>Ristelhueber</u>'s alleviating user loading software/driver into <u>Hashimoto</u> and <u>Smith</u>'s plug-and-play processor, not only is such implementation well known to be in accord with the plug-and-play standard, but also for the benefit of simplifying the end user's PC upgrading and reducing cost for the computing industry (<u>Ristelhueber</u>, page 2, 3rd paragraph) to obtain the invention as specified in claim 239.

<u>Hashimoto</u>, <u>Smith</u> and <u>Ristelhueber</u> do not expressly teach the ADGPD comprising: identifying the analog data generating and processing device, independent of analog data source, as a digital storage device instead of as an analog data generating and processing device without requiring any end user to interact with the computer to set up a file system in the ADGPD at any time;

wherein the at least one parameter provides information to the computer about file transfer characteristics of the ADGPD; and

data transferring, after the at least one parameter has been sent from the i/o port to the multi-purpose interface of the computer, using a device driver for the digital storage device while causing the analog data generating and processing device to appear to the computer as if it were the digital storage device without requiring any user-loaded file transfer enabling software to be loaded on or installed in the computer at any time.

Shinohara teaches a system and a method comprising:

identifying the analog data generating and processing device, independent of analog data source, as a digital storage device instead of as an analog data generating and processing device without requiring any end user to interact with the computer to set up a file system in the ADGPD at any time (col. 1, II. 48-60 and col. 3, I. 33 to col. 4, I. 49), by combining the flash memory card emulating of a mass storage device (e.g. hard disk drive) with <u>Hashimoto</u>, <u>Smith</u>, <u>Kerigan</u> and <u>Ristelhueber</u>'s plug-and-play digital camera device having the processor and the flash memory card for data transferring with the host computer, the resulting combination of the references further teaches the above claimed feature, which is in accordance to the applicant's disclosure of the core novelty for the instant invention as disclosed by the applicant during the interview dated 10/06/2010;

wherein the at least one parameter provides information to the computer about file transfer characteristics (e.g. associated emulating hard disk drive data transferring

characteristics) of the ADGPD (col. 1, II. 48-60 and col. 3, I. 33 to col. 4, I. 49), by combining the flash memory card emulating a mass storage device (e.g. hard disk drive) with <u>Hashimoto</u>, <u>Smith</u>, <u>Kerigan</u> and <u>Ristelhueber</u>'s plug-and-play digital camera device having the processor and the flash memory card for data transferring with the host computer, the resulting combination of the references further teaches the above claimed feature, which is in accordance to the applicant's disclosure of the core novelty for the instant invention as disclosed by the applicant during the interview dated 10/06/2010; and

data transferring, after the at least one parameter has been sent from the i/o port to the multi-purpose interface of the computer, using a device driver (e.g. hard disk drive device driver) for the digital storage device while causing the analog data generating and processing device to appear to the computer as if it were the digital storage device (e.g. hard disk drive) without requiring any user-loaded file transfer enabling software to be loaded on or installed in the computer at any time (col. 1, II. 48-60 and col. 3, I. 33 to col. 4, I. 49), by combining the flash memory card emulating a mass storage device (e.g. hard disk drive) with <u>Hashimoto</u>, <u>Smith</u>, <u>Kerigan</u> and <u>Ristelhueber</u>'s plug-and-play digital camera device having the processor and the flash memory card for data transferring with the host computer, the resulting combination of the references further teaches the above claimed feature, which is in accordance to the applicant's disclosure of the core novelty for the instant invention as disclosed by the applicant during the interview dated 10/06/2010.

It would have been obvious for one of ordinary skill in this art, at the time of invention was made to include <u>Shinohara</u>'s hard disk drive emulation into <u>Hashimoto</u>, <u>Smith</u>, <u>Kerigan</u> and <u>Ristelhueber</u>'s plug-and-play processor for reading data from the memory card for the benefit of expanding the lifetime usage of the memory card (<u>Shinohara</u>, col. 2, II. 7-8) to obtain the invention as specified in claim 239.

8. As per claim 333, <u>Hashimoto, Smith, Ristelhueber</u> and <u>Shinohara</u> teach all the of limitations claim 239 as discussed above, where <u>Hashimoto, Smith, Ristelhueber</u> and <u>Shinohara</u> further teach the ADGPD comprising wherein the processor is configured to transmit to the computer active commands through the multi-purpose interface to access a system bus of the computer to enable communication directly with other devices of the computer while bypassing the computer processor (<u>Hashimoto, Fig. 1A-1B; Fig. 8; Fig. 11-12; Fig. 14-15; col. 1, II. 27-57; col. 3, I. 43 to col. 4, I. 67; col. 5, II. 43-57; col. 6, I. 16 to col. 9, I. 17; col. 9, I. 46 to col. 11, I. 42; col. 12, I. 16 to col. 14, I. 14; <u>Smith</u>, Fig. 2-5; col. 1, II. 9-22; col. 2, I. 40 to col. 3, I. 8; col. 3, II. 22-27; col. 3, II. 53-59; col. 4, II. 5-34; col. 6, II. 63-62; <u>Ristelhueber</u>, pages 1-3; and <u>Shinohara</u>, col. 1, II. 48-60; col. 3, I. 56 to col. 4, I. 49), as the resulting combination of the references does teach/suggest the heart/core of applicant's invention, it would have been obvious for the resulting combination of the references to further teach the transferring of data from the digital camera directly to the hard disk drive device of the computer.</u>

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9. As per claim 334, <u>Hashimoto</u>, <u>Smith</u>, <u>Ristelhueber</u> and <u>Shinohara</u> teach all the of limitations claim 239 as discussed above, where <u>Hashimoto</u>, <u>Smith</u>, <u>Ristelhueber</u> and <u>Shinohara</u> further teach the ADGPD comprising wherein the at least one parameter identifies the analog data generating and processing device as a hard disk drive (e.g. hard disk emulation) (<u>Hashimoto</u>, Fig. 1A-1B; Fig. 8; Fig. 11-12; Fig. 14-15; col. 1, II. 27-57; col. 3, I. 43 to col. 4, I. 67; col. 5, II. 43-57; col. 6, I. 16 to col. 9, I. 17; col. 9, I. 46 to col. 11, I. 42; col. 12, I. 16 to col. 14, I. 14; <u>Smith</u>, Fig. 2-5; col. 1, II. 9-22; col. 2, I. 40 to col. 3, I. 8; col. 3, II. 22-27; col. 3, II. 53-59; col. 4, II. 5-34; col. 6, II. 63-62; <u>Ristelhueber</u>, pages 1-3; and Shinohara, col. 1, II. 48-60; col. 3, I. 56 to col. 4, I. 49).

10. As per claim 335, <u>Hashimoto</u>, <u>Smith</u>, <u>Ristelhueber</u> and <u>Shinohara</u> teach all the of limitations claim 239 as discussed above, where <u>Hashimoto</u>, <u>Smith</u>, <u>Ristelhueber</u> and <u>Shinohara</u> further teach the ADGPD further comprising at least one additional analog data generating and processing device coupled to the computer in parallel and each analog data generating and processing device attached to a difference analog data source (<u>Hashimoto</u>, Fig. 1A-1B; Fig. 8; Fig. 11-12; Fig. 14-15; col. 1, II. 27-57; col. 3, I. 43 to col. 4, I. 67; col. 5, II. 43-57; col. 6, I. 16 to col. 9, I. 17; col. 9, I. 46 to col. 11, I. 42; col. 12, I. 16 to col. 14, I. 14; <u>Smith</u>, Fig. 2-5; col. 1, II. 9-22; col. 2, I. 40 to col. 3, I. 8; col. 3, II. 22-27; col. 3, II. 53-59; col. 4, II. 5-34; col. 6, II. 63-62; <u>Ristelhueber</u>, pages 1-3; and <u>Shinohara</u>, col. 1, II. 48-60; col. 3, I. 56 to col. 4, I. 49), as the resulting combination of the references does teach/suggest the heart/core of applicant's invention, it would have

been obvious for the resulting combination of the references to further teach more than one peripheral device (e.g. digital camera) is connected to the computer.

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11. As per claim 336, <u>Hashimoto</u>, <u>Smith</u>, <u>Ristelhueber</u> and <u>Shinohara</u> teach all the of limitations claim 239 as discussed above, where <u>Hashimoto</u>, <u>Smith</u>, <u>Ristelhueber</u> and <u>Shinohara</u> further teach the ADGPD comprising wherein processor is configured to format the digitized analog data into blocks of data with block sizes suitable for a hard disk of the computer (<u>Hashimoto</u>, Fig. 1A-1B; Fig. 8; Fig. 11-12; Fig. 14-15; col. 1, II. 27-57; col. 3, I. 43 to col. 4, I. 67; col. 5, II. 43-57; col. 6, I. 16 to col. 9, I. 17; col. 9, I. 46 to col. 11, I. 42; col. 12, I. 16 to col. 14, I. 14; <u>Smith</u>, Fig. 2-5; col. 1, II. 9-22; col. 2, I. 40 to col. 3, I. 8; col. 3, II. 22-27; col. 3, II. 53-59; col. 4, II. 5-34; col. 6, II. 63-62; <u>Ristelhueber</u>, pages 1-3; and <u>Shinohara</u>, col. 1, II. 48-60; col. 3, I. 56 to col. 4, I. 49), as the digital camera is emulating the hard disk drive, data being transferred from the digital camera is hard disk drive data, suitable for the computer's hard disk.

12. As per claim 337, <u>Hashimoto</u>, <u>Smith</u>, <u>Ristelhueber</u> and <u>Shinohara</u> teach all the of limitations claim 239 as discussed above, where <u>Hashimoto</u>, <u>Smith</u>, <u>Ristelhueber</u> and <u>Shinohara</u> further teach the ADGPD further comprising a data buffer coupled to the processor to permit independence of time of data acquisition and data transfer to the host computer (<u>Hashimoto</u>, Fig. 1A-1B; Fig. 8; Fig. 11-12; Fig. 14-15; col. 1, II. 27-57; col. 3, I. 43 to col. 4, I. 67; col. 5, II. 43-57; col. 6, I. 16 to col. 9, I. 17; col. 9, I. 46 to col. 11, I. 42; col. 12, I. 16 to col. 14, I. 14; <u>Smith</u>, Fig. 2-5; col. 1, II. 9-22; col. 2, I. 40 to col.

3, I. 8; col. 3, II. 22-27; col. 3, II. 53-59; col. 4, II. 5-34; col. 6, II. 63-62; <u>Ristelhueber</u>, pages 1-3; and <u>Shinohara</u>, col. 1, II. 48-60; col. 3, I. 56 to col. 4, I. 49), as the resulting combination of the references does teach/suggest the heart/core of applicant's invention, it would have been obvious for the resulting combination of the references to further teach above the data buffer architecture.

13. As per claim 338, Hashimoto, Smith, Ristelhueber and Shinohara teach all the of limitations claim 239 as discussed above, where Hashimoto, Smith, Ristelhueber and Shinohara further teach the ADGPD comprising wherein each of the plurality of analog acquisition channels are independently programmable and further comprise a plurality of corresponding sample and hold amplifiers for simultaneous sampling on the plurality of analog acquisition channels to permit simultaneous analog data acquisition from a plurality of respective analog data sources (<u>Hashimoto</u>, Fig. 1A-1B; Fig. 8; Fig. 11-12; Fig. 14-15; col. 1, ll. 27-57; col. 3, l. 43 to col. 4, l. 67; col. 5, ll. 43-57; col. 6, l. 16 to col. 9, I. 17; col. 9, I. 46 to col. 11, I. 42; col. 12, I. 16 to col. 14, I. 14; Smith, Fig. 2-5; col. 1, II. 9-22; col. 2, I. 40 to col. 3, I. 8; col. 3, II. 22-27; col. 3, II. 53-59; col. 4, II. 5-34; col. 6, II. 63-62; Ristelhueber, pages 1-3; and Shinohara, col. 1, II. 48-60; col. 3, I. 56 to col. 4, I. 49), as the resulting combination of the references does teach/suggest the heart/core of applicant's invention, it would have been obvious for the resulting combination of the references to further teach the above claimed feature as the audio and image data are simultaneously captured in order for proper generating the corresponding video data.

14. As per claim 339, <u>Hashimoto, Smith, Ristelhueber</u> and <u>Shinohara</u> teach all the of limitations claim 233 as discussed above, where <u>Hashimoto, Smith, Ristelhueber</u> and <u>Shinohara</u> further teach the ADGPD comprising wherein the active commands initiate active access to write data directly to a hard drive in the host computer independent of the host computer central processor (<u>Hashimoto</u>, Fig. 1A-1B; Fig. 8; Fig. 11-12; Fig. 14-15; col. 1, II. 27-57; col. 3, I. 43 to col. 4, I. 67; col. 5, II. 43-57; col. 6, I. 16 to col. 9, I. 17; col. 9, I. 46 to col. 11, I. 42; col. 12, I. 16 to col. 14, I. 14; <u>Smith</u>, Fig. 2-5; col. 1, II. 9-22; col. 2, I. 40 to col. 3, I. 8; col. 3, II. 22-27; col. 3, II. 53-59; col. 4, II. 5-34; col. 6, II. 63-62; <u>Ristelhueber</u>, pages 1-3; and <u>Shinohara</u>, col. 1, II. 48-60; col. 3, I. 56 to col. 4, I. 49), as the resulting combination of the references does teach/suggest the heart/core of applicant's invention, it would have been obvious for the resulting combination of the references to further teach the transferring of data from the digital camera directly to the hard disk drive device of the computer.

15. As per claim 341, <u>Hashimoto</u>, <u>Smith</u>, <u>Ristelhueber</u> and <u>Shinohara</u> teach all the of limitations claim 239 as discussed above, where <u>Hashimoto</u>, <u>Smith</u>, <u>Ristelhueber</u> and <u>Shinohara</u> further teach the ADGPD comprising wherein the analog data generating and processing device is attached directly to at least one analog source (<u>Hashimoto</u>, Fig. 1A-1B; Fig. 8; Fig. 11-12; Fig. 14-15; col. 1, II. 27-57; col. 3, I. 43 to col. 4, I. 67; col. 5, II. 43-57; col. 6, I. 16 to col. 9, I. 17; col. 9, I. 46 to col. 11, I. 42; col. 12, I. 16 to col. 14, I. 14; <u>Smith</u>, Fig. 2-5; col. 1, II. 9-22; col. 2, I. 40 to col. 3, I. 8; col. 3, II. 22-27; col. 3, II. 53-

59; col. 4, II. 5-34; col. 6, II. 63-62; <u>Ristelhueber</u>, pages 1-3; and <u>Shinohara</u>, col. 1, II. 48-60; col. 3, I. 56 to col. 4, I. 49).

16. As per claim 342, <u>Hashimoto</u>, <u>Smith</u>, <u>Ristelhueber</u> and <u>Shinohara</u> teach all the of limitations claim 239 as discussed above, where <u>Hashimoto</u>, <u>Smith</u>, <u>Ristelhueber</u> and <u>Shinohara</u> further teach the ADGPD comprising wherein the analog data generating and processing device is a stand alone device (<u>Hashimoto</u>, Fig. 1A-1B; Fig. 8; Fig. 11-12; Fig. 14-15; col. 1, II. 27-57; col. 3, I. 43 to col. 4, I. 67; col. 5, II. 43-57; col. 6, I. 16 to col. 9, I. 17; col. 9, I. 46 to col. 11, I. 42; col. 12, I. 16 to col. 14, I. 14; <u>Smith</u>, Fig. 2-5; col. 1, II. 9-22; col. 2, I. 40 to col. 3, I. 8; col. 3, II. 22-27; col. 3, II. 53-59; col. 4, II. 5-34; col. 6, II. 63-62; <u>Ristelhueber</u>, pages 1-3; and <u>Shinohara</u>, col. 1, II. 48-60; col. 3, I. 56 to col. 4, I. 49).

17. As per claim 343, <u>Hashimoto</u>, <u>Smith</u>, <u>Ristelhueber</u> and <u>Shinohara</u> teach all the of limitations claim 239 as discussed above, where <u>Hashimoto</u>, <u>Smith</u>, <u>Ristelhueber</u> and <u>Shinohara</u> further teach the ADGPD comprising wherein the input/output port further comprises a SCSI interface circuit (<u>Hashimoto</u>, Fig. 1A-1B; Fig. 8; Fig. 11-12; Fig. 14-15; col. 1, II. 27-57; col. 3, I. 43 to col. 4, I. 67; col. 5, II. 43-57; col. 6, I. 16 to col. 9, I. 17; col. 9, I. 46 to col. 11, I. 42; col. 12, I. 16 to col. 14, I. 14; <u>Smith</u>, Fig. 2-5; col. 1, II. 9-22; col. 2, I. 40 to col. 3, I. 8; col. 3, II. 22-27; col. 3, II. 53-59; col. 4, II. 5-34; col. 6, II. 63-62; <u>Ristelhueber</u>, pages 1-3; and <u>Shinohara</u>, col. 1, II. 48-60; col. 3, I. 56 to col. 4, I. 49).

18. As per claim 344, <u>Hashimoto</u>, <u>Smith</u>, <u>Ristelhueber</u> and <u>Shinohara</u> teach all the of limitations claim 335 as discussed above, where <u>Hashimoto</u>, <u>Smith</u>, <u>Ristelhueber</u> and <u>Shinohara</u> further teach the ADGPD comprising wherein as least some of the analog data sources are analog data sources of different types (<u>Hashimoto</u>, Fig. 1A-1B; Fig. 8; Fig. 11-12; Fig. 14-15; col. 1, ll. 27-57; col. 3, l. 43 to col. 4, l. 67; col. 5, ll. 43-57; col. 6, l. 16 to col. 9, l. 17; col. 9, l. 46 to col. 11, l. 42; col. 12, l. 16 to col. 14, l. 14; <u>Smith</u>, Fig. 2-5; col. 1, ll. 9-22; col. 2, l. 40 to col. 3, l. 8; col. 3, ll. 22-27; col. 3, ll. 53-59; col. 4, ll. 5-34; col. 6, ll. 63-62; <u>Ristelhueber</u>, pages 1-3; and <u>Shinohara</u>, col. 1, ll. 48-60; col. 3, l. 56 to col. 4, l. 49).

19. As per claim 346, <u>Hashimoto</u>, <u>Smith</u>, <u>Ristelhueber</u> and <u>Shinohara</u> teach all the of limitations claim 239 as discussed above, where <u>Hashimoto</u>, <u>Smith</u>, <u>Ristelhueber</u> and <u>Shinohara</u> further teach the ADGPD comprising wherein the analog data generating and processing device is adapted to be interfaced with the multi-purpose interface of the computer by means of a cable (<u>Hashimoto</u>, Fig. 1A-1B; Fig. 8; Fig. 11-12; Fig. 14-15; col. 1, II. 27-57; col. 3, I. 43 to col. 4, I. 67; col. 5, II. 43-57; col. 6, I. 16 to col. 9, I. 17; col. 9, I. 46 to col. 11, I. 42; col. 12, I. 16 to col. 14, I. 14; <u>Smith</u>, Fig. 2-5; col. 1, II. 9-22; col. 2, I. 40 to col. 3, I. 8; col. 3, II. 22-27; col. 3, II. 53-59; col. 4, II. 5-34; col. 6, II. 63-62; <u>Ristelhueber</u>, pages 1-3; and <u>Shinohara</u>, col. 1, II. 48-60; col. 3, I. 56 to col. 4, I. 49).

20. As per claim 347, <u>Hashimoto</u>, <u>Smith</u>, <u>Ristelhueber</u> and <u>Shinohara</u> teach all the of limitations claim 239 as discussed above, where <u>Hashimoto</u>, <u>Smith</u>, <u>Ristelhueber</u> and

Shinohara further teach the ADGPD comprising wherein at least one of the analog sources is a sensor that is operatively interfaced with the analog data generating and processing device and that is designed to generate the analog data (Hashimoto, Fig. 1A-1B; Fig. 8; Fig. 11-12; Fig. 14-15; col. 1, II. 27-57; col. 3, I. 43 to col. 4, I. 67; col. 5, II. 43-57; col. 6, I. 16 to col. 9, I. 17; col. 9, I. 46 to col. 11, I. 42; col. 12, I. 16 to col. 14, I. 14; Smith, Fig. 2-5; col. 1, II. 9-22; col. 2, I. 40 to col. 3, I. 8; col. 3, II. 22-27; col. 3, II. 53-59; col. 4, II. 5-34; col. 6, II. 63-62; Ristelhueber, pages 1-3; and Shinohara, col. 1, II. 48-60; col. 3, I. 56 to col. 4, I. 49).

21. As per claim 348, <u>Hashimoto</u>, <u>Smith</u>, <u>Ristelhueber</u> and <u>Shinohara</u> teach all the of limitations claim 239 as discussed above, where <u>Hashimoto</u>, <u>Smith</u>, <u>Ristelhueber</u> and <u>Shinohara</u> further teach the ADGPD comprising wherein the processor is configured to transmit to the computer active commands through the multipurpose interface to access a system bus of the computer to enable communication directly with other devices of the computer while bypassing the computer processor without requiring the user to load enabling software (<u>Hashimoto</u>, Fig. 1A-1B; Fig. 8; Fig. 11-12; Fig. 14-15; col. 1, II. 27-57; col. 3, I. 43 to col. 4, I. 67; col. 5, II. 43-57; col. 6, I. 16 to col. 9, I. 17; col. 9, I. 46 to col. 11, I. 42; col. 12, I. 16 to col. 14, I. 14; <u>Smith</u>, Fig. 2-5; col. 1, II. 9-22; col. 2, I. 40 to col. 3, I. 8; col. 3, II. 22-27; col. 3, II. 53-59; col. 4, II. 5-34; col. 6, II. 63-62; <u>Ristelhueber</u>, pages 1-3; and <u>Shinohara</u>, col. 1, II. 48-60; col. 3, I. 56 to col. 4, I. 49), as the resulting combination of the references does teach/suggest the heart/core of applicant's invention, it would have been obvious for the resulting combination of the references to

further teach the transferring of data from the digital camera directly to the hard disk drive device of the computer via the system bus of the computer.

22. As per claim 349, <u>Hashimoto</u>, <u>Smith</u>, <u>Ristelhueber</u> and <u>Shinohara</u> teach all the of limitations claim 239 as discussed above, where <u>Hashimoto</u>, <u>Smith</u>, <u>Ristelhueber</u> and <u>Shinohara</u> further teach the ADGPD comprising wherein the plurality of analog acquisition channels are independently programmable (<u>Hashimoto</u>, Fig. 1A-1B; Fig. 8; Fig. 11-12; Fig. 14-15; col. 1, II. 27-57; col. 3, I. 43 to col. 4, I. 67; col. 5, II. 43-57; col. 6, I. 16 to col. 9, I. 17; col. 9, I. 46 to col. 11, I. 42; col. 12, I. 16 to col. 14, I. 14; <u>Smith</u>, Fig. 2-5; col. 1, II. 9-22; col. 2, I. 40 to col. 3, I. 8; col. 3, II. 22-27; col. 3, II. 53-59; col. 4, II. 5-34; col. 6, II. 63-62; <u>Ristelhueber</u>, pages 1-3; and <u>Shinohara</u>, col. 1, II. 48-60; col. 3, I. 56 to col. 4, I. 49), as the resulting combination of the references does teach/suggest the heart/core of applicant's invention, it would have been obvious for the resulting combination of the references.

23. As per claim 350, <u>Hashimoto</u>, <u>Smith</u>, <u>Ristelhueber</u> and <u>Shinohara</u> teach all the of limitations claim 239 as discussed above, where <u>Hashimoto</u>, <u>Smith</u>, <u>Ristelhueber</u> and <u>Shinohara</u> further teach the ADGPD comprising wherein at least one analog source is designed to receive data from a host device (<u>Hashimoto</u>, Fig. 1A-1B; Fig. 8; Fig. 11-12; Fig. 14-15; col. 1, II. 27-57; col. 3, I. 43 to col. 4, I. 67; col. 5, II. 43-57; col. 6, I. 16 to col. 9, I. 17; col. 9, I. 46 to col. 11, I. 42; col. 12, I. 16 to col. 14, I. 14; <u>Smith</u>, Fig. 2-5; col. 1, II. 9-22; col. 2, I. 40 to col. 3, I. 8; col. 3, II. 22-27; col. 3, II. 53-59; col. 4, II. 5-34; col. 6, II.

63-62; <u>Ristelhueber</u>, pages 1-3; and <u>Shinohara</u>, col. 1, II. 48-60; col. 3, I. 56 to col. 4, I. 49), as the resulting combination of the references does teach/suggest the heart/core of applicant's invention, it would have been obvious for the resulting combination of the references to further teach the host device receiving audiovisual information from the camera and communicating to the camera by updating control program to control the sensor.

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24. As per claim 351, <u>Hashimoto, Smith, Ristelhueber</u> and <u>Shinohara</u> teach all the of limitations claim 239 as discussed above, where <u>Hashimoto, Smith, Ristelhueber</u> and <u>Shinohara</u> further teach the ADGPD comprising wherein at least one analog source comprises a multimeter that is operatively interfaced with the analog data generating and processing device and that is designed to generate the analog data (<u>Hashimoto</u>, Fig. 1A-1B; Fig. 8; Fig. 11-12; Fig. 14-15; col. 1, II. 27-57; col. 3, I. 43 to col. 4, I. 67; col. 5, II. 43-57; col. 6, I. 16 to col. 9, I. 17; col. 9, I. 46 to col. 11, I. 42; col. 12, I. 16 to col. 14, I. 14; <u>Smith</u>, Fig. 2-5; col. 1, II. 9-22; col. 2, I. 40 to col. 3, I. 8; col. 3, II. 22-27; col. 3, II. 53-59; col. 4, II. 5-34; col. 6, II. 63-62; <u>Ristelhueber</u>, pages 1-3; and <u>Shinohara</u>, col. 1, II. 48-60; col. 3, I. 56 to col. 4, I. 49), as the resulting combination of the references does teach/suggest the heart/core of applicant's invention, it would have been obvious for the resulting combination of the references to further implement the heart/core of applicant's invention in an alternative embodiment on the multimeter, as the multimeter, like the digital camera, is a portable stand along peripheral device.

25. As per claim 352, <u>Hashimoto</u>, <u>Smith</u>, <u>Ristelhueber</u> and <u>Shinohara</u> teach all the of limitations claim 239 as discussed above, where <u>Hashimoto</u>, <u>Smith</u>, <u>Ristelhueber</u> and <u>Shinohara</u> further teach the ADGPD comprising wherein the at least one parameter is consistent with the analog data generating and processing device being responsive to a SCSI inquiry command (<u>Hashimoto</u>, Fig. 1A-1B; Fig. 8; Fig. 11-12; Fig. 14-15; col. 1, II. 27-57; col. 3, I. 43 to col. 4, I. 67; col. 5, II. 43-57; col. 6, I. 16 to col. 9, I. 17; col. 9, I. 46 to col. 11, I. 42; col. 12, I. 16 to col. 14, I. 14; <u>Smith</u>, Fig. 2-5; col. 1, II. 9-22; col. 2, I. 40 to col. 3, I. 8; col. 3, II. 22-27; col. 3, II. 53-59; col. 4, II. 5-34; col. 6, II. 63-62; Ristelhueber, pages 1-3; and Shinohara, col. 1, II. 48-60; col. 3, I. 56 to col. 4, I. 49).

26. As per claim 353, <u>Hashimoto</u>, <u>Smith</u>, <u>Ristelhueber</u> and <u>Shinohara</u> teach all the of limitations claim 239 as discussed above, where <u>Hashimoto</u>, <u>Smith</u>, <u>Ristelhueber</u> and <u>Shinohara</u> further teach the ADGPD comprising wherein the at least one parameter identifies the analog data generating and processing device as a digital mass storage device (<u>Hashimoto</u>, Fig. 1A-1B; Fig. 8; Fig. 11-12; Fig. 14-15; col. 1, II. 27-57; col. 3, I. 43 to col. 4, I. 67; col. 5, II. 43-57; col. 6, I. 16 to col. 9, I. 17; col. 9, I. 46 to col. 11, I. 42; col. 12, I. 16 to col. 14, I. 14; <u>Smith</u>, Fig. 2-5; col. 1, II. 9-22; col. 2, I. 40 to col. 3, I. 8; col. 3, II. 22-27; col. 3, II. 53-59; col. 4, II. 5-34; col. 6, II. 63-62; <u>Ristelhueber</u>, pages 1-3; and <u>Shinohara</u>, col. 1, II. 48-60; col. 3, I. 56 to col. 4, I. 49).

27. As per claim 354, <u>Hashimoto</u>, <u>Smith</u>, <u>Ristelhueber</u> and <u>Shinohara</u> teach all the of limitations claim 239 as discussed above, where <u>Hashimoto</u>, <u>Smith</u>, <u>Ristelhueber</u> and

Shinohara further teach the ADGPD comprising wherein the processor is configured to, when the processor is operatively interfaced with the multi-purpose interface of the computer and after the at least one parameter has been sent to the multi-purpose interface of the computer, execute at least one set of computer code stored in program memory and thereby cause analog data generating and processing device file system information to be automatically sent to the multipurpose interface without requiring any end user to interact with the computer to set up a file system in the analog data generating and processing device at any time (Hashimoto, Fig. 1A-1B; Fig. 8; Fig. 11-12; Fig. 14-15; col. 1, II. 27-57; col. 3, I. 43 to col. 4, I. 67; col. 5, II. 43-57; col. 6, I. 16 to col. 9, I. 17; col. 9, I. 46 to col. 11, I. 42; col. 12, I. 16 to col. 14, I. 14; Smith, Fig. 2-5; col. 1, II. 9-22; col. 2, I. 40 to col. 3, I. 8; col. 3, II. 22-27; col. 3, II. 53-59; col. 4, II. 5-34; col. 6, II. 63-62; Ristelhueber, pages 1-3; and Shinohara, col. 1, II. 48-60; col. 3, I. 56 to col. 4, I. 49).

28. As per claim 355, <u>Hashimoto</u>, <u>Smith</u>, <u>Ristelhueber</u> and <u>Shinohara</u> teach all the of limitations claim 254 as discussed above, where <u>Hashimoto</u>, <u>Smith</u>, <u>Ristelhueber</u> and <u>Shinohara</u> further teach the ADGPD comprising wherein the analog data generating and processing device file system information comprises at least one indication of a file system type that is used to store the at least one file of digitized analog data in the data storage memory (<u>Hashimoto</u>, Fig. 1A-1B; Fig. 8; Fig. 11-12; Fig. 14-15; col. 1, II. 27-57; col. 3, I. 43 to col. 4, I. 67; col. 5, II. 43-57; col. 6, I. 16 to col. 9, I. 17; col. 9, I. 46 to col. 11, I. 42; col. 12, I. 16 to col. 14, I. 14; <u>Smith</u>, Fig. 2-5; col. 1, II. 9-22; col. 2, I. 40 to col.

3, I. 8; col. 3, II. 22-27; col. 3, II. 53-59; col. 4, II. 5-34; col. 6, II. 63-62; <u>Ristelhueber</u>, pages 1-3; and <u>Shinohara</u>, col. 1, II. 48-60; col. 3, I. 56 to col. 4, I. 49), as the type of file system corresponds to the plug-and-play ADGPD having the memory card emulating as the hard disk drive for data transferring after the plug-and-play ADGPD is connected to the PC.

29. As per claim 356, <u>Hashimoto</u>, <u>Smith</u>, <u>Ristelhueber</u> and <u>Shinohara</u> teach all the of limitations claim 239 as discussed above, where <u>Hashimoto</u>, <u>Smith</u>, <u>Ristelhueber</u> and <u>Shinohara</u> further teach the ADGPD comprising wherein the at least one parameter is consistent with the analog data generating and processing device being a digital mass storage device other than a magnetic floppy disk drive (<u>Hashimoto</u>, Fig. 1A-1B; Fig. 8; Fig. 11-12; Fig. 14-15; col. 1, II. 27-57; col. 3, I. 43 to col. 4, I. 67; col. 5, II. 43-57; col. 6, I. 16 to col. 9, I. 17; col. 9, I. 46 to col. 11, I. 42; col. 12, I. 16 to col. 14, I. 14; <u>Smith</u>, Fig. 2-5; col. 1, II. 9-22; col. 2, I. 40 to col. 3, I. 8; col. 3, II. 22-27; col. 3, II. 53-59; col. 4, II. 5-34; col. 6, II. 63-62; <u>Ristelhueber</u>, pages 1-3; and <u>Shinohara</u>, col. 1, II. 48-60; col. 3, I. 56 to col. 4, I. 49).

30. As per claim 357, <u>Hashimoto</u>, <u>Smith</u>, <u>Ristelhueber</u> and <u>Shinohara</u> teach all the of limitations claim 239 as discussed above, where <u>Hashimoto</u>, <u>Smith</u>, <u>Ristelhueber</u> and <u>Shinohara</u> further teach the ADGPD comprising wherein the processor is configured to cause, after the at least one parameter has been sent to the multipurpose interface, file allocation table information to be sent to the multipurpose interface, wherein the

processor is configured to cause a virtual boot sequence to be sent to the multipurpose interface which includes at least information that is representative of a number of sectors of a storage disk, and wherein the file allocation table information includes at least a start location of a file allocation table (<u>Hashimoto</u>, Fig. 1A-1B; Fig. 8; Fig. 11-12; Fig. 14-15; col. 1, II. 27-57; col. 3, I. 43 to col. 4, I. 67; col. 5, II. 43-57; col. 6, I. 16 to col. 9, I. 17; col. 9, I. 46 to col. 11, I. 42; col. 12, I. 16 to col. 14, I. 14; <u>Smith</u>, Fig. 2-5; col. 1, II. 9-22; col. 2, I. 40 to col. 3, I. 8; col. 3, II. 22-27; col. 3, II. 53-59; col. 4, II. 5-34; col. 6, II. 63-62; <u>Ristelhueber</u>, pages 1-3; and <u>Shinohara</u>, col. 1, II. 48-60; col. 3, I. 56 to col. 4, I. 49), wherein the transferring of the parameter, the file allocation table information and the virtual boot sequence corresponds to the plug-and-play ADGPD having the memory card emulating as the hard disk drive for data transferring after the plug-and-play ADGPD is connected to the PC.

31. As per claim 358, <u>Hashimoto</u>, <u>Smith</u>, <u>Ristelhueber</u> and <u>Shinohara</u> teach all the of limitations claim 357 as discussed above, where <u>Hashimoto</u>, <u>Smith</u>, <u>Ristelhueber</u> and <u>Shinohara</u> further teach the ADGPD further comprising the processor configured to implement a process to acquire digital data from at least one digital source (<u>Hashimoto</u>, Fig. 1A-1B; Fig. 8; Fig. 11-12; Fig. 14-15; col. 1, II. 27-57; col. 3, I. 43 to col. 4, I. 67; col. 5, II. 43-57; col. 6, I. 16 to col. 9, I. 17; col. 9, I. 46 to col. 11, I. 42; col. 12, I. 16 to col. 14, I. 14; <u>Smith</u>, Fig. 2-5; col. 1, II. 9-22; col. 2, I. 40 to col. 3, I. 8; col. 3, II. 22-27; col. 3, II. 53-59; col. 4, II. 5-34; col. 6, II. 63-62; <u>Ristelhueber</u>, pages 1-3; and <u>Shinohara</u>, col. 1, II. 48-60; col. 3, I. 56 to col. 4, I. 49), as the resulting combination of the references does

teach/suggest the heart/core of applicant's invention, it would have been obvious for the resulting combination of the references to further teach acquiring the digital data from the digital source (e.g. digital data from memory card or I/O card).

32. As per claim 359, <u>Hashimoto</u>, <u>Smith</u>, <u>Ristelhueber</u> and <u>Shinohara</u> teach all the of limitations claim 239 as discussed above, where <u>Hashimoto</u>, <u>Smith</u>, <u>Ristelhueber</u> and <u>Shinohara</u> further teach the ADGPD comprising wherein the processor comprises a single digital signal processor (<u>Hashimoto</u>, Fig. 1A-1B; Fig. 8; Fig. 11-12; Fig. 14-15; col. 1, II. 27-57; col. 3, I. 43 to col. 4, I. 67; col. 5, II. 43-57; col. 6, I. 16 to col. 9, I. 17; col. 9, I. 46 to col. 11, I. 42; col. 12, I. 16 to col. 14, I. 14; <u>Smith</u>, Fig. 2-5; col. 1, II. 9-22; col. 2, I. 40 to col. 3, I. 8; col. 3, II. 22-27; col. 3, II. 53-59; col. 4, II. 5-34; col. 6, II. 63-62; <u>Ristelhueber</u>, pages 1-3; and <u>Shinohara</u>, col. 1, II. 48-60; col. 3, I. 56 to col. 4, I. 49).

33. As per claim 360, <u>Hashimoto</u>, <u>Smith</u>, <u>Ristelhueber</u> and <u>Shinohara</u> teach all the of limitations claim 239 as discussed above, where <u>Hashimoto</u>, <u>Smith</u>, <u>Ristelhueber</u> and <u>Shinohara</u> further teach the ADGPD comprising wherein the processor is configured to initiate a process by which digitized analog data are directly transferred to an input/output device (e.g. I/O card) (<u>Hashimoto</u>, Fig. 1A-1B; Fig. 8; Fig. 11-12; Fig. 14-15; col. 1, II. 27-57; col. 3, I. 43 to col. 4, I. 67; col. 5, II. 43-57; col. 6, I. 16 to col. 9, I. 17; col. 9, I. 46 to col. 11, I. 42; col. 12, I. 16 to col. 14, I. 14; <u>Smith</u>, Fig. 2-5; col. 1, II. 9-22; col. 2, I. 40 to col. 3, I. 8; col. 3, II. 22-27; col. 3, II. 53-59; col. 4, II. 5-34; col. 6, II. 63-62; <u>Ristelhueber</u>, pages 1-3; and <u>Shinohara</u>, col. 1, II. 48-60; col. 3, I. 56 to col. 4, I. 49).

34. As per claim 361, <u>Hashimoto</u>, <u>Smith</u>, <u>Ristelhueber</u> and <u>Shinohara</u> teach all the of limitations claim 239 as discussed above, where <u>Hashimoto</u>, <u>Smith</u>, <u>Ristelhueber</u> and <u>Shinohara</u> further teach the ADGPD comprising wherein the processor is configured to allow an aspect of operation (e.g. updating control program) of the analog data generating and processing device other than the transfer of at least some of the digitized analog data from the data storage memory to the multi-purpose interface to be controlled by means of an external computer (<u>Hashimoto</u>, Fig. 1A-1B; Fig. 8; Fig. 11-12; Fig. 14-15; col. 1, II. 27-57; col. 3, I. 43 to col. 4, I. 67; col. 5, II. 43-57; col. 6, I. 16 to col. 9, I. 17; col. 9, I. 46 to col. 11, I. 42; col. 12, I. 16 to col. 14, I. 14; <u>Smith</u>, Fig. 2-5; col. 1, II. 9-22; col. 2, I. 40 to col. 3, I. 8; col. 3, II. 22-27; col. 3, II. 53-59; col. 4, II. 5-34; col. 6, II. 63-62; <u>Ristelhueber</u>, pages 1-3; and <u>Shinohara</u>, col. 1, II. 48-60; col. 3, I. 56 to col. 4, I. 49), as the PC directly update the control program in the ADGPD.

35. As per claim 362, <u>Hashimoto</u>, <u>Smith</u>, <u>Ristelhueber</u> and <u>Shinohara</u> teach all the of limitations claim 239 as discussed above, where <u>Hashimoto</u>, <u>Smith</u>, <u>Ristelhueber</u> and <u>Shinohara</u> further teach the ADGPD comprising wherein the analog data generating and processing device comprises at least a portion of a medical device (<u>Hashimoto</u>, Fig. 1A-1B; Fig. 8; Fig. 11-12; Fig. 14-15; col. 1, II. 27-57; col. 3, I. 43 to col. 4, I. 67; col. 5, II. 43-57; col. 6, I. 16 to col. 9, I. 17; col. 9, I. 46 to col. 11, I. 42; col. 12, I. 16 to col. 14, I. 14; <u>Smith</u>, Fig. 2-5; col. 1, II. 9-22; col. 2, I. 40 to col. 3, I. 8; col. 3, II. 22-27; col. 3, II. 53-

59; col. 4, II. 5-34; col. 6, II. 63-62; <u>Ristelhueber</u>, pages 1-3; and <u>Shinohara</u>, col. 1, II. 48-60; col. 3, I. 56 to col. 4, I. 49), such as pictures taken for medical use.

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36. As per claim 364, <u>Hashimoto, Smith, Ristelhueber</u> and <u>Shinohara</u> teach all the of limitations claim 239 as discussed above, where <u>Hashimoto, Smith, Ristelhueber</u> and <u>Shinohara</u> further teach the ADGPD comprising wherein the analog data generation and automatic file transfer at least partially overlap in time (<u>Hashimoto</u>, Fig. 1A-1B; Fig. 8; Fig. 11-12; Fig. 14-15; col. 1, II. 27-57; col. 3, I. 43 to col. 4, I. 67; col. 5, II. 43-57; col. 6, I. 16 to col. 9, I. 17; col. 9, I. 46 to col. 11, I. 42; col. 12, I. 16 to col. 14, I. 14; <u>Smith</u>, Fig. 2-5; col. 1, II. 9-22; col. 2, I. 40 to col. 3, I. 8; col. 3, II. 22-27; col. 3, II. 53-59; col. 4, II. 5-34; col. 6, II. 63-62; <u>Ristelhueber</u>, pages 1-3; and <u>Shinohara</u>, col. 1, II. 48-60; col. 3, I. 56 to col. 4, I. 49), as the resulting combination of the references does teach/suggest the heart/core of applicant's invention, it would have been obvious for the resulting combination of the references to further teach after the first analog data is generated and being transferred, the second analog data is being generated (e.g. generating the second analog data while transferring of the first analog data).

37. As per claim 365, <u>Hashimoto</u>, <u>Smith</u>, <u>Ristelhueber</u> and <u>Shinohara</u> teach all the of limitations claim 239 as discussed above, where <u>Hashimoto</u>, <u>Smith</u>, <u>Ristelhueber</u> and <u>Shinohara</u> further teach the ADGPD comprising wherein at least one analog source is coupled to the analog data generating and processing device and is designed for either one-way or two-way communication (<u>Hashimoto</u>, Fig. 1A-1B; Fig. 8; Fig. 11-12; Fig. 14-

15; col. 1, II. 27-57; col. 3, I. 43 to col. 4, I. 67; col. 5, II. 43-57; col. 6, I. 16 to col. 9, I. 17; col. 9, I. 46 to col. 11, I. 42; col. 12, I. 16 to col. 14, I. 14; <u>Smith</u>, Fig. 2-5; col. 1, II. 9-22; col. 2, I. 40 to col. 3, I. 8; col. 3, II. 22-27; col. 3, II. 53-59; col. 4, II. 5-34; col. 6, II. 63-62; <u>Ristelhueber</u>, pages 1-3; and <u>Shinohara</u>, col. 1, II. 48-60; col. 3, I. 56 to col. 4, I. 49).

38. As per claim 366, <u>Hashimoto</u>, <u>Smith</u>, <u>Ristelhueber</u> and <u>Shinohara</u> teach all the of limitations claim 239 as discussed above, where <u>Hashimoto</u>, <u>Smith</u>, <u>Ristelhueber</u> and <u>Shinohara</u> further teach the ADGPD comprising wherein the analog data generating and processing device is designed so that the at least one aspect of operation is controlled by means of a configuration file (<u>Hashimoto</u>, Fig. 1A-1B; Fig. 8; Fig. 11-12; Fig. 14-15; col. 1, II. 27-57; col. 3, I. 43 to col. 4, I. 67; col. 5, II. 43-57; col. 6, I. 16 to col. 9, I. 17; col. 9, I. 46 to col. 11, I. 42; col. 12, I. 16 to col. 14, I. 14; <u>Smith</u>, Fig. 2-5; col. 1, II. 9-22; col. 2, I. 40 to col. 3, I. 8; col. 3, II. 22-27; col. 3, II. 53-59; col. 4, II. 5-34; col. 6, II. 63-62; <u>Ristelhueber</u>, pages 1-3; and <u>Shinohara</u>, col. 1, II. 48-60; col. 3, I. 56 to col. 4, I. 49) as the resulting combination of the references does teach/suggest the heart/core of applicant's invention, it would have been obvious for the resulting combination of the references to further teach the configuration file.

39. As per claim 367, <u>Hashimoto</u>, <u>Smith</u>, <u>Ristelhueber</u> and <u>Shinohara</u> teach all the of limitations claim 239 as discussed above, where <u>Hashimoto</u>, <u>Smith</u>, <u>Ristelhueber</u> and <u>Shinohara</u> further teach the ADGPD comprising wherein the analog data generating and processing device is designed to be responsive to a test unit ready command

(<u>Hashimoto</u>, Fig. 1A-1B; Fig. 8; Fig. 11-12; Fig. 14-15; col. 1, II. 27-57; col. 3, I. 43 to col. 4, I. 67; col. 5, II. 43-57; col. 6, I. 16 to col. 9, I. 17; col. 9, I. 46 to col. 11, I. 42; col. 12, I. 16 to col. 14, I. 14; <u>Smith</u>, Fig. 2-5; col. 1, II. 9-22; col. 2, I. 40 to col. 3, I. 8; col. 3, II. 22-27; col. 3, II. 53-59; col. 4, II. 5-34; col. 6, II. 63-62; <u>Ristelhueber</u>, pages 1-3; and <u>Shinohara</u>, col. 1, II. 48-60; col. 3, I. 56 to col. 4, I. 49).

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40. As per claim 369, Hashimoto, Smith, Ristelhueber and Shinohara teach all the of limitations claim 268 as discussed above, where Hashimoto, Smith, Ristelhueber and Shinohara further teach the ADGPD comprising wherein the input connector comprises a plurality of BNC inputs each coupled to the processor through a respective independently programmable amplifier, a multiplexer, and an analog to digital converter (Hashimoto, Fig. 1A-1B; Fig. 8; Fig. 11-12; Fig. 14-15; col. 1, II. 27-57; col. 3, I. 43 to col. 4, I. 67; col. 5, II. 43-57; col. 6, I. 16 to col. 9, I. 17; col. 9, I. 46 to col. 11, I. 42; col. 12, I. 16 to col. 14, I. 14; Smith, Fig. 2-5; col. 1, II. 9-22; col. 2, I. 40 to col. 3, I. 8; col. 3, II. 22-27; col. 3, II. 53-59; col. 4, II. 5-34; col. 6, II. 63-62; Ristelhueber, pages 1-3; and Shinohara, col. 1, II. 48-60; col. 3, I. 56 to col. 4, I. 49), as the resulting combination of the references does teach/suggest the heart/core of applicant's invention, it would have been obvious for the resulting combination of the references to further implement the heart/core of applicant's invention in an alternative embodiment on a device having the plurality of BNC inputs each coupled to the processor through the respective independently programmable amplifier, the multiplexer, and the analog to digital converter.

41. As per claims 370-376, as claims 370-376 are claiming the same invention as claims 239, 333-339, 341-344, 346-362, 364-367 and 369, the examiner will reject claims 370-376 base on the same rational as the rejection for claims 239, 333-339, 341-344, 346-362, 364-367 and 369.

42. Claims 340, 345 and 368 are rejected under 35 U.S.C. 103(a) as being unpatentable over <u>Hashimoto et al.</u> (US Patent 6,111,604) in view of <u>Hashimoto et al.</u> (US Patent 6,111,604) in view of <u>Smith et al.</u> (US Patent 5,634,075), <u>Ristelhueber : "Plug and play is almost here"</u> and <u>Shinohara</u> (US Patent 5,742,934) as applied to claim 239 above, and further in view of <u>Endo et al.</u> (US Patent 4,652,928).

<u>Hashimoto</u>, <u>Smith</u>, <u>Ristelhueber</u> and <u>Shinohara</u> teach all the limitations of claim 239 as discussed above, wherein <u>Hashimoto</u> further teaches the ADGPD comprising wherein the analog data generating and processing device configured to allow at least one analog source (<u>Hashimoto</u>, Fig. 8, ref. 1, 6, 9) to be attached thereto (<u>Hashimoto</u>, Fig. 8).

Hashimoto, Smith, Ristelhueber and Shinohara do not expressly teach the ADGPD comprising:

configured to allow at least one analog source to be detached therefrom;

the analog data generating and processing device is designed so that a user can attach at least one analog source thereto or detach the at least one analog source therefrom;

the respective independent analog acquisition channels are coupled to an input connector for detachably connecting to a plurality of analog sources.

Endo teaches the ADGPD (e.g. digital camera) comprising:

configured to allow at least one analog source to be detached therefrom (col. 1, ll. 18-25 and col. 13, ll. 57-58), by combining the coupling and de-coupling of the CCD with <u>Hashimoto</u>, <u>Smith</u>, <u>Ristelhueber</u> and <u>Shinohara</u>'s sensor coupled to the analog data generating and processing device, the resulting combination of the references further teaches the above claimed feature;

the analog data generating and processing device is designed so that a user can attach at least one analog source thereto or detach the at least one analog source therefrom (col. 1, II. 18-25 and col. 13, II. 57-58), by combining the coupling and de-coupling of the CCD with <u>Hashimoto</u>, <u>Smith</u>, <u>Ristelhueber</u> and <u>Shinohara</u>'s sensor coupled to the analog data generating and processing device, the resulting combination of the references further teaches the above claimed feature; and

the respective independent analog acquisition channels are coupled to an input connector for detachably connecting to a plurality of analog sources (col. 1, II. 18-25 and col. 13, II. 57-58), by combining the coupling and de-coupling of the CCD with <u>Hashimoto</u>, <u>Smith</u>, <u>Ristelhueber</u> and <u>Shinohara</u>'s sensor coupled to the analog data generating and processing device, the resulting combination of the references further teaches the above claimed feature.

It would have been obvious for one of ordinary skill in this art, at the time of invention was made to include <u>Endo</u>'s interchangeable sensor into <u>Hashimoto</u>, <u>Smith</u>, <u>Ristelhueber</u> and <u>Shinohara</u>'s sensor coupled to the processor for the benefit of adaptively increase the resolution of the camera to obtaining a better quality image (<u>Endo</u>, col. 1, II. 18-20) to obtain the invention as specified in claims 340, 345 and 368.

43. Claim 363 is rejected under 35 U.S.C. 103(a) as being unpatentable over <u>Hashimoto et</u> <u>al.</u> (US Patent 6,111,604) in view of <u>Smith et al.</u> (US Patent 5,634,075), <u>Ristelhueber : "Plug</u> <u>and play is almost here"</u> and <u>Shinohara</u> (US Patent 5,742,934) as applied to claim 329 above, and further in view of <u>Roberts et al.</u> (US Patent 5,576,757).

Hashimoto, Smith, Ristelhueber and Shinohara teach all the limitations of claim 329 as discussed above, wherein Hashimoto further teaches the ADGPD comprising wherein the digitized analog data is processed by the processor (Hashimoto, Fig. 1A-1B; Fig. 8; Fig. 11-12; Fig. 14-15; col. 1, II. 27-57; col. 3, I. 43 to col. 4, I. 67; col. 5, II. 43-57; col. 6, I. 16 to col. 9, I. 17; col. 9, I. 46 to col. 11, I. 42; col. 12, I. 16 to col. 14, I. 14).

<u>Hashimoto</u>, <u>Smith</u>, <u>Ristelhueber</u> and <u>Shinohara</u> do not expressly teach the ADGPD comprising performing a fast Fourier transform.

<u>Roberts</u> teaches a system and a method comprising an electronic still camera processing data by being subject to a fast Fourier transform (Abstract and col. 9, I. 60 to col. 10, I. 7).

It would have been obvious for one of ordinary skill in this art, at the time of invention was made to include <u>Roberts</u>'s fast Fourier transform into <u>Hashimoto</u>, <u>Smith</u>, <u>Ristelhueber</u> and <u>Shinohara</u>'s ADGPD for the benefit of having an easier computation for image processing while providing a reasonable visual fidelity (<u>Roberts</u>, col. 10, II. 1-3) to obtain the invention as specified in claim 363.

IV. PERTINENT PRIOR ART NOT RELIED UPON

Kerigan et al. (US Patent 5,948,091): Kerigan expressly shows that it is well known for camera type peripheral device to have plug and play functionality (col. 3, II. 29-33 and col. 6, II. 3-10)

V. CLOSING COMMENTS

Conclusion

a. STATUS OF CLAIMS IN THE APPLICATION

The following is a summary of the treatment and status of all claims in the application as recommended by **M.P.E.P. 707.07(i)**:

a(1) CLAIMS REJECTED IN THE APPLICATION

Per the instant office action, claims 239 and 333-374 have received a first action on the merits and are subject of a first action non-final.

b. DIRECTION OF FUTURE CORRESPONDENCES

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chun-Kuan (Mike) Lee whose telephone number is (571) 272-0671. The examiner can normally be reached on 8AM to 5PM.

IMPORTANT NOTE

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Alford Kindred can be reached on (571) 272-4037. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Chun-Kuan Lee/ Primary Examiner Art Unit 2181 October 04, 2010

Docket No.: 0757-112384 (PATENT)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of: Michael Tasler

Application No.: 11/467,092

Filed: August 24, 2006

Art Unit: 2181

For: ANALOG DATA GENERATING AND PROCESSING DEVICE HAVING A MULTI-USE AUTOMATIC PROCESSOR (as amended) Examiner: C. K. Lee

Confirmation No.: 3038

PRELIMINARY AMENDMENT

MS Amendment Commissioner for Patents P.O. Box 1450 Alexandria, VA 22313-1450

Dear Sir:

INTRODUCTORY COMMENTS

Please enter this amendment in response to the Office Action mailed from the USPTO on

October 28, 2009. A Notice of Appeal was filed on April 27, 2010. A Request for Continued

Examination and the required fee, and a petition and fee for a three month extension of time

are being filed herewith.

The Listing of the Claims begins on page 2 of this paper.

Remarks/Arguments begin on page 26 of this paper.

Claims:

1-238. (cancelled).

239. (currently amended) An analog data generating and processing device (ADGPD), comprising:

an input/output (i/o) port;

a program memory;

a data storage memory;

a processor operatively interfaced with the i/o port, the program memory and the data storage memory;

wherein the processor is adapted to <u>be involved in implement</u> a data generation process by which analog data is <u>generated acquired from each respective analog acquisition</u> <u>channel of a plurality of independent analog acquisition channels</u>, the analog data is processed <u>and</u> <u>digitized</u>, and the processed <u>and digitized</u> analog data is stored in the data storage memory as at least one file of digitized analog data;

wherein the processor also is adapted to be involved in an automatic recognition process in which, when the i/o port is operatively interfaced with a multi-purpose interface of a computer, the processor executes at least one instruction set stored in the program memory and thereby causes at least one parameter <u>identifying the analog data generating and processing</u> <u>device, independent of analog data source, as a digital storage device instead of as an analog data</u> <u>generating and processing device</u> to be automatically sent through the i/o port and to the multipurpose interface of the computer (a) without requiring any end user to load any software onto the computer at any time and (b) without requiring any end user to interact with the computer to set up a file system in the ADGPD at any time;

wherein the at least one parameter provides information to the computer about file transfer characteristics of the ADGPD; and

wherein the processor is further adapted to be involved in an automatic file transfer process in which, when the i/o port is operatively interfaced with the multi-purpose interface of the computer, and after the at least one parameter has been sent from the i/o port to the multipurpose interface of the computer, the processor executes at least one other instruction set stored in the program memory and-to thereby eauses- cause the at least one file of digitized analog data acquired from at least one of the plurality of analog acquisition channels to be transferred to the computer using a device driver for the digital storage device while causing the analog data generating and processing device to appear to the computer as if it were a digital storage device without requiring any user-loaded file transfer enabling software to be loaded on or installed in the computer at any time;

240. – 332. (cancelled).

333. (new) The analog data generating and processing device of claim 239 wherein the processor is configured to transmit to the computer active commands through the multipurpose interface to access a system bus of the computer to enable communication directly with other devices of the computer while bypassing the computer processor.

334. (new) The analog data generating and processing device of claim 239 wherein the at least one parameter identifies the analog data generating and processing device as a hard disk drive.

335. (new) The analog data generating and processing device of claim 239 further comprising at least one additional analog data generating and processing device coupled to the computer in parallel and each analog data generating and processing device attached to a difference analog data source.

336. (new) The analog data generating and processing device of claim 239

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wherein processor is configured to format the digitized analog data into blocks of data with block sizes suitable for a hard disk of the computer.

337. (new) The analog data generating and processing device of claim 239 further comprising a data buffer coupled to the processor to permit independence of time of data acquisition and data transfer to the host computer.

338. (new) The analog data generating and processing device of claim 239 wherein each of the plurality of analog acquisition channels are independently programmable and further comprise a plurality of corresponding sample and hold amplifiers for simultaneous sampling on the plurality of analog acquisition channels to permit simultaneous analog data acquisition from a plurality of respective analog data sources.

339. (new) The analog data generating and processing device of claim 333 wherein the active commands initiate active access to write data directly to a hard drive in the host computer independent of the host computer central processor.

340. (new) The analog data generating and processing device of claim 239 is configured to allow at least one analog source to be attached thereto and detached therefrom.

341. (new) The analog data generating and processing device of claim 239, wherein the analog data generating and processing device is attached directly to at least one analog source.

342. (new) The analog data generating and processing device of claim 239, wherein the analog data generating and processing device is a stand alone device.

343. (new) The analog data generating and processing device of claim 239, wherein the input/output port further comprises a SCSI interface circuit.

344. (new) The analog data generating and processing device of claim 335, wherein as least some of the analog data sources are analog data sources of different types.

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345. (new) The analog data generating and processing device of claim 239, wherein the analog data generating and processing device is designed so that a user can attach at least one analog source thereto or detach the at least one analog source therefrom.

346. (new) The analog data generating and processing device of claim 239, wherein the analog data generating and processing device is adapted to be interfaced with the multi-purpose interface of the computer by means of a cable.

347. (new) The analog data generating and processing device of claim 239, wherein at least one of the analog sources is a sensor that is operatively interfaced with the analog data generating and processing device and that is designed to generate the analog data.

348. (new) The analog data generating and processing device of claim 239 wherein the processor is configured to transmit to the computer active commands through the multipurpose interface to access a system bus of the computer to enable communication directly with other devices of the computer while bypassing the computer processor without requiring the user to load enabling software.

349. (new) The analog data generating and processing device of claim 239, wherein the plurality of analog acquisition channels are independently programmable.

350. (new) The analog data generating and processing device of claim 239, wherein at least one analog source is designed to receive data from a host device.

351. (new) The analog data generating and processing device of claim 239 wherein at least one analog source comprises a multimeter that is operatively interfaced with the analog data generating and processing device and that is designed to generate the analog data.

352. (new) The analog data generating and processing device of claim 239, wherein the at least one parameter is consistent with the analog data generating and

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processing device being responsive to a SCSI inquiry command.

353. (new) The analog data generating and processing device of claim 239, wherein the at least one parameter identifies the analog data generating and processing device as a digital mass storage device.

354. (new) The analog data generating and processing device of claim 239, wherein the processor is configured to, when the processor is operatively interfaced with the multi-purpose interface of the computer and after the at least one parameter has been sent to the multi-purpose interface of the computer, execute at least one set of computer code stored in program memory and thereby cause analog data generating and processing device file system information to be automatically sent to the multipurpose interface without requiring any end user to interact with the computer to set up a file system in the analog data generating and processing device at any time.

355. (new) The analog data generating and processing device of claim 354, wherein the analog data generating and processing device file system information comprises at least one indication of a file system type that is used to store the at least one file of digitized analog data in the data storage memory.

356. (new) The analog data generating and processing device of claim 239, wherein the at least one parameter is consistent with the analog data generating and processing device being a digital mass storage device other than a magnetic floppy disk drive.

357. (new) The analog data generating and processing device of claim 239,

wherein the processor is configured to cause, after the at least one parameter has been sent to the multipurpose interface, file allocation table information to be sent to the multipurpose interface,

wherein the processor is configured to cause a virtual boot sequence to be sent to the

multipurpose interface which includes at least information that is representative of a number of sectors of a storage disk, and

wherein the file allocation table information includes at least a start location of a file allocation table.

358. (new) The analog data generating and processing device of claim 357, further comprising the processor configured to implement a process to acquire digital data from at least one digital source.

359. (new) The analog data generating and processing device of claim 239, wherein the processor comprises a single digital signal processor.

360. (new) The analog data generating and processing device of claim 239, wherein the processor is configured to initiate a process by which digitized analog data are directly transferred to an input/output device.

361. (new) The analog data generating and processing device of claim 239, wherein the processor is configured to allow an aspect of operation of the analog data generating and processing device other than the transfer of at least some of the digitized analog data from the data storage memory to the multi-purpose interface to be controlled by means of an external computer.

362. (new) The analog data generating and processing device of claim 239, wherein the analog data generating and processing device comprises at least a portion of a medical device.

363. (new) The analog data generating and processing device of claim 239, wherein the digitized analog data is processed by the processor performing a fast Fourier transform.

364. (new) The analog data generating and processing device of claim 239, wherein the analog data generation and automatic file transfer at least partially overlap in

time.

365. (new) The analog data generating and processing device of claim 239 wherein at least one analog source is coupled to the analog data generating and processing device and is designed for either one-way or two-way communication.

366. (new) The analog data generating and processing device of claim 239, wherein the analog data generating and processing device is designed so that the at least one aspect of operation is controlled by means of a configuration file.

367. (new) The analog data generating and processing device of claim 239, wherein the analog data generating and processing device is designed to be responsive to a test unit ready command.

368. (new) The analog data generating and processing device of claim 239 wherein the respective independent analog acquisition channels are coupled to an input connector for detachably connecting to a plurality of analog sources.

369. (new) The analog data generating and processing device of claim 268 wherein the input connector comprises a plurality of BNC inputs each coupled to the processor through a respective independently programmable amplifier, a multiplexer, and an analog to digital converter.

370. (new) An analog data generating and processing device for acquiring analog data and for communicating with a host computer comprising:

a program memory;

a data storage memory;

a digital processor configured to interface to a multi-purpose interface of the host computer, the program memory, and the data storage memory;

an analog to digital converter operatively coupled to the digital processor and configured to acquire analog data from each respective analog acquisition channel of a plurality of analog

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acquisition channels, the analog to digital converter configured to convert the acquired analog data to digitized acquired analog data and to couple the digitized acquired analog data to the digital processor under control of the digital processor;

the digital processor configured to automatically generate and transmit to the host computer via the multipurpose interface an identification parameter which identifies the analog data generating and processing device to the host computer as a digital storage device but which is different than an analog data generating and processing device and independent of analog data source, and the processor communicating with the host computer through the multi-purpose interface as if the analog data generating and processing device were the digital storage device including transferring the digitized acquired analog data acquired from at least one of the analog acquisition channels, using a device driver present for a digital storage device in the host computer without requiring the user to load the device driver; and

wherein the digital processor is configured to transmit to the host computer active commands through the multipurpose interface to access a system bus of the host computer to enable communication directly with other devices of the host computer while bypassing the host computer processor without requiring the user to load enabling software.

371. (new) The analog data generating and processing device of claim 370, wherein the plurality of analog acquisition channels are independently programmable and further comprising a plurality of corresponding sample and hold amplifiers configured to simultaneously sample the plurality of analog acquisition channels.

372. (new) An analog data generating and processing device for acquiring analog data and for communicating with a host computer comprising:

a program memory;

a data storage memory;

a digital processor configured to interface to a multi-purpose interface of the host

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computer, the program memory, and the data storage memory;

an analog to digital converter operatively coupled to the digital processor and configured to simultaneously acquire analog data from each respective analog source of a plurality of analog sources on a respective one of a plurality of independent analog acquisition channels, the analog to digital converter configured to convert the acquired analog data to digitized acquired analog data and to couple the digitized acquired analog data to the digital processor under control of the digital processor;

the digital processor configured to automatically generate and transmit to the host computer via the multipurpose interface an identification parameter which identifies the analog data generating and processing device to the host computer as a digital mass storage device which is customary in host computers but which is different than an analog data generating and processing device and independent of the analog sources, and the processor communicating with the host computer through the multi-purpose interface as if the analog data generating and processing device were the digital mass storage device including transferring the digitized analog data acquired from at least one of the analog sources, using a device driver present for the digital mass storage device in the host computer without requiring the user to load the device driver.

373. (new) The analog data generating and processing device of claim 372, wherein the digital processor is configured to transmit to the host computer active commands through the multipurpose interface to access a system bus of the host computer to enable communication directly with other devices of the host computer while bypassing the host computer processor without requiring the user to load enabling software.

374. (new) An analog data generating and processing method for acquiring analog data and for communicating with a host computer comprising:

operatively interfacing an analog data device including a digital processor, a program memory and a data storage memory, to a multi-purpose interface of the host computer;

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acquiring analog data on each respective analog acquisition channel of a plurality of independent analog acquisition channels, converting the acquired analog data to digitized acquired analog data, and coupling the digitized acquired analog data to the digital processor under control of the digital processor;

automatically generating and transmitting to the host computer via the multipurpose interface an identification parameter which identifies the analog data generating and processing device to the host computer as a digital storage device but which is different than an analog data device, and independent of analog data source, and the analog data generating and processing device communicating with the host computer through the multi-purpose interface as if the analog data generating and processing device were the digital storage device including transferring the digitized acquired analog data acquired from at least one of the analog acquisition channels, using a device driver present for a digital storage device in the host computer without requiring the user to load the device driver.

375. (new) The analog data generating and processing method of claim 375, further comprising transmitting to the host computer, from the analog device, active commands through the multipurpose interface to access a system bus of the host computer to enable communication directly with other devices of the host computer while bypassing the host computer processor without requiring the user to load enabling software.

376. (new) The analog data generating and processing method of claim 374 wherein the plurality of analog acquisition channels are independently programmable and further comprising a plurality of corresponding sample and hold amplifiers configured to simultaneously sample a plurality of the plurality of analog acquisition channels.

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REMARKS

This amendment responds to the Office Action dated October 28, 2009 in conjunction with the RCE submitted herewith. A Notice of Appeal was filed on April 27, 2010 and the RCE has been filed herewith thereby abandoning the appeal. Reconsideration and further examination of the subject patent application in view of the accompanying Request for Continued Examination and in view of the present Amendment and the following Remarks is respectfully requested. Claims 1-238 were previously cancelled, and claim 239-332 were pending. Claim 239 has been amended, claims 1-238 and 240-332 have been cancelled, and new claims 333-376 have been added. All pending claims were rejected under 35 U.S.C.§103(a) as being unpatentable over the cited references Hashimoto (U.S. Pat. No. 6,111,604), Smith (U.S. Pat. No. 5,634,075), Ristelhueber ("Plug and Play is almost here"), Kerigan (U.S. Pat. No. 5,948,091), Endo (U.S. Pat. N. 4,652,928), Roberts (U.S. Pat. No. 5,576,757) and Shinohara (U.S. Pat. No. 5,742,934). After careful review of the claims and references, it is believed that the claims are in allowable form and a Notice of Allowance if respectfully requested.

In an effort to expedite the prosecution of this application, additional language has been added into all of the claims to further clarify the differences between them and the prior art. In particular, independent claim 239 and the new independent claims 370, 372 and 374 specify that analog data is acquired on a plurality of respective independent analog acquisition channels (see, e.g. paragraphs 0040 and 0043) and that the identifying parameter identifies the analog data generating and processing device as a digital storage device instead of as an the analog data

generating and processing device that it is (see e.g. paragraph 0017) In addition, claims 333, 339, 348, 370, 373, and 375 recite the processor enabled to communicate directly with other devices of the host computer while bypassing the host computer central processor (see e.g. paragraph 0053). New Claims 338, 349, 368, 369, 370-376 also includes other data acquisition features disclosed in paragraphs 0040 and 0043. These feature further distinguish the claims over the cited prior art.

It is respectfully submitted that, the claims as presented are distinguishable over any combination of the previously cited references (i.e. Hashimoto, Smith, Ristelhueber, Kerigan, Shinohara, Endo and Roberts). As such, it is respectfully submitted that the amended claim 239 and the new claims are patentable over all prior art of record.

The Office Action rejected most of the claims as obvious based on a combination of Hashimoto, Smith, Ristelhueber, Kerigan and Shinohara. The Office Action asserts that Shinohara teaches a system and a method comprising data transferring without requiring any user-loaded file transfer enabling software to be loaded on or installed in the computer at anytime at Col. 1 lines 48-60 and Col. 3, line 33 to Col. 4, line 49 (Final Office Action, p. 14, lines 3-18). The Final Office Action alleges that by combining the emulation of a mass storage device of Shinohara with the data transferring Plug and Play functionality of the combined other references, the resulting combination would teach this feature.

However, this is not the case because Shinohara merely describes an approach to extending the life of the flash memory in a flash disk drive. Shinohara at the cited Col. 1, line 48-60 merely describes a flash disk memory which can erase and write data in a unit sector of a flash memory to emulate a hard disk, where the host computer erases and writes a sector designated by the host computer so an address conversion table is not needed and also describes

a disk operating system. There is no mention of device drivers, no mention of not needing to load file transfer enabling software. Similarly Col. 3, line 33 to Col. 4, line 49 merely describe details of the flash disk which can cause the flash memory to last for a longer time using an address conversion table. However, nowhere in Shinohara is there any mention of transferring a file of digitized analog data without requiring any user loaded file transfer enabling software. Rather, the detailed description cited calls for the host computer to perform unique file management functions (Col. 4, lines 34-49) which would require data transfer software in the host computer to set up the disk emulation. Further, there is no teaching or mention of the disclosed disk emulator being able to transfer data without data-transfer software loaded on the host computer. The Shinohara reference is devoid of any such teaching. Thus, Shinohara does not teach the feature of transferring digitized analog data without requiring any user loaded file transfer enabling software.

The Final Office Action also asserts that combining the device of Shinohara with the Plug and Play functionality of the other references such as Smith, teaches this feature. (Plug and Play refers to ISA PnP system bus technology referred to in the Smith and Ristelhueber reference) However, Plug and Play is concerned only with allocation of the resources of the host computer to avoid conflicts between resources within the host computer. Thus, the Plug and Play process does not need to recognize the peripheral, it only needs to determine what resources of the host computer the peripheral needs. In Plug and Play, the host computer reads the resource requirements from each attached peripheral, such resources as i/o addresses, interrupts levels, and DMA channels, (see, Smith, Col. 3, lines 1-4; also see Plug and Play ISA Specification, Version 1.0a, May 5, 1994 ("Plug and Play Specification") p.1, abstract, line 5, and lines 9-11). The computer then assigns to each peripheral device the necessary resources

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so as to avoid resource conflicts (see Smith, Col. 4, lines 25-32; and Plug and Play Spec. p.1, lines 11-12). Once the host computer has assigned its resources and activated the device, an appropriate device driver must then be loaded to permit operation. As described in Smith, Col. 4, lines 26-33 in a PnP (Plug and Play) system:

"...the operating system will isolate each PNP device, assign a 'handle' (number) to each card, and read the resource data from that card. Once each card had been isolated, assigned a handle and read, the operating system software will arbitrate system resources for all PNP devices. Conflict-free resources may then be assigned and the devices activated. Finally, appropriate device drivers may be loaded and the system thus configured."

Also see Plug and Play Spec. p.1, Abstract, and Smith, Col. 3, lines 52-59. The Plug and Play process thus does not eliminate the need to supply a driver but rather calls for loading the driver after the system resources are allocated and the devices activated. The Plug and Play standard does not address device drivers other than the fact that one is needed. (Plug and Play Specification p. 1 Abstract: "However, user interface issues for installation of device drivers are not addressed".) Thus, even with Plug and Play, a device specific driver is still needed for each peripheral installed in the Plug and Play computer system in order for the peripheral's processor to execute an instruction to automatically transfer a file of digitized analog data to the computer from the peripheral device. This is clearly demonstrated by the Smith reference and the Plug and Play Specification document. Applicant has also submitted numerous other prior art references during prosecution which further demonstrate that Plug and Play requires loading a device driver after resource allocation is performed. Thus, neither Shinohara nor the Plug and Play functionality disclosed in the other cited references teach data transfer without a user loaded driver.

In addition, the device described in Shinohara is merely a memory for storage of digital

data by a host computer and for retrieval of that data by the host computer, and thus is not suitable for receiving analog data from a source independent of the host computer nor for transferring acquired digitized analog data to a host computer. Further, Shinohara does not teach transferring the acquired analog data while causing the analog data generating and processing device to appear to the computer as a digital storage device, as claimed. The Shinohara device has one port that merely receives and stores digital data from the computer and allows that same computer to retrieve that stored data through the same port. The claimed invention has two separate ports providing input of analog data on one port and subsequent transfer of digitized analog data to a computer on another port. Thus, the disk memory emulation of Shinohara is dramatically different from the claimed invention and not compatible with or combinable with Hashimoto to obtain the claimed invention.

Stated another way, at most Shinohara merely teaches that a digital memory device having a single read/write port such as a flash memory, may be configured to emulate another digital memory device. This does not teach and is not related to an analog data acquisition device having both an analog input and a host computer interface port which can emulate a hard disk. Thus, the combination of Shinohara with the other references does not teach or suggest the claimed automatic file transfer of acquired digitized analog data without requiring user loaded file transfer enabling software. Indeed, there is nothing to suggest the advantage of not requiring user loaded file transfer enabling software in any device, let alone in an analog data acquisition device.

Accordingly, it is respectfully submitted that all the pending claims are distinguishable over the cited references because none of the references teaches the claimed transfer of a file of acquired digitized analog data by an analog generating and processing device while appearing

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to be a digital mass storage device without loading file transfer enabling software. That is, even if all the references could somehow be combined (which they cannot, as explained hereinafter), the result would still not meet the combined limitations of the claims.

The Office Action also asserts that Hashimoto teaches an "automatic recognition" feature, and therefore allegedly requires no user-loaded software. However, Hashimoto does not describe an automatic recognition process, or the processor automatically sending an identification parameter. Rather, Hashimoto describes a camera circuit in which a processor 23 detects proper connection to a host personal computer interface by monitoring the data terminal ready (DTR) signal of the RS-232 connection or another signal of similar function of another user selected communications protocol (Hashimoto, Col. 10, lines 44-65; Fig. 4). When the signal from the computer communication interface is detected, a communication algorithm is set up in the camera to prepare the camera to transmit or receive information. Then the camera system detects whether a switch on the camera has been set to transmit or to receive to determine whether to transmit image data or receive (Hashimoto, Col. 15, lines 3-16). Thus, Hashimoto merely describes a process for detection of a connection to a computer by monitoring for a signal from the computer. This detection process is not the recognition process claimed in which the processor automatically sends identification information to the host computer, rather, it merely detects a proper connection to the computer interface. There is no description anywhere in Hashimoto of an automatic recognition process. Further, there is no description anywhere in Hashimoto of any process that sends an identification parameter to the host computer, automatically or otherwise.

Similarly, none of the other references disclose a processor in the peripheral device in an automatic recognition process which automatically sends an identification parameter to the

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host computer. The Final Office Action concedes that Hashimoto does not teach identification information automatically sent as claimed, but asserts that Smith teaches an "automatic recognition process wherein at least one parameter is automatically sent through the i/o port by combining Hashimoto's "automatic recognition process with Smith's Plug and Play functionality. However, not only does Hashimoto not disclose automatic recognition as discussed above, but Smith also fails to disclose automatic recognition and automatically sending identification information. Smith describes Plug and Play systems as requiring the Plug and Play host computer to assign a "handle" (i.d. number) to each peripheral card and then the host computer reads resource data from the peripheral (see, e.g. Col. 4, lines 26-34; Col. 3, lines 41-59). Thus, the host computer in Smith assigns an identifying number rather than the peripheral processor automatically sending identification information. Then the host computer reads resource data from the peripheral (Smith, Col. 4, lines 26-28: "the operating system will isolate each PnP device assign a "handle" (number) to each card, and read the resource data from that card"). There is no description of automatic sending of identification data. The Plug and Play process described in Smith or any other of the references is not concerned with recognizing the device. It is not a device recognition process, rather it is a host computer resource allocation process. The host computer after supplying an i.d. merely performs a process of reading resource data and then allocating its resources. There is no mention of identification information being read or sent. The cited passages of Smith do not even mention a peripheral processor automatically providing identification information to the host computer. Instead, the host computer initiates a "read" function to obtain only resource data from the peripheral.

Smith also does not describe a peripheral having a processor involved in the Plug and

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Play process. The only Plug and Play peripheral device circuitry is shown in Figs. 6, 7, and 9 which show a circuit made up of registers, flips flops, etc. to allow the peripheral to configure upon power up to operate in legacy mode or plug or play mode. There is no peripheral processor described involved in automatic recognition of the peripheral.

The Office Action further asserts that the combination of the Plug and Play functionality of Smith with Hashimoto's automatic recognition process results in teaching an automatic recognition process corresponding to configuring a Plug and Play system utilizing ROM BIOS having the operating system load the device driver after the peripheral device is coupled to the host PC for installation. However, saying that the ROM BIOS of the computer loads the device driver does not teach or relate in any way to the ADGPD processor automatically sending identifying information. Further, the loading of the device driver occurs after the peripheral device has been assigned resources and activated, and requires that a device driver then be provided. Thus, the Plug and Play functionality of Smith is also contrary to the claim feature calling for not requiring any user-loaded file transfer enabling software to be installed in the computer at any time, and this would include any special software driver.

The Final Office Action also suggests that the combination of Smith's Plug and Play functionality into Hashimoto's "automatic recognition" would be obvious to one of ordinary skill in the art because it would simplify the installation for the user without the need to install software or configure the peripheral devices. However, as we have seen, Smith expressly teaches the contrary, that a device driver must be loaded once the peripherals have been set up and host computer resources assigned (see e.g., Smith, Fig. 2, ref. 126 and Col. 4 lines 32-33).

Further, the Plug and Play functionality of Smith is functionality which is primarily located in the host computer not the peripheral. The Plug and Play compatibility as

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implemented in the peripheral in Smith is merely a set of logic gates and registers (not a processor) to give the peripheral compatibility with the Plug and Play functionality of the host computer. Plug and Play functionality calls for the host computer to configure its resources according to the needs of all the peripherals attached to it and thus primarily concerns software or firmware supplied functions located in the host computer. Thus, it would not make sense to one skilled in the art to put these Plug and Play functions into the peripheral device which would have no use for them. The peripheral device is only going to connect to a host computer and thus does not need to allocate its resources to handle multiple Plug and Play devices. In addition, as discussed above, neither Hashimoto nor Smith teach automatically sending identification information.

The Final Office Action does not assert that Kerigan, Ristelhueber or Shinohara disclose a processor of the peripheral device in an automatic recognition process which automatically sends an identification parameter to the host computer. Kerigan merely describes a digital display interface with no disclosure of a peripheral processor, or of the processor automatically sending identification information in an automatic identification process. Similarly, Ristelhueber provides a very generic description of Plug and Play, but does not disclose a processor of a peripheral in an automatic recognition process or the processor automatically sending identification information. Shinohara merely describes a flash disk drive and thus also does not mention a processor of the peripheral device involved in an automatic recognition process or the processor automatically sending an identification parameter to a host computer. Accordingly, all pending claims are distinguishable over the combination of the cited references because none of the references teaches the claimed automatic recognition process.

The Final Office Action asserts that Ristelhueber describes a peripheral device having

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an automatic recognition process without requiring any end user to load any software on the computer at anytime. Ristelhueber is a non-technical buyer magazine article which generically describes a coming Plug and Play standard with an enthusiastic description of the future ("In about a year the key standard and specifications will be in place to make PnP a reality", p. 1, paragraph 3). Ristelhueber is relied upon for disclosure of Plug and Play functionality. The Final Office Action appears to rely on vague predictions in Ristelhueber regarding recognition of new hardware, and configuring of hardware to relieve the user of the need to fumble with floppy disks and user manuals to get the device up and running. However, when read in context these phrases are predicting PnP will recognize that a new device is connected. The author is not describing recognizing what peripheral is attached, only whether there is a peripheral attached to the port. Further, there is no enabling disclosure of how such recognition would one day be implemented. The description in Ristelhueber is just an over enthusiastic prediction of the hoped for goals for PnP, which is to detect when a new device is attached (i.e. identifying presence not what it is), configure the host computer resources to accommodate it, and then activate the device. However, Ristelhueber nowhere discusses or even mentions device drivers, or what will happen after a device is configured and activated. As discussed herein above, the Smith reference and the PnP Standards Specification make clear that a device driver is still needed after the peripheral has been detected, assigned resources and activated in accordance with Plug and Play.

Further, there is no teaching of the processor of the peripheral (i.e. the ADGPD) automatically sending identification information to the computer, or of anything done or not done by a processor of a Plug and Play peripheral device. It merely describes the host computer determining the presence of a peripheral device, identifying the resources needed by

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the peripheral device and configuring its hardware thereby relieving the user from having to do so. There is no teaching in Ristelhueber to relieve the user from having to load a device driver. There is no mention of a processor on the peripheral, and no mention of the need or lack of need for user loaded software on the host computer. Thus, Ristelhueber does not disclose this claimed feature. Rather, Ristelhueber merely broadly describes Plug and Play without discussing device driver software for proper functioning of the peripheral after it is activated. As discussed above, the Plug and Play still requires loading a device driver after the peripheral device has been activated using a Plug and Play process. Thus, Ristelhueber does not teach a peripheral device which doesn't require an end user to load software onto the computer at anytime and none of the other cited references teach this feature. Therefore, all pending claims are distinguishable over the cited references on this ground as well.

All the claims similarly call for the processor in an automatic recognition process to automatically send identification information which identifies the analog data generating and processing device as a digital storage device instead of as an analog data generating and processing device without requiring any end user to interact with the computer to set up a file system at any time.

The Office Action asserts that Shinohara discloses this feature. Shinohara describes a flash disk drive which couples only to a host computer to allow the host computer to send data for storage and retrieve the data stored by the host computer. This is entirely different from the claimed analog data generating and processing device which receives data from an analog source, and provides for transfer of the digitized analog data to a separate host computer. Therefore, the environment and functionality, and the problems to be resolved are completely different, and it would thus not be obvious to combine the Shinohara flash disk drive features

with Hashimoto, and because of these fundamental differences, Shinohara is not compatible with Hashimoto. Moreover, the combination (even if considered somehow together) still would not end up meeting the terms of the claims. Shinohara merely describes how the host computer sends data and sets up the data structure in the flash disk drive but does not teach or even mention that there is no need for user interaction to set up a file system or that an analog data generating and processing device is identified instead as a digital mass storage device. Shinohara is merely a mass storage device being a mass storage device. Further, the data structure set up would require software on the host computer to perform these set-up functions. Thus, additional software must be added to the host computer to set up the data structure for the flash drive.

Further, since Shinohara is merely a hard disk emulator connected to a computer, it cannot cause an acquired file of digitized analog data acquired from a analog source to be transferred (i.e., there is only digital data stored by the host computer).

Since Hashimoto, Smith, Kerigan, and Ristelhueber do not teach the automatic identification process identifying an analog generating and processing device as a digital storage device or doing so without requiring any end user to interact with the computer to set up a file system in the ADGPD, and Shinohara also does not teach this feature, all pending claims are distinguishable over the cited references.

Further, none of the references disclose a device which acquires and processes analog data but operates and identifies itself as a digital storage device. Shinohara discloses a mass storage device (i.e. a flash memory) which operates as a mass storage device. This teaching of Shinohara does not suggest to one of ordinary skill in the art the operation and identification of an analog generating and processing device as an entirely different type of device, i.e. a mass

storage device, and does not suggest a device which sends an identifying parameter to the host computer identifying the device as a device of dramatically different type than what it actually is. Thus the claims are further distinguishable over the cited references for this reason in addition to the reasons discussed herein above.

In addition to the lack of disclosure of the claimed feature discussed hereinabove, Hashimoto and Smith are incompatible and cannot be properly combined. As previously discussed, Hashimoto detects that it is properly connected to a host computer interface by monitoring for a DTR signal. Until the DTR signal is detected the power to the communication circuitry is turned off or in standby mode (Hashimoto, Col. 12, lines 62 to Col. 13, lines 8). After detecting the proper connection and activating the communication circuitry, Hashimoto checks a switch 110 which is manually set by the camera user, to determine whether it is in the transmit mode or is in a receive mode. (Hashimoto, Fig. 14, Ref. No. 308; Col. 10, lines 51-54 and Col. 11, lines 7-13). Thus, at any point in time, the Hashimoto camera is enabled to only transmit, or only receive; it is not enabled to do both. The user must manually switch between modes. Smith, however, describes a Plug and Play process which requires the host computer to read resource data from the PnP peripheral device (see e.g. Smith, Col. 3, lines 41-43; Col. 4, lines 25-28). This read function requires the peripheral to receive a read request, which would include an address, and then requires the peripheral to transmit the resource data to the host computer. Thus, Smith's Plug and Play (and PnP in general) cannot be added to Hashimoto because the Hashimoto camera cannot both transmit and receive data at any one moment. If the mode switch in the Hashimoto camera is in the transmit position, then the camera would not be able to receive the read request and address, and if the mode switch is in the receive position, the camera would not be able to transmit the resource data. Thus, Hashimoto and Smith, are

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incompatible and cannot properly be combined. This is also true of Plug and Play in general.

The combination of Hashimoto and Shinohara is also improper. Hashimoto describes an electronic camera while Shinohara describes a flash disk drive. The Final Office Action combines Shinohara with Hashimoto by converting the Hashimoto camera to a disk drive emulator, thereby dramatically changing the fundamental structure, operation, and purpose of Hashimoto. Shinohara is merely a digital memory device having a single port to receive digital data from a computer for storage and to allow the same computer to retrieve that data through the same port. In other words, Shinohara merely teaches that a single port digital memory device can be configured to emulate a hard disk. This does not teach or suggest an analog data acquisition device having both an analog input and a separate host computer interface port emulating a hard disk. Thus, the combination requires improper hindsight and therefore, Hashimoto and Shinohara cannot be properly combined.

In addition, as discussed above, Hashimoto operates in a transmit only mode or a receive only mode selected by the user with a mode selection switch. However, to function properly the Shinohara flash disk requires the host computer to read data from it. This is incompatible with Hashimoto one way communication, because the read function requires that the flash memory receive a read request with the address or sectors of the data requested, followed by an immediate transmission of the data. Hashimoto's one way communication would prevent this two way exchange. Thus, Shinohara is incompatible and not properly combinable with Hashimoto for this reason as well.

The combination requires hindsight assumptions about the disclosures in the references. The Final Office Action improperly presumes that the processor of Hashimoto (item 23 in Figure 8) is adapted to be involved in an "automatic file transfer process" and, therefore,

purportedly requires no added software. The following portion of Hashimoto was cited to provided to support this proposition:

"The digital images captured by the camera are used to create exposure controlling evaluation information, automatic focus controlling information, and automatic white balance evaluation information by the CPU 23. Automatic control of the camera is performed using this information." (Hashimoto, col. 7, lines 50-55).

Hashimoto discloses that a camera can be controlled in a manual and non-automatic fashion by an end user manipulating the camera control buttons, and that a camera can be controlled by its CPU. The "automatic control" of Hashimoto's camera, therefore is control of the camera sensor accomplished by means of a computer (CPU) which is part of the camera circuitry. However, there is no disclosure of automatic file transfer of digitized acquired analog data to a host computer without requiring user-loaded file transfer software, as recited by the instant claims.

In view of the foregoing, applicant submits that claims 239, and 333-376 are not obvious over Hashimoto in view of the combined teachings of Smith, Ristelhueber, Kerigan, Roberts, Endo and Shinohara. Accordingly, applicant respectfully submit that the instant application is in condition for allowance, and a Notice of Allowance is respectfully requested. Should the Examiner be of the opinion that a telephone conference would expedite prosecution of the subject application, the Primary Examiner is respectfully requested to call the undersigned at the below-listed number.

The Commissioner is hereby authorized to charge any additional fee which may be required for this application under 37 C.F.R. §§ 1.16-1.18, including but not limited to the extension of time fee, RCE fee, petition fee, extra claims fee, the issue fee, or credit any overpayment, to Deposit Account No. 23-0920. Should no proper amount be enclosed herewith, as by a check being in the wrong amount, unsigned, post-dated, otherwise improper

or informal, or even entirely missing, the Commissioner is authorized to charge the unpaid amount to Deposit Account No. 23-0920.

Respectfully submitted,

HUSCH BLACKWELL WELSH KATZ

James a. S. Leen By: James A. Scheer

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Dated: September 24, 2010

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	'ed States Patent a	and Trademark Office	UNITED STATES DEPAR United States Patent and Address: COMMISSIONER F P.O. Box 1450 Alexandria, Virginia 22: www.uspto.gov	OR PATENTS
APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/467,092	08/24/2006	Michael Tasler	31436/43993	3038
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Jeffrey W. Salmon, Esq. Marshall Gerstein & Borun LLP 233, South Wacker Drive, Suite 6300 Chicago, IL 60606			LEE, CHUN KUAN	
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			10/28/2009	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

	Application No.	Applicant(s)				
	11/467,092	TASLER, MICHAEL				
Office Action Summary	Examiner	Art Unit				
	Chun-Kuan Lee	2181				
The MAILING DATE of this communication appears on the cover sheet with the correspondence address Period for Reply						
 A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>3</u> MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION. Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication. If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication. Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b). 						
Status						
1) Responsive to communication(s) filed on 31 A	ugust 2009.					
2a) This action is FINAL . $2b)$ This action is non-final.						
closed in accordance with the practice under <i>Ex parte Quayle</i> , 1935 C.D. 11, 453 O.G. 213.						
Disposition of Claims						
 4) Claim(s) <u>239-332</u> is/are pending in the application. 4a) Of the above claim(s) <u>265,273,278,280,282,309-311 and 317</u> is/are withdrawn from consideration. 						
5) Claim(s) is/are allowed.						
6)⊠ Claim(s) <u>239-264,266-272,274-277,279,281,2</u>	83-308.312-316 and 318-332 is/a	re rejected.				
7) Claim(s) is/are objected to.						
8) Claim(s) are subject to restriction and/c	r election requirement.					
Application Papers						
9) The specification is objected to by the Examine	er.					
10)⊠ The drawing(s) filed on <u>08/24/2006 & 08/31/2009</u> is/are: a)⊠ accepted or b)⊡ objected to by the Examiner.						
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).						
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).						
11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.						
Priority under 35 U.S.C. § 119						
12)⊠ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).						
a)⊠ All b)⊡ Some * c)⊡ None of:						
1. Certified copies of the priority documents have been received.						
2. Certified copies of the priority documents have been received in Application No. <u>09/331,002</u> .						
3. Copies of the certified copies of the priority documents have been received in this National Stage						
application from the International Bureau (PCT Rule 17.2(a)).						
* See the attached detailed Office action for a list of the certified copies not received.						
Attachment(s)						
1) □ Notice of References Cited (PTO-892) 4) ☑ Interview Summary (PTO-413)						
2) Notice of Draftsperson's Patent Drawing Review (PTO-948)						
3) Information Disclosure Statement(s) (PTO/SB/08) 5) Notice of Informal Patent Application Paper No(s)/Mail Date 09/02/2009. 6) Other:						
U.S. Patent and Trademark Office						
	ction Summary Pa	rt of Paper No./Mail Date 20091023				

DETAILED ACTION

RESPONSE TO ARGUMENTS

1. Applicant's arguments filed 08/31/2009 have been fully considered but they are not persuasive. Currently claims 1-238 are cancelled, and claims 239-332 are pending.

2. In response to applicant's plurality of arguments, every argument seems to be directed towards to that the combination of references (i.e. <u>Hashimoto</u>, <u>Smith</u>, <u>Kerigan</u>, <u>Ristelhueber</u> and <u>Shinohara</u>) does not teach/suggest the novelty of the claimed invention; applicant's arguments have fully been considered, but are not found to be persuasive

The examiner respectfully disagrees, because in accordance to applicant's disclosure that the core novelty of the claimed invention is as following:

"... the ability for a peripheral device to implement plug-and-play functionality when connected with computers of different manufacturers ... " for example "... connecting a camera peripheral device to a computer of any manufacturer, the computer by the corresponding manufacturer would then inquire what the connected camera peripheral device is, the connected camera peripheral device then responded to the computer by the corresponding manufacturer that "I am a mass storage device", and then the computer utilize computer's mass storage device driver to communicate with the connected camera peripheral device. Therefore the connected camera peripheral device (e.g. HP Camera) will work with any computer irrespective of computer

manufacturer (e.g. Acme, Compaq, Toshiba), as the connected camera peripheral device is emulating the mass storage device ..."

Wherein the examiner relined on the references as following for the teaching of the core novelty of the instant claimed invention:

<u>Hashimoto</u> teaches connecting a camera peripheral device to a computer and the computer communicating with the connected camera peripheral device.

<u>Smith</u>, <u>Kerigan</u>, and <u>Ristelhueber</u>'s plug-and-play functionality in combination with <u>Hashimoto</u>'s camera peripheral device further teaches the computer inquires the connected camera peripheral device, in order to receive a response from the connected camera peripheral device, such that the computer can identify what peripheral device is connected and utilize the corresponding driver to communicate with the connected camera peripheral device; wherein the motivation to combine the plug-and-play functionality with <u>Hashimoto</u>'s camera peripheral device is for the benefit of simplifying the installation of the peripheral device for the user as the peripheral device may be installed without the need for the user to install software or configure the peripheral device.

<u>Shinohara</u>'s hard disk drive emulation in combination with <u>Hashimoto</u>, <u>Smith</u>, <u>Kerigan</u>, and <u>Ristelhueber</u>'s plug and play camera peripheral device with a memory card further teaches connecting the camera peripheral device to a computer of any manufacturer, and when the connected camera peripheral device is inquired by the computer, responds that "I am a mass storage device" (e.g. via hard disk drive emulation), then the computer utilize computer's mass storage device driver to

communicate with the connected camera peripheral device for accessing data in the memory card; wherein the motivation to combine the hard disk drive emulation with <u>Hashimoto</u>, <u>Smith</u>, <u>Kerigan</u>, and <u>Ristelhueber</u>'s plug and play camera peripheral device is for the benefit of expanding the lifetime usage of the memory card.

In summary, the combination of <u>Hashimoto</u>, <u>Smith</u>, <u>Kerigan</u>, <u>Ristelhueber</u> and <u>Shinohara</u> does teach the claimed invention of "a peripheral device to implement plugand-play functionality when connected with computers of different manufacturers" as the plug and play camera peripheral device emulates a hard disk drive.

3. In response to applicant's arguments regarding <u>Kerigan</u>'s disclosure is associated with video application, and lack specific recitation of the term "digital still camera," <u>Kerigan</u>'s disclosure would obviously not refer to <u>Hashimoto</u>'s digital still camera, and would be known today as a "web cam"; applicant's arguments have fully been considered, but are not found to be persuasive.

The examiner respectfully disagrees, because <u>Hashimoto</u>'s digital still camera is also utilized for video application (<u>Hashimoto</u>, col. 3, I. 43 to col. 4, I. 12), and the examiner is not fully clear as to where in <u>Kerigan</u> teaches a "web camera". Furthermore, as explained in the previous office action, the examiner is relying on <u>Kerigan</u> only to expressly demonstrate the prior art utilization of the plug and play functionality with camera type peripheral device is well known; and relying on <u>Hashimoto</u>, <u>Smith</u>, <u>Kerigan</u>, <u>Ristelhueber</u> and <u>Shinohara</u>, not <u>Kerigan</u> along, to demonstrate the claimed invention.

4. In response to applicant's arguments that the combination of the references would change the fundamental of <u>Hashimoto</u> because <u>Hashimoto</u>'s CPU is only suppose to be "monitoring" for the DTR signal; applicant's arguments have fully been considered, but are not found to be persuasive.

The examiner respectfully disagrees, because the examiner is not clear as to where in <u>Hashimoto</u> teaches the CPU cannot be utilized for implementing plug-and-play functionality; and, considering <u>Hashimoto</u>'s CPU is a lot more powerful (e.g. capable of controlling a plurality of operation in the camera) then just monitoring for a signal, the combination of the references does teach/suggest <u>Hashimoto</u>'s CPU implementing plug-and-play functionality. Additionally, by combining the references to implement the plug-and-play camera, the plug-and-play camera include interfacing means, other then "monitoring" for the DTR signal, to the computer.

5. In response to applicant's arguments regarding that the combination of the reference still require user-loaded software, because according to PNP specification "user interface issues for installation of the device driver are not addressed"; applicant's arguments have fully been considered, but are not found to be persuasive.

The examiner respectfully disagrees, because PNP specification's disclosure teaches that user interface issues for installation of the device driver are not address, wherein "not addressed" is not equivalent to "required;" additionally <u>Ristelhueber</u> does teach/suggest installation of peripheral device without user-loaded software (<u>Ristelhueber</u>, pages 1-3).

6. In response to applicant's arguments that the examiner fail to consider the teaching of prior art (i.e. Canon Powershot 600 and Ricoh RDC-2 digital still cameras, manual for US Robotics Sportster Voice Modem, SyQuest's Removable Cartridge Hard Disk Drive, Iomega Zip 100 Parallel Port Drive, and NEC's PowerMate V486) that contradicts the examiner's position regarding plug-and-play functionality (i.e. Canon Powershot 600 and Ricoh RDC-2 digital still cameras, manual for US Robotics Sportster Voice Modem, SyQuest's Removable Cartridge Hard Disk Drive, Iomega Zip 100 Parallel Port Drive, and NEC's PowerMate V486) that contradicts the examiner's position regarding plug-and-play functionality (i.e. Canon Powershot 600 and Ricoh RDC-2 digital still cameras, manual for US Robotics Sportster Voice Modem, SyQuest's Removable Cartridge Hard Disk Drive, Iomega Zip 100 Parallel Port Drive, and NEC's PowerMate V486 suggest the need for a user-loaded software).

The examiner does give full weight to each of the prior art provided by the applicant, but none of the prior art (i.e. Canon Powershot 600 and Ricoh RDC-2 digital still cameras, manual for US Robotics Sportster Voice Modem, SyQuest's Removable Cartridge Hard Disk Drive, lomega Zip 100 Parallel Port Drive, and NEC's PowerMate V486) discloses the plug-and-play functionality requiring the user-loaded software is enabled by the prior art (i.e. <u>Hashimoto</u>, <u>Smith</u>, <u>Kerigan</u>, <u>Ristelhueber</u> and <u>Shinohara</u>) cited by the examiner, such as stated in the prior art (i.e. Canon Powershot 600 and Ricoh RDC-2 digital still cameras, manual for US Robotics Sportster Voice Modem, SyQuest's Removable Cartridge Hard Disk Drive, lomega Zip 100 Parallel Port Drive, and NEC's PowerMate V486) provided by the applicant that the plug-and-play functionality is implement via the examiner's cited prior art (i.e. <u>Hashimoto</u>, <u>Smith</u>, <u>Kerigan</u>, <u>Ristelhueber</u> and <u>Shinohara</u>).

7. In response to applicant's arguments corresponding to Baker, 15 UNIX review 13 corresponding to "plug and play" having known problems and probable inoperability; applicant's arguments have fully been considered, but are not found to be persuasive.

The examiner respectfully disagrees, as the examiner is not fully clear in regards to applicant's argument, because the applicant did not fully cite in the arguments exactly what is stated by Baker, 15 UNIX review 13, therefore, the examiner is unable to properly respond to applicant's arguments.

I. ACKNOWLEDGEMENT OF REFERENCES CITED BY APPLICANT

8. The Information Disclosure Statement(s) has been reviewed by the examiner and is found to comply with the provisions of 37 CFR 1.97, 1.98 and MPEP § 609.

II. ELECTION/RESTRICTIONS

9. Newly submitted claims 239-332 directed to an invention that is independent or distinct from the invention originally claimed for the following reasons:

This application contains claims directed to the following patentably distinct species of the claimed invention:

Specie I: Claims 239-264, 266-272, 274-277, 279, 281, 283-308, 312-316, and 318-332 are directed to an ADFPD having a plug-and-play functionality.

Specie II: Claim 265 is directed to an ADFPD forming a multimeter.

Specie III: Claim 273 are directed to an ADFPD located within an interior of a housing of a personal computing device.

Specie IV: Claim 278 is directed to an ADFPD having temporary memory.

Specie V: Claim 280 is directed to an ADFPD having random access memory.

Specie VI: Claim 282 is directed to an ADFPD having electronically

programmable read only memory.

Specie VII: Claims 309-311 are directed to various timing of ADFPD's analog data generation.

Specie VIII: Claim 317 is directed to an ADFPD having a configuration file.

Since applicant has received an action on the merits for the originally presented invention, this invention has been constructively elected by original presentation for prosecution on the merits. Accordingly, claims 265, 273, 278, 280, 282, 309-311, and 317 are withdrawn from consideration as being directed to a non-elected invention. See 37 CFR 1.142(b) and MPEP § 821.03.

III. OBJECTIONS TO THE CLAIMS

10. Claims 329 is objected to because of the following informalities:

in claim 329, line 40, "... analog data to be transferred to the first computer ..." should be replaced with -... analog data to be transferred to the <u>second</u> computer ...-;

Please note that the request for the replacements as stated above is for the purpose to improve the clarity of the claim language. Appropriate correction is required.

IV. REJECTIONS BASED ON PRIOR ART

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

11. Claims 239-248, 252-256, 258, 261-264, 266-272, 274-277, 279, 281, 283-306,

308, 312-316, and 318-332 are rejected under 35 U.S.C. 103(a) as being unpatentable over <u>Hashimoto et al.</u> (US Patent 6,111,604) in view of <u>Smith et al.</u> (US Patent 5,634,075), <u>Kerigan et al.</u> (US Patent 5,948,091), <u>Ristelhueber : "Plug and play is almost here"</u> and <u>Shinohara</u> (US Patent 5,742,934).

12. As per claim 239, <u>Hashimoto</u> teaches an analog data generating and processing device (ADGPD), comprising:

an input/output (i/o) port (Fig. 1A-1B; Fig. 8; col. 1, II. 35-57; col. 3, I. 43 to col. 4,

I. 67; col. 5, II. 43-57; col. 6, I. 16 to col. 9, I. 17; col. 10, I. 41 to col. 11, I. 42 and col. 12,

I. 16 to col. 13, I. 14), as the digital camera system have the corresponding i/o port for connecting to the PC (Fig. 8, ref. 29);

a program memory (Fig. 9, ref. 52, 54-55 and col. 8, I. 48 to col. 9, I. 17);

a data storage memory (Fig. 8, ref. 16; Fig. 10; col. 6, l. 16 to col. 8, l. 47 and col.

9, II. 18-45);

a processor (Fig. 8, ref. 11, 23) operatively interfaced with the i/o port, the program memory (Fig. 9, ref. 52, 54-55) and the data storage memory (Fig. 8, ref. 16) (Fig. 8; Fig. 9; col. 6, l. 16 to col. 9, l. 17 and col. 10, l. 41 to col. 11, l. 42);

wherein the processor is adapted to be involved in a data generation process by which analog data (e.g. audio and visual analog data) is generated, the analog data is processed, and the processed analog data is stored in the data storage memory (Fig. 8, ref. 16 and Fig. 10) as at least one file of digitized analog data (Fig. 12) (Fig. 1A-1B; Fig. 11-12; Fig. 14-15; col. 1, II. 35-57; col. 3, I. 43 to col. 4, I. 57; col. 5, II. 43-57; col. 6, I. 16 to col. 9, I. 17 and col. 9, I. 46 to col. 10, I. 16);

wherein the processor also is adapted to be involved in an automatic recognition process in which, when the i/o port is operatively interfaced with a multi-purpose interface of a computer; and wherein the processor is further adapted to be involved in an automatic file transfer process in which, when the i/o port is operatively interfaced with the multi-purpose interface of the computer, the processor executes at least one other instruction set stored in the program memory and thereby causes the at least one file of digitized analog data to be transferred to the computer (Fig. 11-12; Fig. 14-15; col. 1, II. 27-57; col. 6, I. 16 to col. 9, I. 17; col. 9, I. 46 to col. 11, I. 42 and col. 12, I. 16 to col. 14, I. 14), wherein the digital camera's CPU (Fig. 8, ref. 23) control the operation of the digital camera for the data transferring after the digital camera is connected to and recognized by the PC, and as the digital camera's CPU control any function of the digital camera, the digital camera's CPU further controls the digital camera to be recognized by the PC; wherein the digital camera needs to be recognized by the PC in

order for the PC to know what peripheral device is connected such that the PC knows how to properly communicate with the connected peripheral device.

Hashimoto does not teach the ADGPD comprising:

causes at least one parameter to be automatically sent through the i/o port and to the multi-purpose interface of the computer (a) without requiring any end user to load any software onto the computer at any time and (b) without requiring any end user to interact with the computer to set up a file system in the ADGPD at any time;

wherein the at least one parameter provides information to the computer about file transfer characteristics of the ADGPD; and

data transferring after the at least one parameter has been sent from the i/o port to the multi-purpose interface of the computer without requiring any user-loaded file transfer enabling software to be loaded on or installed in the computer at any time.

Smith teaches a system and a method comprising: automatic recognition process wherein at least one parameter (e.g. parameter signifying that the peripheral device has the ability communicate in accordance to the at least one software driver) to be automatically sent through the i/o port and to the multi-purpose interface of the computer (Fig. 2-5; col. 1, II. 9-22; col. 2, I. 40 to col. 3, I. 59; col. 4, II. 5-34 and col. 6, II. 63-62), by combining the plug-and-play functionality with <u>Hashimoto</u>'s automatic recognition process, the resulting combination further teaches the automatic recognition process corresponding to configuring plug and play system utilizing ROM BIOS by having the operating system load the device driver after the peripheral device is coupled to the PC for installation.

It would have been obvious for one of ordinary skill in this art, at the time of invention was made to include <u>Smith</u>'s plug and play functionality into <u>Hashimoto</u>'s automatic recognition process for the benefit of simplifying the installation of the peripheral device for the user as the peripheral device may be installed without the need for the user to install software or configure the peripheral device (<u>Smith</u>, col. 2, II. 40-67 and col. 5, II. 41-51 and col. 6, II. 63-65); additionally, <u>Kerigan</u> expressly teaches the utilization of the plug and play functionality with camera type peripheral device (<u>Kerigan</u>, col. 3, II. 29-33 and col. 6, II. 3-10) to obtain the invention as specified in claim 239.

<u>Hashimoto</u>, <u>Smith</u> and <u>Kerigan</u> do not teach the ADGPD comprising: without ... load any software onto the computer at any time and (b) without requiring any end user to interact with the computer to set up a file system in the ADGPD at any time;

wherein the at least one parameter provides information to the computer about file transfer characteristics of the ADGPD; and

data transferring after the at least one parameter has been sent from the i/o port to the multi-purpose interface of the computer without requiring any user-loaded file transfer enabling software to be loaded on or installed in the computer at any time.

<u>Ristelhueber</u> teaches a system and a method comprising a peripheral device having an automatic recognition process without requiring any end user to load any software onto the computer at any time (pages 1-3), wherein the resulting combination of the references further teaches the above automatic recognition process corresponds to plug and play of a peripheral device by having a user to simply insert a peripheral into

a desktop system and have it start running immediately, as the PnP computer will automatically identify any new hardware installed and configure the new hardware, and relieving the end user of any need to fumble with floppy disks and user manuals to get the device up and running; therefore, the installation of the peripheral device is accomplished without any type of user intervention at any time.

It would have been obvious for one of ordinary skill in this art, at the time of invention was made to include <u>Ristelhueber</u>'s without user intervention into <u>Hashimoto</u>, <u>Smith</u> and <u>Kerigan</u>'s plug-and-play processor, not only is such implementation well known to be in accord with the plug-and-play standard, but also for the benefit of simplifying the end user's PC upgrading and reducing cost for the computing industry (<u>Ristelhueber</u>, page 2, 3rd paragraph) to obtain the invention as specified in claim 239.

<u>Hashimoto</u>, <u>Smith</u>, <u>Kerigan</u> and <u>Ristelhueber</u> do not expressly teach the ADGPD comprising: without requiring any end user to interact with the computer to set up a file system in the ADGPD at any time;

wherein the at least one parameter provides information to the computer about file transfer characteristics of the ADGPD; and

data transferring after the at least one parameter has been sent from the i/o port to the multi-purpose interface of the computer without requiring any user-loaded file transfer enabling software to be loaded on or installed in the computer at any time.

Shinohara teaches a system and a method comprising:

without requiring any end user to interact with the computer to set up a file system in the ADGPD at any time (col. 1, II. 48-60 and col. 3, I. 33 to col. 4, I. 49), by combining the emulation of a mass storage device (e.g. hard disk drive) with <u>Hashimoto, Smith, Kerigan and Ristelhueber</u>'s processor in the device with plug-andplay functionality, the resulting combination of the references further teaches the above claimed feature, which is in accordance to the applicant's disclosure of the core novelty for the instant invention as disclosed by the applicant during the interview dated 10/07/2009;

wherein the at least one parameter provides information to the computer about file transfer characteristics (e.g. associated emulating hard disk drive data transferring characteristics) of the ADGPD (col. 1, II. 48-60 and col. 3, I. 33 to col. 4, I. 49), by combining the emulation of a mass storage device (e.g. hard disk drive) with <u>Hashimoto, Smith, Kerigan and Ristelhueber</u>'s processor in the device with plug-and-play functionality, the resulting combination of the references further teaches the above claimed feature, which is in accordance to the applicant's disclosure of the core novelty for the instant invention as disclosed by the applicant during the interview dated 10/07/2009; and

data transferring after the at least one parameter has been sent from the i/o port to the multi-purpose interface of the computer (e.g. as data transfer is transferred after proper hard disk drive emulation by the peripheral device) without requiring any userloaded file transfer enabling software to be loaded on or installed in the computer at any time (col. 1, II. 48-60 and col. 3, I. 33 to col. 4, I. 49), by combining the emulation of a

mass storage device (e.g. hard disk drive) with <u>Hashimoto</u>, <u>Smith</u>, <u>Kerigan</u> and <u>Ristelhueber</u>'s data transferring by the device with plug-and-play functionality, the resulting combination of the references further teaches the above claimed feature, which is in accordance to the applicant's disclosure of the core novelty for the instant invention as disclosed by the applicant during the interview dated 10/07/2009.

It would have been obvious for one of ordinary skill in this art, at the time of invention was made to include <u>Shinohara</u>'s hard disk drive emulation into <u>Hashimoto</u>, <u>Smith</u>, <u>Kerigan</u> and <u>Ristelhueber</u>'s plug-and-play processor for reading data from the memory card for the benefit of expanding the lifetime usage of the memory card (<u>Shinohara</u>, col. 2, II. 7-8) to obtain the invention as specified in claim 239.

13. As per claim 240, <u>Hashimoto</u>, <u>Smith</u>, <u>Kerigan</u>, <u>Ristelhueber</u> and <u>Shinohara</u> teach all the of limitations claim 239 as discussed above, where <u>Hashimoto</u>, <u>Smith</u>, <u>Ristelhueber</u> and <u>Shinohara</u> further teach the ADGPD comprising wherein the i/o port, the program memory, the data storage memory, and the processor form an interface device (<u>Hashimoto</u>, Fig. 1A-1B; Fig. 8; Fig. 11-12; Fig. 14-15; col. 1, II. 27-57; col. 3, I. 43 to col. 4, I. 67; col. 5, II. 43-57; col. 6, I. 16 to col. 9, I. 17; col. 9, I. 46 to col. 11, I. 42; col. 12, I. 16 to col. 14, I. 14; <u>Smith</u>, Fig. 2-5; col. 1, II. 9-22; col. 2, I. 40 to col. 3, I. 8; col. 3, II. 22-27; col. 3, II. 53-59; col. 4, II. 5-34; col. 6, II. 63-62; <u>Ristelhueber</u>, pages 1-3; and <u>Shinohara</u>, col. 1, II. 48-60; col. 3, I. 56 to col. 4, I. 49).

14. As per claim 241, <u>Hashimoto</u>, <u>Smith</u>, <u>Kerigan</u>, <u>Ristelhueber</u> and <u>Shinohara</u> teach all the of limitations claim 240 as discussed above, where <u>Hashimoto</u>, <u>Smith</u>, <u>Ristelhueber</u> and

<u>Shinohara</u> further teach the ADGPD comprising wherein the interface device allows for a plurality of different data transmit devices to be attached thereto and detached therefrom (<u>Hashimoto</u>, Fig. 1A-1B; Fig. 8; Fig. 11-12; Fig. 14-15; col. 1, II. 27-57; col. 3, I. 43 to col. 4, I. 67; col. 5, II. 43-57; col. 6, I. 16 to col. 9, I. 17; col. 9, I. 46 to col. 11, I. 42; col. 12, I. 16 to col. 14, I. 14; <u>Smith</u>, Fig. 2-5; col. 1, II. 9-22; col. 2, I. 40 to col. 3, I. 8; col. 3, II. 22-27; col. 3, II. 53-59; col. 4, II. 5-34; col. 6, II. 63-62; <u>Ristelhueber</u>, pages 1-3; and <u>Shinohara</u>, col. 1, II. 48-60; col. 3, I. 56 to col. 4, I. 49).

15. As per claim 242, <u>Hashimoto</u>, <u>Smith</u>, <u>Kerigan</u>, <u>Ristelhueber</u> and <u>Shinohara</u> teach all the of limitations claim 240 as discussed above, where <u>Hashimoto</u>, <u>Smith</u>, <u>Ristelhueber</u> and <u>Shinohara</u> further teach the ADGPD comprising wherein the interface device comprises a portable interface device (<u>Hashimoto</u>, Fig. 1A-1B; Fig. 8; Fig. 11-12; Fig. 14-15; col. 1, II. 27-57; col. 3, I. 43 to col. 4, I. 67; col. 5, II. 43-57; col. 6, I. 16 to col. 9, I. 17; col. 9, I. 46 to col. 11, I. 42; col. 12, I. 16 to col. 14, I. 14; <u>Smith</u>, Fig. 2-5; col. 1, II. 9-22; col. 2, I. 40 to col. 3, I. 8; col. 3, II. 22-27; col. 3, II. 53-59; col. 4, II. 5-34; col. 6, II. 63-62; <u>Ristelhueber</u>, pages 1-3; and <u>Shinohara</u>, col. 1, II. 48-60; col. 3, I. 56 to col. 4, I. 49)..

16. As per claim 243, <u>Hashimoto</u>, <u>Smith</u>, <u>Kerigan</u>, <u>Ristelhueber</u> and <u>Shinohara</u> teach all the of limitations claim 240 as discussed above, where <u>Hashimoto</u>, <u>Smith</u>, <u>Ristelhueber</u> and <u>Shinohara</u> further teach the ADGPD comprising wherein the interface device comprises a flexible interface device (<u>Hashimoto</u>, Fig. 1A-1B; Fig. 8; Fig. 11-12; Fig. 14-15; col. 1, II. 27-57; col. 3, I. 43 to col. 4, I. 67; col. 5, II. 43-57; col. 6, I. 16 to col. 9, I. 17; col. 9, I. 46 to col. 11, I.

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 42; col. 12, l. 16 to col. 14, l. 14; <u>Smith</u>, Fig. 2-5; col. 1, ll. 9-22; col. 2, l. 40 to col. 3, l. 8; col. 3,

II. 22-27; col. 3, II. 53-59; col. 4, II. 5-34; col. 6, II. 63-62; <u>Ristelhueber</u>, pages 1-3; and <u>Shinohara</u>, col. 1, II. 48-60; col. 3, I. 56 to col. 4, I. 49).

17. As per claim 244, <u>Hashimoto</u>, <u>Smith</u>, <u>Kerigan</u>, <u>Ristelhueber</u> and <u>Shinohara</u> teach all the of limitations claim 240 as discussed above, where <u>Hashimoto</u>, <u>Smith</u>, <u>Ristelhueber</u> and <u>Shinohara</u> further teach the ADGPD comprising wherein the interface device comprises a universal interface device (<u>Hashimoto</u>, Fig. 1A-1B; Fig. 8; Fig. 11-12; Fig. 14-15; col. 1, II. 27-57; col. 3, I. 43 to col. 4, I. 67; col. 5, II. 43-57; col. 6, I. 16 to col. 9, I. 17; col. 9, I. 46 to col. 11, I. 42; col. 12, I. 16 to col. 14, I. 14; <u>Smith</u>, Fig. 2-5; col. 1, II. 9-22; col. 2, I. 40 to col. 3, I. 8; col. 3, II. 22-27; col. 3, II. 53-59; col. 4, II. 5-34; col. 6, II. 63-62; <u>Ristelhueber</u>, pages 1-3; and Shinohara, col. 1, II. 48-60; col. 3, I. 56 to col. 4, I. 49).

18. As per claim 245, <u>Hashimoto</u>, <u>Smith</u>, <u>Kerigan</u>, <u>Ristelhueber</u> and <u>Shinohara</u> teach all the of limitations claim 240 as discussed above, where <u>Hashimoto</u>, <u>Smith</u>, <u>Ristelhueber</u> and <u>Shinohara</u> further teach the ADGPD comprising wherein the interface device comprises a stand alone interface device (<u>Hashimoto</u>, Fig. 1A-1B; Fig. 8; Fig. 11-12; Fig. 14-15; col. 1, II. 27-57; col. 3, I. 43 to col. 4, I. 67; col. 5, II. 43-57; col. 6, I. 16 to col. 9, I. 17; col. 9, I. 46 to col. 11, I. 42; col. 12, I. 16 to col. 14, I. 14; <u>Smith</u>, Fig. 2-5; col. 1, II. 9-22; col. 2, I. 40 to col. 3, I. 8; col. 3, II. 22-27; col. 3, II. 53-59; col. 4, II. 5-34; col. 6, II. 63-62; <u>Ristelhueber</u>, pages 1-3; and <u>Shinohara</u>, col. 1, II. 48-60; col. 3, I. 56 to col. 4, I. 49).

19. As per claim 246, <u>Hashimoto</u>, <u>Smith</u>, <u>Kerigan</u>, <u>Ristelhueber</u> and <u>Shinohara</u> teach all the of limitations claim 240 as discussed above, where <u>Hashimoto</u>, <u>Smith</u>, <u>Ristelhueber</u> and <u>Shinohara</u> further teach the ADGPD comprising wherein the interface device includes a parallel logic circuit (<u>Hashimoto</u>, Fig. 1A-1B; Fig. 8; Fig. 11-12; Fig. 14-15; col. 1, II. 27-57; col. 3, I. 43 to col. 4, I. 67; col. 5, II. 43-57; col. 6, I. 16 to col. 9, I. 17; col. 9, I. 46 to col. 11, I. 42; col. 12, I. 16 to col. 14, I. 14; <u>Smith</u>, Fig. 2-5; col. 1, II. 9-22; col. 2, I. 40 to col. 3, I. 8; col. 3, II. 22-27; col. 3, II. 53-59; col. 4, II. 5-34; col. 6, II. 63-62; <u>Ristelhueber</u>, pages 1-3; and <u>Shinohara</u>, col. 1, II. 48-60; col. 3, I. 56 to col. 4, I. 49).

20. As per claim 247, <u>Hashimoto</u>, <u>Smith</u>, <u>Kerigan</u>, <u>Ristelhueber</u> and <u>Shinohara</u> teach all the of limitations claim 240 as discussed above, where <u>Hashimoto</u>, <u>Smith</u>, <u>Ristelhueber</u> and <u>Shinohara</u> further teach the ADGPD comprising wherein the interface device includes a SCSI interface circuit (<u>Hashimoto</u>, Fig. 1A-1B; Fig. 8; Fig. 11-12; Fig. 14-15; col. 1, II. 27-57; col. 3, I. 43 to col. 4, I. 67; col. 5, II. 43-57; col. 6, I. 16 to col. 9, I. 17; col. 9, I. 46 to col. 11, I. 42; col. 12, I. 16 to col. 14, I. 14; <u>Smith</u>, Fig. 2-5; col. 1, II. 9-22; col. 2, I. 40 to col. 3, I. 8; col. 3, II. 22-27; col. 3, II. 53-59; col. 4, II. 5-34; col. 6, II. 63-62; <u>Ristelhueber</u>, pages 1-3; and <u>Shinohara</u>, col. 1, II. 48-60; col. 3, I. 56 to col. 4, I. 49).

21. As per claim 248, <u>Hashimoto</u>, <u>Smith</u>, <u>Kerigan</u>, <u>Ristelhueber</u> and <u>Shinohara</u> teach all the of limitations claim 240 as discussed above, where <u>Hashimoto</u>, <u>Smith</u>, <u>Ristelhueber</u> and <u>Shinohara</u> further teach the ADGPD comprising wherein the interface device is operatively interfaced with a sensor that is designed to generate the analog data (<u>Hashimoto</u>, Fig. 1A-1B;

Fig. 8; Fig. 11-12; Fig. 14-15; col. 1, II. 27-57; col. 3, I. 43 to col. 4, I. 67; col. 5, II. 43-57; col. 6, I. 16 to col. 9, I. 17; col. 9, I. 46 to col. 11, I. 42; col. 12, I. 16 to col. 14, I. 14; <u>Smith</u>, Fig. 2-5; col. 1, II. 9-22; col. 2, I. 40 to col. 3, I. 8; col. 3, II. 22-27; col. 3, II. 53-59; col. 4, II. 5-34; col. 6, II. 63-62; Ristelhueber, pages 1-3; and Shinohara, col. 1, II. 48-60; col. 3, I. 56 to col. 4, I. 49).

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22. As per claim 252, <u>Hashimoto</u>, <u>Smith</u>, <u>Kerigan</u>, <u>Ristelhueber</u> and <u>Shinohara</u> teach all the of limitations claim 239 as discussed above, where <u>Smith</u> further teaches the ADGPD comprising wherein the i/o port comprises a parallel port (<u>Smith</u>, col. 1, II. 9-22).

23. As per claim 253, <u>Hashimoto</u>, <u>Smith</u>, <u>Kerigan</u>, <u>Ristelhueber</u> and <u>Shinohara</u> teach all the of limitations claim 239 as discussed above, where <u>Smith</u> further teaches the ADGPD comprising wherein the i/o port comprises a SCSI connector (<u>Smith</u>, col. 1, II. 9-22).

24. As per claim 254, <u>Hashimoto</u>, <u>Smith</u>, <u>Kerigan</u>, <u>Ristelhueber</u> and <u>Shinohara</u> teach all the of limitations claim 239 as discussed above, where <u>Smith</u> and <u>Hashimoto</u> further teach the ADGPD comprising wherein the i/o port is adapted to be interfaced with a multi-purpose interface of an external computing device only by means of a cable (<u>Smith</u>, col. 1, II. 9-22; and <u>Hashimoto</u>, 1A-1B; Fig. 8; Fig. 14-16; col. 1, II. 35-57; col. 3, I. 43 to col. 4, I. 57; col. 6, I. 16 to col. 9, I. 17; col. 9, I. 46 to col. 10, I. 16).

25. As per claim 255, <u>Hashimoto</u>, <u>Smith</u>, <u>Kerigan</u>, <u>Ristelhueber</u> and <u>Shinohara</u> teach all the of limitations claim 239 as discussed above, where <u>Smith</u> and <u>Hashimoto</u> further teach the ADGPD comprising wherein the i/o port is adapted to be physically connected to a multi-purpose interface of an external computing device by a cable (<u>Smith</u>, col. 1, II. 9-22; and <u>Hashimoto</u>, 1A-1B; Fig. 8; Fig. 14-16; col. 1, II. 35-57; col. 3, I. 43 to col. 4, I. 57; col. 6, I. 16 to col. 9, I. 17; col. 9, I. 46 to col. 10, I. 16).

26. As per claim 256, <u>Hashimoto</u>, <u>Smith</u>, <u>Kerigan</u>, <u>Ristelhueber</u> and <u>Shinohara</u> teach all the of limitations claim 239 as discussed above, where <u>Hashimoto</u> further teaches the ADGPD comprising a sensor that is operatively interfaced with the processor and that is designed to generate the analog data (<u>Hashimoto</u>, Fig. 8, ref. 1, 6, 9 and col. 6, I. 16 to col. 8, I. 47).

27. As per claim 258, <u>Hashimoto</u>, <u>Smith</u>, <u>Kerigan</u>, <u>Ristelhueber</u> and <u>Shinohara</u> teach all the of limitations claim 256 as discussed above, where <u>Hashimoto</u>, <u>Smith</u>, <u>Ristelhueber</u> and <u>Shinohara</u> further teach the ADGPD comprising wherein the processor allows for a plurality of different data transmit devices (e.g. memory card, I/O card, host computer) to be attached thereto and detached therefrom (<u>Hashimoto</u>, Fig. 1A-1B; Fig. 8, ref. 16; Fig. 11-12; Fig. 14-15; col. 1, II. 27-57; col. 3, I. 43 to col. 4, I. 67; col. 5, II. 43-57; col. 6, I. 16 to col. 9, I. 17; col. 9, I. 46 to col. 11, I. 42; col. 12, I. 16 to col. 14, I. 14; <u>Smith</u>, Fig. 2-5; col. 1, II. 9-22; col. 2, I. 40 to col. 3, I. 8; col. 3, II. 22-27;

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 col. 3, II. 53-59; col. 4, II. 5-34; col. 6, II. 63-62; <u>Ristelhueber</u>, pages 1-3; and <u>Shinohara</u>,

col. 1, II. 48-60; col. 3, I. 56 to col. 4, I. 49).

28. As per claim 261, <u>Hashimoto</u>, <u>Smith</u>, <u>Kerigan</u>, <u>Ristelhueber</u> and <u>Shinohara</u> teach all the of limitations claim 256 as discussed above, where <u>Hashimoto</u> further teaches the ADGPD comprising wherein the sensor comprises a data transmit/receive device (<u>Hashimoto</u>, Fig. 8; col. 6, l. 16 to col. 9, l. 17 and col. 10, l. 41 to col. 11, l. 19), wherein the data transmit/receive device is required for transferring the audiovisual information to the computer and receiving control instruction from the computer.

29. As per claim 262, <u>Hashimoto</u>, <u>Smith</u>, <u>Kerigan</u>, <u>Ristelhueber</u> and <u>Shinohara</u> teach all the of limitations claim 256 as discussed above, where <u>Hashimoto</u> further teaches the ADGPD comprising wherein the data transmit/receive device is designed for two-way communication with a host device (<u>Hashimoto</u>, Fig. 8; col. 6, l. 16 to col. 9, l. 17 and col. 10, l. 41 to col. 11, l. 19).

30. As per claim 263, <u>Hashimoto</u>, <u>Smith</u>, <u>Kerigan</u>, <u>Ristelhueber</u> and <u>Shinohara</u> teach all the of limitations claim 256 as discussed above, where <u>Hashimoto</u> further teaches the ADGPD comprising wherein the data transmit/receive device is designed for oneway or two-way communication with a host device (<u>Hashimoto</u>, Fig. 8; col. 6, l. 16 to col. 9, l. 17 and col. 10, l. 41 to col. 11, l. 19).

31. As per claim 264, <u>Hashimoto</u>, <u>Smith</u>, <u>Kerigan</u>, <u>Ristelhueber</u> and <u>Shinohara</u> teach all the of limitations claim 256 as discussed above, where <u>Hashimoto</u> further teaches the ADGPD comprising wherein the data transmit/receive device is designed to receive data from a host device (<u>Hashimoto</u>, Fig. 8; col. 6, l. 16 to col. 9, l. 17 and col. 10, l. 41 to col. 11, l. 19).

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32. As per claim 266, <u>Hashimoto</u>, <u>Smith</u>, <u>Kerigan</u>, <u>Ristelhueber</u> and <u>Shinohara</u> teach all the of limitations claim 239 as discussed above, where <u>Hashimoto</u>, <u>Smith</u>, <u>Ristelhueber</u> and <u>Shinohara</u> further teach the ADGPD further comprising at least first and second transducers both of which are designed to transmit data and are operatively interfaced with the processor (<u>Hashimoto</u>, Fig. 1A-1B; Fig. 8; Fig. 11-12; Fig. 14-15; col. 1, II. 27-57; col. 3, I. 43 to col. 4, I. 67; col. 5, II. 43-57; col. 6, I. 16 to col. 9, I. 17; col. 9, I. 46 to col. 11, I. 42; col. 12, I. 16 to col. 14, I. 14; <u>Smith</u>, Fig. 2-5; col. 1, II. 9-22; col. 2, I. 40 to col. 3, I. 8; col. 3, II. 22-27; col. 3, II. 53-59; col. 4, II. 5-34; col. 6, II. 63-62; <u>Ristelhueber</u>, pages 1-3; and <u>Shinohara</u>, col. 1, II. 48-60; col. 3, I. 56 to col. 4, I. 49).

33. As per claim 267, <u>Hashimoto</u>, <u>Smith</u>, <u>Kerigan</u>, <u>Ristelhueber</u> and <u>Shinohara</u> teach all the of limitations claim 239 as discussed above, where <u>Hashimoto</u>, <u>Smith</u>, <u>Ristelhueber</u> and <u>Shinohara</u> further teach the ADGPD comprising wherein the at least one parameter is consistent with the ADGPD being an information storage device (e.g. hard disk drive) other than a magnetic floppy disk drive (<u>Hashimoto</u>, Fig. 8, ref. 16; <u>Smith</u>, Fig. 2-5; col. 1, II. 9-22; col. 2, I. 40 to col. 3, I. 8; col. 3, II. 22-27; col. 3, II. 53-59;

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col. 4, II. 5-34; col. 6, II. 63-62; <u>Ristelhueber</u>, pages 1-3; and <u>Shinohara</u>, col. 1, II. 48-60; col. 3, I. 56 to col. 4, I. 49).

34. As per claim 268, <u>Hashimoto</u>, <u>Smith</u>, <u>Kerigan</u>, <u>Ristelhueber</u> and <u>Shinohara</u> teach all the of limitations claim 239 as discussed above, where <u>Hashimoto</u>, <u>Smith</u>, <u>Ristelhueber</u> and <u>Shinohara</u> further teach the ADGPD comprising wherein the at least one parameter is consistent with the ADGPD being a mass storage device (e.g. hard disk drive) (<u>Hashimoto</u>, Fig. 8, ref. 16; <u>Smith</u>, Fig. 2-5; col. 1, II. 9-22; col. 2, I. 40 to col. 3, I. 8; col. 3, II. 22-27; col. 3, II. 53-59; col. 4, II. 5-34; col. 6, II. 63-62; <u>Ristelhueber</u>, pages 1-3; and <u>Shinohara</u>, col. 1, II. 48-60; col. 3, I. 56 to col. 4, I. 49).

35. As per claim 269, <u>Hashimoto</u>, <u>Smith</u>, <u>Kerigan</u>, <u>Ristelhueber</u> and <u>Shinohara</u> teach all the of limitations claim 239 as discussed above, where <u>Hashimoto</u>, <u>Smith</u>, <u>Ristelhueber</u> and <u>Shinohara</u> further teach the ADGPD comprising wherein the at least one parameter is consistent with the ADGPD being responsive to a SCSI inquiry command (<u>Hashimoto</u>, Fig. 8; Fig. 9, ref. 52, 54-55; col. 6, I. 16 to col. 9, I. 17 and col. 10, I. 41 to col. 11, I. 42; <u>Smith</u>, Fig. 2-5; col. 1, II. 9-22; col. 2, I. 40 to col. 3, I. 8; col. 3, II. 22-27; col. 3, II. 53-59; col. 4, II. 5-34; col. 6, II. 63-62; <u>Ristelhueber</u>, pages 1-3; and <u>Shinohara</u>, col. 1, II. 48-60; col. 3, I. 56 to col. 4, I. 49).

36. As per claim 270, <u>Hashimoto</u>, <u>Smith</u>, <u>Kerigan</u>, <u>Ristelhueber</u> and <u>Shinohara</u> teach all the of limitations claim 239 as discussed above, where <u>Hashimoto</u>, <u>Smith</u>,

<u>Ristelhueber</u> and <u>Shinohara</u> further teach the ADGPD comprising wherein the at least one parameter is not consistent with the true nature of the ADGPD (<u>Hashimoto</u>, Fig. 8; <u>Smith</u>, Fig. 2-5; col. 1, II. 9-22; col. 2, I. 40 to col. 3, I. 8; col. 3, II. 22-27; col. 3, II. 53-59; col. 4, II. 5-34; col. 6, II. 63-62; <u>Ristelhueber</u>, pages 1-3 and <u>Shinohara</u>, col. 1, II. 48-60; col. 3, I. 56 to col. 4, I. 49), as the ADGPD's true nature is associated with processing analog signal and the parameter corresponds to emulating the hard disk drive.

37. As per claim 271, <u>Hashimoto</u>, <u>Smith</u>, <u>Kerigan</u>, <u>Ristelhueber</u> and <u>Shinohara</u> teach all the of limitations claim 239 as discussed above, where <u>Hashimoto</u>, <u>Smith</u>, and <u>Shinohara</u> further teach the ADGPD comprising wherein the at least one parameter does not indicate that the ADGPD includes a sensor that is designed to generate the analog data (<u>Hashimoto</u>, Fig. 8; <u>Smith</u>, Fig. 2-5; col. 1, II. 9-22; col. 2, I. 40 to col. 3, I. 8; col. 3, II. 22-27; col. 3, II. 53-59; col. 4, II. 5-34; col. 6, II. 63-62; and <u>Shinohara</u>, col. 1, II. 48-60; col. 3, I. 56 to col. 4, I. 49), as the parameter indicates the hard disk drive (e.g. via emulation) without indicating that the ADGPD includes the sensors for recording the image and audio.

38. As per claim 272, <u>Hashimoto</u>, <u>Smith</u>, <u>Kerigan</u>, <u>Ristelhueber</u> and <u>Shinohara</u> teach all the of limitations claim 239 as discussed above, where <u>Hashimoto</u>, <u>Smith</u>, <u>Ristelhueber</u> and <u>Shinohara</u> further teach the ADGPD comprising wherein the at least one parameter is consistent with the ADGPD being an input/output device (<u>Hashimoto</u>, Fig. 8, ref. 16; <u>Smith</u>, Fig. 2-5; col. 1, II. 9-22; col. 2, I. 40 to col. 3, I. 8; col. 3, II. 22-27;

col. 4, II. 5-34; col. 5, II.41-51; col. 6, II. 63-62; <u>Ristelhueber</u>, pages 1-3 and <u>Shinohara</u>, col. 1, II. 48-60; col. 3, I. 56 to col. 4, I. 49).

39. As per claim 274, <u>Hashimoto</u>, <u>Smith</u>, <u>Kerigan</u>, <u>Ristelhueber</u> and <u>Shinohara</u> teach all the of limitations claim 239 as discussed above, where <u>Hashimoto</u>, <u>Smith</u>, <u>Ristelhueber</u> and <u>Shinohara</u> further teach the ADGPD comprising wherein the at least one parameter is consistent with the ADGPD being adapted to operate in a manner consistent with a hard disk drive (e.g. via hard disk drive emulation) (<u>Hashimoto</u>, Fig. 8, ref. 16; <u>Smith</u>, Fig. 2-5; col. 1, II. 9-22; col. 2, I. 40 to col. 3, I. 8; col. 3, II. 22-27; col. 3, II. 53-59; col. 4, II. 5-34; col. 6, II. 63-62; <u>Ristelhueber</u>, pages 1-3 and <u>Shinohara</u>, col. 1, II. 48-60; col. 3, I. 56 to col. 4, I. 49).

40. As per claim 275, <u>Hashimoto</u>, <u>Smith</u>, <u>Kerigan</u>, <u>Ristelhueber</u> and <u>Shinohara</u> teach all the of limitations claim 239 as discussed above, where <u>Hashimoto</u>, <u>Smith</u>, <u>Ristelhueber</u> and <u>Shinohara</u> further teach the ADGPD comprising wherein the at least one parameter is consistent with the ADGPD being a hard disk drive (e.g. via hard disk drive emulation) (<u>Hashimoto</u>, Fig. 8, ref. 16; <u>Smith</u>, Fig. 2-5; col. 1, II. 9-22; col. 2, I. 40 to col. 3, I. 8; col. 3, II. 22-27; col. 3, II. 53-59; col. 4, II. 5-34; col. 6, II. 63-62; <u>Ristelhueber</u>, pages 1-3 and <u>Shinohara</u>, col. 1, II. 48-60; col. 3, I. 56 to col. 4, I. 49).

41. As per claim 276, <u>Hashimoto</u>, <u>Smith</u>, <u>Kerigan</u>, <u>Ristelhueber</u> and <u>Shinohara</u> teach all the of limitations claim 239 as discussed above, where <u>Hashimoto</u>, <u>Smith</u>,

<u>Ristelhueber</u> and <u>Shinohara</u> further teach the ADGPD comprising wherein the at least one parameter is consistent with the ADGPD being an input/output device (e.g. hard disk drive) that is customary in a host device (<u>Hashimoto</u>, Fig. 8, ref. 16; <u>Smith</u>, Fig. 2-5; col. 1, II. 9-22; col. 2, I. 40 to col. 3, I. 8; col. 3, II. 22-27; col. 4, II. 5-34; col. 5, II.41-51; col. 6, II. 63-62; <u>Ristelhueber</u>, pages 1-3 and <u>Shinohara</u>, col. 1, II. 48-60; col. 3, I. 56 to col. 4, I. 49).

42. As per claim 277, <u>Hashimoto</u>, <u>Smith</u>, <u>Kerigan</u>, <u>Ristelhueber</u> and <u>Shinohara</u> teach all the of limitations claim 239 as discussed above, where <u>Hashimoto</u>, <u>Smith</u>, <u>Ristelhueber</u> and <u>Shinohara</u> further teach the ADGPD comprising wherein the at least one parameter is consistent with the ADGPD being responsive to commands issued from a customary driver (e.g. hard disk drive driver) (<u>Hashimoto</u>, Fig. 8, ref. 16; <u>Smith</u>, Fig. 2-5; col. 1, II. 9-22; col. 2, I. 40 to col. 3, I. 8; col. 3, II. 22-27; col. 4, II. 5-34; col. 5, II.41-51; col. 6, II. 63-62; <u>Ristelhueber</u>, pages 1-3 and <u>Shinohara</u>, col. 1, II. 48-60; col. 3, I. 56 to col. 4, I. 49).

43. As per claim 279, <u>Hashimoto</u>, <u>Smith</u>, <u>Kerigan</u>, <u>Ristelhueber</u> and <u>Shinohara</u> teach all the of limitations claim 239 as discussed above, where <u>Hashimoto</u> further teaches the ADGPD comprising wherein the data storage memory comprises a semiconductor based memory (e.g. flash memory) (<u>Hashimoto</u>, Fig. 8, ref. 16; Fig. 10; col. 6, l. 16 to col. 8, l. 47 and col. 9, ll. 18-45).

44. As per claim 281, <u>Hashimoto</u>, <u>Smith</u>, <u>Kerigan</u>, <u>Ristelhueber</u> and <u>Shinohara</u> teach all the of limitations claim 239 as discussed above, where <u>Hashimoto</u> further teaches the ADGPD comprising wherein the data storage memory comprises a single memory device (<u>Hashimoto</u>, Fig. 8, ref. 16; Fig. 10; col. 6, l. 16 to col. 8, l. 47 and col. 9, ll. 18-45).

45. As per claim 283, <u>Hashimoto, Smith, Kerigan, Ristelhueber</u> and <u>Shinohara</u> teach all the of limitations claim 239 as discussed above, where <u>Hashimoto, Smith, Ristelhueber</u> and <u>Shinohara</u> further teach the ADGPD comprising wherein the processor is adapted to, when the i/o port is operatively interfaced with the multi-purpose interface of the computer, and after the at least one parameter has been sent to the multi-purpose interface of the computer, execute at least one set of computer code stored in the program memory and thereby cause ADGPD file system information to be automatically sent to the i/o port (a) without requiring any end user to load any software onto the computer at any time and (b) without requiring any end user to interact with the computer to set up a file system in the ADGPD at any time (<u>Hashimoto</u>, Fig. 8, ref. 11, 23; Fig. 9; col. 6, l. 16 to col. 9, l. 17; col. 10, l. 41 to col. 11, l. 42; <u>Smith</u>, Fig. 2-5; col. 1, ll. 9-22; col. 2, l. 40 to col. 3, l. 8; col. 3, ll. 22-27; col. 3, ll. 53-59; col. 4, ll. 5-34; col. 6, ll. 63-62; <u>Ristelhueber</u>, pages 1-3; and <u>Shinohara</u>, col. 1, ll. 48-60; col. 3, l. 56 to col. 4, l. 49).

46. As per claim 284, <u>Hashimoto</u>, <u>Smith</u>, <u>Kerigan</u>, <u>Ristelhueber</u> and <u>Shinohara</u> teach all the of limitations claim 283 as discussed above, where <u>Hashimoto</u>, <u>Smith</u>, <u>Ristelhueber</u> and <u>Shinohara</u> further teach the ADGPD comprising wherein the ADGPD file system information comprises at least an indication of the type of a file system that is used to store the at least one file of digitized analog data in the data storage memory (<u>Hashimoto</u>, Fig. 8, ref. 11, 23; Fig. 9; col. 6, I. 16 to col. 9, I. 17; col. 10, I. 41 to col. 11, I. 42; <u>Smith</u>, Fig. 2-5; col. 1, II. 9-22; col. 2, I. 40 to col. 3, I. 8; col. 3, II. 22-27; col. 3, II. 53-59; col. 4, II. 5-34; col. 6, II. 63-62; <u>Ristelhueber</u>, pages 1-3; and <u>Shinohara</u>, col. 1, II. 48-60; col. 3, I. 56 to col. 4, I. 49), as the type of file system corresponds to the plugand-play ADGPD having the memory card emulating as the hard disk drive for data transferring after the plug-and-play ADGPD is connected to the PC.

47. As per claim 285, <u>Hashimoto</u>, <u>Smith</u>, <u>Kerigan</u>, <u>Ristelhueber</u> and <u>Shinohara</u> teach all the of limitations claim 283 as discussed above, where <u>Hashimoto</u>, <u>Smith</u>, <u>Ristelhueber</u> and <u>Shinohara</u> further teach the ADGPD comprising wherein the at least one parameter is consistent with the ADGPD being an information storage device (e.g. hard disk drive) other than a magnetic floppy disk drive (<u>Hashimoto</u>, Fig. 8, ref. 16; <u>Smith</u>, Fig. 2-5; col. 1, II. 9-22; col. 2, I. 40 to col. 3, I. 8; col. 3, II. 22-27; col. 3, II. 53-59; col. 4, II. 5-34; col. 6, II. 63-62; <u>Ristelhueber</u>, pages 1-3; and <u>Shinohara</u>, col. 1, II. 48-60; col. 3, I. 56 to col. 4, I. 49).

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48. As per claim 286, <u>Hashimoto</u>, <u>Smith</u>, <u>Kerigan</u>, <u>Ristelhueber</u> and <u>Shinohara</u> teach all the of limitations claim 285 as discussed above, where <u>Hashimoto</u>, <u>Smith</u>, <u>Ristelhueber</u> and <u>Shinohara</u> further teach the ADGPD comprising wherein the at least one parameter is consistent with the ADGPD being a mass storage device (<u>Hashimoto</u>, Fig. 8, ref. 16; <u>Smith</u>, Fig. 2-5; col. 1, II. 9-22; col. 2, I. 40 to col. 3, I. 8; col. 3, II. 22-27; col. 3, II. 53-59; col. 4, II. 5-34; col. 6, II. 63-62; <u>Ristelhueber</u>, pages 1-3; and <u>Shinohara</u>, col. 1, II. 48-60; col. 3, I. 56 to col. 4, I. 49), wherein the ADGPD being a mass storage device corresponds to the plug-and-play ADGPD having the memory card emulating as the hard disk drive.

49. As per claim 287, <u>Hashimoto</u>, <u>Smith</u>, <u>Kerigan</u>, <u>Ristelhueber</u> and <u>Shinohara</u> teach all the of limitations claim 286 as discussed above, where <u>Hashimoto</u>, <u>Smith</u>, <u>Ristelhueber</u> and <u>Shinohara</u> further teach the ADGPD comprising wherein the processor and the program memory are adapted to be configured to cause, after the at least one parameter has been sent to the i/o port, file allocation table information to be sent to the i/o port, wherein the processor and the program memory are adapted to be configured to cause a virtual boot sequence to be sent to the i/o port which includes at least information that is representative of a number of sectors of a storage disk, and wherein the file allocation table information includes at least a start location of a file allocation table (<u>Hashimoto</u>, Fig. 8, ref. 16; <u>Smith</u>, Fig. 2-5; col. 1, II. 9-22; col. 2, I. 40 to col. 3, I. 8; col. 3, II. 22-27; col. 3, II. 53-59; col. 4, II. 5-34; col. 6, II. 63-62; <u>Ristelhueber</u>, pages 1-3; and <u>Shinohara</u>, col. 1, II. 48-60; col. 3, I. 56 to col. 4, I. 49), wherein the

transferring of the parameter, the file allocation table information and the virtual boot sequence corresponds to the plug-and-play ADGPD having the memory card emulating as the hard disk drive for data transferring after the plug-and-play ADGPD is connected to the PC.

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50. As per claim 288, <u>Hashimoto</u>, <u>Smith</u>, <u>Kerigan</u>, <u>Ristelhueber</u> and <u>Shinohara</u> teach all the of limitations claim 287 as discussed above, where <u>Hashimoto</u>, <u>Smith</u>, <u>Ristelhueber</u> and <u>Shinohara</u> further teach the ADGPD comprising wherein the at least one parameter is consistent with the ADGPD being adapted to operate in a manner consistent with a hard disk drive (e.g. hard drive emulation) (<u>Hashimoto</u>, Fig. 8, ref. 16; <u>Smith</u>, Fig. 2-5; col. 1, II. 9-22; col. 2, I. 40 to col. 3, I. 8; col. 3, II. 22-27; col. 3, II. 53-59; col. 4, II. 5-34; col. 6, II. 63-62; <u>Ristelhueber</u>, pages 1-3; and <u>Shinohara</u>, col. 1, II. 48-60; col. 3, I. 56 to col. 4, I. 49), wherein the operation consistent with the hard disk drive corresponds to the plug-and-play ADGPD having the memory card emulating as the hard disk drive for data transferring after the plug-and-play ADGPD is connected to the PC.

51. As per claim 289, <u>Hashimoto</u>, <u>Smith</u>, <u>Kerigan</u>, <u>Ristelhueber</u> and <u>Shinohara</u> teach all the of limitations claim 288 as discussed above, where <u>Hashimoto</u>, <u>Smith</u>, <u>Ristelhueber</u> and <u>Shinohara</u> further teach the ADGPD comprising wherein the at least one parameter is consistent with the ADGPD being a hard disk drive (<u>Hashimoto</u>, Fig. 8, ref. 16; <u>Smith</u>, Fig. 2-5; col. 1, II. 9-22; col. 2, I. 40 to col. 3, I. 8; col. 3, II. 22-27; col. 3, II.

53-59; col. 4, II. 5-34; col. 6, II. 63-62; <u>Ristelhueber</u>, pages 1-3; and <u>Shinohara</u>, col. 1, II. 48-60; col. 3, I. 56 to col. 4, I. 49), wherein the ADGPD being a mass storage device corresponds to the plug-and-play ADGPD having the memory card emulating as the hard disk drive.

52. As per claim 290, <u>Hashimoto</u>, <u>Smith</u>, <u>Kerigan</u>, <u>Ristelhueber</u> and <u>Shinohara</u> teach all the of limitations claim 239 as discussed above, where <u>Hashimoto</u> further teaches the ADGPD comprising wherein the processor includes a single central processing unit (<u>Hashimoto</u>, col. 8, I. 49 to col. 9, I. 17).

53. As per claim 291, <u>Hashimoto</u>, <u>Smith</u>, <u>Kerigan</u>, <u>Ristelhueber</u> and <u>Shinohara</u> teach all the of limitations claim 239 as discussed above, where <u>Hashimoto</u> further teaches the ADGPD comprising wherein the program memory comprises a single memory device (<u>Hashimoto</u>, col. 8, I. 49 to col. 9, I. 17).

54. As per claim 292, <u>Hashimoto</u>, <u>Smith</u>, <u>Kerigan</u>, <u>Ristelhueber</u> and <u>Shinohara</u> teach all the of limitations claim 239 as discussed above, where <u>Hashimoto</u> further teaches the ADGPD comprising wherein the program memory is formed in a single chip (<u>Hashimoto</u>, col. 8, I. 49 to col. 9, I. 17).

55. As per claim 293, <u>Hashimoto</u>, <u>Smith</u>, <u>Kerigan</u>, <u>Ristelhueber</u> and <u>Shinohara</u> teach all the of limitations claim 239 as discussed above, where <u>Hashimoto</u> further teaches

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the ADGPD comprising wherein the processor comprises a microprocessor (<u>Hashimoto</u>, col. 8, I. 49 to col. 9, I. 17).

56. As per claim 294, <u>Hashimoto</u>, <u>Smith</u>, <u>Kerigan</u>, <u>Ristelhueber</u> and <u>Shinohara</u> teach all the of limitations claim 239 as discussed above, where <u>Hashimoto</u> further teaches the ADGPD comprising wherein the processor comprises a single microprocessor (<u>Hashimoto</u>, col. 8, I. 49 to col. 9, I. 17).

57. As per claim 295, <u>Hashimoto</u>, <u>Smith</u>, <u>Kerigan</u>, <u>Ristelhueber</u> and <u>Shinohara</u> teach all the of limitations claim 239 as discussed above, where <u>Hashimoto</u> further teaches the ADGPD comprising wherein the processor comprises a digital signal processor (<u>Hashimoto</u>, Fig. 8, ref. 11 and col. 8, l. 49 to col. 9, l. 17).

58. As per claim 296, <u>Hashimoto</u>, <u>Smith</u>, <u>Kerigan</u>, <u>Ristelhueber</u> and <u>Shinohara</u> teach all the of limitations claim 239 as discussed above, where <u>Hashimoto</u> further teaches the ADGPD comprising wherein the processor comprises a single digital signal processor (<u>Hashimoto</u>, Fig. 8, ref. 11 and col. 8, l. 49 to col. 9, l. 17).

59. As per claim 297, <u>Hashimoto</u>, <u>Smith</u>, <u>Kerigan</u>, <u>Ristelhueber</u> and <u>Shinohara</u> teach all the of limitations claim 239 as discussed above, where <u>Hashimoto</u> further teaches the ADGPD comprising wherein the processor and the program memory are adapted to be configured to initiate a process by which the at least one file of digitized analog data

stored in the data storage memory are directly transferred to an input/output device by means of the i/o port (<u>Hashimoto</u>, Fig. 8; Fig. 12; Fig. 14-15; col. 1, II. 35-57; col. 6, I. 16 to col. 9, I. 17 and col. 9, I. 46 to col. 11, I. 42).

60. As per claim 298, <u>Hashimoto</u>, <u>Smith</u>, <u>Kerigan</u>, <u>Ristelhueber</u> and <u>Shinohara</u> teach all the of limitations claim 297 as discussed above, where <u>Hashimoto</u> further teaches the ADGPD comprising wherein the processor and the program memory are adapted to allow an aspect of operation (e.g. updating control program) of the ADGPD other than the transfer of at least some of the at least one file of digitized analog data from the data storage memory to the i/o port to be controlled by means of an external computer with which the i/o port is interfaced (<u>Hashimoto</u>, col. 6, I. 16 to col. 9, I. 17), as the PC directly update the control program in the ADGPD.

61. As per claim 299, <u>Hashimoto</u>, <u>Smith</u>, <u>Kerigan</u>, <u>Ristelhueber</u> and <u>Shinohara</u> teach all the of limitations claim 239 as discussed above, where <u>Hashimoto</u> further teaches the ADGPD comprising wherein the ADGPD comprises at least a portion of a medical device (<u>Hashimoto</u>, Fig. 1A-1B; Fig. 8; Fig. 11-12; Fig. 14-15; col. 1, II. 35-57; col. 6, I. 16 to col. 9, I. 17; col. 9, I. 46 to col. 11, I. 42 and col. 12, I. 16 to col. 14, I. 14), such as pictures taken for medical use.

62. As per claim 300, <u>Hashimoto</u>, <u>Smith</u>, <u>Kerigan</u>, <u>Ristelhueber</u> and <u>Shinohara</u> teach all the of limitations claim 239 as discussed above, where <u>Hashimoto</u> further teaches

the ADGPD comprising wherein the ADGPD comprises at least a portion of a data acquisition system (<u>Hashimoto</u>, Fig. 1A-1B; Fig. 8; Fig. 11-12; Fig. 14-15; col. 1, II. 35-57; col. 6, I. 16 to col. 9, I. 17; col. 9, I. 46 to col. 11, I. 42 and col. 12, I. 16 to col. 14, I. 14), as the ADGPD acquires the image and audio data.

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63. As per claim 301, <u>Hashimoto</u>, <u>Smith</u>, <u>Kerigan</u>, <u>Ristelhueber</u> and <u>Shinohara</u> teach all the of limitations claim 239 as discussed above, where <u>Smith</u> further teaches the ADGPD comprising wherein the ADGPD is designed for use with an external computing device that has an operating system that is designed by a particular software company (<u>Smith</u>, col. 3, II. 48-51).

64. As per claim 302, <u>Hashimoto</u>, <u>Smith</u>, <u>Kerigan</u>, <u>Ristelhueber</u> and <u>Shinohara</u> teach all the of limitations claim 239 as discussed above, where <u>Hashimoto</u>, <u>Smith</u>, <u>Ristelhueber</u> and <u>Shinohara</u> further teach the ADGPD comprising wherein the processor is adapted to, when it is involved in the automatic recognition process, to execute the at least one instruction set to thereby directly cause the at least one parameter regarding the ADGPD to be automatically sent (<u>Hashimoto</u>, Fig. 8; Fig. 11-12; Fig. 14-15; col. 1, II. 27-57; col. 6, I. 16 to col. 9, I. 17; col. 9, I. 46 to col. 11, I. 42; col. 12, I. 16 to col. 14, I. 14; <u>Smith</u>, Fig. 2-5; col. 1, II. 9-22; col. 2, I. 40 to col. 3, I. 8; col. 3, II. 22-27; col. 3, II. 53-59; col. 4, II. 5-34; col. 6, II. 63-62; <u>Ristelhueber</u>, pages 1-3; and <u>Shinohara</u>, col. 1, II. 48-60; col. 3, I. 56 to col. 4, I. 49).

65. As per claim 303, <u>Hashimoto</u>, <u>Smith</u>, <u>Kerigan</u>, <u>Ristelhueber</u> and <u>Shinohara</u> teach all the of limitations claim 239 as discussed above, where <u>Hashimoto</u>, <u>Smith</u>, <u>Ristelhueber</u> and <u>Shinohara</u> further teach the ADGPD comprising wherein the processor is adapted to be employed in the automatic recognition process (<u>Hashimoto</u>, Fig. 8; Fig. 11-12; Fig. 14-15; col. 1, II. 27-57; col. 6, I. 16 to col. 9, I. 17; col. 9, I. 46 to col. 11, I. 42; col. 12, I. 16 to col. 14, I. 14; <u>Smith</u>, Fig. 2-5; col. 1, II. 9-22; col. 2, I. 40 to col. 3, I. 8; col. 3, II. 22-27; col. 3, II. 53-59; col. 4, II. 5-34; col. 6, II. 63-62; <u>Ristelhueber</u>, pages 1-3; and <u>Shinohara</u>, col. 1, II. 48-60; col. 3, I. 56 to col. 4, I. 49).

As per claim 304, <u>Hashimoto</u>, <u>Smith</u>, <u>Kerigan</u>, <u>Ristelhueber</u> and <u>Shinohara</u> teach all the of limitations claim 239 as discussed above, where <u>Hashimoto</u>, <u>Smith</u>, <u>Ristelhueber</u> and <u>Shinohara</u> further teach the ADGPD comprising wherein the processor is adapted to be directly involved in all aspects of the automatic recognition process (<u>Hashimoto</u>, Fig. 8; Fig. 11-12; Fig. 14-15; col. 1, II. 27-57; col. 6, I. 16 to col. 9, I. 17; col. 9, I. 46 to col. 11, I. 42; col. 12, I. 16 to col. 14, I. 14; <u>Smith</u>, Fig. 2-5; col. 1, II. 9-22; col. 2, I. 40 to col. 3, I. 8; col. 3, II. 22-27; col. 3, II. 53-59; col. 4, II. 5-34; col. 6, II. 63-62; <u>Ristelhueber</u>, pages 1-3; and <u>Shinohara</u>, col. 1, II. 48-60; col. 3, I. 56 to col. 4, I. 49).

67. As per claim 305, <u>Hashimoto</u>, <u>Smith</u>, <u>Kerigan</u>, <u>Ristelhueber</u> and <u>Shinohara</u> teach all the of limitations claim 239 as discussed above, where <u>Hashimoto</u>, <u>Smith</u>, <u>Ristelhueber</u> and <u>Shinohara</u> further teach the ADGPD comprising wherein the

processor is adapted to be employed in the data generation process (<u>Hashimoto</u>, Fig. 8; Fig. 11-12; Fig. 14-15; col. 1, II. 27-57; col. 6, I. 16 to col. 9, I. 17; col. 9, I. 46 to col. 11, I. 42; col. 12, I. 16 to col. 14, I. 14; <u>Smith</u>, Fig. 2-5; col. 1, II. 9-22; col. 2, I. 40 to col. 3, I. 8; col. 3, II. 22-27; col. 3, II. 53-59; col. 4, II. 5-34; col. 6, II. 63-62; <u>Ristelhueber</u>, pages 1-3; and <u>Shinohara</u>, col. 1, II. 48-60; col. 3, I. 56 to col. 4, I. 49).

As per claim 306, <u>Hashimoto</u>, <u>Smith</u>, <u>Kerigan</u>, <u>Ristelhueber</u> and <u>Shinohara</u> teach all the of limitations claim 239 as discussed above, where <u>Hashimoto</u>, <u>Smith</u>, <u>Ristelhueber</u> and <u>Shinohara</u> further teach the ADGPD comprising wherein the processor is adapted to be directly involved in all aspects of the data generation process (<u>Hashimoto</u>, Fig. 8; Fig. 11-12; Fig. 14-15; col. 1, II. 27-57; col. 6, I. 16 to col. 9, I. 17; col. 9, I. 46 to col. 11, I. 42; col. 12, I. 16 to col. 14, I. 14; <u>Smith</u>, Fig. 2-5; col. 1, II. 9-22; col. 2, I. 40 to col. 3, I. 8; col. 3, II. 22-27; col. 3, II. 53-59; col. 4, II. 5-34; col. 6, II. 63-62; <u>Ristelhueber</u>, pages 1-3; and <u>Shinohara</u>, col. 1, II. 48-60; col. 3, I. 56 to col. 4, I. 49).

69. As per claim 308, <u>Hashimoto</u>, <u>Smith</u>, <u>Kerigan</u>, <u>Ristelhueber</u> and <u>Shinohara</u> teach all the of limitations claim 239 as discussed above, where <u>Hashimoto</u>, <u>Smith</u>, <u>Ristelhueber</u> and <u>Shinohara</u> further teach the ADGPD comprising wherein the processed analog data is stored in the data storage memory as only one file of digitized analog data (<u>Hashimoto</u>, Fig. 8; Fig. 11-12; Fig. 14-15; col. 1, II. 27-57; col. 6, I. 16 to col. 9, I. 17; col. 9, I. 46 to col. 11, I. 42; col. 12, I. 16 to col. 14, I. 14; <u>Smith</u>, Fig. 2-5; col.

1, II. 9-22; col. 2, I. 40 to col. 3, I. 8; col. 3, II. 22-27; col. 3, II. 53-59; col. 4, II. 5-34; col. 6, II. 63-62; <u>Ristelhueber</u>, pages 1-3; and <u>Shinohara</u>, col. 1, II. 48-60; col. 3, I. 56 to col. 4, I. 49).

70. As per claim 312, <u>Hashimoto</u>, <u>Smith</u>, <u>Kerigan</u>, <u>Ristelhueber</u> and <u>Shinohara</u> teach all the of limitations claim 239 as discussed above, where <u>Hashimoto</u> further teaches the ADGPD further comprising a sensor that is operatively interfaced with the processor and that is designed for two-way communication with a host device (<u>Hashimoto</u>, Fig. 8; col. 6, l. 16 to col. 9, l. 17 and col. 10, l. 41 to col. 11, l. 19), such as the host device receiving audiovisual information from the camera and communicating to the camera by updating control program to control the sensor.

71. As per claim 313, <u>Hashimoto</u>, <u>Smith</u>, <u>Kerigan</u>, <u>Ristelhueber</u> and <u>Shinohara</u> teach all the of limitations claim 239 as discussed above, where <u>Hashimoto</u> further teaches the ADGPD further comprising a sensor that is operatively interfaced with the processor and that is designed for one-way or two-way communication with a host device (<u>Hashimoto</u>, Fig. 8; col. 6, I. 16 to col. 9, I. 17 and col. 10, I. 41 to col. 11, I. 19), such as the host device receiving audiovisual information from the camera and communicating to the camera by updating control program to control the sensor.

72. As per claim 314, <u>Hashimoto</u>, <u>Smith</u>, <u>Kerigan</u>, <u>Ristelhueber</u> and <u>Shinohara</u> teach all the of limitations claim 239 as discussed above, where <u>Hashimoto</u> further teaches

the ADGPD further comprising a sensor that is operatively interfaced with the processor and that is designed to receive data from a host device (<u>Hashimoto</u>, Fig. 8; col. 6, I. 16 to col. 9, I. 17 and col. 10, I. 41 to col. 11, I. 19), such as the host device communicating to the camera by updating control program to control the sensor.

73. As per claim 315, <u>Hashimoto</u>, <u>Smith</u>, <u>Kerigan</u>, <u>Ristelhueber</u> and <u>Shinohara</u> teach all the of limitations claim 239 as discussed above, where <u>Hashimoto</u> further teaches the ADGPD further comprising a sensor that is operatively interfaced with the processor and that is designed to receive signals from a host device (<u>Hashimoto</u>, Fig. 8; col. 6, l. 16 to col. 9, l. 17 and col. 10, l. 41 to col. 11, l. 19), such as the host device communicating to the camera by updating control program to control the sensor.

74. As per claim 316, <u>Hashimoto</u>, <u>Smith</u>, <u>Kerigan</u>, <u>Ristelhueber</u> and <u>Shinohara</u> teach all the of limitations claim 239 as discussed above, where <u>Hashimoto</u>, <u>Smith</u>, <u>Ristelhueber</u> and <u>Shinohara</u> further teach the ADGPD comprising wherein the ADGPD is designed so that at least one aspect of how the ADGPD creates the at least one file of digitized analog data can be controlled by means of commands that are issueable from a source external to the ADGPD (<u>Hashimoto</u>, Fig. 8, ref. 16; Fig. 11-12; Fig. 14-15; col. 1, II. 27-57; col. 6, I. 16 to col. 9, I. 17; col. 9, I. 46 to col. 11, I. 42; col. 12, I. 16 to col. 14, I. 14; <u>Smith</u>, Fig. 2-5; col. 1, II. 9-22; col. 2, I. 40 to col. 3, I. 8; col. 3, II. 22-27; col. 3, II. 53-59; col. 4, II. 5-34; col. 6, II. 63-62; <u>Ristelhueber</u>, pages 1-3; and <u>Shinohara</u>, col. 1, II. 48-60; col. 3, I. 56 to col. 4, I. 49).

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As per claim 318, <u>Hashimoto</u>, <u>Smith</u>, <u>Kerigan</u>, <u>Ristelhueber</u> and <u>Shinohara</u> teach all the of limitations claim 239 as discussed above, where <u>Hashimoto</u>, <u>Smith</u>,
<u>Ristelhueber</u> and <u>Shinohara</u> further teach the ADGPD comprising wherein the ADGPD is designed to be responsive to a test unit ready command (<u>Hashimoto</u>, Fig. 8, ref. 16;
Fig. 11-12; Fig. 14-15; col. 1, II. 27-57; col. 6, I. 16 to col. 9, I. 17; col. 9, I. 46 to col. 11, I. 42; col. 12, I. 16 to col. 14, I. 14; <u>Smith</u>, Fig. 2-5; col. 1, II. 9-22; col. 2, I. 40 to col. 3, I. 8; col. 3, II. 22-27; col. 3, II. 53-59; col. 4, II. 5-34; col. 6, II. 63-62; <u>Ristelhueber</u>, pages 1-3; and Shinohara, col. 1, II. 48-60; col. 3, I. 56 to col. 4, I. 49).

76. As per claim 319, <u>Hashimoto</u>, <u>Smith</u>, <u>Kerigan</u>, <u>Ristelhueber</u> and <u>Shinohara</u> teach all the of limitations claim 239 as discussed above, where <u>Hashimoto</u>, <u>Smith</u>, <u>Ristelhueber</u> and <u>Shinohara</u> further teach the ADGPD comprising wherein the set of instructions executed by the processor in the automatic recognition process is stored in a single memory device (<u>Hashimoto</u>, Fig. 8, ref. 16; Fig. 11-12; Fig. 14-15; col. 1, II. 27-57; col. 6, I. 16 to col. 9, I. 17; col. 9, I. 46 to col. 11, I. 42; col. 12, I. 16 to col. 14, I. 14; <u>Smith</u>, Fig. 2-5; col. 1, II. 9-22; col. 2, I. 40 to col. 3, I. 8; col. 3, II. 22-27; col. 3, II. 53-59; col. 4, II. 5-34; col. 6, II. 63-62; <u>Ristelhueber</u>, pages 1-3; and <u>Shinohara</u>, col. 1, II. 48-60; col. 3, I. 56 to col. 4, I. 49).

77. As per claim 320, <u>Hashimoto</u>, <u>Smith</u>, <u>Kerigan</u>, <u>Ristelhueber</u> and <u>Shinohara</u> teach all the of limitations claim 239 as discussed above, where <u>Hashimoto</u>, <u>Smith</u>,

<u>Ristelhueber</u> and <u>Shinohara</u> further teach the ADGPD comprising wherein the set of instructions executed by the processor in the automatic file transfer process is stored in a single memory device (<u>Hashimoto</u>, Fig. 8, ref. 16; Fig. 11-12; Fig. 14-15; col. 1, II. 27-57; col. 6, I. 16 to col. 9, I. 17; col. 9, I. 46 to col. 11, I. 42; col. 12, I. 16 to col. 14, I. 14; <u>Smith</u>, Fig. 2-5; col. 1, II. 9-22; col. 2, I. 40 to col. 3, I. 8; col. 3, II. 22-27; col. 3, II. 53-59; col. 4, II. 5-34; col. 6, II. 63-62; <u>Ristelhueber</u>, pages 1-3; and <u>Shinohara</u>, col. 1, II. 48-60; col. 3, I. 56 to col. 4, I. 49).

78. As per claim 321, <u>Hashimoto</u>, <u>Smith</u>, <u>Kerigan</u>, <u>Ristelhueber</u> and <u>Shinohara</u> teach all the of limitations claim 239 as discussed above, where <u>Hashimoto</u>, <u>Smith</u>, <u>Ristelhueber</u> and <u>Shinohara</u> further teach a combination comprising the ADGPD of claim 239 and a computer (<u>Hashimoto</u>, Fig. 8; <u>Smith</u>, Fig. 2-5; col. 1, II. 9-22; col. 2, I. 40 to col. 3, I. 8; col. 3, II. 22-27; col. 3, II. 53-59; col. 4, II. 5-34; col. 6, II. 63-62; <u>Ristelhueber</u>, pages 1-3; and <u>Shinohara</u>, col. 1, II. 48-60; col. 3, I. 56 to col. 4, I. 49).

79. As per claim 322, <u>Hashimoto</u>, <u>Smith</u>, <u>Kerigan</u>, <u>Ristelhueber</u> and <u>Shinohara</u> teach all the of limitations claim 321 as discussed above, where <u>Hashimoto</u>, <u>Smith</u>, <u>Ristelhueber</u> and <u>Shinohara</u> further teach the combination comprising wherein the computer includes a driver for an input/output device customary in a host device (<u>Hashimoto</u>, Fig. 8, ref. 16; Fig. 11-12; Fig. 14-15; col. 1, II. 27-57; col. 6, I. 16 to col. 9, I. 17; col. 9, I. 46 to col. 11, I. 42; col. 12, I. 16 to col. 14, I. 14; <u>Smith</u>, Fig. 2-5; col. 1, II. 9

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 22; col. 2, l. 40 to col. 3, l. 8; col. 3, ll. 22-27; col. 3, ll. 53-59; col. 4, ll. 5-34; col. 6, ll. 63

 62; Ristelhueber, pages 1-3; and Shinohara, col. 1, ll. 48-60; col. 3, l. 56 to col. 4, l. 49).

80. As per claim 323, <u>Hashimoto</u>, <u>Smith</u>, <u>Kerigan</u>, <u>Ristelhueber</u> and <u>Shinohara</u> teach all the of limitations claim 321 as discussed above, where <u>Hashimoto</u>, <u>Smith</u>, <u>Ristelhueber</u> and <u>Shinohara</u> further teach the combination comprising wherein the computer includes at least one customary driver (<u>Hashimoto</u>, Fig. 8, ref. 16; Fig. 11-12; Fig. 14-15; col. 1, II. 27-57; col. 6, I. 16 to col. 9, I. 17; col. 9, I. 46 to col. 11, I. 42; col. 12, I. 16 to col. 14, I. 14; <u>Smith</u>, Fig. 2-5; col. 1, II. 9-22; col. 2, I. 40 to col. 3, I. 8; col. 3, II. 22-27; col. 3, II. 53-59; col. 4, II. 5-34; col. 6, II. 63-62; <u>Ristelhueber</u>, pages 1-3; and <u>Shinohara</u>, col. 1, II. 48-60; col. 3, I. 56 to col. 4, I. 49).

81. As per claim 324, <u>Hashimoto</u>, <u>Smith</u>, <u>Kerigan</u>, <u>Ristelhueber</u> and <u>Shinohara</u> teach all the of limitations claim 321 as discussed above, where <u>Hashimoto</u>, <u>Smith</u>, <u>Ristelhueber</u> and <u>Shinohara</u> further teach the combination comprising wherein the computer includes at least one driver for an input/output device customary in a host device (<u>Hashimoto</u>, Fig. 8, ref. 16; Fig. 11-12; Fig. 14-15; col. 1, II. 27-57; col. 6, I. 16 to col. 9, I. 17; col. 9, I. 46 to col. 11, I. 42; col. 12, I. 16 to col. 14, I. 14; <u>Smith</u>, Fig. 2-5; col. 1, II. 9-22; col. 2, I. 40 to col. 3, I. 8; col. 3, II. 22-27; col. 3, II. 53-59; col. 4, II. 5-34; col. 6, II. 63-62; <u>Ristelhueber</u>, pages 1-3; and <u>Shinohara</u>, col. 1, II. 48-60; col. 3, I. 56 to col. 4, I. 49).

82. As per claim 325, <u>Hashimoto</u> teaches an analog data generating and processing device (ADGPD), comprising:

an input/output (i/o) port (Fig. 1A-1B; Fig. 8; col. 1, II. 35-57; col. 3, I. 43 to col. 4, I. 67; col. 5, II. 43-57; col. 6, I. 16 to col. 9, I. 17; col. 10, I. 41 to col. 11, I. 42 and col. 12, I. 16 to col. 13, I. 14), as the digital camera system have the corresponding i/o port for connecting to the PC (Fig. 8, ref. 29);

a program memory (Fig. 9, ref. 52, 54-55 and col. 8, I. 48 to col. 9, I. 17);

a data storage memory (Fig. 8, ref. 16; Fig. 10; col. 6, l. 16 to col. 8, l. 47 and col. 9, ll. 18-45);

a processor (Fig. 8, ref. 11, 23) operatively interfaced with the i/o port, the program memory (Fig. 9, ref. 52, 54-55) and the data storage memory (Fig. 8, ref. 16) (Fig. 8; Fig. 9; col. 6, l. 16 to col. 9, l. 17 and col. 10, l. 41 to col. 11, l. 42);

wherein the processor is adapted to be involved in a data generation process by which analog data (e.g. audio and visual analog data) is generated, the analog data is processed, and the processed analog data is stored in the data storage memory (Fig. 8, ref. 16 and Fig. 10) as at least one file of digitized analog data (Fig. 12) (Fig. 1A-1B; Fig. 11-12; Fig. 14-15; col. 1, II. 35-57; col. 3, I. 43 to col. 4, I. 57; col. 5, II. 43-57; col. 6, I. 16 to col. 9, I. 17 and col. 9, I. 46 to col. 10, I. 16);

wherein the processor also is adapted to be involved in an automatic recognition process in which, when the i/o port is operatively interfaced with a multi-purpose interface of a computer; and wherein the processor is further adapted to be involved in an automatic file transfer process in which, when the i/o port is operatively interfaced

with the multi-purpose interface of the computer, the processor executes at least one set of computer code stored in the program memory and thereby causes the at least one file of digitized analog data to be transferred to the computer (Fig. 11-12; Fig. 14-15; col. 1, II. 27-57; col. 6, I. 16 to col. 9, I. 17; col. 9, I. 46 to col. 11, I. 42 and col. 12, I. 16 to col. 14, I. 14), wherein the digital camera's CPU (Fig. 8, ref. 23) control the operation of the digital camera for the data transferring after the digital camera is connected to and recognized by the PC, and as the digital camera's CPU control any function of the digital camera, the digital camera's CPU further controls the digital camera to be recognized by the PC; wherein the digital camera needs to be recognized by the PC in order for the PC to know what peripheral device is connected such that the PC knows how to properly communicate with the connected peripheral device.

Hashimoto does not teach the ADGPD comprising:

causes at least one parameter to be automatically sent through the i/o port and to the multi-purpose interface of the computer (a) without requiring any end user to load any software onto the computer at any time and (b) without requiring any end user to interact with the computer to set up a file system in the ADGPD at any time;

wherein the at least one parameter provides information that the ADGPD is a mass storage device that operates in a manner consistent with a hard disk drive;

wherein the processor is adapted to, when the i/o port is operatively interfaced with the multi-purpose interface of the computer, and after the at least one parameter has been sent to the multi-purpose interface of the computer, execute one or more other instruction sets stored in the program memory and thereby cause ADGPD file

system information to be automatically sent to the i/o port (a) without requiring any end user to load any software onto the interfaced computing device at any time and (b) without requiring any end user to enter interact with the computer to set up a file system in the ADGPD at any time, the ADGPD file system information comprising at least an indication of the type of a file system that is used to store the at least one file of digitized analog data in the data storage memory;

data transferring after the at least one parameter has been sent from the i/o port to the multi-purpose interface of the computer without requiring any user-loaded file transfer enabling software to be loaded on or installed in the computer at any time;

wherein the processor and the program memory are adapted to be configured to cause, after the at least one parameter has been sent to the i/o port, file allocation table information to be sent to the i/o port, the file allocation table information including at least a start location of a file allocation table; and

wherein the processor and the program memory are adapted to be configured to cause a virtual boot sequence to be sent to the i/o port which includes at least information that is representative of a number of sectors of a storage disk.

Smith teaches a system and a method comprising: automatic recognition process wherein at least one parameter (e.g. parameter signifying that the peripheral device has the ability communicate in accordance to the at least one software driver) to be automatically sent through the i/o port and to the multi-purpose interface of the computer (Fig. 2-5; col. 1, II. 9-22; col. 2, I. 40 to col. 3, I. 59; col. 4, II. 5-34 and col. 6, II. 63-62), by combining the plug-and-play functionality with <u>Hashimoto</u>'s automatic

recognition process, the resulting combination further teaches the automatic recognition process corresponding to configuring plug and play system utilizing ROM BIOS by having the operating system load the device driver after the peripheral device is coupled to the PC for installation.

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It would have been obvious for one of ordinary skill in this art, at the time of invention was made to include <u>Smith</u>'s plug and play functionality into <u>Hashimoto</u>'s automatic recognition process for the benefit of simplifying the installation of the peripheral device for the user as the peripheral device may be installed without the need for the user to install software or configure the peripheral device (<u>Smith</u>, col. 2, II. 40-67 and col. 5, II. 41-51 and col. 6, II. 63-65); additionally, <u>Kerigan</u> expressly teaches the utilization of the plug and play functionality with camera type peripheral device (<u>Kerigan</u>, col. 3, II. 29-33 and col. 6, II. 3-10) to obtain the invention as specified in claim 325.

Hashimoto, Smith and Kerigan do not teach the ADGPD comprising:

without ... load any software onto the computer at any time and (b) without requiring any end user to interact with the computer to set up a file system in the ADGPD at any time;

wherein the at least one parameter provides information that the ADGPD is a mass storage device that operates in a manner consistent with a hard disk drive;

wherein the processor is adapted to, when the i/o port is operatively interfaced with the multi-purpose interface of the computer, and after the at least one parameter has been sent to the multi-purpose interface of the computer, execute one or more

other instruction sets stored in the program memory and thereby cause ADGPD file system information to be automatically sent to the i/o port (a) without requiring any end user to load any software onto the interfaced computing device at any time and (b) without requiring any end user to enter interact with the computer to set up a file system in the ADGPD at any time, the ADGPD file system information comprising at least an indication of the type of a file system that is used to store the at least one file of digitized analog data in the data storage memory;

data transferring after the at least one parameter has been sent from the i/o port to the multi-purpose interface of the computer without requiring any user-loaded file transfer enabling software to be loaded on or installed in the computer at any time;

wherein the processor and the program memory are adapted to be configured to cause, after the at least one parameter has been sent to the i/o port, file allocation table information to be sent to the i/o port, the file allocation table information including at least a start location of a file allocation table; and

wherein the processor and the program memory are adapted to be configured to cause a virtual boot sequence to be sent to the i/o port which includes at least information that is representative of a number of sectors of a storage disk.

<u>Ristelhueber</u> teaches a system and a method comprising a peripheral device having an automatic recognition process without requiring any end user to load any software onto the computer at any time (pages 1-3), wherein the resulting combination of the references further teaches the above automatic recognition process corresponds to plug and play of a peripheral device by having a user to simply insert a peripheral into

a desktop system and have it start running immediately, as the PnP computer will automatically identify any new hardware installed and configure the new hardware, and relieving the end user of any need to fumble with floppy disks and user manuals to get the device up and running; therefore, the installation of the peripheral device is accomplished without any type of user intervention at any time.

It would have been obvious for one of ordinary skill in this art, at the time of invention was made to include <u>Ristelhueber</u>'s without user intervention into <u>Hashimoto</u>, <u>Smith</u> and <u>Kerigan</u>'s plug-and-play processor, not only is such implementation well known to be in accord with the plug-and-play standard, but also for the benefit of simplifying the end user's PC upgrading and reducing cost for the computing industry (<u>Ristelhueber</u>, page 2, 3rd paragraph) to obtain the invention as specified in claim 325.

Hashimoto, Smith, Kerigan and Ristelhueber do not expressly teach the ADGPD comprising:

without requiring any end user to interact with the computer to set up a file system in the ADGPD at any time;

wherein the at least one parameter provides information that the ADGPD is a mass storage device that operates in a manner consistent with a hard disk drive;

wherein the processor is adapted to, when the i/o port is operatively interfaced with the multi-purpose interface of the computer, and after the at least one parameter has been sent to the multi-purpose interface of the computer, execute one or more other instruction sets stored in the program memory and thereby cause ADGPD file

system information to be automatically sent to the i/o port (a) without requiring any end user to load any software onto the interfaced computing device at any time and (b) without requiring any end user to enter interact with the computer to set up a file system in the ADGPD at any time, the ADGPD file system information comprising at least an indication of the type of a file system that is used to store the at least one file of digitized analog data in the data storage memory;

data transferring after the at least one parameter has been sent from the i/o port to the multi-purpose interface of the computer without requiring any user-loaded file transfer enabling software to be loaded on or installed in the computer at any time;

wherein the processor and the program memory are adapted to be configured to cause, after the at least one parameter has been sent to the i/o port, file allocation table information to be sent to the i/o port, the file allocation table information including at least a start location of a file allocation table; and

wherein the processor and the program memory are adapted to be configured to cause a virtual boot sequence to be sent to the i/o port which includes at least information that is representative of a number of sectors of a storage disk.

Shinohara teaches a system and a method comprising:

without requiring any end user to interact with the computer to set up a file system in the ADGPD at any time (col. 1, II. 48-60 and col. 3, I. 33 to col. 4, I. 49), by combining the emulation of a mass storage device (e.g. hard disk drive) with <u>Hashimoto</u>, <u>Smith</u>, <u>Kerigan</u> and <u>Ristelhueber</u>'s processor in the device with plug-andplay functionality, the resulting combination of the references further teaches the above

claimed feature, which is in accordance to the applicant's disclosure of the core novelty for the instant invention as disclosed by the applicant during the interview dated 10/07/2009;

wherein the at least one parameter provides information that the ADGPD is a mass storage device that operates in a manner consistent with a hard disk drive (e.g. hard disk drive emulation) (col. 1, II. 48-60 and col. 3, I. 33 to col. 4, I. 49), by combining the emulation of a mass storage device (e.g. hard disk drive) with <u>Hashimoto</u>, <u>Smith</u>, <u>Kerigan</u> and <u>Ristelhueber</u>'s processor in the device with plug-and-play functionality, the resulting combination of the references further teaches the above claimed feature, which is in accordance to the applicant's disclosure of the core novelty for the instant invention as disclosed by the applicant during the interview dated 10/07/2009;

wherein the processor is adapted to, when the i/o port is operatively interfaced with the multi-purpose interface of the computer, and after the at least one parameter has been sent to the multi-purpose interface of the computer, execute one or more other instruction sets stored in the program memory and thereby cause ADGPD file system information to be automatically sent to the i/o port (a) without requiring any end user to load any software onto the interfaced computing device at any time and (b) without requiring any end user to enter interact with the computer to set up a file system in the ADGPD at any time, the ADGPD file system information comprising at least an indication of the type of a file system that is used to store the at least one file of digitized analog data in the data storage memory; wherein the processor and the program memory are adapted to be configured to cause, after the at least one parameter has

been sent to the i/o port, file allocation table information to be sent to the i/o port, the file allocation table information including at least a start location of a file allocation table; wherein the processor and the program memory are adapted to be configured to cause a virtual boot sequence to be sent to the i/o port which includes at least information that is representative of a number of sectors of a storage disk (col. 1, II. 48-60; col. 3, I. 56 to col. 4, I. 49) by combining the emulation of a mass storage device (e.g. hard disk drive) with <u>Hashimoto</u>, <u>Smith</u>, <u>Kerigan</u> and <u>Ristelhueber</u>'s processor in the device with plugand-play functionality, wherein the transferring of the parameter, the ADGPD file system information, the file allocation table information and the virtual boot sequence corresponds to the plug-and-play ADGPD having the memory card emulating as the hard disk drive for data transferring after the plug-and-play ADGPD is connected to the PC, which is in accordance to the applicant's disclosure of the core novelty for the instant invention as disclosed by the applicant during the interview dated 10/07/2009;

data transferring after the at least one parameter has been sent from the i/o port to the multi-purpose interface of the computer (e.g. as data transfer is transferred after proper hard disk drive emulation by the peripheral device) without requiring any userloaded file transfer enabling software to be loaded on or installed in the computer at any time (col. 1, II. 48-60 and col. 3, I. 33 to col. 4, I. 49), by combining the emulation of a mass storage device (e.g. hard disk drive) with <u>Hashimoto</u>, <u>Smith</u>, <u>Kerigan</u> and <u>Ristelhueber</u>'s data transferring by the device with plug-and-play functionality, the resulting combination of the references further teaches the above claimed feature,

which is in accordance to the applicant's disclosure of the core novelty for the instant invention as disclosed by the applicant during the interview dated 10/07/2009.

It would have been obvious for one of ordinary skill in this art, at the time of invention was made to include <u>Shinohara</u>'s hard disk drive emulation into <u>Hashimoto</u>, <u>Smith</u>, <u>Kerigan</u> and <u>Ristelhueber</u>'s plug-and-play processor for reading data from the memory card for the benefit of expanding the lifetime usage of the memory card (<u>Shinohara</u>, col. 2, II. 7-8) to obtain the invention as specified in claim 325.

83. As per claim 326, <u>Hashimoto</u>, <u>Smith</u>, <u>Kerigan</u>, <u>Ristelhueber</u> and <u>Shinohara</u> teach all the limitation of claim 325 as discussed above, where <u>Hashimoto</u>, <u>Smith</u>, <u>Ristelhueber</u> and <u>Shinohara</u> further teaches the ADGPD comprising wherein the at least one parameter is consistent with the ADGPD being a hard disk drive (<u>Hashimoto</u>, Fig. 8, ref. 16; Fig. 11-12; Fig. 14-15; col. 1, II. 27-57; col. 6, I. 16 to col. 9, I. 17; col. 9, I. 46 to col. 11, I. 42; col. 12, I. 16 to col. 14, I. 14; <u>Smith</u>, Fig. 2-5; col. 1, II. 9-22; col. 2, I. 40 to col. 3, I. 8; col. 3, II. 22-27; col. 3, II. 53-59; col. 4, II. 5-34; col. 6, II. 63-62; <u>Ristelhueber</u>, pages 1-3; and <u>Shinohara</u>, col. 1, II. 48-60; col. 3, I. 56 to col. 4, I. 49).

84. As per claim 327, <u>Hashimoto</u> teaches an analog data generating and processing device (ADGPD), comprising:

an input/output (i/o) port (Fig. 1A-1B; Fig. 8; col. 1, ll. 35-57; col. 3, l. 43 to col. 4, l. 67; col. 5, ll. 43-57; col. 6, l. 16 to col. 9, l. 17; col. 10, l. 41 to col. 11, l. 42 and col. 12,

I. 16 to col. 13, I. 14), as the digital camera system have the corresponding i/o port for connecting to the PC (Fig. 8, ref. 29);

a program memory (Fig. 9, ref. 52, 54-55 and col. 8, l. 48 to col. 9, l. 17);

a data storage memory (Fig. 8, ref. 16; Fig. 10; col. 6, l. 16 to col. 8, l. 47 and col. 9, ll. 18-45);

a processor (Fig. 8, ref. 11, 23) operatively interfaced with the i/o port, the program memory (Fig. 9, ref. 52, 54-55) and the data storage memory (Fig. 8, ref. 16) (Fig. 8; Fig. 9; col. 6, l. 16 to col. 9, l. 17 and col. 10, l. 41 to col. 11, l. 42);

wherein the processor is adapted to be involved in a data generation process by which analog data (e.g. audio and visual analog data) is generated, the analog data is processed, and the processed analog data is stored in the data storage memory (Fig. 8, ref. 16 and Fig. 10) as at least one file of digitized analog data (Fig. 12) (Fig. 1A-1B; Fig. 11-12; Fig. 14-15; col. 1, II. 35-57; col. 3, I. 43 to col. 4, I. 57; col. 5, II. 43-57; col. 6, I. 16 to col. 9, I. 17 and col. 9, I. 46 to col. 10, I. 16);

wherein the processor also is adapted to be involved in an automatic recognition process in which, when the i/o port is operatively interfaced with a multi-purpose interface of a computer, the processor executes at least one instruction set stored in the program memory; and wherein the processor is further adapted to be involved in an automatic file transfer process in which, when the i/o port is operatively interfaced with the multi-purpose interface of the computer, the processor executes at least one other instruction set stored in the program memory and thereby causes the at least one file of digitized analog data to be transferred to the computer (Fig. 11-12; Fig. 14-15; col. 1, II.

27-57; col. 6, I. 16 to col. 9, I. 17; col. 9, I. 46 to col. 11, I. 42 and col. 12, I. 16 to col. 14, I. 14), wherein the digital camera's CPU (Fig. 8, ref. 23) control the operation of the digital camera for the data transferring after the digital camera is connected to and recognized by the PC, and as the digital camera's CPU control any function of the digital camera, the digital camera's CPU further controls the digital camera to be recognized by the PC; wherein the digital camera needs to be recognized by the PC in order for the PC to know what peripheral device is connected such that the PC knows how to properly communicate with the connected peripheral device.

Hashimoto does not teach the ADGPD comprising:

causes at least one parameter to be automatically sent through the i/o port and to the multi-purpose interface of the computer (a) without requiring any end user to load any software onto the computer at any time, (b) without requiring any end user to interact with the computer to set up a file system in the ADGPD at any time, and (c) regardless of the identity of a manufacturer of the computer;

wherein the at least one parameter provides information to the computer about file transfer characteristics of the ADGPD; and

data transferring after the at least one parameter has been sent from the i/o port to the multi-purpose interface of the computer regardless of the identity of the manufacturer of the computer and without requiring any user-loaded file transfer enabling software to be loaded on or installed in the computer at any time.

<u>Smith</u> teaches a system and a method comprising: automatic recognition process wherein at least one parameter (e.g. parameter signifying that the peripheral device has

the ability communicate in accordance to the at least one software driver) to be automatically sent through the i/o port and to the multi-purpose interface of the computer (Fig. 2-5; col. 1, II. 9-22; col. 2, I. 40 to col. 3, I. 59; col. 4, II. 5-34 and col. 6, II. 63-62), by combining the plug-and-play functionality with <u>Hashimoto</u>'s automatic recognition process, the resulting combination further teaches the automatic recognition process corresponding to configuring plug and play system utilizing ROM BIOS by having the operating system load the device driver after the peripheral device is coupled to the PC for installation.

It would have been obvious for one of ordinary skill in this art, at the time of invention was made to include <u>Smith</u>'s plug and play functionality into <u>Hashimoto</u>'s automatic recognition process for the benefit of simplifying the installation of the peripheral device for the user as the peripheral device may be installed without the need for the user to install software or configure the peripheral device (<u>Smith</u>, col. 2, II. 40-67 and col. 5, II. 41-51 and col. 6, II. 63-65); additionally, <u>Kerigan</u> expressly teaches the utilization of the plug and play functionality with camera type peripheral device (<u>Kerigan</u>, col. 3, II. 29-33 and col. 6, II. 3-10) to obtain the invention as specified in claim 327.

Hashimoto, Smith and Kerigan do not teach the ADGPD comprising:

without ... load any software onto the computer at any time, (b) without requiring any end user to interact with the computer to set up a file system in the ADGPD at any time, and (c) regardless of the identity of a manufacturer of the computer;

wherein the at least one parameter provides information to the computer about file transfer characteristics of the ADGPD; and

data transferring after the at least one parameter has been sent from the i/o port to the multi-purpose interface of the computer regardless of the identity of the manufacturer of the computer and without requiring any user-loaded file transfer enabling software to be loaded on or installed in the computer at any time.

<u>Ristelhueber</u> teaches a system and a method comprising a peripheral device having an automatic recognition process without requiring any end user to load any software onto the computer at any time (pages 1-3), wherein the resulting combination of the references further teaches the above automatic recognition process corresponds to plug and play of a peripheral device by having a user to simply insert a peripheral into a desktop system and have it start running immediately, as the PnP computer will automatically identify any new hardware installed and configure the new hardware, and relieving the end user of any need to fumble with floppy disks and user manuals to get the device up and running; therefore, the installation of the peripheral device is accomplished without any type of user intervention at any time.

It would have been obvious for one of ordinary skill in this art, at the time of invention was made to include <u>Ristelhueber</u>'s without user intervention into <u>Hashimoto</u>, <u>Smith</u> and <u>Kerigan</u>'s plug-and-play processor, not only is such implementation well known to be in accord with the plug-and-play standard, but also for the benefit of simplifying the end user's PC upgrading and reducing cost for the computing industry (<u>Ristelhueber</u>, page 2, 3rd paragraph) to obtain the invention as specified in claim 327.

Hashimoto, Smith, Kerigan and Ristelhueber do not expressly teach the ADGPD comprising:

without requiring any end user to interact with the computer to set up a file system in the ADGPD at any time, and (c) regardless of the identity of a manufacturer of the computer;

wherein the at least one parameter provides information to the computer about file transfer characteristics of the ADGPD; and

data transferring after the at least one parameter has been sent from the i/o port to the multi-purpose interface of the computer regardless of the identity of the manufacturer of the computer and without requiring any user-loaded file transfer enabling software to be loaded on or installed in the computer at any time.

Shinohara teaches a system and a method comprising:

without requiring any end user to interact with the computer to set up a file system in the ADGPD at any time, and regardless of the identity of a manufacturer of the computer (e.g. regardless via hard disk drive emulation) (col. 1, II. 48-60 and col. 3, I. 33 to col. 4, I. 49), by combining the emulation of a mass storage device (e.g. hard disk drive) with <u>Hashimoto</u>, <u>Smith</u>, <u>Kerigan</u> and <u>Ristelhueber</u>'s processor in the device with plug-and-play functionality, the resulting combination of the references further teaches the above claimed feature, which is in accordance to the applicant's disclosure of the core novelty for the instant invention as disclosed by the applicant during the interview dated 10/07/2009;

wherein the at least one parameter provides information to the computer about file transfer characteristics (e.g. associated emulating hard disk drive data transferring characteristics) of the ADGPD (col. 1, II. 48-60 and col. 3, I. 33 to col. 4, I. 49), by combining the emulation of a mass storage device (e.g. hard disk drive) with <u>Hashimoto, Smith, Kerigan and Ristelhueber</u>'s processor in the device with plug-and-play functionality, the resulting combination of the references further teaches the above claimed feature, which is in accordance to the applicant's disclosure of the core novelty for the instant invention as disclosed by the applicant during the interview dated 10/07/2009; and

data transferring after the at least one parameter has been sent from the i/o port to the multi-purpose interface of the computer (e.g. as data transfer is transferred after proper hard disk drive emulation by the peripheral device) regardless of the identity of the manufacturer of the computer and without requiring any user-loaded file transfer enabling software to be loaded on or installed in the computer at any time (col. 1, II. 48-60 and col. 3, I. 33 to col. 4, I. 49), by combining the emulation of a mass storage device (e.g. hard disk drive) with <u>Hashimoto</u>, <u>Smith</u>, <u>Kerigan</u> and <u>Ristelhueber</u>'s data transferring by the device with plug-and-play functionality, the resulting combination of the references further teaches the above claimed feature, which is in accordance to the applicant's disclosure of the core novelty for the instant invention as disclosed by the applicant during the interview dated 10/07/2009.

It would have been obvious for one of ordinary skill in this art, at the time of invention was made to include <u>Shinohara</u>'s hard disk drive emulation into <u>Hashimoto</u>, <u>Smith</u>, <u>Kerigan</u>

and <u>Ristelhueber</u>'s plug-and-play processor for reading data from the memory card for the benefit of expanding the lifetime usage of the memory card (<u>Shinohara</u>, col. 2, II. 7-8) to obtain the invention as specified in claim 327.

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85. As per claim 328, <u>Hashimoto</u>, <u>Smith</u>, <u>Kerigan</u>, <u>Ristelhueber</u> and <u>Shinohara</u> teach all the limitation of claim 327 as discussed above, where <u>Hashimoto</u>, <u>Smith</u>, <u>Ristelhueber</u> and <u>Shinohara</u> further teaches the ADGPD comprising wherein the at least one parameter is consistent with the ADGPD being a mass storage device (e.g. hard disk drive) (<u>Hashimoto</u>, Fig. 8, ref. 16; Fig. 11-12; Fig. 14-15; col. 1, II. 27-57; col. 6, I. 16 to col. 9, I. 17; col. 9, I. 46 to col. 11, I. 42; col. 12, I. 16 to col. 14, I. 14; <u>Smith</u>, Fig. 2-5; col. 1, II. 9-22; col. 2, I. 40 to col. 3, I. 8; col. 3, II. 22-27; col. 3, II. 53-59; col. 4, II. 5-34; col. 6, II. 63-62; <u>Ristelhueber</u>, pages 1-3; and <u>Shinohara</u>, col. 1, II. 48-60; col. 3, I. 56 to col. 4, I. 49).

86. As per claim 329, <u>Hashimoto</u> teaches an analog data generating and processing device (ADGPD), comprising:

an input/output (i/o) port (Fig. 1A-1B; Fig. 8; col. 1, II. 35-57; col. 3, I. 43 to col. 4, I. 67; col. 5, II. 43-57; col. 6, I. 16 to col. 9, I. 17; col. 10, I. 41 to col. 11, I. 42 and col. 12, I. 16 to col. 13, I. 14), as the digital camera system have the corresponding i/o port for connecting to the PC (Fig. 8, ref. 29);

a program memory (Fig. 9, ref. 52, 54-55 and col. 8, l. 48 to col. 9, l. 17);

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a data storage memory (Fig. 8, ref. 16; Fig. 10; col. 6, l. 16 to col. 8, l. 47 and col. 9, ll. 18-45);

a processor (Fig. 8, ref. 11, 23) operatively interfaced with the i/o port, the program memory (Fig. 9, ref. 52, 54-55) and the data storage memory (Fig. 8, ref. 16) (Fig. 8; Fig. 9; col. 6, l. 16 to col. 9, l. 17 and col. 10, l. 41 to col. 11, l. 42);

wherein the processor is adapted to be involved in a data generation process by which analog data (e.g. audio and visual analog data) is generated, the analog data is processed, and the processed analog data is stored in the data storage memory (Fig. 8, ref. 16 and Fig. 10) as at least one file of digitized analog data (Fig. 12) (Fig. 1A-1B; Fig. 11-12; Fig. 14-15; col. 1, II. 35-57; col. 3, I. 43 to col. 4, I. 57; col. 5, II. 43-57; col. 6, I. 16 to col. 9, I. 17 and col. 9, I. 46 to col. 10, I. 16);

wherein the processor also is adapted to be involved in an automatic recognition process in which, when the i/o port is operatively interfaced with a multi-purpose interface of a first and second computers respectively, the processor executes at least one instruction set stored in the program memory; and wherein the processor is further adapted to be involved in an automatic file transfer process in which, when the i/o port is operatively interfaced with the multi-purpose interface of the first and second computers respectively, the processor executes at least operatively interfaced with the multi-purpose interface of the first and second computers respectively, the processor executes at least one other instruction set stored in the program memory and thereby causes the at least one file of digitized analog data to be transferred to the first and second computers respectively (Fig. 11-12; Fig. 14-15; col. 1, II. 27-57; col. 6, I. 16 to col. 9, I. 17; col. 9, I. 46 to col. 11, I. 42 and col. 12, I. 16 to col. 14, I. 14), wherein the digital camera's CPU (Fig. 8, ref. 23) control the operation of the

digital camera for the data transferring after the digital camera is connected to and recognized by the respective computer, and as the digital camera's CPU control any function of the digital camera, the digital camera's CPU further controls the digital camera to be recognized by the respective computer; wherein the digital camera needs to be recognized by the respective computer in order for the respective computer to know what peripheral device is connected such that the respective computer knows how to properly communicate with the connected peripheral device.

Hashimoto does not teach the ADGPD comprising:

thereby causes at least one parameter to be automatically sent through the i/o port and to the multi-purpose interface of the first and second computers respectively without requiring any end user to load any software onto the computer at any time and without requiring any end user to interact with the first and second computers respectively to set up a file system in the ADGPD at any time, and the second computer is manufactured by a company other than the company that manufactured the first computer;

wherein the at least one parameter provides information to the computer about file transfer characteristics of the ADGPD; and

data transferring after the at least one parameter has been sent from the i/o port to the multi-purpose interface of the first and second computers respectively without requiring any user-loaded file transfer enabling software to be loaded on or installed in the computer at any time.

Smith teaches a system and a method comprising: automatic recognition process wherein at least one parameter (e.g. parameter signifying that the peripheral device has the ability communicate in accordance to the at least one software driver) to be automatically sent through the i/o port and to the multi-purpose interface of the first and second computers respectively (Fig. 2-5; col. 1, II. 9-22; col. 2, I. 40 to col. 3, I. 59; col. 4, II. 5-34 and col. 6, II. 63-62), by combining the plug-and-play functionality with <u>Hashimoto</u>'s automatic recognition process, the resulting combination further teaches the automatic recognition process corresponding to configuring plug and play system utilizing ROM BIOS by having the operating system load the device driver after the peripheral device is coupled to the PC for installation.

It would have been obvious for one of ordinary skill in this art, at the time of invention was made to include <u>Smith</u>'s plug and play functionality into <u>Hashimoto</u>'s automatic recognition process for the benefit of simplifying the installation of the peripheral device for the user as the peripheral device may be installed without the need for the user to install software or configure the peripheral device (<u>Smith</u>, col. 2, II. 40-67 and col. 5, II. 41-51 and col. 6, II. 63-65); additionally, <u>Kerigan</u> expressly teaches the utilization of the plug and play functionality with camera type peripheral device (<u>Kerigan</u>, col. 3, II. 29-33 and col. 6, II. 3-10) to obtain the invention as specified in claim 329.

Hashimoto, Smith and Kerigan do not teach the ADGPD comprising:

without ... load any software onto the computer at any time and without requiring any end user to interact with the first and second computers respectively to set up a file

system in the ADGPD at any time, and the second computer is manufactured by a company other than the company that manufactured the first computer;

wherein the at least one parameter provides information to the computer about file transfer characteristics of the ADGPD; and

data transferring after the at least one parameter has been sent from the i/o port to the multi-purpose interface of the first and second computers respectively without requiring any user-loaded file transfer enabling software to be loaded on or installed in the computer at any time.

<u>Ristelhueber</u> teaches a system and a method comprising a peripheral device having an automatic recognition process without requiring any end user to load any software onto the computer at any time (pages 1-3), wherein the resulting combination of the references further teaches the above automatic recognition process corresponds to plug and play of a peripheral device by having a user to simply insert a peripheral into a desktop system and have it start running immediately, as the PnP computer will automatically identify any new hardware installed and configure the new hardware, and relieving the end user of any need to fumble with floppy disks and user manuals to get the device up and running; therefore, the installation of the peripheral device is accomplished without any type of user intervention at any time.

It would have been obvious for one of ordinary skill in this art, at the time of invention was made to include <u>Ristelhueber</u>'s without user intervention into <u>Hashimoto</u>, <u>Smith</u> and <u>Kerigan</u>'s plug-and-play processor, not only is such implementation well known to be in accord with the plug-and-play standard, but also for the benefit of

Application/Control Number: 11/467,092Page 63Art Unit: 2181simplifying the end user's PC upgrading and reducing cost for the computing industry(Ristelhueber, page 2, 3rd paragraph) to obtain the invention as specified in claim 329.

Hashimoto, Smith, Kerigan and Ristelhueber do not expressly teach the ADGPD comprising:

without requiring any end user to interact with the first and second computers respectively to set up a file system in the ADGPD at any time, and the second computer is manufactured by a company other than the company that manufactured the first computer;

wherein the at least one parameter provides information to the computer about file transfer characteristics of the ADGPD; and

data transferring after the at least one parameter has been sent from the i/o port to the multi-purpose interface of the first and second computers respectively without requiring any user-loaded file transfer enabling software to be loaded on or installed in the computer at any time.

Shinohara teaches a system and a method comprising:

without requiring any end user to interact with the first and second computers respectively to set up a file system in the ADGPD at any time, and the second computer is manufactured by a company other than the company that manufactured the first computer (col. 1, II. 48-60 and col. 3, I. 33 to col. 4, I. 49), by combining the emulation of a mass storage device (e.g. hard disk drive) with <u>Hashimoto</u>, <u>Smith</u>, <u>Kerigan</u> and <u>Ristelhueber</u>'s processor in the device with plug-and-play functionality, the resulting

combination of the references further teaches the above claimed feature, which is in accordance to the applicant's disclosure of the core novelty for the instant invention as disclosed by the applicant during the interview dated 10/07/2009;

wherein the at least one parameter provides information to the computer about file transfer characteristics (e.g. associated emulating hard disk drive data transferring characteristics) of the ADGPD (col. 1, II. 48-60 and col. 3, I. 33 to col. 4, I. 49), by combining the emulation of a mass storage device (e.g. hard disk drive) with <u>Hashimoto</u>, <u>Smith</u>, <u>Kerigan</u> and <u>Ristelhueber</u>'s processor in the device with plug-and-play functionality, the resulting combination of the references further teaches the above claimed feature, which is in accordance to the applicant's disclosure of the core novelty for the instant invention as disclosed by the applicant during the interview dated 10/07/2009; and

data transferring after the at least one parameter has been sent from the i/o port to the multi-purpose interface of the first and second computers respectively (e.g. as data transfer is transferred after proper hard disk drive emulation by the peripheral device) without requiring any user-loaded file transfer enabling software to be loaded on or installed in the first and second computers respectively at any time (col. 1, II. 48-60 and col. 3, I. 33 to col. 4, I. 49), by combining the emulation of a mass storage device (e.g. hard disk drive) with <u>Hashimoto</u>, <u>Smith</u>, <u>Kerigan</u> and <u>Ristelhueber</u>'s data transferring by the device with plug-and-play functionality, the resulting combination of the references further teaches the above claimed feature, which is in accordance to the

applicant's disclosure of the core novelty for the instant invention as disclosed by the applicant during the interview dated 10/07/2009.

It would have been obvious for one of ordinary skill in this art, at the time of invention was made to include <u>Shinohara</u>'s hard disk drive emulation into <u>Hashimoto</u>, <u>Smith</u>, <u>Kerigan</u> and <u>Ristelhueber</u>'s plug-and-play processor for reading data from the memory card for the benefit of expanding the lifetime usage of the memory card (<u>Shinohara</u>, col. 2, II. 7-8) to obtain the invention as specified in claim 329.

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87. As per claim 330, <u>Hashimoto</u>, <u>Smith</u>, <u>Kerigan</u>, <u>Ristelhueber</u> and <u>Shinohara</u> teach all the limitation of claim 329 as discussed above, where <u>Hashimoto</u>, <u>Smith</u>, <u>Ristelhueber</u> and <u>Shinohara</u> further teaches the ADGPD comprising wherein the at least one parameter is consistent with the ADGPD being a mass storage device (e.g. hard disk drive) (<u>Hashimoto</u>, Fig. 8, ref. 16; Fig. 11-12; Fig. 14-15; col. 1, II. 27-57; col. 6, I. 16 to col. 9, I. 17; col. 9, I. 46 to col. 11, I. 42; col. 12, I. 16 to col. 14, I. 14; <u>Smith</u>, Fig. 2-5; col. 1, II. 9-22; col. 2, I. 40 to col. 3, I. 8; col. 3, II. 22-27; col. 3, II. 53-59; col. 4, II. 5-34; col. 6, II. 63-62; <u>Ristelhueber</u>, pages 1-3; and <u>Shinohara</u>, col. 1, II. 48-60; col. 3, I. 56 to col. 4, I. 49).

88. As per claim 331, <u>Hashimoto</u> teaches an analog data generating and processing device (ADGPD), comprising:

an input/output (i/o) port (Fig. 1A-1B; Fig. 8; col. 1, ll. 35-57; col. 3, l. 43 to col. 4, l. 67; col. 5, ll. 43-57; col. 6, l. 16 to col. 9, l. 17; col. 10, l. 41 to col. 11, l. 42 and col. 12,

I. 16 to col. 13, I. 14), as the digital camera system have the corresponding i/o port for connecting to the PC (Fig. 8, ref. 29);

a program memory (Fig. 9, ref. 52, 54-55 and col. 8, I. 48 to col. 9, I. 17);

a data storage memory (Fig. 8, ref. 16; Fig. 10; col. 6, l. 16 to col. 8, l. 47 and col. 9, ll. 18-45);

a processor (Fig. 8, ref. 11, 23) operatively interfaced with the i/o port, the program memory (Fig. 9, ref. 52, 54-55) and the data storage memory (Fig. 8, ref. 16) (Fig. 8; Fig. 9; col. 6, l. 16 to col. 9, l. 17 and col. 10, l. 41 to col. 11, l. 42);

wherein the processor is adapted to be involved in a data generation process by which analog data (e.g. audio and visual analog data) is generated, the analog data is processed, and the processed analog data is stored in the data storage memory (Fig. 8, ref. 16 and Fig. 10) as at least one file of digitized analog data (Fig. 12) (Fig. 1A-1B; Fig. 11-12; Fig. 14-15; col. 1, II. 35-57; col. 3, I. 43 to col. 4, I. 57; col. 5, II. 43-57; col. 6, I. 16 to col. 9, I. 17 and col. 9, I. 46 to col. 10, I. 16); and

wherein the processor also is adapted to be involved in an automatic recognition process in which, when the i/o port is operatively interfaced with a multi-purpose interface of a computer, the processor executes at least one instruction set stored in the program memory; and wherein the processor is further adapted to be involved in an automatic file transfer process in which, when the i/o port is operatively interfaced with the multi-purpose interface of the computer, the processor executes at least one other instruction set stored in the program memory and thereby causes the at least one file of digitized analog data to be transferred to the computer (Fig. 11-12; Fig. 14-15; col. 1, II.

27-57; col. 6, I. 16 to col. 9, I. 17; col. 9, I. 46 to col. 11, I. 42 and col. 12, I. 16 to col. 14, I. 14), wherein the digital camera's CPU (Fig. 8, ref. 23) control the operation of the digital camera for the data transferring after the digital camera is connected to and recognized by the computer, and as the digital camera's CPU control any function of the digital camera, the digital camera's CPU further controls the digital camera to be recognized by the computer; wherein the digital camera needs to be recognized by the computer to know what peripheral device is connected such that the computer knows how to properly communicate with the connected peripheral device.

Hashimoto does not teach the ADGPD comprising:

causes at least one parameter to be automatically sent through the i/o port and to the multi-purpose interface of the computer (a) without requiring any end user to load any software onto the computer at any time and (b) without requiring any end user to interact with the computer to set up a file system in the ADGPD at any time, the execution of the at least one instruction set not taking into account the identity of the manufacturer of the computer;

wherein the at least one parameter provides information to the computer about file transfer characteristics of the ADGPD; and

data transferring after the at least one parameter has been sent from the i/o port to the multi-purpose interface of the computer without requiring any user-loaded file transfer enabling software to be loaded on or installed in the computer at any time.

Smith teaches a system and a method comprising: automatic recognition process wherein at least one parameter (e.g. parameter signifying that the peripheral device has the ability communicate in accordance to the at least one software driver) to be automatically sent through the i/o port and to the multi-purpose interface of the computer (Fig. 2-5; col. 1, II. 9-22; col. 2, I. 40 to col. 3, I. 59; col. 4, II. 5-34 and col. 6, II. 63-62), by combining the plug-and-play functionality with <u>Hashimoto</u>'s automatic recognition process, the resulting combination further teaches the automatic recognition process corresponding to configuring plug and play system utilizing ROM BIOS by having the operating system load the device driver after the peripheral device is coupled to the PC for installation.

It would have been obvious for one of ordinary skill in this art, at the time of invention was made to include <u>Smith</u>'s plug and play functionality into <u>Hashimoto</u>'s automatic recognition process for the benefit of simplifying the installation of the peripheral device for the user as the peripheral device may be installed without the need for the user to install software or configure the peripheral device (<u>Smith</u>, col. 2, II. 40-67 and col. 5, II. 41-51 and col. 6, II. 63-65); additionally, <u>Kerigan</u> expressly teaches the utilization of the plug and play functionality with camera type peripheral device (<u>Kerigan</u>, col. 3, II. 29-33 and col. 6, II. 3-10) to obtain the invention as specified in claim 331.

Hashimoto, Smith and Kerigan do not teach the ADGPD comprising:

without ... load any software onto the computer at any time and (b) without requiring any end user to interact with the computer to set up a file system in the

ADGPD at any time, the execution of the at least one instruction set not taking into account the identity of the manufacturer of the computer;

wherein the at least one parameter provides information to the computer about file transfer characteristics of the ADGPD; and

data transferring after the at least one parameter has been sent from the i/o port to the multi-purpose interface of the computer without requiring any user-loaded file transfer enabling software to be loaded on or installed in the computer at any time.

<u>Ristelhueber</u> teaches a system and a method comprising a peripheral device having an automatic recognition process without requiring any end user to load any software onto the computer at any time (pages 1-3), wherein the resulting combination of the references further teaches the above automatic recognition process corresponds to plug and play of a peripheral device by having a user to simply insert a peripheral into a desktop system and have it start running immediately, as the PnP computer will automatically identify any new hardware installed and configure the new hardware, and relieving the end user of any need to fumble with floppy disks and user manuals to get the device up and running; therefore, the installation of the peripheral device is accomplished without any type of user intervention at any time.

It would have been obvious for one of ordinary skill in this art, at the time of invention was made to include <u>Ristelhueber</u>'s without user intervention into <u>Hashimoto</u>, <u>Smith</u> and <u>Kerigan</u>'s plug-and-play processor, not only is such implementation well known to be in accord with the plug-and-play standard, but also for the benefit of

Application/Control Number: 11/467,092Page 70Art Unit: 2181simplifying the end user's PC upgrading and reducing cost for the computing industry(Ristelhueber, page 2, 3rd paragraph) to obtain the invention as specified in claim 331.

Hashimoto, Smith, Kerigan and Ristelhueber do not expressly teach the ADGPD comprising:

without requiring any end user to interact with the computer to set up a file system in the ADGPD at any time, the execution of the at least one instruction set not taking into account the identity of the manufacturer of the computer;

wherein the at least one parameter provides information to the computer about file transfer characteristics of the ADGPD; and

data transferring after the at least one parameter has been sent from the i/o port to the multi-purpose interface of the computer without requiring any user-loaded file transfer enabling software to be loaded on or installed in the computer at any time.

Shinohara teaches a system and a method comprising:

without requiring any end user to interact with the computer to set up a file system in the ADGPD at any time, the execution of the at least one instruction set not taking into account the identity of the manufacturer of the computer (col. 1, ll. 48-60 and col. 3, l. 33 to col. 4, l. 49), by combining the emulation of a mass storage device (e.g. hard disk drive) with <u>Hashimoto</u>, <u>Smith</u>, <u>Kerigan</u> and <u>Ristelhueber</u>'s processor in the device with plug-and-play functionality, the resulting combination of the references further teaches the above claimed feature, which is in accordance to the applicant's

disclosure of the core novelty for the instant invention as disclosed by the applicant during the interview dated 10/07/2009;

wherein the at least one parameter provides information to the computer about file transfer characteristics (e.g. associated emulating hard disk drive data transferring characteristics) of the ADGPD (col. 1, II. 48-60 and col. 3, I. 33 to col. 4, I. 49), by combining the emulation of a mass storage device (e.g. hard disk drive) with <u>Hashimoto, Smith, Kerigan and Ristelhueber</u>'s processor in the device with plug-and-play functionality, the resulting combination of the references further teaches the above claimed feature, which is in accordance to the applicant's disclosure of the core novelty for the instant invention as disclosed by the applicant during the interview dated 10/07/2009; and

data transferring after the at least one parameter has been sent from the i/o port to the multi-purpose interface of the computer (e.g. as data transfer is transferred after proper hard disk drive emulation by the peripheral device) without requiring any userloaded file transfer enabling software to be loaded on or installed in the computer at any time (col. 1, II. 48-60 and col. 3, I. 33 to col. 4, I. 49), by combining the emulation of a mass storage device (e.g. hard disk drive) with <u>Hashimoto</u>, <u>Smith</u>, <u>Kerigan</u> and <u>Ristelhueber</u>'s data transferring by the device with plug-and-play functionality, the resulting combination of the references further teaches the above claimed feature, which is in accordance to the applicant's disclosure of the core novelty for the instant invention as disclosed by the applicant during the interview dated 10/07/2009.

It would have been obvious for one of ordinary skill in this art, at the time of invention was made to include <u>Shinohara</u>'s hard disk drive emulation into <u>Hashimoto</u>, <u>Smith</u>, <u>Kerigan</u> and <u>Ristelhueber</u>'s plug-and-play processor for reading data from the memory card for the benefit of expanding the lifetime usage of the memory card (<u>Shinohara</u>, col. 2, II. 7-8) to obtain the invention as specified in claim 331.

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89. As per claim 332, <u>Hashimoto</u>, <u>Smith</u>, <u>Kerigan</u>, <u>Ristelhueber</u> and <u>Shinohara</u> teach all the limitation of claim 331 as discussed above, where <u>Hashimoto</u>, <u>Smith</u>, <u>Ristelhueber</u> and <u>Shinohara</u> further teaches the ADGPD comprising wherein the at least one parameter is consistent with the ADGPD being a mass storage device (e.g. hard disk drive) (<u>Hashimoto</u>, Fig. 8, ref. 16; Fig. 11-12; Fig. 14-15; col. 1, II. 27-57; col. 6, I. 16 to col. 9, I. 17; col. 9, I. 46 to col. 11, I. 42; col. 12, I. 16 to col. 14, I. 14; <u>Smith</u>, Fig. 2-5; col. 1, II. 9-22; col. 2, I. 40 to col. 3, I. 8; col. 3, II. 22-27; col. 3, II. 53-59; col. 4, II. 5-34; col. 6, II. 63-62; <u>Ristelhueber</u>, pages 1-3; and <u>Shinohara</u>, col. 1, II. 48-60; col. 3, I. 56 to col. 4, I. 49).

90. Claims 249-251, 257 and 259-260 are rejected under 35 U.S.C. 103(a) as being unpatentable over <u>Hashimoto et al.</u> (US Patent 6,111,604) in view of <u>Hashimoto et al.</u> (US Patent 6,111,604) in view of <u>Smith et al.</u> (US Patent 5,634,075), <u>Kerigan et al.</u> (US Patent 5,948,091), <u>Ristelhueber : "Plug and play is almost here"</u> and <u>Shinohara</u> (US Patent 5,742,934) as applied to claims 248 and 256 above, and further in view of <u>Endo et al.</u> (US Patent 4,652,928).

<u>Hashimoto</u>, <u>Smith</u>, <u>Kerigan</u>, <u>Ristelhueber</u> and <u>Shinohara</u> teach all the limitations of claim 256 as discussed above, wherein <u>Hashimoto</u> further teaches the ADGPD comprising wherein the processor is designed so that the sensor (<u>Hashimoto</u>, Fig. 8, ref. 6, 9) can be attached to the processor (<u>Hashimoto</u>, Fig. 8).

Hashimoto, Smith, Kerigan and Shinohara do not expressly teach the ADGPD comprising:

the interface device is designed so that the sensor is detachable from the interface device;

the sensor is designed to be readily disconnected from the interface device;

the interface device is designed so that a user can detach the sensor from the interface device;

the processor is designed so that the sensor is detachable therefrom;

wherein the sensor is designed to be readily disconnected from the processor; and

the processor is designed so that a user can detach the sensor therefrom.

Endo teaches the ADGPD (e.g. digital camera) comprising:

the interface device is designed so that the sensor (e.g. CCD) is detachable (e.g. decoupling) from the interface device (col. 1, II. 18-25 and col. 13, II. 57-58), by combining the decoupling of the CCD with <u>Hashimoto</u>, <u>Smith</u>, <u>Kerigan</u> and <u>Shinohara</u>'s sensor coupled to the interface device, the resulting combination of the references further teaches the above claimed limitation;

the sensor (e.g. CCD) is designed to be readily disconnected (e.g. de-coupling) from the interface device (col. 1, II. 18-25 and col. 13, II. 57-58), by combining the de-coupling of the

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CCD with <u>Hashimoto</u>, <u>Smith</u>, <u>Kerigan</u> and <u>Shinohara</u>'s sensor coupled to the interface device, the resulting combination of the references further teaches the above claimed limitation;

the interface device is designed so that a user can detach (e.g. de-coupling) the sensor (e.g. CCD) from the interface device (col. 1, II. 18-25 and col. 13, II. 57-58), by combining the de-coupling of the CCD with <u>Hashimoto</u>, <u>Smith</u>, <u>Kerigan</u> and <u>Shinohara</u>'s sensor coupled to the interface device, the resulting combination of the references further teaches the above claimed limitation;

the processor is designed so that the sensor (e.g. CCD) is detachable (e.g. decoupling) therefrom (col. 1, II. 18-25 and col. 13, II. 57-58), by combining the de-coupling of the CCD with <u>Hashimoto</u>, <u>Smith</u>, <u>Kerigan</u> and <u>Shinohara</u>'s sensor coupled to the processor, the resulting combination of the references further teaches the above claimed limitation;

wherein the sensor (e.g. CCD) is designed to be readily disconnected (e.g. de-coupling) from the processor (col. 1, II. 18-25 and col. 13, II. 57-58), by combining the de-coupling of the CCD with <u>Hashimoto</u>, <u>Smith</u>, <u>Kerigan</u> and <u>Shinohara</u>'s sensor coupled to the processor, the resulting combination of the references further teaches the above claimed limitation; and

the processor is designed so that a user can detach (e.g. de-coupling) the sensor (e.g. CCD) therefrom (col. 1, II. 18-25 and col. 13, II. 57-58), by combining the de-coupling of the CCD with <u>Hashimoto</u>, <u>Smith</u>, <u>Kerigan</u> and <u>Shinohara</u>'s sensor coupled to the processor, the resulting combination of the references further teaches the above claimed limitation.

It would have been obvious for one of ordinary skill in this art, at the time of invention was made to include <u>Endo</u>'s interchangeable sensor into <u>Hashimoto</u>, <u>Smith</u>,

<u>Kerigan</u> and <u>Shinohara</u>'s sensor coupled to the processor for the benefit of adaptively increase the resolution of the camera to obtaining a better quality image (<u>Endo</u>, col. 1, II. 18-20) to obtain the invention as specified in claims 249-251, 257 and 259-260.

91. Claim 307 is rejected under 35 U.S.C. 103(a) as being unpatentable over <u>Hashimoto et</u> <u>al.</u> (US Patent 6,111,604) in view of <u>Smith et al.</u> (US Patent 5,634,075), <u>Kerigan et al.</u> (US Patent 5,948,091), <u>Ristelhueber : "Plug and play is almost here"</u> and <u>Shinohara</u> (US Patent 5,742,934) as applied to claim 329 above, and further in view of <u>Roberts et al.</u> (US Patent 5,576,757).

Hashimoto, Smith, Kerigan, Ristelhueber and Shinohara teach all the limitations of claim 183 as discussed above, wherein Hashimoto further teaches the ADGPD comprising generating and processing of the analog data (Hashimoto, Fig. 1A-1B; Fig. 11-12; Fig. 14-15; col. 1, II. 35-57; col. 3, I. 43 to col. 4, I. 57; col. 5, II. 43-57; col. 6, I. 16 to col. 9, I. 17 and col. 9, I. 46 to col. 10, I. 16).

Hashimoto, Smith, Kerigan, Ristelhueber and Shinohara do not expressly teach the ADGPD comprising a fast Fourier transform.

<u>Roberts</u> teaches a system and a method comprising an electronic still camera processing data by being subject to a fast Fourier transform (Abstract and col. 9, I. 60 to col. 10, I. 7).

It would have been obvious for one of ordinary skill in this art, at the time of invention was made to include <u>Roberts</u>'s fast Fourier transform into <u>Hashimoto</u>, <u>Smith</u>, <u>Kerigan</u>, <u>Ristelhueber</u> and <u>Shinohara</u>'s ADGPD for the benefit of having an easier

computation for image processing while providing a reasonable visual fidelity (Roberts,

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col. 10, Il. 1-3) to obtain the invention as specified in claim 307.

V. CLOSING COMMENTS

<u>Conclusion</u>

a. STATUS OF CLAIMS IN THE APPLICATION

The following is a summary of the treatment and status of all claims in the application as recommended by **M.P.E.P. 707.07(i)**:

a(1) CLAIMS REJECTED IN THE APPLICATION

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

b. DIRECTION OF FUTURE CORRESPONDENCES

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chun-Kuan (Mike) Lee whose telephone number is (571) 272-0671. The examiner can normally be reached on 8AM to 5PM.

IMPORTANT NOTE

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Alford Kindred can be reached on (571) 272-4037. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/C.K.L./

October 23, 2009 /Alford W. Kindred/ Supervisory Patent Examiner, Art Unit 2181 Chun-Kuan (Mike) Lee Examiner Art Unit 2181

Docket No.: 31436/43993 (PATENT)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of: Michael Tasler

Application No.: 11/467,092

Filed: August 24, 2006

Confirmation No.: 3038

Art Unit: 2181

For: ANALOG DATA GENERATING AND Examiner: C. K. Lee PROCESSING DEVICE HAVING A MULTI-USE AUTOMATIC PROCESSOR (as amended)

AMENDMENT

MS Amendment Commissioner for Patents P.O. Box 1450 Alexandria, VA 22313-1450

Dear Sir:

INTRODUCTORY COMMENTS

Please enter this amendment in response to the Office Action mailed from the USPTO on

March 2, 2009. A petition and fee for a three month extension of time are being filed herewith.

Amendments to the Title and the Drawings are on page 2 of this paper.

Amendments to the Specification start on page 2 of this paper.

The Listing of the Claims begins on page 8 of this paper.

Remarks/Arguments begin on page 26 of this paper.

Amendment To The Title:

Please amend the title of this application to read as follows: Analog Data Generating And Processing Device Having A Multi-Use Automatic Processor.

Amendment To The Drawings:

Replacement drawings are submitted herewith to add a lead line in Figure 2 from number 1260 to the EPP box as noted in the Office Action. Approval of the replacement drawings is earnestly solicited.

Amendments To The Specification:

1. Replace paragraph [0001] of the specification in its entirety with the following paragraph:

[0001] This application is a continuation of application Ser. No. 11/078,778, filed March 11, 2005, now currentlypending expressly abandoned, which is a continuation of application Ser. No. 10/219,105, filed August 15, 2002, now Pat. No. 6,895,449, which is a divisional of application Ser. No. 09/331,002, filed Jun. 14, 1999, now Pat. No. 6,470,399.

2. Replace paragraph [0009] of the specification in its entirety with the following

paragraph:

[0009] A solution to this problem is offered by the interface devices of IOtech (business address: 25971 Cannon Road, Cleveland, Ohio 44146, USA) which are suitable for laptops such as the WaveBook/512 (registered trademark). The interface devices are connected by means of a plug-in card, approximately the size of a credit card, to the <u>PCMCIApersonal</u> <u>computer memory card association (PCMIA)</u> interface which is now a standard feature in laptops. The plug-in card converts the PCMCIA interface into an interface known in the art

as **IEEE**<u>Institute of Electrical and Electronics (IEEE)</u> 1284. The said plug-in card provides a special printer interface which is enhanced as regards the data transfer rate and delivers a data transfer rate of approximately 2 MBps as compared with a rate of approx. 1 MBps for known printer interfaces. The known interface device generally consists of a driver component, a digital signal processor, a buffer and a hardware module which terminates in a connector to which the device whose data is to be acquired is attached. The driver component is attached directly to the enhanced printer interface thus permitting the known interface device to establish a connection between a computer and the device whose data is to be acquired.

3. Replace paragraph [0013] of the specification in its entirety with the following paragraph:

[0013] The specialist publication IBM Technical Disclosure Bulletin, Vol. 38, No. 05, page 245; "Communication Method between Devices through FDD Interface" discloses an interface which connects a host device to a peripheral device via a floppy disk drive interface. The interface consists in particular of an address generator, an MFMmodified frequency modulation (MFM) encoder/decoder, a serial/parallel adapter and a format signal generator. The interface makes it possible to attach not only a floppy disk drive (FDD) but also a further peripheral device to the FDD host controller of a host device. The host device assumes that a floppy disk drive is always attached to its floppy disk drive controller and communication is initiated if the address is correct. However, this document contains no information as to how communication should be possible if the interface is connected to a multi-purpose interface instead of to a floppy disk drive controller.

4. Replace paragraph [0015] of the specification in its entirety with the following paragraph:

[0015] The present invention is based on the finding that both a high data transfer rate and host device-independent use can be achieved if a driver for an input/output device customary in a host device, normally present in most commercially available host devices, is

utilized. Drivers for input/output devices customary in a host device which are found in practically all host devices are, for example, drivers for hard disks, for graphics devices or for printer devices. As however the hard disk interfaces in common host devices which can be, for example, IBM PCs-personal computers (PCs), IBM-compatible PCs, Commodore PCs, Apple computers or even workstations, are the interfaces with the highest data transfer rate, the hard disk driver is utilized in the preferred embodiment of the interface device of the present invention. Drivers for other storage devices such as floppy disk drives, CD-ROM compact disk read-only memory (CD-ROM) drives or tape drives could also be utilized in order to implement the interface device according to the present invention.

5. Replace paragraph [0016] of the specification in its entirety with the following paragraph:

[0016] As described in the following, the interface device according to the present invention is to be attached to a host device by means of a multi-purpose interface of the host device which can be implemented, for example, as an SCSI-small computer systems interface (SCSI) interface or as an enhanced printer interface. Multi-purpose interfaces comprise both an interface card and specific driver software for the interface card. The driver software can be designed so that it can replace the BIOS-basic input/output system (BIOS) driver routines. Communication between the host device and the devices attached to the multi-purpose interface then essentially takes place by means of the specific driver software for the multipurpose interface and no longer primarily by means of BIOS routines of the host device. Recently however drivers for multi-purpose interfaces can also already be integrated in the BIOS system of the host device as, alongside classical input/output interfaces, multi-purpose interfaces are becoming increasingly common in host devices. It is of course also possible to use BIOS routines in parallel with the specific driver software for the multipurpose interface, if this is desired.

6. Replace paragraph [0023] of the specification in its entirety with the following paragraph:

> [0023] Communication between the host system or host device and the interface device is based on known standard access commands as supported by all known operating systems (e.g. DOS-DOS[®], Windows-Windows[®], Unix-Unix[®]). Preferably, the interface device according to the present invention simulates a hard disk with a root directory whose entries are "virtual" files which can be created for the most varied functions. When the host device system with which the interface device according to the present invention is connected is booted and a data transmit/receive device is also attached to the interface device 10, usual BIOS routines or multi-purpose interface programs issue an instruction, known by those skilled in the art as the INQUIRY instruction, to the input/output interfaces in the host device. The digital signal processor 13 receives this inquiry instruction via the first connecting device and generates a signal which is sent to the host device (not shown) again via the first connecting device 12 and the host line 11. This signal indicates to the host device that, for example, a hard disk drive is attached at the interface to which the INQUIRY instruction was sent. Optionally, the host device can send an instruction, known by those skilled in the art as "Test Unit Ready", to the interface device to request more precise details regarding the queried device.

7. Replace paragraph [0027] of the specification in its entirety with the following paragraph:

[0027] In addition to the digital signal processor instruction memory, which comprises the operating system of the digital signal processor and can be implemented as an EPROM erasable programmable read-only memory (EPROM) or EEPROM electrically erasable programmable read-only memory (EEPROM), the memory means 14 can have an additional buffer for purposes of synchronizing data transfer from the data transmit/receive device to the interface device 10 and data transfer from the interface device 10 to the host device.

8. Replace paragraph [0028] of the specification in its entirety with the following paragraph:

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[0028] Preferably, the buffer is implemented as a fast random access memory or RAM random access memory (RAM) buffer.

9. Replace paragraph [0030] of the specification in its entirety with the following paragraph:

[0030] As a result of the option of storing any files in agreed formats in the memory means 14 of the interface device 10, taking into account the maximum capacity of the memory means, any enhancements or even completely new functions of the interface device 10 can be quickly implemented. Even files executable by the host device, such as batch files or executable files (BAT or EXE files), and also help files can be implemented in the interface device, thus achieving independence of the interface device. On the one hand, this avoids licensing and/or registration problems and, on the other hand, installation of certain routines which can be frequently used, for example an FFT fast Fourier transformation (FFT) routine to examine acquired time-domain data in the frequency domain, is rendered unnecessary as the EXE files are already installed on the interface device 10 and appear in the virtual root directory, by means of which the host device can access all programs stored on the interface device 10.

10. Replace paragraph [0041] of the specification in its entirety with the following paragraph:

[0041] The complete interface device 10 is supplied with power by an external AC/DC alternating current to direct current (AC/DC) converter 2230 which delivers a digital supply voltage of .+-.5 V and is attached to a DC/DC-direct current to direct current (DC/DC) converter 2240 which can deliver analog supply voltages of .+-.5 V and .+-.15 V as required for the interface device 10. Further, the DC/DC direct current to direct current (DC/DC) converter controls a precision voltage reference 2250 which controls the 8 Bayonet Neill Concelman (BNC) inputs 1505 and the ADC 1530 as well as a digital/analog converter (DAC) 2260 which permits, via an output amplifier block with 4 output amplifiers 2270 and

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a 9-pin connector 2280, analog output direct from the DSP 1300 to an output device, e.g. printer device or monitor device, which can be attached via the 9-pin connector 2280, thus providing the option of monitoring the data transferred to the host device or also, for example, of viewing an FFT to obtain rapid and comprehensive data analysis without using processor time of the host device.

11. Replace paragraph [0048] of the specification in its entirety with the following

paragraph:

[0048] As described above, the interface device 10 is supplied with power by means of an external AC/DC adapter which has a universal power input (85-264 VAC, 47-63 Hz). Interference suppression complies with the standards EN 55022, curve B and FFC, Class B). Further, it is also in accordance with international safety regulations (TUV, UL, CSA, TuV (Technischer Überwachongsverein), UL (Underwriters Laboratories), CSA (Canadian Standard Association). The interface device 10 is externally shielded and achieves a value of 55 dB at 30-60 MHz and a value of approximately 40 dB at 1 GHz, and therefore complies with the <u>MILSTD-military standarsd (MILSTD)</u> 285-1 standard.

Amendments To The Claims:

Please cancel claims 1-238 and please new claims 239-332 as follows:

1-238. (cancelled).

239. (new) An analog data generating and processing device (ADGPD), comprising:an input/output (i/o) port;

a program memory;

a data storage memory;

a processor operatively interfaced with the i/o port, the program memory and the data storage memory;

wherein the processor is adapted to be involved in a data generation process by which analog data is generated, the analog data is processed, and the processed analog data is stored in the data storage memory as at least one file of digitized analog data;

wherein the processor also is adapted to be involved in an automatic recognition process in which, when the i/o port is operatively interfaced with a multi-purpose interface of a computer, the processor executes at least one instruction set stored in the program memory and thereby causes at least one parameter to be automatically sent through the i/o port and to the multi-purpose interface of the computer (a) without requiring any end user to load any software onto the computer at any time and (b) without requiring any end user to interact with the computer to set up a file system in the ADGPD at any time;

wherein the at least one parameter provides information to the computer about file transfer characteristics of the ADGPD; and

wherein the processor is further adapted to be involved in an automatic file 8

transfer process in which, when the i/o port is operatively interfaced with the multi-purpose interface of the computer, and after the at least one parameter has been sent from the i/o port to the multi-purpose interface of the computer, the processor executes at least one other instruction set stored in the program memory and thereby causes the at least one file of digitized analog data to be transferred to the computer without requiring any user-loaded file transfer enabling software to be loaded on or installed in the computer at any time.

240. (new) The ADGPD of claim 239, wherein the i/o port, the program memory, the data storage memory, and the processor form an interface device.

241. (new) The ADGPD of claim 240, wherein the interface device allows for a plurality of different data transmit devices to be attached thereto and detached therefrom.

242. (new) The ADGPD of claim 240, wherein the interface device comprises a portable interface device.

243. (new) The ADGPD of claim 240, wherein the interface device comprises a flexible interface device.

244. (new) The ADGPD of claim 240, wherein the interface device comprises a universal interface device.

245. (new) The ADGPD of claim 240, wherein the interface device comprises a stand alone interface device.

246. (new) The ADGPD of claim 240, wherein the interface device includes a parallel logic circuit.

247. (new) The ADGPD of claim 240, wherein the interface device includes a SCSI

interface circuit.

248. (new) The ADGPD of claim 240, wherein the interface device is operatively interfaced with a sensor that is designed to generate the analog data.

249. (new) The ADGPD of claim 248, wherein the interface device is designed so that the sensor is detachable from the interface device.

250. (new) The ADGPD of claim 248, wherein the sensor is designed to be readily disconnected from the interface device.

251. (new) The ADGPD of claim 248, wherein the interface device is designed so that a user can attach the sensor to or detach the sensor from the interface device.

252. (new) The ADGPD of claim 239, wherein the i/o port comprises a parallel port.

253. (new) The ADGPD of claim 239, wherein the i/o port comprises a SCSI

connector.

254. (new) The ADGPD of claim 239, wherein the i/o port is adapted to be interfaced with a multi-purpose interface of an external computing device only by means of a cable.

255. (new) The ADGPD of claim 239, wherein the i/o port is adapted to be physically connected to a multi-purpose interface of an external computing device by a cable.

256. (new) The ADGPD of claim 239 further comprising a sensor that is operatively interfaced with the processor and that is designed to generate the analog data.

257. (new) The ADGPD of claim 256, wherein the processor is designed so that the sensor is detachable therefrom.

258. (new) The ADGPD of claim 256, wherein the processor allows for a plurality of

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different data transmit devices to be attached thereto and detached therefrom.

259. (new) The ADGPD of claim 256, wherein the sensor is designed to be readily disconnected from the processor.

260. (new) The ADGPD of claim 256, wherein the processor is designed so that a user can attach the sensor to or detach the sensor therefrom.

261. (new) The ADGPD of claim 256, wherein the sensor comprises a data transmit/receive device.

262. (new) The ADGPD of claim 261, wherein the data transmit/receive device is designed for two-way communication with a host device.

263. (new) The ADGPD of claim 261, wherein the data transmit/receive device is designed for one-way or two-way communication with a host device.

264. (new) The ADGPD of claim 261, wherein the data transmit/receive device is designed to receive data from a host device.

265. (new) The ADGPD of claim 239, further comprising a multimeter that is operatively interfaced with the processor and that is designed to generate the analog data.

266. (new) The ADGPD of claim 239, further comprising at least first and second transducers both of which are designed to transmit data and are operatively interfaced with the processor.

267. (new) The ADGPD of claim 239, wherein the at least one parameter is consistent with the ADGPD being an information storage device other than a magnetic floppy disk drive.

268. (new) The ADGPD of claim 239, wherein the at least one parameter is consistent

with the ADGPD being a mass storage device.

269. (new) The ADGPD of claim 239, wherein the at least one parameter is consistent with the ADGPD being responsive to a SCSI inquiry command.

270. (new) The ADGPD of claim 239, wherein the at least one parameter is not consistent with the true nature of the ADGPD.

271. (new) The ADGPD of claim 239, wherein the at least one parameter does not indicate that the ADGPD includes a sensor that is designed to generate the analog data.

272. (new) The ADGPD of claim 239, wherein the at least one parameter is consistent with the ADGPD being an input/output device.

273. (new) The ADGPD of claim 239, wherein the at least one parameter is consistent with the ADGPD being an input/output device located within an interior of a housing of a personal computing device.

274. (new) The ADGPD of claim 239, wherein the at least one parameter is consistent with the ADGPD being adapted to operate in a manner consistent with a hard disk drive.

275. (new) The ADGPD of claim 239, wherein the at least one parameter is consistent with the ADGPD being a hard disk drive.

276. (new) The ADGPD of claim 239, wherein the at least one parameter is consistent with the ADGPD being an input/output device that is customary in a host device.

277. (new) The ADGPD of claim 239, wherein the at least one parameter is consistent with the ADGPD being responsive to commands issued from a customary driver.

278. (new) The ADGPD of claim 239, wherein the data storage memory comprises a

temporary memory.

279. (new) The ADGPD of claim 239, wherein the data storage memory comprises a semiconductor based memory.

280. (new) The ADGPD of claim 239, wherein the data storage memory comprises random access memory.

281. (new) The ADGPD of claim 239, wherein the data storage memory comprises a single memory device.

282. (new) The ADGPD of claim 239, wherein the program memory comprises electronically programmable read only memory.

283. (new) The ADGPD of claim 239, wherein the processor is adapted to, when the i/o port is operatively interfaced with the multi-purpose interface of the computer, and after the at least one parameter has been sent to the multi-purpose interface of the computer, execute at least one set of computer code stored in the program memory and thereby cause ADGPD file system information to be automatically sent to the i/o port (a) without requiring any end user to load any software onto the computer at any time and (b) without requiring any end user to interact with the computer to set up a file system in the ADGPD at any time.

284. (new) The ADGPD of claim 283, wherein the ADGPD file system information comprises at least an indication of the type of a file system that is used to store the at least one file of digitized analog data in the data storage memory.

285. (new) The ADGPD of claim 283, wherein the at least one parameter is consistent with the ADGPD being an information storage device other than a magnetic floppy disk drive.

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286. (new) The ADGPD of claim 285, wherein the at least one parameter is consistent with the ADGPD being a mass storage device.

287. (new) The ADGPD of claim 286,

wherein the processor and the program memory are adapted to be configured to cause, after the at least one parameter has been sent to the i/o port, file allocation table information to be sent to the i/o port,

wherein the processor and the program memory are adapted to be configured to cause a virtual boot sequence to be sent to the i/o port which includes at least information that is representative of a number of sectors of a storage disk, and

wherein the file allocation table information includes at least a start location of a file allocation table.

288. (new) The ADGPD of claim 287, wherein the at least one parameter is consistent with the ADGPD being adapted to operate in a manner consistent with a hard disk drive.

289. (new) The ADGPD of claim 288, wherein the at least one parameter is consistent with the ADGPD being a hard disk drive.

290. (new) The ADGPD of claim 239, wherein the processor includes a single central processing unit.

291. (new) The ADGPD of claim 239, wherein the program memory comprises a single memory device.

292. (new) The ADGPD of claim 239, wherein the program memory is formed in a single chip.

293. (new) The ADGPD of claim 239, wherein the processor comprises a microprocessor.

294. (new) The ADGPD of claim 239, wherein the processor comprises a single microprocessor.

295. (new) The ADGPD of claim 239, wherein the processor comprises a digital signal processor.

296. (new) The ADGPD of claim 239, wherein the processor comprises a single digital signal processor.

297. (new) The ADGPD of claim 239, wherein the processor and the program memory are adapted to be configured to initiate a process by which the at least one file of digitized analog data stored in the data storage memory are directly transferred to an input/output device by means of the i/o port.

298. (new) The ADGPD of claim 297, wherein the processor and the program memory are adapted to allow an aspect of operation of the ADGPD other than the transfer of at least some of the at least one file of digitized analog data from the data storage memory to the i/o port to be controlled by means of an external computer with which the i/o port is interfaced.

299. (new) The ADGPD of claim 239, wherein the ADGPD comprises at least a portion of a medical device.

300. (new) The ADGPD of claim 239, wherein the ADGPD comprises at least a portion of a data acquisition system.

301. (new) The ADGPD of claim 239, wherein the ADGPD is designed for use with

an external computing device that has an operating system that is designed by a particular software company.

302. (new) The ADGPD of claim 239, wherein the processor is adapted to, when it is involved in the automatic recognition process, to execute the at least one instruction set to thereby directly cause the at least one parameter regarding the ADGPD to be automatically sent.

303. (new) The ADGPD of claim 239, wherein the processor is adapted to be employed in the automatic recognition process.

304. (new) The ADGPD of claim 239, wherein the processor is adapted to be directly involved in all aspects of the automatic recognition process.

305. (new) The ADGPD of claim 239, wherein the processor is adapted to be employed in the data generation process.

306. (new) The ADGPD of claim 239, wherein the processor is adapted to be directly involved in all aspects of the data generation process.

307. (new) The ADGPD of claim 239, wherein the analog data is, when the analog data generation process takes place, processed by being subject to a fast Fourier transform.

308. (new) The ADGPD of claim 239, wherein the processed analog data is stored in the data storage memory as only one file of digitized analog data.

309. (new) The ADGPD of claim 239, wherein the ADGPD is designed so that both the analog data generation and automatic file transfer processes, when they occur, take place only after the automatic recognition process has been executed.

310. (new) The ADGPD of claim 239, wherein the analog data generation and

automatic file transfer processes, when they occur, at least partially overlap in time.

311. (new) The ADGPD of claim 239, wherein the ADGPD is designed so that the analog data generation process, when it occurs, takes place only after the i/o port is interfaced with a host device.

312. (new) The ADGPD of claim 239 further comprising a sensor that is operatively interfaced with the processor and that is designed for two-way communication with a host device.

313. (new) The ADGPD of claim 239 further comprising a sensor that is operatively interfaced with the processor and that is designed for one-way or two-way communication with a host device.

314. (new) The ADGPD of claim 239 further comprising a sensor that is operatively interfaced with the processor and that is designed to receive data from a host device.

315. (new) The ADGPD of claim 239 further comprising a sensor that is operatively interfaced with the processor and that is designed to receive signals from a host device.

316. (new) The ADGPD of claim 239, wherein the ADGPD is designed so that at least one aspect of how the ADGPD creates the at least one file of digitized analog data can be controlled by means of commands that are issueable from a source external to the ADGPD.

317. (new) The ADGPD of claim 316, wherein the ADGPD is designed so that the at least one aspect is controlled by means of a configuration file.

318. (new) The ADGPD of claim 239, wherein the ADGPD is designed to be responsive to a test unit ready command.

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319. (new) The ADGPD of claim 239, wherein the set of instructions executed by the processor in the automatic recognition process is stored in a single memory device.

320. (new) The ADGPD of claim 239, wherein the set of instructions executed by the processor in the automatic file transfer process is stored in a single memory device.

321. (new) A combination comprising the ADGPD of claim 239 and a computer.

322. (new) The combination of claim 321, wherein the computer includes a driver for an input/output device customary in a host device.

323. (new) The combination of claim 321, wherein the computer includes at least one customary driver.

324. (new) The combination of claim 321, wherein the computer includes at least one driver for an input/output device customary in a host device.

325. (new) An analog data generating and processing device (ADGPD), comprising: an input/output (i/o) port;

a program memory;

a data storage memory;

a processor operatively interfaced with the i/o port, the program memory and the data storage memory;

wherein the processor is adapted to be involved in a data generation process by which analog data is generated, the analog data is processed, and the processed analog data is stored in the data storage memory as at least one file of digitized analog data;

wherein the processor also is adapted to be involved in an automatic recognition

process in which, when the i/o port is operatively interfaced with a multi-purpose interface of a computer, the processor executes at least one instruction set stored in the program memory and thereby causes at least one parameter to be automatically sent through the i/o port and to the multi-purpose interface of the computer (a) without requiring any end user to load any software onto the computer at any time and (b) without requiring any end user to interact with the computer to set up a file system in the ADGPD at any time;

wherein the at least one parameter provides information that the ADGPD is a mass storage device that operates in a manner consistent with a hard disk drive;

wherein the processor is adapted to, when the i/o port is operatively interfaced with the multi-purpose interface of the computer, and after the at least one parameter has been sent to the multi-purpose interface of the computer, execute one or more other instruction sets stored in the program memory and thereby cause ADGPD file system information to be automatically sent to the i/o port (a) without requiring any end user to load any software onto the interfaced computing device at any time and (b) without requiring any end user to enter interact with the computer to set up a file system in the ADGPD at any time, the ADGPD file system information comprising at least an indication of the type of a file system that is used to store the at least one file of digitized analog data in the data storage memory;

wherein the processor is further adapted to be involved in an automatic file transfer process in which, when the i/o port is operatively interfaced with the multi-purpose interface of the computer, and after the at least one parameter has been sent from the i/o port to the multi-purpose interface of the computer, the processor executes at least one set of computer

code stored in the program memory and thereby causes the at least one file of digitized analog data to be transferred to the computer without requiring any user-loaded file transfer enabling software to be loaded on or installed in the computer at any time;

wherein the processor and the program memory are adapted to be configured to cause, after the at least one parameter has been sent to the i/o port, file allocation table information to be sent to the i/o port, the file allocation table information including at least a start location of a file allocation table; and

wherein the processor and the program memory are adapted to be configured to cause a virtual boot sequence to be sent to the i/o port which includes at least information that is representative of a number of sectors of a storage disk.

326. (new) The ADGPD of claim 325, wherein the at least one parameter is consistent with the ADGPD being a hard disk drive.

327. (new) An analog data generating and processing device (ADGPD), comprising: an input/output (i/o) port;

a program memory;

a data storage memory;

a processor operatively interfaced with the i/o port, the program memory and the data storage memory;

wherein the processor is adapted to be involved in a data generation process by which analog data is generated, the analog data is processed, and the processed analog data is stored in the data storage memory as at least one file of digitized analog data;

wherein the processor also is adapted to be involved in an automatic recognition process in which, when the i/o port is operatively interfaced with a multi-purpose interface of a computer, the processor executes at least one instruction set stored in the program memory and thereby causes at least one parameter to be automatically sent through the i/o port and to the multi-purpose interface of the computer (a) without requiring any end user to load any software onto the computer at any time, (b) without requiring any end user to interact with the computer to set up a file system in the ADGPD at any time, and (c) regardless of the identity of a manufacturer of the computer;

wherein the at least one parameter provides information to the computer about file transfer characteristics of the ADGPD; and

wherein the processor is further adapted to be involved in an automatic file transfer process in which, when the i/o port is operatively interfaced with the multi-purpose interface of the computer, and after the at least one parameter has been sent from the i/o port to the multi-purpose interface of the computer, the processor executes at least one other instruction set stored in the program memory and thereby causes the at least one file of digitized analog data to be transferred to the computer regardless of the identity of the manufacturer of the computer and without requiring any user-loaded file transfer enabling software to be loaded on or installed in the computer at any time.

328. (new) The ADGPD of claim 327, wherein the at least one parameter is consistent with the ADGPD being a mass storage device.

329. (new) An analog data generating and processing device (ADGPD), comprising:

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an input/output (i/o) port;

a program memory;

a data storage memory;

a processor operatively interfaced with the i/o port, the program memory and the data storage memory;

wherein the processor is adapted to be involved in a data generation process by which analog data is generated, the analog data is processed, and the processed analog data is stored in the data storage memory as at least one file of digitized analog data;

wherein the processor also is adapted to be involved in an automatic recognition process

(a) in which, when the i/o port is operatively interfaced with a multipurpose interface of a first computer, the processor executes at least one instruction set stored in the program memory and thereby causes at least one parameter to be automatically sent through the i/o port and to the multi-purpose interface of the first computer without requiring any end user to load any software onto the computer at any time and without requiring any end user to interact with the first computer to set up a file system in the ADGPD at any time, and

(b) in which, when the i/o port is operatively interfaced with a multipurpose interface of a second computer that is manufactured by a company other than the company that manufactured the first computer, the processor executes the at least one instruction set stored in the program memory and thereby causes the at least one parameter to be automatically sent through the i/o port and to the multi-purpose interface of the second computer

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without requiring any end user to load any software onto the second computer at any time and without requiring any end user to interact with the second computer to set up a file system in the ADGPD at any time;

wherein the at least one parameter provides information to the computer about file transfer characteristics of the ADGPD; and

wherein the processor is further adapted to be involved in an automatic file transfer process

(a) in which, when the i/o port is operatively interfaced with the multipurpose interface of the first computer, and after the at least one parameter has been sent from the i/o port to the multi-purpose interface of the first computer, the processor executes at least one other instruction set stored in the program memory and thereby causes the at least one file of digitized analog data to be transferred to the first computer without requiring any user-loaded file transfer enabling software to be loaded on or installed in the computer at any time, and

(b) in .which, when the i/o port is operatively interfaced with the multipurpose interface of the second computer, and after the at least one parameter has been sent from the i/o port to the multi-purpose interface of the second computer, the processor executes the at least one other instruction set stored in the program memory and thereby causes the at least one file of digitized analog data to be transferred to the first computer without requiring any userloaded file transfer enabling software to be loaded on or installed in the computer at any time.

330. (new) The ADGPD of claim 329, wherein the at least one parameter is consistent with the ADGPD being a mass storage device.

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331. (new) An analog data generating and processing device (ADGPD), comprising:an input/output (i/o) port;

a program memory;

a data storage memory;

a processor operatively interfaced with the i/o port, the program memory and the data storage memory;

wherein the processor is adapted to be involved in a data generation process by which analog data is generated, the analog data is processed, and the processed analog data is stored in the data storage memory as at least one file of digitized analog data;

wherein the processor also is adapted to be involved in an automatic recognition process in which, when the i/o port is operatively interfaced with a multi-purpose interface of a computer, the processor executes at least one instruction set stored in the program memory and thereby causes at least one parameter to be automatically sent through the i/o port and to the multi-purpose interface of the computer (a) without requiring any end user to load any software onto the computer at any time and (b) without requiring any end user to interact with the computer to set up a file system in the ADGPD at any time, the execution of the at least one instruction set not taking into account the identity of the manufacturer of the computer;

wherein the at least one parameter provides information to the computer about file transfer characteristics of the ADGPD; and

wherein the processor is further adapted to be involved in an automatic file transfer process in which, when the i/o port is operatively interfaced with the multi-purpose

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interface of the computer, and after the at least one parameter has been sent from the i/o port to the multi-purpose interface of the computer, the processor executes at least one other instruction set stored in the program memory and thereby causes the at least one file of digitized analog data to be transferred to the computer without requiring any user-loaded file transfer enabling software to be loaded on or installed in the computer at any time.

332. (new) The ADGPD of claim 331, wherein the at least one parameter is consistent with the ADGPD being a mass storage device.

REMARKS

Preliminary Comments

This responds to the Office Action dated March 2, 2009. Claims 1-238 have been cancelled. New claims 239-332 are submitted for the Examiner's consideration. New claims 321, 325, 327 and 329, as well as the claims depending therefrom, contain all of the limitations but also are narrower in scope than independent claim 239.

For purposes of clarity, applicant states that all of the remarks and arguments made in all previous communications with the Examiner about the purported "plug and play functionality" were made only with reference to a situation where a peripheral of one manufacturer was plugged into a PC of a different manufacturer. With that said, the Examiner is respectfully requested to consider only the remarks and amendments made in this Amendment, as well as any remarks made only about this application in any interview that takes place after this document is filed, when considering the patentability of the newly submitted claims.

Regarding the interpretation of each one of the new claims, it is respectfully submitted that it is not proper to read into any such claim a limitation that is not specifically recited therein. For example, it is not proper to write into independent claim 239 any of the features recited in, for example, any of the dependent claims 240-320 or any of the combination claims 321-324. As specific examples of this, it is not proper to limit the scope of claim 239 to affirmatively require a "stand-alone interface device" recited in dependent claim 245 or the "computer" recited in combination claim 321. As another specific example of this, it is improper to limit the scope of the "processor" recited in either of claims 239, 325, 327 or 329 to cover only a single

microprocessor or digital signal processor that may be formed in a single chip or in several physically separate chips.

Acceptance of the previously filed terminal disclaimer is earnestly solicited.

On page 30 of the Office Action, it is alleged that the 1/7/09, the 1/26/2009, and the 2/6/09 IDSs fail to comply with 37 CFR 1.98(a)(2). The 1449 forms attached to the Office Action indicate that certain references from these IDSs were not considered by the Examiner. It is believed that legible copies of the noted references were transmitted to the USPTO because pdf files of them were successfully uploaded using the USPTO Electronic Filing System. However, additional legible copies of the missing references are being submitted for the Examiner's consideration in connection with the IDS that is being filed herewith.

The Examiner is respectfully requested to review all of the prior art of record when considering the patentability of the new claims.

Replacement drawings are also being submitted herewith. Approval of the replacement drawings is earnestly solicited.

Applicant proposes to amend the title to be "Analog Data Generating And Processing Device Having A Multi-Use Automatic Processor." The Examiner's approval of the proposed new title for the invention is earnestly solicited.

Various paragraphs of the specification have been amended in accordance with the suggestions noted in the Office Action. Approval of the specification with these changes is earnestly solicited.

On pages 33-35 of the Office Action, the Examiner made certain objections to the

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cancelled claims. The new claims have been carefully reviewed in view of the Examiner's comments and to provide proper antecedent basis. The Examiner's confirmation that the new claims are not subject to objection or rejection under 35 USC §112 is earnestly solicited.

The Interview Summary Record Inadvertently Misstates What The Claimed Invention Is

It is respectfully submitted that the interview summary record attached to the Office Action does not accurately reflect what was discussed at the last personal interview. The statement that the "novelty of the invention corresponds to the end result/outcome of the peripheral device operating in correspondence to plug-and-play" gives the misleading impression that the claimed invention simply concerns an implementation of the 1994 plug and play standard ("PNP standard"). That is not the case. As discussed in greater detail below, to use a first manufacturer's peripheral device that only implements the PNP standard with a PC of a second manufacturer, a user must load at least a device/vendor specific driver onto that particular PC at least one time, which is the antithesis of the *multi-use automatic processor* feature of all of the new claims.

Today, the words "plug and play" have a loose meaning. However, today's loose meaning of "plug and play" is not prior art and has nothing to do with the PNP standard from the early 90s that is at issue in the Smith and Ristelhueber references. It appears that the interview summary record inadvertently conflates today's loose meaning of "plug and play" with the prior art PNP standard. This conflation is not proper, and does not provide a legitimate basis to reject the newly submitted claims.

Unlike peripherals that operate only in accordance with the PNP standard as it was understood at the time the invention was made, the implementation of the claimed invention in a peripheral device makes it possible to be able to transfer a file of self-generated digitized analog data to different PCs without requiring any end user to, for example, load any software <u>at any</u> time (not even once) on any particular one of the plurality of PCs to which the device is connected. Instead, at least one software driver that is already present in that particular PC when it is sold from a computer manufacturer or seller to a first end user is able to handle the file transfer.

This is accomplished by, in accordance with the *multi-use automatic processor* claim feature, automatically sending "at least one parameter" from a peripheral device incorporating the claimed invention to a computer. The "at least one parameter" provides information to the computer about file transfer characteristics of the peripheral without requiring a user to, for example, load software onto the computer with which the peripheral is interfaced. After the computer receives and processes the at least one parameter, the computer "understands" how to have files transferred to it from the peripheral device. At the personal interview, it was discussed that the "at least one parameter" reads on, for example, the non-vendor specific code(s) that are sent to indicate that the peripheral device is a mass storage device (*e.g.*, a hard disk drive) and as a response to an inquiry command. The new claims cover but are not limited to this subject matter.

The new claims also cover other subject matter. The "at least one parameter" also reads on, for example, an Interface Descriptor for a Mass Storage Class device which identifies the

device as having a bInterfaceClass = 0x08, a bInterfaceSubClass = 0x06 and a bInterfaceProtocol = 0x50. Another example of the "at least one parameter" is, for example, an Interface Descriptor for a Media or Picture Transport Protocol device which identifies the device as having a bInterfaceClass = 0x06. Both of these Interface Descriptors are provided as a response to a "Get_Descriptor" USB inquiry command. The new claims cover but are not limited to this subject matter.

In an effort to expedite the prosecution of this application, additional language has been added into all of the new claims to further clarify the differences between them and the prior art. In particular, the *multi-use automatic processor* claim feature has been amended to specify that it is further adapted to be involved in an automatic file transfer process which takes place after the at least one parameter has been sent from the i/o port to a multi-purpose interface of a particular computer with which the claimed device is interfaced. In accordance with this process, the processor executes at least one instruction to cause one or more user-selected files to be transferred to the particular computer with which the claimed device is interfaced at any time onto the PC after it has been sold to its initial end user.

The utilization of the *multi-use automatic processor* claim feature allows, for example, a file of digitized analog data to be sent from the claimed device to at least first and second computers that are manufactured by different companies. As a specific example of this, the claimed device can be used to transfer a digitized analog data file to a multi-purpose interface of, for example, either a Compaq brand computer or a Dell brand computer without also requiring

user-loaded software to be added to either computer and without requiring a user to interact with either computer to set up a file system in the claimed device. Note new claims 327-332. Also, note that neither the first computer nor the second computer of claims 329-330 are elements of the claims.

It is respectfully submitted that, based on the arguments provided herein, it is not proper to contend that the *multi-use automatic processor* feature of the new claims be given a broadest reasonable interpretation that reads on any purported combination of Hashimoto, Smith, Ristelhueber, Kerigan and Shinohara. As such, it is respectfully submitted that the new claims are patentable over all prior art of record.

<u>The Office Action Does Not Establish A Prima Facie Case Of Obviousness Because No</u> <u>Reference Teaches Or Suggests The Multi-Use Automatic Processor Claim Feature</u>

The Office Action purports to lay out a *prima facie* case of obviousness based on a combination of Hashimoto, Smith, Ristelhueber, Kerigan and Shinohara. In this combination, only Ristelhueber and Smith are alleged to teach the following aspect of the *multi-use automatic processor* claim feature: the ability to send to a PC at least one "parameter" which provides information about file transfer characteristics of a peripheral device incorporating the claimed invention to a computer to which it is connected without any end user at any time (not even once) having to, for example, load any software onto the computer. The Office Action also purports to lay out a *prima facie* case of obviousness that Hashimoto teaches an "automatic recognition" feature and, therefore, allegedly requires no user-loaded software.

Pursuant to MPEP § 2142 (8th Ed., Rev. 7, July 2008), the Examiner bears the initial burden of factually supporting an obviousness rejection. Applicant challenges the rejections

stated in the Office Action because, as discussed in greater detail hereinafter, they are based on a number of erroneous assumptions or factual predicates, and the Office Action improperly ignores prior art that contradicts factual contentions made therein. *See In re Rouffet*, 149 F.3d 1350, 1355 (Fed. Cir. 1998) (An "applicant may specifically challenge an obviousness rejection by showing that the Board" based "its obviousness determination on incorrect factual predicates."). For the reasons discussed in greater detail hereinafter, the new claims are not subject to rejection on the grounds stated in the Office Action, are patentable, and are in condition for allowance.

<u>The Factual Assertions Made About Smith And Ristelhueber Are Directly Contradicted</u> <u>By The PNP Specification And The Disclosure Of The Smith Patent Itself</u>

The Office Action's statements about how the purported "plug and play functionality" of Smith and Ristelhueber do not require any user-loaded software cannot be reconciled with Smith's disclosure and with the PNP specification incorporated by reference therein for at least four different reasons.

First, while Figure 2 of Smith shows that the O/S obtains information from BIOS on a user-loaded ROM chip, it does not state that the O/S also gets the "device drivers" therefrom. Ristelhueber refers to the PNP specification, but does not mention "device drivers" at all. The abstract of the PNP specification sheds light on the source of the drivers used by the Smith and Ristelhueber peripherals by stating that "user interface issues for installation of device drivers are not addressed." If a "user interface" is required to install a driver, then it follows that the drivers must be user-loaded on a particular PC at least one time. Consistent with this understanding, submitted herewith are materials regarding a number of "plug and play" peripheral devices of the type mentioned in the background of Smith, all of which require user-loaded software at least

one time on any particular different manufacturer's PC to which they are connected. A one-time user-loaded software requirement of this sort is the antithesis of the *multi-use automatic processor* feature of the new claims.

Second, neither Smith, Ristelhueber nor the PNP specification contain any disclosure of a peripheral device complying with the protocols of a generic class of devices that respond to a generic driver already present on a PC when the PC was purchased by its first end user. In contrast to the use of generic drivers, the PNP specification (see pages 25-26) only concerns device specific drivers by stating that "plug and play cards return read-only configuration information in two formats," both of which include a vendor code and serial number that are unique to each device. The provision of such vendor specific information for each peripheral is consistent with applicant's contention that a peripheral operating in accordance with the PNP specification also requires a user to load software onto a particular different manufacturer's PC at least one time. For this reason alone, neither Smith nor Ristelhueber discloses, teaches or suggests at least the no-user loaded software aspect of the *multi-use automatic processor* claim feature.

Third, the "device drivers" of Figure 2 are referenced in Smith at column 3, lines 56-57, as being "appropriate." This leads to the conclusion that each driver corresponds to a unique peripheral and, therefore, must be user-loaded because PC memory resources are finite and cannot contain every driver for every possible peripheral. The provision of a user-loaded device driver is the antithesis of the *multi-use automatic processor* claim feature.

Fourth, unlike the claimed invention, all of Smith's embodiments require significant

involvement of an end user after the PC has been sold to him or her - either a user-installed ROM chip (Figure 2), a user-loaded operating system (Figure 3), a user-loaded application program (Figure 4), or one of the user-installed devices referenced at column 8, lines 27-43, all of which are internal to the PC. Requiring an end user to act in this manner is the antithesis of the *multi-use automatic processor* claim feature.

In view of the foregoing, the factual allegations in the Office Action about Smith and Ristelhueber purportedly not having a user-loaded software requirement are not correct. Applicant challenges the obviousness rejections stated in the Office Action because they are based on the erroneous assumption or factual predicate that neither Smith nor Ristelhueber require user-loaded software. The Office Action concedes that no other reference in the purported combination provides the teachings missing from Smith and Ristelhueber to render the new claims *prima facie* obvious. For this reason alone, it is respectfully submitted a *prima facie* case of obviousness cannot be based in whole or in part on Smith or Ristelhueber. Therefore, the new claims are patentable over a purported combination of Hashimoto, Smith, Ristelhueber, Kerigan, and Shinohara.

The Office Action Is Not Consistent With MPEP §2142 By Failing To Provide Any Support For Its Factual Assertion That Hashimoto Requires No User-Loaded Software

The Office Action alleges at page 37 that Hashimoto discloses an "ADPGD processor" that is purportedly involved in an "automatic recognition process." By making this allegation, the Office Action impliedly asserts that the Hashimoto camera can be used without any user loaded software. The only support provided for this allegation is a parroting of the claim language with conclusory references to Hashimoto's specification. This does not provide any

"articulated reasoning with some rational underpinning" as to how, for example, the Hashimoto

camera CPU is involved in an "automatic recognition process" or how the camera itself can be

used without any user-loaded software in a manner consistent with the claimed invention.

Because the Office Action is obligated to provide this information pursuant to MPEP § 2142 (8th

Ed., Rev. 7, July 2008), the Office Action fails to make out a prima facie case of obviousness.

For at least this reason, for example, the new claims are patentable over Hashimoto in

combination with Smith, Kerigan, Ristelhueber and Shinohara.

<u>The Unsupported Contention In The Office Action About Hashimoto</u> <u>Not Requiring User-Loaded Software Cannot Be Reconciled</u> <u>With Its Disclosure Which Is Not Consistent With MPEP §2142</u>

Regarding the issue of whether Hashimoto requires user-loaded software, it should be

noted that Hashimoto expressly teaches the following points:

- The CPU inside the Hashimoto camera waits until a PC to which it is connected sends it a DTR signal for the purpose of indicating file transfer readiness (*see* Hashimoto, Abstract);
- A PC to which the Hashimoto camera is connected can "monitor" or "control" the camera by means of photography related information such as "automatic white balance evaluation information" (*see* col. 7, lines 50-62); and
- A PC has the ability to send "combined image and audio files" to the Hashimoto camera (item 340 in Figure 16).

It is respectfully submitted that one of ordinary skill in the relevant art at the time the claimed invention was made would understand that user-loaded software would be required in order for a PC, at that time, to perform as expressly taught in Hashimoto as noted above. There is nothing

in Hashimoto that would suggest to one of ordinary skill in the art that this understanding would

not apply to the Hashimoto device.

Instead of considering the above-noted express teachings from Hashimoto in the context of whether a proper *prima facie* case of obviousness has been made, the Office Action improperly disregards these express teachings. Because they arise from within the four corners of the Hashimoto patent, it is respectfully submitted that it is the Examiner's burden to show that there was at least one PC in existence at the time the invention was made that could operate in accordance with these express teachings without user-loaded software. *See* MPEP §2142 ("The Examiner bears the initial burden of factually supporting any *prima facie* conclusion of obviousness."). However, the Office Action fails to do so which is inconsistent with MPEP §2142. For this additional reason, for example, it is respectfully submitted that no *prima facie* case for obviousness has been made and, therefore, that the new claims are patentable over Hashimoto in combination with Smith, Ristelhueber, Kerigan and Shinohara.

<u>The Office Action Is Not Consistent With MPEP §2142</u> <u>By Failing To Support A Contention That Kerigan's "Camera Type</u> <u>Peripheral Device" Is Combinable With Hashimoto's Digital Still Camera</u>

The Office Action, at page 26, refers to the Hashimoto camera as a "digital still camera," and states that the "camera" disclosed in Kerigan "demonstrates the applicability of plug and play functionality with camera type peripheral device." However, the Office Action provides no explanation as to why one of ordinary skill in the art would be motivated to use Kerigan's "camera type peripheral device" to modify Hashimoto's "digital still camera." No "articulated reasoning with some rational underpinning" on this issue is given. Because the Office Action is obligated to provide this information pursuant to MPEP §2142 (8th Ed., Rev. 7, July 2008), the Office Action fails to make out a *prima facie* case of obviousness. For at least this reason, for

example, the claimed invention is patentable over Kerigan in combination with Hashimoto,

Smith, Ristelhueber and Shinohara.

The Office Action Is Not Consistent With MPEP §2142 For The Additional Reason That The Factual Assertions Made About Kerigan Cannot Be Reconciled With Its Disclosure

Regarding the issue of whether Kerigan teaches a bridge between the purported "plug and play functionality" of Smith/Ristelhueber and Hashimoto's digital still camera, the following points about Kerigan should be noted:

- The phrase "digital still camera" does not appear anywhere in Kerigan;
- At column 4, line 30 in Table I of Kerigan, a reference is made to "Camera Video in;"
- At column 4, about line 55 in Table II of Kerigan, a reference is made to "full motion video;" and
- Kerigan specifically references the use of "video drivers" in the same sentence in which "plug and play interface components are referenced" (col. 6, lines 7-10).

All of these points are consistent with the Kerigan "camera" merely providing streamed video to a PC as is the case with what would be known today as a "web cam." The Office Action makes no showing whatsoever that Kerigan teaches a "digital still camera" that arguably may be combinable with Hashimoto's digital still camera. The Office Action also makes no showing whatsoever as to how or why one of ordinary skill in the art would be motivated to apply the teachings of Kerigan's "web cam" to the Hashimoto digital still camera. Even if it were proper to do so (which it is not), the resulting combination of Hashimoto, Smith, Ristelhueber, Shinohara and Kerigan does not result in the invention of claim 239 because, for example, the resulting combination requires user-loaded software, which is the antithesis of the *multi-use automatic processor* claim feature.

Because the above-noted express teachings arise from within the four corners of the Kerigan patent, it is respectfully submitted that it is the Examiner's burden to consider them in the context of whether or not Kerigan provides a proper bridge between Hashimoto and Smith/Ristelhueber. *See* MPEP §2142 ("The Examiner bears the initial burden of factually supporting any *prima facie* conclusion of obviousness."). However, the Office Action contains no analysis whatsoever of these express points or of, for example, the reasons why would one of ordinary skill in the art motivated to look to Kerigan's "web cam" as a basis to modify Hashimoto's "digital still camera." Thus, by improperly disregarding these express points and by providing no evidentiary support as to why Kerigan bridges the gap between Hashimoto and Smith/Ristelhueber, the Office Action is not consistent with MPEP §2142. For this additional reason, for example, it is respectfully submitted that no *prima facie* case for obviousness has been made and, therefore, that the new claims are patentable over Kerigan in combination with Hashimoto, Smith, Ristelhueber, and Shinohara.

The Rejections Fail Because Hashimoto, Smith, Ristelhueber and Kerigan Are Applied In A Manner Inconsistent With MPEP §2143.01(VI)

MPEP §2143.01(vi) (8th Ed., Rev. 7, July 2008) provides that if "the proposed modification or combination of the prior art would change the principle of operation of the prior art invention being modified, then the teachings of the references are not sufficient to render the claims *prima facie* obvious." The new claims cannot be found to be *prima facie* obvious because the application of each reference in the purported combination with the other references fundamentally changes the principles about how the devices disclosed in each reference operate as discussed in greater detail hereinafter. As such, it is improper to combine Hashimoto, Smith,

Ristelhueber, Kerigan, and Shinohara as suggested in the Office Action, and no *prima facie* case of obviousness has been established. For this reason alone, it is respectfully submitted that the new claims are patentable over that purported combination.

First, the Office Action alleges that the processor in the Hashimoto camera is involved in an automatic recognition process. However, Hashimoto is perfectly clear about the role of the CPU 23 shown in Figure 8 – it waits until a DTR signal is received from a PC to which the camera is connected. Because the DTR signal indicates to the camera that the PC to which the camera is connected is ready for immediate file transfer, the PC already has "recognized" the camera before the DTR signal is sent. As such, the CPU inside the camera is not involved in causing the camera to be recognized by the PC. Rather, the CPU merely passively waits for the DTR signal. By applying Hashimoto in the manner asserted, the purported combination ascribes an active responsibility to the camera CPU at a point in time when the patent expressly teaches that the CPU is only supposed to be "monitoring" for the DTR signal. Such modification changes the principle of operation of the Hashimoto device, which is contrary to MPEP §2143.01(vi). At least for this reason, it is respectfully submitted that it is not proper to use Hashimoto in the manner asserted in the Office Action.

Second, with regard to the Office Action's contention that the Hashimoto camera processor is involved in an automatic recognition process, please note that Hashimoto expressly teaches that a signal level conversion box (item 28 in Figure 8) prevents any and all signals from be transmitted from the camera to the PC until the DTR signal is received. The application of Hashimoto in the purported combination requires that a signal be sent from the camera to the PC

at a point in time when the signal level conversation box prevents any such signals from being transferred. Thus, applying Hashimoto in the manner asserted fundamentally changes the way Hashimoto operates by requiring a signal be sent from the camera to the PC in a manner inconsistent with what is taught in the patent, which is inconsistent with MPEP §2143.01(vi). Moreover, such a modification would not be made because Hashimoto expressly teaches away from allowing the camera to send a signal to the PC prior to receipt of the DTR signal from the PC. *See* MPEP § 2141.02 (vi) ("A prior art reference must be considered in its entirety, i.e., as a whole, including portions that would lead away from the claimed invention.) At least for these additional reasons, it is respectfully submitted that it is not proper to use Hashimoto in the manner asserted in the Office Action.

Third, Smith and Ristelhueber are cited in the Office Action as allegedly teaching a peripheral device that can be used with a PC without any user-loaded software. As demonstrated above, the peripheral devices disclosed in those references affirmatively require at least one end user to load at least a device specific software driver onto a particular PC of a different manufacturer. That is the only reasonable conclusion that can be reached from the statement in the PNP specification that "user interface issues for installation of device drivers are not addressed" in the standard. As such, the Office Action applies Smith and Ristelhueber in a manner inconsistent with a core requirement of their operation (user-loaded software at least one time for each particular PC), which is inconsistent with MPEP §2143.01(vi).

Fourth, Kerigan is cited in the Office Action as purportedly teaching the applicability of "plug and play functionality" to a camera without any user-loaded software being required.

However, a user is required to load software onto a PC in order for the PC to be able to understand what signals are present on the connector pins that form a particular Kerigan interface. The Office Action does not dispute this user-loaded software requirement. Instead of considering this requirement in the context of a proper *prima facie* obviousness analysis, the Office Action takes an isolated statement from Kerigan out of context, and applies Kerigan in a combination that purportedly does not require user-loaded software. Doing so is contrary to the express user-loaded software requirement of Kerigan, which is inconsistent with MPEP §2143.01(vi).

Accordingly, for at least these additional reasons, it is respectfully submitted that no *prima facie* case of obviousness can be established based on the cited combination of references. The claimed invention is, therefore, patentable over the cited combination.

<u>The Office Action Fails To Consider The Teachings Of Prior Art That Contradicts The</u> <u>Rejections Stated Therein Which Is Inconsistent With MPEP §2143.01(II)</u>

The purported combination of references in the Office Action allegedly teaches a digital still camera that can be used to transfer pictures to a PC without having to load any software onto the PC at any time. It is respectfully submitted that the prior art documents about the Canon Powershot 600 and Ricoh RDC-2 digital still cameras establish that both cameras require user-loaded software even though they are described in those documents as having either "plug and play support" or a "plug-n-play serial connection cable." The user-loaded software requirement of the Ricoh and Canon camera prior art stands in direct conflict with the alleged no-user loaded software requirement of the purported combination.

When prior art references are in conflict with each other, pursuant to MPEP §2143.01(II), the "examiner must weight the power of each reference to suggest solutions to one of ordinary skill in the art, considering the degree to which one reference might accurately discredit another." Instead of considering the Ricoh and Canon camera prior art as required by this section of the MPEP, the Office Action simply ignores the contradictory prior art by stating, for example, that "it is not entirely clear how" the Canon camera is "accomplished via utilizing Kerigan's interface." *See* Office Action, page 9, second full paragraph. It is respectfully submitted that this is not sufficient under MPEP §2143.01(II). Because the Office Action gives no weight at all to the contradictory Canon and Ricoh prior art, the rejections based on the purported combination are not legitimate and should be withdrawn.

It is respectfully submitted that ignoring the Canon and Ricoh camera prior art runs afoul of the Supreme Court's *KSR* decision. In addressing the risk of courts and patent examiners falling prey to hindsight bias, the Supreme Court stated in *KSR Int'l v. Teleflex*, 82 USPQ2d 1385,1390 (2007) that rigid "preventative rules that deny recourse to common sense are neither necessary under, nor consistent with, this Court's case law." The Smith/Ristelhuber/Kerigan combination does not clearly and unambiguously define the term "plug and play" to mean that no user-loaded software is required in all cases. It defies common sense to rely on the combination of Smith/Ristelhuber/Kerigan to import a purported no-user loaded software requirement into Hashimoto's digital still camera while ignoring the Canon and Ricoh prior art documents which show that user-loaded software is required for two "plug and play" related digital still cameras. It is respectfully submitted that the basis for ignoring the Canon and Ricoh

prior art is a "rigid preventative rule" of the type prohibited in *KSR*, and that the Office Action impermissibly relies on the teachings of the instant application to ignore the contradictory prior art documents. For this reason alone, for example, it is respectfully submitted that the new claims are patentable over a purported combination of Hashimoto, Smith, Ristelhuber, Kerigan, and Shinohara.

Further, additional prior art of record stands in direct conflict with the alleged teachings of the purported combination. In the third full paragraph in column one of Smith, modems, hard disk drive controllers and floppy drive controllers are cited as examples of devices that can be added to a computer, and that presumably have "plug and play functionality" as referenced in the Office Action. However, the following three prior art references disclose examples of each one of these products, all of which require user-loaded software:

- Manual For US Robotics Sportster Voice Modem, copyright date 1996. Page 3 of this manual states that "plug and play" is a feature of the modem. Page 8 of the manual states that there are two parts to installation: software and hardware.
- March 20, 1996 Article Regarding SyQuest's Removable Cartridge Hard Disk Drive The article states that the "world of plug and play has just gotten a little larger." The article also states that a user must "load the software that comes with" the product.
- Iomega Zip 100 Parallel Port Drive (similar to a floppy disk drive) Even though the manual copyright date is 2000, the drive itself is prior art. The manual shows that the drive is used by being plugged into the parallel port of a PC The manual also clearly states that user-loaded software is required.

Pursuant to MPEP §2143.01(II), the Examiner is obligated to consider this information that

directly contradicts the assertions in the Office Action about the alleged teachings of the

purported combination. When this information is given its due weight, the analysis leads to the

inescapable conclusion that the purported combination also requires user-loaded software, which is the antithesis of the *multi-use automatic processor* claim feature. For this additional reason, for example, the new claims are patentable.

The Office Action Is Not Consistent With MPEP <u>\$2142</u> By Impermissibly Making It Applicant's Burden To Show That No Prior Art PCs Can Send DTR Signals Without User-Loaded Software

It is respectfully submitted that a user is required to load software onto a PC to which a Hashimoto camera is connected in order to transfer pictures from the camera to the PC. One reason for this is that no prior art PC had the ability to send a DTR signal for camera purposes without user loaded software being required. A number of prior art PC manuals are of record, none of which references any ability of the PC to send a DTR signal for camera purposes in the manner disclosed in Hashimoto. The lack of such a reference in the manuals is consistent with a user having to load software onto the PC in order to be able to send the DTR signal.

Instead of considering the PC manuals in the context of a *prima facie* obviousness analysis with respect to Hashimoto, the Office Action disregards it allegedly because information about all prior art PCs was not given. Shifting the burden of proof to the applicant in this manner is improper because, pursuant to MPEP §2142, it is the Examiner's burden, not the applicant's burden, to factually support a *prima facie* case for obviousness.

To be consistent with the Office Action's position that Hashimoto does not require userloaded software, at least one prior art PC that is capable of sending a DTR signal for camera purposes must have been available before March 4, 1997. It is the Examiner's burden to show this, not the applicant's burden to prove a negative that no PC had the ability to send a DTR signal for camera purposes without user loaded software. Because the Office Action cites no evidence whatsoever that any PCs in the relevant time from could send a DTR signal for camera purposes without user-loaded software also being required, it is respectfully submitted that no *prima facie* case of obviousness can be made that Hashimoto does not require user-loaded software. For this reason alone, the new claims are patentable over the purported combination.

Additional prior art is being made of record in connection with the IDS filed herewith that is consistent with the above-noted analysis. In this regard, a manual bearing a copyright date of March, 1995 for NEC's PowerMate V486 computer is submitted for the Examiner's consideration. Page 1-48 of the manual states that the computer has "plug and play support for easy board installation" as one of the "integrated technologies" that are formed into it. Page 5-5 of the manual states that your "computer supports Plug and Play ISA expansion boards" which is a direct reference to the PNP specification cited in Smith and discussed previously in this amendment. Significantly, the manual contains no reference whatsoever to "DTR" or a "DTR signal" or to a "camera." The absence of these words from the manual indicates that the NEC PC does not have the ability to send a DTR signal to a camera without user-loaded software. It follows from this and from the fact that Hashimoto's camera operates based upon receipt of a DTR signal that, to use the Hashimoto camera, user-loaded software is required, which is the antithesis of the *multi-use automatic processor* claim feature.

<u>The Purported Combination Would Not Be Made Because The "Plug And Play Functionality"</u> <u>Referenced In The Office Action Is Known In The Art As Being "Plug And Pray"</u>

Pursuant to MPEP §2143.02, the prior art can be combined to reject claims as prima facie

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obvious only if there is a reasonable expectation of success. The use of Smith and Ristelhuber in the purported combination is suspect at best in view of the fact that the plug and play technology referenced therein was derisively known in the art as being "plug and pray." *See* Baker, 15 Unix Review 13 (1997). In view of these known problems and probable inoperability, one of ordinary skill in the art would not reasonably expect to successfully implement the PNP standard in a digital camera with user loaded software as taught by Hashimoto as discussed above, much less reasonably expect to successfully modify the PNP standard to function without user loaded software. Accordingly, a *prima facie* case of obviousness cannot be based on the proposed combination of references. MPEP 2143.02 (I) (citing *In re Merck & Co., Inc.* 800 F.2d 1091 (Fed. Cir. 1986)) ("The prior art can be modified or combined to reject claims as *prima facie* obvious *as long as there is a reasonable expectation of success.*") (emphasis added).

Docket No.: 31436/43993

Application No. 11/467,092 Amendment August 31, 2009

<u>Closing</u>

It is respectfully submitted that the instant application is in condition for allowance. A

formal notice to that effect is earnestly solicited.

Dated: August 31, 2009

Respectfully submitted,

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/467,092	08/24/2006	Michael Tasler	31436/43993	3038
7590 03/02/2009 Jeffrey W. Salmon, Esq. Marshall Gerstein & Borun LLP 233, South Wacker Drive, Suite 6300 Chicago, IL 60606			EXAMINER	
			LEE, CHUN KUAN	
			ART UNIT	PAPER NUMBER
			2181	
			MAIL DATE	DELIVERY MODE
			03/02/2009	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

	Application No.	Applicant(s)				
	11/467,092	TASLER, MICHAEL				
Office Action Summary	Examiner	Art Unit				
	Chun-Kuan Lee	2181				
The MAILING DATE of this communication appears on the cover sheet with the correspondence address Period for Reply						
 A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>3</u> MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION. Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication. If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication. Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b). 						
Status						
1) Responsive to communication(s) filed on <u>30 December 2008</u> .						
2a) This action is FINAL . 2b) ⊠ This action is non-final.						
3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is						
closed in accordance with the practice under Ex parte Quayle, 1935 C.D. 11, 453 O.G. 213.						
Disposition of Claims						
4)⊠ Claim(s) <u>183-238</u> is/are pending in the application.						
4a) Of the above claim(s) is/are withdraw						
5) Claim(s) is/are allowed.						
6)⊠ Claim(s) <u>183-238</u> is/are rejected.						
7)⊠ Claim(s) <u>183-185,196,209,224 and 237</u> is/are	obiected to.					
8) Claim(s) are subject to restriction and/o	-					
Application Papers						
9)⊠ The specification is objected to by the Examiner. 10)⊠ The drawing(s) filed on <u>24 August 2006</u> is/are: a)⊡ accepted or b)⊠ objected to by the Examiner.						
Applicant may not request that any objection to the		•				
Replacement drawing sheet(s) including the correct						
11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.						
Priority under 35 U.S.C. § 119						
12)⊠ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).						
a)⊠ All b)⊡ Some * c)⊡ None of:						
1. Certified copies of the priority documents have been received.						
2. Certified copies of the priority documents have been received in Application No. <u>09/331,002</u> .						
3. Copies of the certified copies of the priority documents have been received in this National Stage						
application from the International Bureau (PCT Rule 17.2(a)). * See the attached detailed Office action for a list of the certified copies not received.						
See the attached detailed Onice action for a list of the certified copies not received.						
Attachment(s)						
1) X Notice of References Cited (PTO-892)	4) X Interview Summar	y (PTO-413)				
2) Notice of Draftsperson's Patent Drawing Review (PTO-948) Paper No(s)/Mail Date. 20090211 . 3) Information Disclosure Statement(s) (PTO/SB/08) 5) Notice of Informal Patent Application						
Paper No(s)/Mail Date <u>See Continuation Sheet</u> .	6) 🗌 Other:					
L U.S. Patent and Trademark Office	ation Summary	Part of Paper No. (Mail Data 20000211				
PTOL-326 (Rev. 08-06) Office Ad	ction Summary P	art of Paper No./Mail Date 20090211				

Continuation Sheet (PTOL-326)

Continuation of Attachment(s) 3). Information Disclosure Statement(s) (PTO/SB/08), Paper No(s)/Mail Date :1/7/09; 1/26/09; 2/3/09 & 2/6/09.

DETAILED ACTION

CONTINUED EXAMINATION UNDER 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 12/30/2008 has been entered.

2. The instant application having Application Number: 11/467,092 filed on 08/24/2006 has a total of 56 claims currently pending for examination; claims 1-182 are canceled and new claims 183-238 are added; there are 1 independent claim and 55 dependent claims, all of which are examined below. The examiner acknowledges the second interview request submitted by the applicant's representative on 02/09/2009, and will schedule the specific time for the second interview in the near future.

RESPONSE TO ARGUMENTS

3. Applicant's arguments filed 12/30/2008 have been fully considered but they are not persuasive. Applicant's arguments with respect to the claimed feature "without any type of user intervention at any time by means of the PC" have been considered but are moot in view of the new ground(s) of rejection.

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4. In response to applicant's arguments with regard to the independent claim 183 rejected under 35 U.S.C. 103(a) that the combination of the references does not teach/suggest the claimed feature "wherein the ADGPD processor is adapted to initiate the data generation process and be involved in an automatic recognition process in which, after the i/o connector has been operatively coupled to the MPI of the PC, the ADGPD processor executes at least one instruction set stored in the program memory and thereby causes at least one parameter regarding the ADGPD, which signifies that the ADGPD has the ability to transfer the one or more files of digital data in response to commands issued from the at least one software driver, to be automatically sent through the i/o connector and to the MPI of the PC (a) without any type of user intervention at any time by means of the PC and (b) before a time when the PC is able to receive data files that are transferred to it from the ADGPD"; applicant's arguments have fully been considered, but are not found to be persuasive.

Please note that one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.,* 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

Furthermore, in accord with applicant's disclosure of the instant invention during the interview dated 2/3/2009, the novelty of the instant invention corresponds to the end result/outcome of the peripheral device operating in correspondence to plug-and-play, which is action caused by an individual by plugging a portable peripheral device into the computer and play (e.g. transferring data) the portable peripheral device without the

need for the individual to load corresponding special driver or other software. Furthermore, instant invention transfers data from the camera to the computer using file manager routine, because the computer is viewing the peripheral device as the simulated HDD (mass storage device). Wherein the examiner relied on the combination of the references as following for the teaching/suggestion of the above claim feature:

<u>Hashimoto</u> teaches the ADGPD processor is adapted to initiate the data generation process and be involved in an automatic recognition process in which, after the i/o connector has been operatively coupled to the MPI of the PC, the ADGPD processor executes at least one instruction set stored in the program memory to automatically transfer the one or more files of digital data through the i/o connector and to the MPI of the PC (Fig. 11-12; Fig. 14-15; col. 1, II. 35-57; col. 6, I. 16 to col. 9, I. 17; col. 9, I. 46 to col. 11, I. 42 and col. 12, I. 16 to col. 14, I. 14), wherein the digital camera's CPU (Fig. 8, ref. 23) control the operation of the digital camera for the data transferring after the digital camera is connected to and recognized by the PC, and as the digital camera's CPU control any function of the digital camera, the digital camera's CPU further controls the digital camera to be recognized by the PC; wherein the digital camera needs to be recognized by the PC in order for the PC to know what peripheral device is connected such that the PC knows how to properly communicate with the connected peripheral device.

<u>Smith</u> teaches a peripheral device having an automatic recognition process in which, after the peripheral device's i/o connector has been operatively coupled to a PC, to cause at least one parameter regarding the peripheral device, which signifies that the

peripheral device has the ability communicate in accordance to the at least one software driver, to be automatically sent through the i/o connector and to the PC before a time when the PC is able to communicate with the peripheral device; and wherein the peripheral device is adapted to, after the at least one parameter has been sent to the PC, communicate with the PC (e.g. as the system is configured and communication between the peripheral device is enabled) without requiring a user to have previously loaded software on the PC (i.e. installing device by the user without the need for supplemental software installation or device configuration: col. 5, II. 41-51) (Fig. 2-5; col. 1, II. 9-22; col. 2, I. 40 to col. 3, I. 8; col. 3, II. 22-27; col. 3, II. 53-59; col. 4, II. 5-34 and col. 6, II. 63-62), wherein the above automatic recognition process functionality is equivalent to configuring plug and play system utilizing ROM BIOS by having the operating system load the device driver after the peripheral device is coupled to the PC for installation; additionally, this is in accord with applicant's disclosure of the instant invention during the interview dated 2/3/2009 corresponding to "the end result/outcome of the peripheral device operating in correspondence to plug-and-play ... is action caused by an individual by plugging a portable peripheral device into the computer and play the portable peripheral device without the need for the individual to load corresponding special driver or other software;" furthermore, combining plug-and-play functionality (e.g. Smith's plug-and-play functionality) into a camera type peripheral device (e.g. <u>Hashimoto</u>'s digital camera) is expressly taught/suggested by <u>Kerigan</u>.

<u>Ristelhueber</u> teaches a peripheral device having an automatic recognition process without any type of user intervention at any time by means of the PC (pages 1-

3), which corresponds to plug and play (PnP) of a peripheral device by having a user to simply insert a peripheral into a desktop system and have it start running immediately, as the PnP computer will automatically identify any new hardware installed and configure the new hardware, and relieving the end user of any need to fumble with floppy disks and user manuals to get the device up and running; therefore, the installation of the peripheral device is accomplished without any type of user intervention at any time by means of the PC; furthermore, this is in accord with applicant's disclosure of the instant invention during the interview dated 2/3/2009 corresponding to "the end result/outcome of the peripheral device operating in correspondence to plug-and-play ... is action caused by an individual by plugging a portable peripheral device into the computer and play the portable peripheral device without the need for the individual to load corresponding special driver or other software"

<u>Shinohara</u> teaches a peripheral device (e.g. flash memory peripheral device) has the ability to transfer data in response to commands (e.g. data read command) issued from a PC (col. 1, II. 48-60 and col. 3, I. 33 to col. 4, I. 49).

In summary, the combination of <u>Hashimoto</u>, <u>Smith</u>, <u>Kerigan</u>, <u>Ristelhueber</u>, and <u>Shinohara</u> teach the plug-and-play ADGPD having the flash memory card for data transferring after being connected to the PC, wherein the plug-and-play functionality is accomplished without the user adding software/driver, because of implementation in accordance to "PnP ISA Specification". Furthermore, the result of the combination of the references is equivalent to the instant invention, as in accordance to applicant's

disclosure of "... the end result/outcome ..." for the instant invention during the interview dated 2/3/2009.

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5. In response to applicant's arguments with regard to the independent claim 183 rejected under 35 U.S.C. 103(a) that the combination of the references does not teach/suggest the claimed feature that no user had to interact with a PC at any time for loading a required soft/driver for the connected peripheral device; applicant's arguments have fully been considered, but are not found to be persuasive.

The examiner respectfully disagrees, because <u>Smith</u> and <u>Ristelhueber</u> teaches/suggests the above claimed feature, wherein <u>Smith</u> teaches a peripheral device installed by a user without the need for supplemental software installation or device configuration (<u>Smith</u>, col. 5, II. 41-51) and <u>Ristelhueber</u> teaches a user may insert a peripheral device into a desktop system and have it running immediately, as the PnP computer will automatically identify any new hardware installed and configure the new hardware, and relieving the end user of any need to fumble with floppy disks and user manuals to get the device up and running (<u>Ristelhueber</u>, pages 1-2).

6. In response to applicant's arguments with regard to the independent claim 183 rejected under 35 U.S.C. 103(a) that the combination of the references does not teach/suggest the claimed feature that a PC sends an inquiry signal to a peripheral device, and in response, the peripheral device return a parameter signal for the PC to recognize the peripheral device and select the corresponding software driver, and

during the transferring of the inquiry and parameter signals the PC and the peripheral device are not yet ready to have file transfer, because in order for <u>Hashimoto</u>'s camera to be able to send signals to a PC, the PC must send to the camera a DTR signal, at the time when the DTR signal is forwarded, the PC already has recognized how to communicate with the camera; applicant's arguments have fully been considered, but are not found to be persuasive.

The examiner respectfully disagrees, because as in accord with applicant's disclosure of the instant invention during the interview dated 2/3/2009, the inquiry signal and the parameter signal correspond to the plug-and-play functionality for selecting the corresponding software driver, wherein such claimed feature is taught/suggested by <u>Smith</u> and <u>Ristelhueber</u> (Smith Fig. 2; col. 3, II. 1-59; col. 5, II. 41-51; and <u>Ristelhueber</u>, pages 1-3).

7. In response to applicant's arguments with regard to the independent claim 183 rejected under 35 U.S.C. 103(a) that the combination of the references does not teach/suggest the claimed feature of "Plug and Play" camera without requiring user intervention via a PC such as with user loaded software, because such feature is not disclosed by <u>Kerigan</u>, and the reason that <u>Kerigan</u> does not teach said claimed feature is because of disclosure by the user manual for "Canon Powershot 600, "QuickCam by Connectix" and "Mini FQA Again"; applicant's arguments have fully been considered, but are not found to be persuasive.

The examiner respectfully disagrees, because the examiner is not expressly relying on <u>Kerigan</u> for the teaching/suggesting of "Plug and Play" camera without requiring user intervention via a PC such as with user loaded software, instead the examiner is relying on <u>Hashimoto</u>, <u>Smith</u>, and <u>Ristelhueber</u> (<u>Hashimoto</u>, Fig. 8; col. 1, II. 35-57; col. 3, I. 43 to col. 4, I. 67; col. 5, II. 43-57; col. 6, I. 16 to col. 9, I. 17; col. 10, I. 41 to col. 11, I. 42; col. 12, I. 16 to col. 13, I. 14; <u>Smith</u>, Fig. 2-5; col. 1, II. 9-22; col. 2, I. 40 to col. 3, I. 59; col. 5, II. 41-51; col. 6, II. 63-62 and <u>Ristelhueber</u>, pages 1-3), and relying on <u>Kerigan</u> to only demonstrate the prior art application of plug-and-play functionality to camera type peripheral device.

Furthermore, it is not fully clear as to how the extrinsic evidences (i.e. user manual for "Canon Powershot 600", "QuickCam by Connectix" and "Mini FQA Again") cited by the applicant relate to <u>Kerigan</u>, as none of the extrinsic evidences seem to expressly claim that the implementation of the "Canon Powershot 600" or the QuickCam" is accomplished via utilizing <u>Kerigan</u>'s invention/patent.

8. In response to applicant's arguments with regard to the independent claim 183 rejected under 35 U.S.C. 103(a) that the combination of the references does not teach/suggest the claimed invention because the public available information from the assignee of <u>Hashimoto</u> contradicts the factual findings underlying the rejection, because Ricoh's "award winning" RDC-2 digital camera, together with a portion of the manual for RDC-2 camera, clearly states that "Ricoh Utility Software" is required for "file transmission to a PC"; furthermore, if pictures truly could be transferred to a PC from a

digital camera without user have to load a software on to the PC, then surely Ricoh would be publicizing that at least one of its cameras had that capability, instead Ricoh actively promotes its "PhotoStudio" user-loaded software; applicant's arguments have fully been considered, but are not found to be persuasive.

The examiner respectfully disagrees, because it is not fully clear as to how the extrinsic evidences (i.e. manual for RDC-2 camera, "Ricoh Utility Software" and "PhotoStuio") cited by the applicant relate to <u>Hashimoto</u>, as none of the extrinsic evidences seem to expressly claim that the implementation is accomplished via utilizing <u>Hashimoto</u>'s patent. Additionally, the examiner is not certain as to why Ricoh publicizes certain documentation and not all documentation. Furthermore, the examiner is relying on <u>Smith</u> and <u>Ristelhueber</u> for the teaching/suggesting of the peripheral device having the "plug-and-play" functionality (<u>Smith</u>, Fig. 2-5; col. 1, II. 9-22; col. 2, I. 40 to col. 3, I. 59; col. 5, II. 41-51 and col. 6, II. 63-62 and <u>Ristelhueber</u>, pages 1-3).

9. In response to applicant's arguments with regard to the independent claim 183 rejected under 35 U.S.C. 103(a) that the combination of the references does not teach/suggest the claimed invention because the factual finding about <u>Kerigan</u> are not consistent with publicly available information about the "plug-and-play" standards, because the book titled "Plug-and-Play System Architecture" have no reference of any kind in the index corresponding to the words "digital camera" or "camera"; applicant's arguments have fully been considered, but are not found to be persuasive.

The examiner respectfully disagrees, because even though the index of the book may not expressly include "digital camera" or "camera," no where in the book teaches/suggests that it is impossible for the camera to have plug-and-play functionality; similarly, in accordance to applicant's disclosure during the interview dated 2/3/2009, applicant discloses the implementation of the instant invention as a digital camera, but there is no specific recitation of the word "digital camera" or " camera" in the instant application's Specification. Furthermore, the combined teaching of <u>Hashimoto</u>, <u>Smith</u>, and <u>Ristelhueber</u>, supported by <u>Kerigan</u> expressly teaches/suggests the digital camera having the plug-and-play functionality (<u>Hashimoto</u>, Fig. 8; col. 1, II. 35-57; col. 3, I. 43 to col. 4, I. 67; col. 5, II. 43-57; col. 6, I. 16 to col. 9, I. 17; col. 10, I. 41 to col. 11, I. 42; col. 12, I. 16 to col. 13, I. 14; <u>Smith</u>, Fig. 2-5; col. 1, II. 9-22; col. 2, I. 40 to col. 3, I. 59; col. 5, II. 41-51 and col. 6, II. 63-62 and Ristelhueber, pages 1-3).

10. In response to applicant's arguments with regard to the independent claim 183 rejected under 35 U.S.C. 103(a) that the combination of the reference does not teach/suggest the claimed invention because the sending of DTR by <u>Hashimoto</u>'s PC is provided by user loaded software, as during the relevant time frame, PC would not have the ability to send such signals to indicate a PC's readiness to have picture files transferred to the PC from the digital camera, because none of the references, corresponding to a number of manuals and other spec sheets for various PCs made by Compaq and Apple (Dated 3/4/1997), specifically states that a computer, when initially sold to an end user, contain software on them that allow the computer to send a DTR or

other equivalent signal to indicate the PC's picture transfer readiness; applicant's arguments have fully been considered, but are not found to be persuasive.

The examiner respectfully disagrees, because it is not fully clear as to how the extrinsic evidences (i.e. a number of manuals and other spec sheets for various PCs made by Compaq and Apple) cited by the applicant relate to <u>Hashimoto</u>, as none of the extrinsic evidences seem to expressly claim that <u>Hashimoto</u> is implemented via utilizing the PCs presented in the extrinsic evidences. Additionally, the examiner is expressly replying on <u>Smith</u> and <u>Ristelhueber</u> (i.e. not <u>Hashimoto</u>) for the teaching/suggesting of the peripheral device having plug-and plug functionality (<u>Smith</u>, Fig. 2-5; col. 1, II. 9-22; col. 2, I. 40 to col. 3, I. 59; col. 5, II. 41-51 and col. 6, II. 63-62 and <u>Ristelhueber</u>, pages 1-3); therefore, one of ordinary skilled in the art at the time of the instant invention would combined <u>Hashimoto</u>'s digital camera with <u>Smith</u> and <u>Ristelhueber</u>'s plug and play functionality to have the digital camera with plug-and-play functionality (i.e. without user loaded software).

11. In response to applicant's arguments with regard to the independent claim 183 rejected under 35 U.S.C. 103(a) that the combination of references does not teach/suggest the multiple-use automatic processor be involved with an "automatic recognition" process, which corresponds to the sending of the parameter to the PC, as well as initiating a "data generation" process, because it is impossible for <u>Hashimoto</u>'s CPU to communicate with the PC before the PC sends the DTR signal as the signal level conversion circuit that connects the PC to the camera is in "standby mode" until

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the DTR signal is received; applicant's arguments have fully been considered, but are not found to be persuasive.

The examiner respectfully disagrees, because <u>Hashimoto</u>'s CPU is involved in initiating a "data generation" process (e.g. generating data corresponding to the image and audio data) and involved with an "automatic recognition" process (<u>Hashimoto</u>, col. 7, I. 15 to col. 9, I. 17), as the CPU, having the corresponding communication controller, controls any function of the digital camera including the requirement to identify itself to the PC, in order for the PC to know what peripheral device is connected such that the PC knows how to properly communicate with the connected peripheral device; as for the specific forwarding of the parameter signal in accordance to the plug-and-play functionality, the examiner is relying on <u>Smith</u> and <u>Ristelhueber</u> (<u>Smith</u>, Fig. 2-5; col. 1, II. 9-22; col. 2, I. 40 to col. 3, I. 59; col. 5, II. 41-51 and col. 6, II. 63-62 and <u>Ristelhueber</u>, pages 1-3).

12. In response to applicant's arguments with regard to the independent claim 183 rejected under 35 U.S.C. 103(a) that the combination of references does not teach/suggest the claimed feature corresponding to without end user adding application program because base on the references of record, no PC commercially available on or before the earliest priority date include ability of sending "combined image and audio files" when initially purchased by an end user, and because the monitoring of the camera (<u>Hashimoto</u>, col. 7, II. 50-62) would require for the user to add software; applicant's arguments have fully been considered, but are not found to be persuasive.

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The examiner respectfully disagrees, because it does not seem that the applicant presented every single one of PCs commercially available on or before the earliest priority date, and it is not fully clear to the examiner as to how the extrinsic evidences (i.e. the commercial PCs presented by the applicant) is related to <u>Hashimoto</u>, as none of the extrinsic evidences seem to expressly claim that Hashimoto is implemented via utilizing the PCs presented in the extrinsic evidences. Furthermore, corresponding to column 7, lines 50-62 in Hashimoto, the examiner is not persuaded by applicant's reasoning that it is "inherent" (i.e. in accordance to applicant's explanation for Hashimoto's column 7, lines 51-62 during the interview dated 2/3/2009) for Hashimoto to require user adding application program. Even if assuming applicant's arguments were correct and Hashimoto does require user adding software, the examiner is relying on Smith and Ristelhueber for the teaching/suggesting of the plug-and-play functionality in the peripheral device, which alleviate the need for user adding software, and immediately utilizing the connected peripheral device after connecting the peripheral device to the computer (Smith, Fig. 2-5; col. 1, II. 9-22; col. 2, I. 40 to col. 3, I. 59; col. 5, II. 41-51 and col. 6, II. 63-62 and <u>Ristelhueber</u>, pages 1-3).

13. In response to applicant's arguments with regard to the independent claim 183 rejected under 35 U.S.C. 103(a) that <u>Smith</u> does not teach/suggest "plug-and-play peripheral" because there is not evidence that one skilled in the art would apply the plug-and-play functionality to <u>Hashimoto</u>'s processor in the peripheral device; furthermore, <u>Smith</u> does not teach/suggest ADGPD and generating files of digitized

analog data; applicant's arguments have fully been considered, but are not found to be persuasive.

The examiner respectfully disagrees, because <u>Hashimoto</u>'s processor control any function of the camera by utilizing routine in the control program storing area (<u>Hashimoto</u>, col. 7, I. 15 to col. 9, I. 17), and in view of <u>Smith</u>'s peripheral deice having plug-and-play functionality, one of ordinary skilled in the art would combine <u>Smith</u>'s plug-and-play functionality into <u>Hashimoto</u>'s processor, controlling any functions in the digital camera, for the benefit of simplifying the installation of the peripheral device for the user as the peripheral device may be installed without the need for the user to install software or configure the peripheral device (<u>Smith</u>, col. 2, II. 40-67 and col. 5, II. 41-51 and col. 6, II. 63-65); additionally, to apply the plug and play functionality in the camera type peripheral device is further expressly discloses by <u>Kerigan</u> (<u>Kerigan</u>, col. 3, II. 29-33 and col. 6, II. 3-10).

Furthermore, please note that one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.,* 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986). Wherein the examiner is expressly relying on <u>Hashimoto</u> for the teaching/suggestion of ADGPD and generating files of digitized analog data.

14. In response to applicant's arguments with regard to the independent claim 183 rejected under 35 U.S.C. 103(a) that the combination of the references does not

teach/suggest the claimed invention because <u>Kerigan</u>'s interface can be configured in several ways, therefore, there is no standard set of pins contained inside a connector that can be access in a way known by a standard program that is provided with a PC when it is sold to an end user during the relevant time frame and user is required to load interface enabling software; applicant's arguments have fully been considered, but are not found to be persuasive.

The examiner respectfully disagrees, because by having the different interface configurations all to include the plug and play functionality, the different interface configurations will have the same standard programming in the PC; furthermore, <u>Smith</u> teaches the plug and play functionality for different interface configurations (e.g. parallel interface configuration, serial interface configuration) (<u>Smith</u>, col. 1, II. 9-22 and col. 3, II. 1-59); therefore, having the different interface configurations all to include the plug and play functionality, the user is not required to load interface enabling software, regardless which specific interface is utilized.

15. In response to applicant's arguments with regard to the independent claim 183 rejected under 35 U.S.C. 103(a) that the combination of the references does not teach/suggest the claimed invention because <u>Kerigan</u>'s identifying ability of each peripheral device (Fig. 2, step 24) is equivalent to the need for the user to load software because base on reference of record, no PC that was commercially available as of March 3, 1997 was capable of identifying the "capability" of a camera without requiring a

user to load software onto the PC first; applicant's arguments have fully been considered, but are not found to be persuasive.

The examiner respectfully disagrees, because it is not fully clear as to how the extrinsic evidences (i.e. reference of record corresponding to PC that was commercially available as of March 3, 1997) cited by the applicant relate to <u>Kerigan</u>, as none of the extrinsic evidences seem to expressly claim that <u>Kerigan</u> is implemented via utilizing the PCs presented in the extrinsic evidences. Furthermore, even assuming if the applicant's arguments was correct, the examiner's reliance on <u>Smith</u> and <u>Ristelhueber</u>'s teaching of the peripheral device having the plug-and-play functionality, alleviates the need for loading user software when the peripheral device is connected to the PC (<u>Smith</u>, Fig. 2-5; col. 1, II. 9-22; col. 2, I. 40 to col. 3, I. 59; col. 5, II. 41-51 and col. 6, II. 63-62 and <u>Ristelhueber</u>, pages 1-3).

16. In response to applicant's arguments with regard to the independent claim 183 rejected under 35 U.S.C. 103(a) that the combination of the references does not teach/suggest the claimed invention because <u>Shinohara</u> does not teach the claimed feature corresponding to the plug and play functionality because <u>Shinohara</u> require the processing power to be provided by the "card services" program of a PC in order to be recognized by the PC, and <u>Shinohara</u> does not teach/suggest the multi-use automatic processor; applicant's arguments have fully been considered, but are not found to be persuasive.

The examiner respectfully disagrees, because the examiner is not fully clear as to where in <u>Shinohara</u> discloses the "card services" program or the recognition by the PC is in provided by the "card services" program; furthermore, the examiner is relying on <u>Hashimoto</u>, <u>Smith</u>, <u>Kerigan</u> and <u>Ristelhueber</u> (i.e. not <u>Shinohara</u>) for the teaching/suggesting of the plug and play functionality and the multi-use automatic processor (<u>Hashimoto</u>, Fig. 8; col. 1, II. 35-57; col. 3, I. 43 to col. 4, I. 67; col. 5, II. 43-57; col. 6, I. 16 to col. 9, I. 17; col. 10, I. 41 to col. 11, I. 42; col. 12, I. 16 to col. 13, I. 14; <u>Smith</u>, Fig. 2-5; col. 1, II. 9-22; col. 2, I. 40 to col. 3, I. 59; col. 5, II. 41-51; col. 6, II. 63-62; Kerigan, col. 3, II. 29-33; col. 6, II. 3-10; and Ristelhueber, pages 1-3).

17. In response to applicant's argument that the examiner's conclusion of obviousness is based upon improper hindsight reasoning, it must be recognized that any judgment on obviousness is in a sense necessarily a reconstruction based upon hindsight reasoning. But so long as it takes into account only knowledge which was within the level of ordinary skill at the time the claimed invention was made, and does not include knowledge gleaned only from the applicant's disclosure, such a reconstruction is proper. See *In re McLaughlin*, 443 F.2d 1392, 170 USPQ 209 (CCPA 1971). And the following are answers to the applicant's questions in association with applicant's argument that the examiner's conclusion of obviousness is based upon improper hindsight:

Regarding Hashimoto

1- How can <u>Hashimoto</u>'s camera be use without requiring a user to have previously loaded an application level program on the PC to which the camera is connected when supplemental notice corresponding to Casio Inc. admits that Casio QV-10 camera and Kodak DCS200 camera both need software driver to retrieve images in the camera's memory?

First of all, it is not fully clear to the examiner as to how the extrinsic evidences (i.e. Casio QV-10 camera and Kodak DCS200 camera) provided relate to <u>Hashimoto</u>'s camera, as none of the extrinsic evidences seems to expressly claim that Casio QV-10 and Kodak DCS200 cameras are implemented via utilizing <u>Hashimoto</u>'s patent/camera. Additionally, <u>Hashimoto</u> in view of <u>Smith</u> and <u>Ristelhueber</u>'s peripheral device having plug and play functionality (<u>Smith</u>, Fig. 2-5; col. 1, II. 9-22; col. 2, I. 40 to col. 3, I. 59; col. 5, II. 41-51; col. 6, II. 63-62; and <u>Ristelhueber</u>, pages 1-3), and expressly supported by Kerigan's camera type peripheral device having plug and play functionality, it would have been obvious for one of ordinary skill in this art at the time of invention was made to include <u>Smith</u> and <u>Ristelhueber</u>'s plug and play functionality into <u>Hashimoto</u>'s digital camera for the benefit of simplifying the installation of the peripheral device for the user as the peripheral device may be installed without the need for the user to install software or configure the peripheral device (<u>Smith</u>, col. 2, II. 40-67; col. 5, II. 41-51 and col. 6, II. 63-65 and <u>Ristelhueber</u>, pages 1-3).

2- Do prior art PCs before March 4, 1997, when initially sold to an end user, have the capability of sending a DTR signal of an RS-232 connection (see <u>Hashimoto</u>'s

abstract) without using an end user added applications program for purposes of indicating a readiness for camera file transfer purposes?

By combining <u>Hashimoto</u>, <u>Smith</u>, <u>Kerigan</u>, <u>Ristelhueber</u> and <u>Shinohara</u>, the plugand-play digital camera do not need for the end user to add application program for the purpose of indicating a readiness, because the digital camera have the plug-and-play functionality, and the PCs, in accordance to <u>Smith</u> and <u>Ristelhueber</u>, installs a device by a user without the need for supplemental software installation or device configuration (<u>Smith</u>, col. 5, II. 41-51) such that a user simply insert a peripheral into a desktop system and have it start running immediately, as the PnP computer will automatically identify any new hardware installed and configure the new hardware, and relieving the end user of any need to fumble with floppy disks and user manuals to get the device up and running (<u>Ristelhueber</u>, pages 1-2).

3 - Do prior art PCs before March 4, 1997, when initially sold to an end user, have the capability of sending "combined image and audio files" (step 340 in Figure 16 of <u>Hashimoto</u>) without using an end user added application program?

By combining <u>Hashimoto</u>, <u>Smith</u>, <u>Kerigan</u>, <u>Ristelhueber</u> and <u>Shinohara</u>, the PCs, in accordance to <u>Smith</u> and <u>Ristelhueber</u>, can send <u>Hashimoto</u>'s combined image and audio files without using an end user added application program, because a user do not need to install supplemental software, therefore the user simply insert the peripheral device into the PC and immediately start using (e.g. transferring <u>Hashimoto</u>'s combined Application/Control Number: 11/467,092Page 21Art Unit: 2181image and audio files) the peripheral device (Smith, col. 5, II. 41-51 and Ristelhueber,pages 1-2), as discussed in detail in guestion 2 above.

4 - Why would one of ordinary skill delete the required signal level conversion circuit (item 28 in Figure 8 of <u>Hashimoto</u>) that is kept in a standby mode to save battery power until the DTR signal is received from the PC?

The examiner did not suggest to ignore the standby mode for RS-232 interconnection, the combination would suggest to have both the standby mode and the plug-and-play functionality for the digital camera; additionally, the combination further suggest to implement the interconnection in accordance to a different interface configuration (e.g. parallel or serial interface configuration), instead of the RS-232 interface.

5 - Do prior art PCs before March 4, 1997, when initially sold to an end user, have the capability of "controlling" the Hashimoto camera by means of, for example, "exposure controlling information" without requiring a user to load an applications program on the PC?

First of all, no where in <u>Hashimoto</u> teaches/suggests the need for the user to load an application program; furthermore, by combining <u>Smith</u> and <u>Ristelhueber</u>'s plug and play functionality with <u>Hashimoto</u>, the combination of the references teaches/suggests utilizing (e.g. controlling) the peripheral device without the need for the user to load the application program. Additionally, the examiner is not persuaded with regard to

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applicant's reasoning because applicant's argument that <u>Hashimoto</u> teaches/suggests the need for the user to load an application program is base on "inherency" (i.e. <u>Hashimoto</u>, column 7, lines 50-62) as discussed during the interview dated 2/3/2009.

6 - Do prior art PCs before March 4, 1997, when initially sold to an end user, have the capability of "monitoring" the Hashimoto camera by means of, for example, "exposure controlling information" without requiring a user to load an applications program on the PC?

First of all, no where in <u>Hashimoto</u> teaches/suggests the need for the user to load an application program; furthermore, by combining <u>Smith</u> and <u>Ristelhueber</u>'s plug and play functionality with <u>Hashimoto</u>, the combination of the references teaches/suggests utilizing (e.g. monitoring) the peripheral device without the need for the user to load the application program. Additionally, the examiner is not persuaded with regard to applicant's reasoning because applicant's argument that <u>Hashimoto</u> teaches/suggests the need for the user to load an application program is base on "inherency" (i.e. <u>Hashimoto</u>, column 7, lines 50-62) as discussed during the interview dated 2/3/2009.

7 - Why would one of ordinary skill look to the <u>Kerigan</u> camera as a basis for putting <u>Smith</u>'s purported plug and play functionality into <u>Hashimoto</u> when <u>Hashimoto</u>'s background of the invention states that no "universal standard" exists for exporting images from digital cameras (i.e. no generic driver software can be utilized to allow a digital camera to export images to a PC to which the camera is connected)?

The examiner is not certain how the properly answer the applicant's question, because it is not fully clear as to how the applicant is equivocating universal standard to generic driver software; as no where in <u>Hashimoto</u> seems to discloses the software driver.

Regarding Smith

8 - Why would one or ordinary skill find it obvious to adapt <u>Smith</u>'s purported "single use" non-camera related processor with the camera processor shown in <u>Hashimoto</u> that is incapable of communicating with the PC before the DTR signal is received?

First of all, it is not fully clear to the examiner as to where in <u>Smith</u> teaches a single use non-camera related processor; and to further clarify the examiner's rational for the combination of the references, the examiner relied on <u>Hashimoto</u> to show a digital camera having a CPU that controls any function of the digital camera, and in view of <u>Smith</u> and <u>Ristelhueber</u>'s peripheral device having plug and play functionality, the combination further teaches the control by the digital camera's CPU to further include plug and play functionality (<u>Hashimoto</u>, Fig. 8; col. 1, II. 35-57; col. 3, I. 43 to col. 4, I. 67; col. 5, II. 43-57; col. 6, I. 16 to col. 9, I. 17; col. 10, I. 41 to col. 11, I. 42; col. 12, I. 16 to col. 13, I. 14; <u>Smith</u>, Fig. 2-5; col. 1, II. 9-22; col. 2, I. 40 to col. 3, I. 59; col. 5, II. 41-51; col. 6, II. 63-62 and <u>Ristelhueber</u>, pages 1-3).

Regarding Kerigan

9 - Since <u>Kerigan</u> discloses a "web cam" that merely provides streaming video (and not picture files), why would one of ordinary skill rely on <u>Kerigan</u>'s "web cam" as a basis to read <u>Smith</u>'s purported plug and play functionality into <u>Hashimoto</u>'s digital still camera that is capable of transferring picture files?

First of all, the examiner is not fully clear as to were in <u>Kerigan</u> teaches a "web camera," however the examiner is relying on <u>Kerigan</u> for the teaching of a "camera" (<u>Kerigan</u>, col. 3, II. 29-36). Furthermore, the examiner is not specifically relying on <u>Kerigan</u>'s "camera" for the teaching of the claimed limitation, but only to expressly demonstrate the prior art utilization of the plug and play functionality with camera type peripheral device; as for the plug and play ADGPD of the instant invention, the examiner is relying on <u>Hashimoto</u>'s digital still camera and <u>Smith</u> and <u>Ristelhueber</u>'s plug and play functionality (<u>Hashimoto</u>, Fig. 8; col. 1, II. 35-57; col. 3, I. 43 to col. 4, I. 67; col. 5, II. 43-57; col. 6, I. 16 to col. 9, I. 17; col. 10, I. 41 to col. 11, I. 42; col. 12, I. 16 to col. 13, I. 14; <u>Smith</u>, Fig. 2-5; col. 1, II. 9-22; col. 2, I. 40 to col. 3, I. 59; col. 5, II. 41-51; col. 6, II. 63-62 and <u>Ristelhueber</u>, pages 1-3).

10 - Why would one of ordinary skill rely on the web cam to monitor connection disclosed in <u>Kerigan</u> as a basis for combining <u>Smith</u>'s purported single use processor with <u>Hashimoto</u>'s camera processor that cannot send signals to the PC until after the PC sends it the DTR signal?

As similarly responded above in question 9, the examiner is not fully clear as to where in <u>Kerigan</u> teaches a "web camera;" therefore, the examiner is unable to properly

response to applicant's question; furthermore, as explained above, the examiner is relying on <u>Kerigan</u> only to expressly demonstrate the prior art utilization of the plug and play functionality with camera type peripheral device; as for the plug and play ADGPD of the instant invention, the examiner is relying on <u>Hashimoto</u>'s digital still camera and <u>Smith</u> and <u>Ristelhueber</u>'s plug and play functionality (<u>Hashimoto</u>, Fig. 8; col. 1, II. 35-57; col. 3, I. 43 to col. 4, I. 67; col. 5, II. 43-57; col. 6, I. 16 to col. 9, I. 17; col. 10, I. 41 to col. 11, I. 42; col. 12, I. 16 to col. 13, I. 14; <u>Smith</u>, Fig. 2-5; col. 1, II. 9-22; col. 2, I. 40 to col. 3, I. 59; col. 5, II. 41-51; col. 6, II. 63-62 and <u>Ristelhueber</u>, pages 1-3).

11 - Why would one of ordinary skill rely on <u>Kerigan</u> which specifically mentions the use of a "video driver" as a basis to modify a digital still camera that must use entirely different software?

As similarly responded above in question 9, the examiner is not fully clear as to where in <u>Kerigan</u> teaches a "web camera" or "use a video driver so a PC can receive video to it from a web cam"; therefore, the examiner is unable to properly response to applicant's question; furthermore, as explained above, the examiner is relying on <u>Kerigan</u> only to expressly demonstrate the prior art utilization of the plug and play functionality with camera type peripheral device; as for the plug and play ADGPD of the instant invention, the examiner is relying on <u>Hashimoto</u>'s digital still camera and <u>Smith</u> and <u>Ristelhueber</u>'s plug and play functionality (<u>Hashimoto</u>, Fig. 8; col. 1, II. 35-57; col. 3, I. 43 to col. 4, I. 67; col. 5, II. 43-57; col. 6, I. 16 to col. 9, I. 17; col. 10, I. 41 to col. 11,

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I. 42; col. 12, I. 16 to col. 13, I. 14; <u>Smith</u>, Fig. 2-5; col. 1, II. 9-22; col. 2, I. 40 to col. 3, I. 59; col. 5, II. 41-51; col. 6, II. 63-62 and <u>Ristelhueber</u>, pages 1-3).

12 - Are the Office Action's references to the statements in <u>Kerigan</u> about "plug and play" inconsistent with the fact that one of ordinary skill would understand that, to use the <u>Kerigan</u> interface and the "camera" disclosed therein, an end user must load at least interface enabling software onto a PC to which the <u>Kerigan</u> interface is connected?

As similarly responded above in question 9, the examiner is not specifically relying on <u>Kerigan</u>'s "camera" for the teaching of the claimed limitation, but only to expressly demonstrate the prior art utilization of the plug and play functionality with camera type peripheral device; as for the plug and play ADGPD of the instant invention, the examiner is relying on <u>Hashimoto</u>'s digital still camera and <u>Smith</u> and <u>Ristelhueber</u>'s plug and play functionality (<u>Hashimoto</u>, Fig. 8; col. 1, II. 35-57; col. 3, I. 43 to col. 4, I. 67; col. 5, II. 43-57; col. 6, I. 16 to col. 9, I. 17; col. 10, I. 41 to col. 11, I. 42; col. 12, I. 16 to col. 13, I. 14; <u>Smith</u>, Fig. 2-5; col. 1, II. 9-22; col. 2, I. 40 to col. 3, I. 59; col. 5, II. 41-51; col. 6, II. 63-62 and <u>Ristelhueber</u>, pages 1-3).

Regarding Shinohara

13 - While <u>Shinohara</u> arguably discloses hard disk drive emulation in the context of the transfer of data from a memory to a PC, why would one of ordinary skill apply the arguably disclosed hard disk drive emulation concept in a wholly different context of device recognition as claimed in the new claims?

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The combination of <u>Hashimoto</u>, <u>Smith</u>, <u>Kerigan</u> and <u>Ristelhueber</u> teaches the utilization of a flash memory card (<u>Hashimoto</u>, Fig. 8, ref. 16) by a digital camera; however said combination does not teach the flash memory card emulating a hard disk drive. <u>Shinohara</u> teaches a flash memory card emulating a hard disk drive, and discloses that the lifetime usage of the flash memory card is expanded. It would have thus been obvious to one of ordinary skilled in the art to include the hard disk drive emulation disclosed in <u>Shinohara</u> into the flash memory card of <u>Hashimoto</u>, <u>Smith</u>, <u>Kerigan</u> and <u>Ristelhueber</u>, and as disclosed in <u>Shinohara</u>, the motivation for the combination would be expanding the lifetime usage of the memory card.

14 - While <u>Shinohara</u> teaches a memory card that responds to commands issued by a PC's card services program, why would one of ordinary skill apply <u>Shinohara</u> in the context of the claimed invention which requires the execution of program steps by a multi-use automatic processor?

As presented above in question 13, he combination of <u>Hashimoto</u>, <u>Smith</u>, <u>Kerigan</u> and <u>Ristelhueber</u> teaches the utilization of a flash memory card (<u>Hashimoto</u>, Fig. 8, ref. 16) by a digital camera; however said combination does not teach the flash memory card emulating a hard disk drive. <u>Shinohara</u> teaches a flash memory card emulating a hard disk drive, and discloses that the lifetime usage of the flash memory card is expanded. It would have thus been obvious to one of ordinary skilled in the art to include the hard disk drive emulation disclosed in <u>Shinohara</u> into the flash memory card of <u>Hashimoto</u>, <u>Smith</u>, <u>Kerigan</u> and <u>Ristelhueber</u>, and as disclosed in <u>Shinohara</u>, the

motivation for the combination would be expanding the lifetime usage of the memory card. Additionally, it is not fully clear to the examiner as to where in <u>Shinohara</u> teaches/suggests the card service program.

18. In response to applicant's arguments with regard to the independent claim 183 rejected under 35 U.S.C. 103(a) that <u>Hashimoto</u> and <u>Smith</u> teaches away from each other, because <u>Hashimoto</u> want to save power by having the communication circuitry in a low-power mode or standby mode, whereas <u>Smith</u> require the communication circuitry to be powered up before the DTR signal is received; applicant's arguments have fully been considered, but are not found to be persuasive.

The examiner respectfully disagrees, because no where in <u>Hashimoto</u> seems to teach that the communication circuitry is required to be activated when implementing the plug-and-play functionality. Additionally, the resulting combination of <u>Hashimoto</u>, <u>Smith</u> and <u>Ristelhueber</u> teaches/suggests the communication circuitry (e.g. for communication between the PC and the camera) is maintained in low-power mode or standby mode while implementing plug-and-play functionality (i.e. while the peripheral device is properly recognized by the PC), and subsequent the PC recognizing the connected peripheral device, the PC is ready to communication circuitry. Therefore, the combination of <u>Hashimoto</u>, <u>Smith</u> and <u>Ristelhueber</u> does teach implementing power saving functionality and plug and play functionality.

19. In response to applicant's arguments with regard to the independent claim 183 rejected under 35 U.S.C. 103(a) that <u>Kerigan</u> as a basis to combine <u>Smith</u> and <u>Hashimoto</u> is contrary to the teaching of <u>Kerigan</u>, because the connection of <u>Kerigan</u>'s camera to the PC is via a monitor, not directly to the PC; applicant's arguments have fully been considered, but are not found to be persuasive.

The examiner respectfully disagrees, because the examiner is not relying on <u>Kerigan</u> as the basis for the combination of references, <u>Kerigan</u> is only a supporting evidence to show the utilization of plug and play functionality with camera type peripheral device. <u>Smith</u> and <u>Ristelhueber</u> are the basis for the combination, as <u>Smith</u> and <u>Ristelhueber</u> teach peripheral device have plug and play functionality operating in accordance to the "PnP ISA Specification," and having the plug and play functionality in the peripheral device eases/simplifies the installation of the peripheral device in the PC by the user (<u>Smith</u>, Fig. 2-5; col. 1, II. 9-22; col. 2, I. 40 to col. 3, I. 59; col. 5, II. 41-51; col. 6, II. 63-62 and <u>Ristelhueber</u>, pages 1-3).

I. OATH / DECLARATION

20. The oath/declaration has been reviewed by the examiner and is found to comply with the provisions of 37 CFR 1.63.

II. FOREIGN PRIORITY

Acknowledgment is made of applicant's claim for foreign priority under 35
U.S.C. 119(a)-(d). The certified copy has been filed in parent Application No.
09/331,002, filed on 06/14/1999.

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III. TERMINAL DISCLAIMER

22. The terminal disclaimer filed on 10/30/2007 disclaiming the terminal portion of any patent granted on this application which would extend beyond the expiration date of US Patent 6,470,399 and 6,845,499 and any patent granted on application number 11/467,073 and 11/928,283 has been reviewed and is accepted. The terminal disclaimer has been recorded.

IV. REFERENCES CITED BY APPLICANT

23. The information disclosure statement filed on 01/07/2009; 1/26/2009; and 02/06/2009 fail to comply with 37 CFR 1.98(a)(2), which requires a legible copy of each cited foreign patent document; each non-patent literature publication or that portion which caused it to be listed; and all other information or that portion which caused it to be listed; and all other information or that portion which caused it to be listed in the application file, but the information referred to therein has not been considered.

V. DRAWINGS

24. The drawings are objected to because in Figure 2, element 1260 is not clearly linked to the EPP and element 1820 is not clearly linked to the precision voltage

reference, in a similar manner as other elements shown in Figure 2. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

VI. SPECIFICATION

25. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

26. The use of the trademark "Windows" and "Unix" has been noted in this application. It should be capitalized wherever it appears and be accompanied by the generic terminology.

Although the use of trademarks is permissible in patent applications, the proprietary nature of the marks should be respected and every effort made to prevent their use in any manner which might adversely affect their validity as trademarks.

27. The disclosure is objected to because of the following informalities:

status for each of the applications in paragraph [0001] of the Specification needs to be updated;

in paragraph [0038], "80-MHz clock generator" need to be clearly indicated as element 1320 in Figure 2 of the Drawings; and

multiple instances in the Specification refer to a plurality of abbreviations without clearly indicating what those abbreviations stands for; the plurality of abbreviations include MFM, FDD, PC, CD-ROM, DOS, EPROM, EEPROM, BNC, AC, DC, PCMCIA, TUV, UL, CSA, and MILSTD; the examiner suggest the following amendments to the Specification to clarify the above abbreviation: MFM (modified frequency modulation), FDD (floppy disk drive), PC (personal computer), CD-ROM (compact disk read-only memory), DOS (disk operating system), EPROM (erasable programmable read-only memory), EEPROM (electrical erasable programmable read-only memory), BNC (Bayonet Neil Concelman), AC (alternating current), DC (direct current), PCMCIA (personal computer memory card international association), TUV (Technischer

Überwachungsverein), UL (Underwriters Laboratories Inc.), CSA (Canadian Standard Association), and MILSTD (Military Standard).

Please note that the request for the replacements as stated above is for the purpose to improve the clarity of the Specification. Appropriate correction is required.

VII. OBJECTIONS TO THE CLAIMS

28. Claims 183-185, 196, 209, 224 and 237 are objected to because of the following informalities:

in claim 183, line 4, "... an i/o connector designed to be operatively coupled to an MPI of a PC; a program memory; a data storage memory ..." should be replaced with - ... an i/o (input / output) connector designed to be operatively coupled to the MPI of the PC; a program memory; a data storage memory ...-;

in claim 183, line 12, "... the sensor generates analog data ..." should be replaced with -... the sensor generates the analog data ...-;

in claim 183, line 19, "... the ADGPD has the ability to transfer files of digital data ..." should be replaced with -... the ADGPD has the ability to transfer <u>the one or more</u> files of digital data ...-;

in claim 183, lines 22-23, "... before a time when the PC is able to receive data files that are transferred to it from the ADGPD ..." should be replaced with -... before a time when the PC is able to receive <u>the one or more files of digital data</u> that are transferred to <u>the PC</u> from the ADGPD ...-;

in claim 184, "... wherein the ADGPD processor is adapted to execute one or more instructions sets stored in the program memory and thereby cause ADGPD file system information to be automatically sent to the PC (a) without any type of user intervention at any time by means of the PC and (b) at a point in time before a time when the PC is able to receive data files that are transferred to it from the ADGPD ..." should be replaced with

-... wherein the ADGPD processor is adapted to execute one or more instructions sets stored in the program memory and thereby cause ADGPD file system information to be automatically sent to the PC (a) without any type of user intervention at any time by means of the PC and (b) <u>before the time</u> when the PC is able to receive <u>the one or more files of digital data</u> that are transferred to <u>the PC</u> from the ADGPD ...-;

in claim 185, "... wherein the ADGPD processor is adapted to execute one or more instructions sets stored in the program memory in response to commands from the at least one software driver and thereby transfer one or more user-selected files of digitized analog data from the data storage memory without requiring any user intervention by means of the PC after the commands are sent ..." should be replaced with

-... wherein the ADGPD processor is adapted to execute one or more instructions sets stored in the program memory in response to <u>the</u> commands from the at least one software driver and thereby transfer <u>the</u> one or more user-selected files of digitized analog data from the data storage memory without requiring any user intervention by means of the PC after the commands are sent ...-;

in claim 196, lines 2-3, "... a process by which one or more files of digitized analog data stored in the data storage memory ..." should be replaced with -... a process by which <u>the</u> one or more files of digitized analog data stored in the data storage memory ...-;

in claim 209, lines 1-2, "... the ADGPD is designed for use with a PC ..." should be replaced with -... the ADGPD is designed for use with the PC ...-;

in claim 224, lines 1-2, "... wherein the sensor is designed to have two-way communication with a PC ..." should be replaced with -... wherein the sensor is designed to have two-way communication with <u>the</u> PC ...-; and

in claim 237, "... wherein the ADGPD processor is adapted to, after the at least one parameter has been sent to the PC, execute one or more instruction sets and thereby cause one or more user-selected files of digitized analog data to be transferred to the PC without requiring a user to have previously loaded file transfer enabling software on the PC ..." should be replaced with -... wherein the ADGPD processor is adapted to, after the at least one parameter has been sent to the PC, execute one or more instruction sets and thereby cause <u>the</u> one or more user-selected files of digitized analog data to be transferred to the PC without requiring <u>the</u> user to have previously loaded <u>the</u> file transfer enabling software on the PC ...-.

Please note that the request for the replacements as stated above is for the purpose to improve the clarity of the claim language. Appropriate correction is required.

VIII. <u>REJECTIONS BASED ON 35 U.S.C. 112</u>

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The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

29. Claims 220 is rejected under 35 U.S.C. 112, second paragraph, as being

indefinite for failing to particularly point out and distinctly claim the subject matter which

applicant regards as the invention.

Claim 220 recites the limitation "the same chip" in line 2. There is insufficient

antecedent basis for this limitation in the claim. The examiner will assume the claimed

limitation of "... a same chip ..." for the current examination.

IX. REJECTIONS BASED ON PRIOR ART

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

30. Claims 183-226, 230-235 and 237-238 are rejected under 35 U.S.C. 103(a) as being unpatentable over <u>Hashimoto et al.</u> (US Patent 6,111,604) in view of <u>Smith et al.</u> (US Patent 5,634,075), <u>Kerigan et al.</u> (US Patent 5,948,091), <u>Ristelhueber : "Plug and play is almost here"</u> and <u>Shinohara</u> (US Patent 5,742,934).

31. As per claim 183, <u>Hashimoto</u> teaches an analog data generating and processing device (ADGPD) (Fig. 1A-1B and Fig 8) for use with a personal computer (PC) having a

multi-purpose interface (MPI) (Fig. 8, ref. 29) and at least one software driver, the ADGPD comprising:

an i/o (input / output) connector designed to be operatively coupled to the MPI of the PC (Fig. 1A-1B; Fig. 8; col. 1, II. 35-57; col. 3, I. 43 to col. 4, I. 67; col. 5, II. 43-57; col. 6, I. 16 to col. 9, I. 17; col. 10, I. 41 to col. 11, I. 42 and col. 12, I. 16 to col. 13, I. 14), as the digital camera system have the corresponding i/o connector for connecting to the PC (Fig. 8, ref. 29);

a program memory (Fig. 9, ref. 52, 54-55 and col. 8, l. 48 to col. 9, l. 17);

a data storage memory (Fig. 8, ref. 16; Fig. 10; col. 6, l. 16 to col. 8, l. 47 and col. 9, ll. 18-45);

a sensor designed to generate analog data (e.g. audio and visual analog data) from one or more analog waves (e.g. audio and visual analog wave) to which the sensor is exposed (Fig. 8, ref. 1, 6, 9 and col. 6, l. 16 to col. 8, l. 47);

an ADGPD processor (Fig. 8, ref. 11, 23) operatively coupled to the i/o connector, the program memory (Fig. 9, ref. 52, 54-55), the data storage memory (Fig. 8, ref. 16) and the sensor (Fig. 8, ref. 1, 6, 9) (Fig. 8; Fig. 9; col. 6, I. 16 to col. 9, I. 17 and col. 10, I. 41 to col. 11, I. 42);

wherein the ADGPD is adapted to undergo a data generation process when the i/o connector is not coupled to the MPI of the PC by which the sensor generates the analog data (e.g. audio and visual analog data), the analog data is processed, and the processed analog data is stored in the data storage memory (Fig. 8, ref. 16 and Fig. 10) as one or more files of digitized analog data (Fig. 12) (Fig. 1A-1B; Fig. 11-12; Fig. 14-

15; col. 1, ll. 35-57; col. 3, l. 43 to col. 4, l. 57; col. 5, ll. 43-57; col. 6, l. 16 to col. 9, l. 17 and col. 9, l. 46 to col. 10, l. 16);

wherein the ADGPD processor is adapted to initiate the data generation process and be involved in an automatic recognition process in which, after the i/o connector has been operatively coupled to the MPI of the PC, the ADGPD processor executes at least one instruction set stored in the program memory to automatically transfer the one or more files of digital data through the i/o connector and to the MPI of the PC (Fig. 11-12; Fig. 14-15; col. 1, II. 35-57; col. 6, I. 16 to col. 9, I. 17; col. 9, I. 46 to col. 11, I. 42 and col. 12, I. 16 to col. 14, I. 14), wherein the digital camera's CPU (Fig. 8, ref. 23) control the operation of the digital camera for the data transferring after the digital camera is connected to and recognized by the PC, and as the digital camera's CPU control any function of the digital camera, the digital camera's CPU further controls the digital camera to be recognized by the PC; wherein the digital camera needs to be recognized by the PC in order for the PC to know what peripheral device is connected such that the PC knows how to properly communicate with the connected peripheral device; and

wherein the ADGPD is adapted to transfer the one or more files of digitized analog data to the PC (Fig. 11-12; Fig. 14-15; col. 1, II. 35-57; col. 6, I. 16 to col. 9, I. 17; col. 9, I. 46 to col. 11, I. 42 and col. 12, I. 16 to col. 14, I. 14).

Hashimoto does not teach the ADGPD comprising:

wherein the automatic recognition process in which ... at least one parameter regarding the ADGPD, which signifies that the ADGPD has the ability to transfer the one

or more data in response to commands issued from the at least one software driver, to be automatically sent to the PC (a) without any type of user intervention at any time by means of the PC and (b) before a time when the PC is able to receive the one or more data that are transferred to the PC from the ADGPD; and

wherein the ADGPD is adapted to, after the at least one parameter has been sent to the PC, transfer one or more user-selected data to the PC without requiring a user to have previously loaded file transfer enabling software on the PC.

Smith teaches a system and a method comprising: a peripheral device having an automatic recognition process in which, after the peripheral device's i/o connector has been operatively coupled to a PC, to cause at least one parameter regarding the peripheral device, which signifies that the peripheral device has the ability communicate in accordance to the at least one software driver, to be automatically sent through the i/o connector and to the PC before a time when the PC is able to communicate with the peripheral device; and wherein the peripheral device is adapted to, after the at least one parameter has been sent to the PC, communicate with the PC (e.g. as the system is configured and communication between the peripheral device is enabled) without requiring a user to have previously loaded software on the PC (i.e. installing device by the user without the need for supplemental software installation or device configuration: col. 5, II. 41-51) (Fig. 2-5; col. 1, II. 9-22; col. 2, I. 40 to col. 3, I. 59; col. 4, II. 5-34 and col. 6, II. 63-62), wherein the above automatic recognition process functionality is equivalent to configuring plug and play system utilizing ROM BIOS by having the operating system load the device driver after the peripheral device is coupled to the PC

for installation; furthermore, this equivalency is in accord with applicant's disclosure of the instant invention during the interview dated 2/3/2009 corresponding to "... the end result/outcome of the peripheral device operating in correspondence to plug-and-play ... is action caused by an individual by plugging a portable peripheral device into the computer and play the portable peripheral device without the need for the individual to load corresponding special driver or other software ...".

It would have been obvious for one of ordinary skill in this art, at the time of invention was made to include <u>Smith</u>'s plug and play functionality into <u>Hashimoto</u>'s ADGPD for the benefit of simplifying the installation of the peripheral device for the user as the peripheral device may be installed without the need for the user to install software or configure the peripheral device (<u>Smith</u>, col. 2, II. 40-67 and col. 5, II. 41-51 and col. 6, II. 63-65); additionally, <u>Kerigan</u> expressly teaches the utilization of the plug and play functionality with camera type peripheral device (<u>Kerigan</u>, col. 3, II. 29-33 and col. 6, II. 3-10) to obtain the invention as specified in claim 183.

Hashimoto, Smith and Kerigan do not expressly teach the ADGPD comprising:

wherein the automatic recognition process ... has the ability to transfer the one or more data in response to commands issued ... without any type of user intervention at any time by means of the PC; and

transfer one or more user-selected data to the PC.

Ristelhueber teaches a system and a method comprising a peripheral device having an automatic recognition process without any type of user intervention at any

time by means of the PC (pages 1-3), wherein the above automatic recognition process functionality is equivalent to plug and play of a peripheral device by having a user to simply insert a peripheral into a desktop system and have it start running immediately, as the PnP computer will automatically identify any new hardware installed and configure the new hardware, and relieving the end user of any need to fumble with floppy disks and user manuals to get the device up and running; therefore, the installation of the peripheral device is accomplished without any type of user intervention at any time by means of the PC; furthermore, this equivalency is in accord with applicant's disclosure of the instant invention during the interview dated 2/3/2009 corresponding to "... the end result/outcome of the peripheral device operating in correspondence to plug-and-play ... is action caused by an individual by plugging a portable peripheral device into the computer and play the portable peripheral device without the need for the individual to load corresponding special driver or other software ...".

It would have been obvious for one of ordinary skill in this art, at the time of invention was made to include <u>Ristelhueber</u>'s without user intervention into <u>Hashimoto</u>, <u>Smith</u> and <u>Kerigan</u>'s plug-and-play ADGPD, not only is such implementation well known to be in accord with the plug-and-play standard, but also for the benefit of simplifying the end user's PC upgrading and reducing cost for the computing industry (<u>Ristelhueber</u>, page 2, 3rd paragraph) to obtain the invention as specified in claim 183.

<u>Hashimoto</u>, <u>Smith</u>, <u>Kerigan</u> and <u>Ristelhueber</u> do not expressly teach the ADGPD comprising: ability to transfer the one or more data in response to commands issued; and transfer one or more user-selected data to the PC.

Shinohara teaches a system and a method comprising: a peripheral device (e.g. flash memory peripheral device) has the ability to transfer user-selected data in response to commands (e.g. data read command) issued from a PC; and the PC is able to receive the one or more data that are transferred to the PC from the peripheral device (col. 1, II. 48-60 and col. 3, I. 33 to col. 4, I. 49), in combining with <u>Hashimoto</u>, <u>Smith</u>, <u>Kerigan</u> and <u>Ristelhueber</u>'s user operated ADGPD, the received read command would correspond to the user selecting which data to read (i.e. transfer from peripheral device to PC).

It would have been obvious for one of ordinary skill in this art, at the time of invention was made to include <u>Shinohara</u>'s read command into <u>Hashimoto</u>, <u>Smith</u> and <u>Kerigan</u>'s plugand-play ADGPD for reading data from ADGPD's memory card, for the benefit of expressly allowing the ADGPD's user ease to select which files to read/transfer, as well as expanding the lifetime usage of the ADGPD's memory card (<u>Shinohara</u>, col. 2, II. 7-8) to obtain the invention as specified in claim 183.

32. As per claim 184, <u>Hashimoto</u>, <u>Smith</u>, <u>Kerigan</u>, <u>Ristelhueber</u> and <u>Shinohara</u> teach all the of limitations claim 183 as discussed above, where <u>Hashimoto</u>, <u>Smith</u>, <u>Ristelhueber</u> and <u>Shinohara</u> further teach the ADGPD comprising wherein the ADGPD processor is adapted to execute one or more instructions sets stored in the program

memory and thereby cause ADGPD file system information to be automatically sent to the PC (a) without any type of user intervention at any time by means of the PC and (b) before the time when the PC is able to receive the one or more files of digital data that are transferred to the PC from the ADGPD (Hashimoto, Fig. 8, ref. 11, 23; Fig. 9; col. 6, I. 16 to col. 9, I. 17; col. 10, I. 41 to col. 11, I. 42; <u>Smith</u>, Fig. 2-5; col. 1, II. 9-22; col. 2, I. 40 to col. 3, I. 8; col. 3, II. 22-27; col. 3, II. 53-59; col. 4, II. 5-34; col. 6, II. 63-62; <u>Ristelhueber</u>, pages 1-3; and <u>Shinohara</u>, col. 1, II. 48-60; col. 3, I. 56 to col. 4, I. 49), wherein the transferring of the ADGPD file system information is equivalent to the emulation of the hard disk drive by the plug-and-play ADGPD's memory card, as ADGPD file system information is forwarded to the PC during the recognition of the plug-and-play ADGPD in order to properly allow the ADGPD's memory card to emulate the hard disk driver for data transferring; furthermore, the equivalency is in accord with applicant's disclosure of the instant invention during the interview dated 2/3/2009 corresponding to "... the end result/outcome ... the computer is viewing the peripheral device as the simulated HDD (mass storage device) ...".

33. As per claim 185, <u>Hashimoto</u>, <u>Smith</u>, <u>Kerigan</u>, <u>Ristelhueber</u> and <u>Shinohara</u> teach all the of limitations claim 184 as discussed above, where <u>Hashimoto</u>, <u>Smith</u>, <u>Ristelhueber</u> and <u>Shinohara</u> further teach the ADGPD comprising wherein the ADGPD processor is adapted to execute one or more instructions sets stored in the program memory in response to the commands from the at least one software driver and thereby transfer the one or more user-selected files of digitized analog data from the data

storage memory without requiring any user intervention by means of the PC after the commands are sent (Hashimoto, Fig. 8, ref. 11, 23; Fig. 9; Fig. 14-16; col. 6, I. 16 to col. 9, I. 17; col. 10, I. 41 to col. 11, I. 42; <u>Smith</u>, Fig. 2-5; col. 1, II. 9-22; col. 2, I. 40 to col. 3, I. 8; col. 3, II. 22-27; col. 3, II. 53-59; col. 4, II. 5-34; col. 6, II. 63-62; <u>Ristelhueber</u>, pages 1-3; and <u>Shinohara</u>, col. 1, II. 48-60; col. 3, I. 56 to col. 4, I. 49), wherein the transferring of user-selected files of digitized analog data is equivalent to the transferring of the user selected digitized analog data from the plug-and-play ADGPD's memory card to the PC in response to the received data read command, while the plug-and-play ADGPD's memory card is emulating the hard disk drive; furthermore, the equivalency is in accord with applicant's disclosure of the instant invention during the interview dated 2/3/2009 corresponding to "... the end result/outcome ..." for the instant invention.

34. As per claim 186, <u>Hashimoto</u>, <u>Smith</u>, <u>Kerigan</u>, <u>Ristelhueber</u> and <u>Shinohara</u> teach all the of limitations claim 185 as discussed above, where <u>Hashimoto</u>, <u>Smith</u>, <u>Ristelhueber</u> and <u>Shinohara</u> further teach the ADGPD comprising wherein the at least one parameter is consistent with the ADGPD being a mass storage device (<u>Hashimoto</u>, Fig. 8, ref. 16; <u>Smith</u>, Fig. 2-5; col. 1, II. 9-22; col. 2, I. 40 to col. 3, I. 8; col. 3, II. 22-27; col. 3, II. 53-59; col. 4, II. 5-34; col. 6, II. 63-62; <u>Ristelhueber</u>, pages 1-3; and <u>Shinohara</u>, col. 1, II. 48-60; col. 3, I. 56 to col. 4, I. 49), wherein the ADGPD being a mass storage device is equivalent to the plug-and-play ADGPD having the memory card emulating as the hard disk drive; furthermore, the equivalency is in accord with applicant's disclosure of the instant invention during the interview dated 2/3/2009 corresponding to "... the end

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(mass storage device) ...".

35. As per claim 187, Hashimoto, Smith, Kerigan, Ristelhueber and Shinohara teach all the of limitations claim 186 as discussed above, where Hashimoto, Smith, Ristelhueber and Shinohara further teach the ADGPD comprising wherein the ADGPD processor and the program memory are configured to cause, after the at least one parameter has been sent to the i/o connector, file allocation table information to be sent to the i/o connector, wherein the ADGPD processor and the program memory are configured to cause a virtual boot sequence to be sent to the i/o connector which includes at least information that is representative of a number of sectors of a storage disk, and wherein the file allocation table information includes at least a start location of a file allocation table (Hashimoto, Fig. 8, ref. 16; Smith, Fig. 2-5; col. 1, II. 9-22; col. 2, I. 40 to col. 3, I. 8; col. 3, II. 22-27; col. 3, II. 53-59; col. 4, II. 5-34; col. 6, II. 63-62; Ristelhueber, pages 1-3; and Shinohara, col. 1, II. 48-60; col. 3, I. 56 to col. 4, I. 49), wherein the transferring of the parameter, the file allocation table information and the virtual boot sequence is equivalent to the plug-and-play ADGPD having the memory card emulating as the hard disk drive for data transferring after the plug-and-play ADGPD is connected to the PC; furthermore, this equivalency is in accord with applicant's disclosure of the instant invention during the interview dated 2/3/2009 corresponding to "... the end result/outcome of the peripheral device operating in correspondence to plug-and-play ... is action caused by an individual by plugging a

portable peripheral device into the computer and play (e.g. transferring data) the portable peripheral device without the need for the individual to load corresponding special driver or other software ... the computer is viewing the peripheral device as the simulated HDD (mass storage device) ...".

36. As per claim 188, <u>Hashimoto, Smith, Kerigan, Ristelhueber</u> and <u>Shinohara</u> teach all the of limitations claim 187 as discussed above, where <u>Hashimoto, Smith,</u> <u>Ristelhueber</u> and <u>Shinohara</u> further teach the ADGPD comprising wherein the at least one parameter is consistent with the ADGPD being adapted to operate in a manner consistent with a hard disk drive (e.g. hard drive emulation) (<u>Hashimoto</u>, Fig. 8, ref. 16; <u>Smith</u>, Fig. 2-5; col. 1, II. 9-22; col. 2, I. 40 to col. 3, I. 8; col. 3, II. 22-27; col. 3, II. 53-59; col. 4, II. 5-34; col. 6, II. 63-62; <u>Ristelhueber</u>, pages 1-3; and <u>Shinohara</u>, col. 1, II. 48-60; col. 3, I. 56 to col. 4, I. 49), wherein the operation consistent with the hard disk drive is equivalent to the plug-and-play ADGPD having the memory card emulating as the hard disk drive for data transferring after the plug-and-play ADGPD is connected to the PC; furthermore, this equivalency is in accord with applicant's disclosure of the instant invention during the interview dated 2/3/2009 corresponding to "... the end result/outcome ... the computer is viewing the peripheral device as the simulated HDD (mass storage device) ...".

37. As per claim 189, <u>Hashimoto</u>, <u>Smith</u>, <u>Kerigan</u>, <u>Ristelhueber</u> and <u>Shinohara</u> teach all the of limitations claim 188 as discussed above, where <u>Hashimoto</u> further teaches

Application/Control Number: 11/467,092Page 47Art Unit: 2181the ADGPD comprising wherein the ADGPD processor is formed in a single chip

(<u>Hashimoto</u>, col. 8, l. 49 to col. 9, l. 17).

38. As per claim 190, <u>Hashimoto</u>, <u>Smith</u>, <u>Kerigan</u>, <u>Ristelhueber</u> and <u>Shinohara</u> teach all the of limitations claim 189 as discussed above, where <u>Hashimoto</u> further teaches the ADGPD comprising wherein the ADGPD processor includes a single central processing unit (<u>Hashimoto</u>, col. 8, I. 49 to col. 9, I. 17).

39. As per claim 191, <u>Hashimoto</u>, <u>Smith</u>, <u>Kerigan</u>, <u>Ristelhueber</u> and <u>Shinohara</u> teach all the of limitations claim 188 as discussed above, where <u>Hashimoto</u> further teaches the ADGPD comprising wherein the program memory is formed in a single chip (<u>Hashimoto</u>, col. 8, I. 49 to col. 9, I. 17).

40. As per claim 192, <u>Hashimoto</u>, <u>Smith</u>, <u>Kerigan</u>, <u>Ristelhueber</u> and <u>Shinohara</u> teach all the of limitations claim 191 as discussed above, where <u>Hashimoto</u> further teaches the ADGPD comprising wherein the program memory comprises a single memory device (<u>Hashimoto</u>, col. 8, I. 49 to col. 9, I. 17).

41. As per claim 193, <u>Hashimoto</u>, <u>Smith</u>, <u>Kerigan</u>, <u>Ristelhueber</u> and <u>Shinohara</u> teach all the of limitations claim 188 as discussed above, where <u>Hashimoto</u> further teaches the ADGPD comprising wherein the data storage memory comprises a single memory

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 device (<u>Hashimoto</u>, Fig. 8, ref. 16; Fig. 10; col. 6, l. 16 to col. 8, l. 47 and col. 9, ll. 18

 45).

42. As per claim 194, <u>Hashimoto</u>, <u>Smith</u>, <u>Kerigan</u>, <u>Ristelhueber</u> and <u>Shinohara</u> teach all the of limitations claim 184 as discussed above, where <u>Shinohara</u> further teaches the ADGPD comprising wherein the ADGPD file system information comprises at least an indication of the type of a file system (e.g. hard disk drive file system) that is used to store each one of the one or more files of digitized analog data in the data storage memory (<u>Shinohara</u>, col. 1, II. 48-60; col. 3, I. 56 to col. 4, I. 49), wherein the indication of the type of file system is equivalent to the plug-and-play ADGPD having the memory card emulating as the hard disk drive for data transferring after the plug-and-play ADGPD is connected to the PC; furthermore, this equivalency is in accord with applicant's disclosure of the instant invention during the interview dated 2/3/2009 corresponding to "... the end result/outcome ... the computer is viewing the peripheral device as the simulated HDD (mass storage device) ...".

43. As per claim 195, <u>Hashimoto</u>, <u>Smith</u>, <u>Kerigan</u>, <u>Ristelhueber</u> and <u>Shinohara</u> teach all the of limitations claim 183 as discussed above, where <u>Hashimoto</u> further teaches the ADGPD comprising further comprising an output device (e.g. speaker) that is operatively coupled to the ADGPD processor, the output device being capable of generating one or more analog waves that are representative of at least some of the analog data that is generated by the sensor (<u>Hashimoto</u>, Fig. 8 and col. 6, II. 16-39).

44. As per claim 196, <u>Hashimoto</u>, <u>Smith</u>, <u>Kerigan</u>, <u>Ristelhueber</u> and <u>Shinohara</u> teach all the of limitations claim 183 as discussed above, where <u>Hashimoto</u> further teaches the ADGPD comprising wherein the ADGPD processor and the program memory are configured to initiate a process by which the one or more files of digitized analog data stored in the data storage memory are directly transferred to an input/output device by means of the i/o connector (<u>Hashimoto</u>, Fig. 8; Fig. 12; Fig. 14-15; col. 1, II. 35-57; col. 6, I. 16 to col. 9, I. 17 and col. 9, I. 46 to col. 11, I. 42).

45. As per claim 197, <u>Hashimoto</u>, <u>Smith</u>, <u>Kerigan</u>, <u>Ristelhueber</u> and <u>Shinohara</u> teach all the of limitations claim 196 as discussed above, where <u>Hashimoto</u> further teaches the ADGPD comprising wherein the ADGPD processor and the program memory are adapted to allow an aspect of operation (e.g. updating control program) of the ADGPD other than the transfer of at least some of the one or more files of digitized analog data from the data storage memory to the i/o connector to be controlled by means of the PC (<u>Hashimoto</u>, col. 6, l. 16 to col. 9, l. 17), as the PC directly update the control program in the ADGPD.

46. As per claim 198, <u>Hashimoto</u>, <u>Smith</u>, <u>Kerigan</u>, <u>Ristelhueber</u> and <u>Shinohara</u> teach all the of limitations claim 183 as discussed above, where <u>Hashimoto</u>, <u>Smith</u>, <u>Ristelhueber</u> and <u>Shinohara</u> further teach the ADGPD comprising wherein the at least one parameter is consistent with the ADGPD being a mass storage device (<u>Hashimoto</u>,

Fig. 8, ref. 16; <u>Smith</u>, Fig. 2-5; col. 1, II. 9-22; col. 2, I. 40 to col. 3, I. 8; col. 3, II. 22-27; col. 3, II. 53-59; col. 4, II. 5-34; col. 6, II. 63-62; <u>Ristelhueber</u>, pages 1-3; and <u>Shinohara</u>, col. 1, II. 48-60; col. 3, I. 56 to col. 4, I. 49), wherein the ADGPD being a mass storage device is equivalent to the plug-and-play ADGPD having the memory card emulating as the hard disk drive, and the equivalency in accord with applicant's disclosure of the instant invention during the interview dated 2/3/2009 corresponding to "... the end result/outcome ... the computer is viewing the peripheral device as the simulated HDD (mass storage device) ...".

47. As per claim 199, <u>Hashimoto</u>, <u>Smith</u>, <u>Kerigan</u>, <u>Ristelhueber</u> and <u>Shinohara</u> teach all the of limitations claim 183 as discussed above, where <u>Smith</u> further teaches the ADGPD comprising wherein the at least one parameter is consistent with the ADGPD being responsive to a SCSI command set (<u>Smith</u>, col. 1, II. 9-22), wherein SCSI command set is utilized as the interconnection between the peripheral device and the PC is implemented via SCSI interface.

48. As per claim 200, <u>Hashimoto</u>, <u>Smith</u>, <u>Kerigan</u>, <u>Ristelhueber</u> and <u>Shinohara</u> teach all the of limitations claim 183 as discussed above, where <u>Hashimoto</u>, <u>Smith</u>, <u>Ristelhueber</u> and <u>Shinohara</u> further teach the ADGPD comprising wherein the at least one parameter is not consistent with the true nature of the ADGPD device (<u>Hashimoto</u>, Fig. 8; <u>Smith</u>, Fig. 2-5; col. 1, II. 9-22; col. 2, I. 40 to col. 3, I. 8; col. 3, II. 22-27; col. 3, II. 53-59; col. 4, II. 5-34; col. 6, II. 63-62; <u>Ristelhueber</u>, pages 1-3 and <u>Shinohara</u>, col. 1, II.

48-60; col. 3, I. 56 to col. 4, I. 49), as the ADGPD's true nature is associated with processing analog signal and the parameter corresponds to emulating the hard disk drive, which is in accord with applicant's disclosure of the instant invention during the interview dated 2/3/2009 corresponding to "... the end result/outcome ... " for the instant invention.

49. As per claim 201, <u>Hashimoto</u>, <u>Smith</u>, <u>Kerigan</u>, <u>Ristelhueber</u> and <u>Shinohara</u> teach all the of limitations claim 183 as discussed above, where <u>Hashimoto</u>, <u>Smith</u> and <u>Shinohara</u> further teach the ADGPD comprising wherein the at least one parameter does not indicate that the ADGPD includes the sensor (<u>Hashimoto</u>, Fig. 8; <u>Smith</u>, Fig. 2-5; col. 1, II. 9-22; col. 2, I. 40 to col. 3, I. 8; col. 3, II. 22-27; col. 3, II. 53-59; col. 4, II. 5-34; col. 6, II. 63-62; and <u>Shinohara</u>, col. 1, II. 48-60; col. 3, I. 56 to col. 4, I. 49), as the parameter indicates to the PC the hard disk drive without indicating that the ADGPD includes the sensors for recording the image and audio, which is in accord with applicant's disclosure of the instant invention during the interview dated 2/3/2009 corresponding to "... the end result/outcome ... " for the instant invention.

50. As per claim 202, <u>Hashimoto</u>, <u>Smith</u>, <u>Kerigan</u>, <u>Ristelhueber</u> and <u>Shinohara</u> teach all the of limitations claim 183 as discussed above, where <u>Hashimoto</u>, <u>Smith</u>, <u>Ristelhueber</u> and <u>Shinohara</u> further teach the ADGPD comprising wherein the at least one parameter is consistent with the ADGPD being an input/output device (e.g. hard disk drive) customary in a host device (<u>Hashimoto</u>, Fig. 8, ref. 16; <u>Smith</u>, Fig. 2-5; col. 1,

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 II. 9-22; col. 2, I. 40 to col. 3, I. 8; col. 3, II. 22-27; col. 4, II. 5-34; col. 5, II.41-51; col. 6, II.

 63-62; <u>Ristelhueber</u>, pages 1-3 and <u>Shinohara</u>, col. 1, II. 48-60; col. 3, I. 56 to col. 4, I.

49).

51. As per claim 203, <u>Hashimoto</u>, <u>Smith</u>, <u>Kerigan</u>, <u>Ristelhueber</u> and <u>Shinohara</u> teach all the of limitations claim 202 as discussed above, where <u>Hashimoto</u>, <u>Smith</u>, <u>Ristelhueber</u> and <u>Shinohara</u> further teach the ADGPD comprising wherein the at least one parameter is consistent with the ADGPD being a hard disk drive (<u>Hashimoto</u>, Fig. 8, ref. 16; <u>Smith</u>, Fig. 2-5; col. 1, II. 9-22; col. 2, I. 40 to col. 3, I. 8; col. 3, II. 22-27; col. 3, II. 53-59; col. 4, II. 5-34; col. 6, II. 63-62; <u>Ristelhueber</u>, pages 1-3 and <u>Shinohara</u>, col. 1, II. 48-60; col. 3, I. 56 to col. 4, I. 49), wherein the parameter corresponding to the hard disk drive is equivalent to the plug-and-play ADGPD having the memory card emulating as the hard disk drive; furthermore, the equivalency is in accord with applicant's disclosure of the instant invention during the interview dated 2/3/2009 corresponding to "… the end result/outcome … the computer is viewing the peripheral device as the simulated HDD (mass storage device) …".

52. As per claim 204, <u>Hashimoto</u>, <u>Smith</u>, <u>Kerigan</u>, <u>Ristelhueber</u> and <u>Shinohara</u> teach all the of limitations claim 183 as discussed above, where <u>Hashimoto</u> further teaches the ADGPD comprising wherein the ADGPD comprises at least a portion of a medical device (<u>Hashimoto</u>, Fig. 1A-1B; Fig. 8; Fig. 11-12; Fig. 14-15; col. 1, II. 35-57; col. 6, I.

16 to col. 9, l. 17; col. 9, l. 46 to col. 11, l. 42 and col. 12, l. 16 to col. 14, l. 14), such as pictures taken for medical use.

53. As per claim 205, <u>Hashimoto</u>, <u>Smith</u>, <u>Kerigan</u>, <u>Ristelhueber</u> and <u>Shinohara</u> teach all the of limitations claim 183 as discussed above, where <u>Hashimoto</u> further teaches the ADGPD comprising wherein the ADGPD comprises at least a portion of a data acquisition system (<u>Hashimoto</u>, Fig. 1A-1B; Fig. 8; Fig. 11-12; Fig. 14-15; col. 1, II. 35-57; col. 6, I. 16 to col. 9, I. 17; col. 9, I. 46 to col. 11, I. 42 and col. 12, I. 16 to col. 14, I. 14), as the ADGPD acquires the image and audio data.

54. As per claim 206, <u>Hashimoto</u>, <u>Smith</u>, <u>Kerigan</u>, <u>Ristelhueber</u> and <u>Shinohara</u> teach all the of limitations claim 183 as discussed above, where <u>Smith</u> further teaches the ADGPD comprising wherein the i/o connector comprises a parallel port (<u>Smith</u>, col. 1, II. 9-22), as the interconnection between ADGPD and the PC is implemented via parallel port.

55. As per claim 207, <u>Hashimoto</u>, <u>Smith</u>, <u>Kerigan</u>, <u>Ristelhueber</u> and <u>Shinohara</u> teach all the of limitations claim 183 as discussed above, where <u>Smith</u> further teaches the ADGPD comprising wherein the i/o connector comprises a SCSI connector (<u>Smith</u>, col. 1, II. 9-22), wherein ADGPD include the corresponding SCSI connector for connecting to the PC via a SCSI port.

56. As per claim 208, <u>Hashimoto</u>, <u>Smith</u>, <u>Kerigan</u>, <u>Ristelhueber</u> and <u>Shinohara</u> teach all the of limitations claim 183 as discussed above, where <u>Hashimoto</u> further teaches the ADGPD comprising wherein the i/o connector is adapted to be operatively coupled to a cable (<u>Hashimoto</u>, 1A-1B; Fig. 8; Fig. 14-16; col. 1, II. 35-57; col. 3, I. 43 to col. 4, I. 57; col. 6, I. 16 to col. 9, I. 17 and col. 9, I. 46 to col. 10, I. 16).

57. As per claim 209, <u>Hashimoto</u>, <u>Smith</u>, <u>Kerigan</u>, <u>Ristelhueber</u> and <u>Shinohara</u> teach all the of limitations claim 183 as discussed above, where <u>Smith</u> further teaches the ADGPD comprising wherein the ADGPD is designed for use with the PC that has an operating system that is designed by a particular software company (<u>Smith</u>, col. 3, II. 48-51).

58. As per claim 210, <u>Hashimoto</u>, <u>Smith</u>, <u>Kerigan</u>, <u>Ristelhueber</u> and <u>Shinohara</u> teach all the of limitations claim 183 as discussed above, where <u>Hashimoto</u> further teaches the ADGPD comprising the ADGPD processor is formed in a single chip (<u>Hashimoto</u>, col. 8, l. 49 to col. 9, l. 17).

59. As per claim 211, <u>Hashimoto</u>, <u>Smith</u>, <u>Kerigan</u>, <u>Ristelhueber</u> and <u>Shinohara</u> teach all the of limitations claim 183 as discussed above, where <u>Hashimoto</u> further teaches the ADGPD comprising wherein the ADGPD processor comprises a single microprocessor (<u>Hashimoto</u>, col. 8, I. 49 to col. 9, I. 17).

60. As per claim 212, <u>Hashimoto</u>, <u>Smith</u>, <u>Kerigan</u>, <u>Ristelhueber</u> and <u>Shinohara</u> teach all the of limitations claim 183 as discussed above, where <u>Hashimoto</u> further teaches the ADGPD comprising wherein the ADGPD processor comprises a single digital signal processor (<u>Hashimoto</u>, Fig. 8, ref. 11 and col. 8, l. 49 to col. 9, l. 17).

61. As per claim 213, <u>Hashimoto</u>, <u>Smith</u>, <u>Kerigan</u>, <u>Ristelhueber</u> and <u>Shinohara</u> teach all the of limitations claim 183 as discussed above, where <u>Hashimoto</u> further teaches the ADGPD comprising wherein the program memory is formed in a single chip (<u>Hashimoto</u>, col. 8, I. 49 to col. 9, I. 17).

62. As per claim 214, <u>Hashimoto</u>, <u>Smith</u>, <u>Kerigan</u>, <u>Ristelhueber</u> and <u>Shinohara</u> teach all the of limitations claim 183 as discussed above, where <u>Hashimoto</u> further teaches the ADGPD comprising wherein the program memory comprises a single memory device (<u>Hashimoto</u>, col. 8, I. 49 to col. 9, I. 17).

63. As per claim 215, <u>Hashimoto</u>, <u>Smith</u>, <u>Kerigan</u>, <u>Ristelhueber</u> and <u>Shinohara</u> teach all the of limitations claim 183 as discussed above, where <u>Hashimoto</u> further teaches the ADGPD comprising wherein the data storage memory comprises a single memory device (<u>Hashimoto</u>, Fig. 8, ref. 16; Fig. 10; col. 6, l. 16 to col. 8, l. 47 and col. 9, ll. 18-45).

64. As per claim 216, <u>Hashimoto</u>, <u>Smith</u>, <u>Kerigan</u>, <u>Ristelhueber</u> and <u>Shinohara</u> teach all the of limitations claim 183 as discussed above, where <u>Hashimoto</u> further teaches the ADGPD comprising wherein the data storage memory comprises a semiconductor based memory (e.g. flash memory) (<u>Hashimoto</u>, Fig. 8, ref. 16; Fig. 10; col. 6, l. 16 to col. 8, l. 47 and col. 9, ll. 18-45).

65. As per claim 217, <u>Hashimoto</u>, <u>Smith</u>, <u>Kerigan</u>, <u>Ristelhueber</u> and <u>Shinohara</u> teach all the of limitations claim 183 as discussed above, where <u>Hashimoto</u> and <u>Smith</u> further teach the ADGPD comprising wherein the ADGPD includes a flexible interface (<u>Hashimoto</u>, Fig. 1A-1B; Fig. 8; Fig. 17; col. 1, II. 35-57; col. 6, I. 16 to col. 9, I. 17; col. 9, I. 46 to col. 11, I. 19, and <u>Smith</u>, Fig. 2-5; col. 1, II. 9-22; col. 2, I. 40 to col. 3, I. 8; col. 3, II. 22-27; col. 4, II. 5-34; col. 5, II.41-51 ; col. 6, II. 63-62; col. 11, II. 52-61).

66. As per claim 218, <u>Hashimoto</u>, <u>Smith</u>, <u>Kerigan</u>, <u>Ristelhueber</u> and <u>Shinohara</u> teach all the of limitations claim 183 as discussed above, where <u>Hashimoto</u> and <u>Smith</u> further teach the ADGPD comprising wherein the ADGPD includes a universal interface (<u>Hashimoto</u>, col. 1, II. 35-57 and <u>Smith</u>, Fig. 2-5; col. 1, II. 9-22; col. 2, I. 40 to col. 3, I. 8; col. 3, II. 22-27; col. 4, II. 5-34; col. 5, II.41-51 and col. 6, II. 63-62).

67. As per claim 219, <u>Hashimoto</u>, <u>Smith</u>, <u>Kerigan</u>, <u>Ristelhueber</u> and <u>Shinohara</u> teach all the of limitations claim 183 as discussed above, where <u>Hashimoto</u> further teaches the ADGPD further comprising an ADGPD interface (<u>Hashimoto</u>, Fig. 8, ref. 27) that is

Application/Control Number: 11/467,092Page 57Art Unit: 2181operatively coupled between the i/o connector and the ADGPD processor (Hashimoto,Fig. 8, ref. 11, 23).

68. As per claim 220, <u>Hashimoto</u>, <u>Smith</u>, <u>Kerigan</u>, <u>Ristelhueber</u> and <u>Shinohara</u> teach all the of limitations claim 219 as discussed above, where <u>Hashimoto</u> further teaches the ADGPD comprising wherein the ADGPD interface (<u>Hashimoto</u>, Fig. 8, ref. 27) and the ADGPD processor (<u>Hashimoto</u>, Fig. 8, ref. 11, 23) are not formed in a same chip (e.g. separate chips) (<u>Hashimoto</u>, Fig. 8 and col. 7, I. 64 to col. 9, I. 17).

69. As per claim 221, <u>Hashimoto</u>, <u>Smith</u>, <u>Kerigan</u>, <u>Ristelhueber</u> and <u>Shinohara</u> teach all the of limitations claim 219 as discussed above, where <u>Smith</u> further teaches the ADGPD comprising wherein the ADGPD interface comprises a SCSI interface (<u>Smith</u>, col. 1, II. 9-22 and col. 7, I. 64 to col. 9, I. 17), as the interconnection between ADGPD and the PC is implemented via SCSI port.

70. As per claim 222, <u>Hashimoto</u>, <u>Smith</u>, <u>Kerigan</u>, <u>Ristelhueber</u> and <u>Shinohara</u> teach all the of limitations claim 219 as discussed above, where <u>Smith</u> further teaches the ADGPD comprising wherein the ADGPD interface comprises a parallel logic circuit (<u>Smith</u>, col. 1, II. 9-22 and col. 7, I. 64 to col. 9, I. 17), wherein the corresponding parallel logic circuit is required as the interconnection between ADGPD and the PC is implemented via parallel port.

71. As per claim 223, <u>Hashimoto</u>, <u>Smith</u>, <u>Kerigan</u>, <u>Ristelhueber</u> and <u>Shinohara</u> teach all the of limitations claim 183 as discussed above, where <u>Hashimoto</u> further teaches the ADGPD comprising wherein the ADGPD includes a stand-alone interface device (e.g. stand-along digital camera) (<u>Hashimoto</u>, Fig. 8).

72. As per claim 224, <u>Hashimoto</u>, <u>Smith</u>, <u>Kerigan</u>, <u>Ristelhueber</u> and <u>Shinohara</u> teach all the of limitations claim 183 as discussed above, where <u>Hashimoto</u> further teaches the ADGPD comprising wherein the sensor is designed to have two-way communication with the PC (<u>Hashimoto</u>, Fig. 8; col. 6, I. 16 to col. 9, I. 17 and col. 10, I. 41 to col. 11, I. 19), such as the PC receiving audiovisual information from the camera and communicating to the camera by updating control program to control the sensor.

73. As per claim 225, <u>Hashimoto</u>, <u>Smith</u>, <u>Kerigan</u>, <u>Ristelhueber</u> and <u>Shinohara</u> teach all the of limitations claim 183 as discussed above, where <u>Hashimoto</u> further teaches the ADGPD comprising wherein the sensor comprises a data transmit/receive device <u>Hashimoto</u>, Fig. 8; col. 6, I. 16 to col. 9, I. 17 and col. 10, I. 41 to col. 11, I. 19), wherein the data transmit/receive device is required for transferring the audiovisual information to the PC and receiving control instruction from the PC.

74. As per claim 226, <u>Hashimoto</u>, <u>Smith</u>, <u>Kerigan</u>, <u>Ristelhueber</u> and <u>Shinohara</u> teach all the of limitations claim 225 as discussed above, where <u>Hashimoto</u> further teaches the ADGPD comprising wherein the data transmit/receive device is designed to receive

Application/Control Number: 11/467,092Page 59Art Unit: 2181data from the PC (Hashimoto, Fig. 8; col. 6, I. 16 to col. 9, I. 17 and col. 10, I. 41 to col.11, I. 19), such as the receiver needed for receiving control instruction data from the PC.

75. As per claim 230, <u>Hashimoto</u>, <u>Smith</u>, <u>Kerigan</u>, <u>Ristelhueber</u> and <u>Shinohara</u> teach all the of limitations claim 183 as discussed above, where <u>Hashimoto</u> further teaches the ADGPD comprising wherein the sensor includes at least first and second transducers that are designed to generate analog data that corresponds to first (e.g. imaging) and second (e.g. audio) analog waves, respectively, to which the first and second transducers are exposed (<u>Hashimoto</u>, Fig. 8; Fig. 11; and col. 9, II. 46-54), wherein the first and the second transducer are required for converting the imaging analog wave to the image digital signal by the first transducer and converting the audio analog wave to the audio digital signal by the second transducer.

76. As per claim 231, <u>Hashimoto</u>, <u>Smith</u>, <u>Kerigan</u>, <u>Ristelhueber</u> and <u>Shinohara</u> teach all the of limitations claim 183 as discussed above, where <u>Hashimoto</u>, <u>Smith</u>, <u>Ristelhueber</u> and <u>Shinohara</u> further teach the ADGPD comprising wherein the ADGPD processor and the program memory are configured to be involved with the automatic recognition process as a response to a SCSI inquiry command (<u>Hashimoto</u>, Fig. 8; Fig. 9, ref. 52, 54-55; col. 6, I. 16 to col. 9, I. 17 and col. 10, I. 41 to col. 11, I. 42; <u>Smith</u>, Fig. 2-5; col. 1, II. 9-22; col. 2, I. 40 to col. 3, I. 8; col. 3, II. 22-27; col. 3, II. 53-59; col. 4, II. 5-34; col. 6, II. 63-62; <u>Ristelhueber</u>, pages 1-3; and <u>Shinohara</u>, col. 1, II. 48-60; col. 3, I. 56 to col. 4, I. 49), wherein the response to a SCSI inquiry is equivalent to the plug-and-

play ADGPD having the memory card emulating as the hard disk drive for data transferring after the plug-and-play ADGPD is connected to the PC via the SCSI port; furthermore, this equivalency is in accord with applicant's disclosure of the instant invention during the interview dated 2/3/2009 corresponding to "... the end result/outcome ..." for the instant invention.

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77. As per claim 232, <u>Hashimoto</u>, <u>Smith</u>, <u>Kerigan</u>, <u>Ristelhueber</u> and <u>Shinohara</u> teach all the of limitations claim 183 as discussed above, where <u>Hashimoto</u>, <u>Smith</u>, <u>Ristelhueber</u> and <u>Shinohara</u> further teach the ADGPD comprising wherein the ADGPD processor is adapted to execute the at least one instruction set to thereby directly cause the at least one parameter regarding the ADGPD to be automatically sent to the PC (<u>Hashimoto</u>, Fig. 8; Fig. 9, ref. 52, 54-55; col. 6, I. 16 to col. 9, I. 17 and col. 10, I. 41 to col. 11, I. 42; <u>Smith</u>, Fig. 2-5; col. 1, II. 9-22; col. 2, I. 40 to col. 3, I. 8; col. 3, II. 22-27; col. 3, II. 53-59; col. 4, II. 5-34; col. 6, II. 63-62; <u>Ristelhueber</u>, pages 1-3; and <u>Shinohara</u>, col. 1, II. 48-60; col. 3, I. 56 to col. 4, I. 49), wherein the sending of the parameter is equivalent to the plug-and-play ADGPD; furthermore, this equivalency is in accord with applicant's disclosure of the instant invention during the interview dated 2/3/2009 corresponding to "... the end result/outcome ..." for the instant invention.

78. As per claim 233, <u>Hashimoto</u>, <u>Smith</u>, <u>Kerigan</u>, <u>Ristelhueber</u> and <u>Shinohara</u> teach all the of limitations claim 232 as discussed above, where <u>Hashimoto</u> further teaches

Application/Control Number: 11/467,092Page 61Art Unit: 2181the ADGPD comprising wherein the ADGPD processor is formed in a single chip

(<u>Hashimoto</u>, Fig. 8 and col. 8, I. 49 to col. 9, I. 17).

79. As per claim 234, <u>Hashimoto</u>, <u>Smith</u>, <u>Kerigan</u>, <u>Ristelhueber</u> and <u>Shinohara</u> teach all the of limitations claim 233 as discussed above, where <u>Hashimoto</u> further teaches the ADGPD comprising wherein the ADGPD processor includes a single central processing unit (CPU) (<u>Hashimoto</u>, Fig. 8 and col. 8, I. 49 to col. 9, I. 17).

80. As per claim 235, <u>Hashimoto</u>, <u>Smith</u>, <u>Kerigan</u>, <u>Ristelhueber</u> and <u>Shinohara</u> teach all the of limitations claim 233 as discussed above, where <u>Hashimoto</u> further teaches the ADGPD comprising wherein the program memory comprises a single memory device (<u>Hashimoto</u>, col. 8, I. 49 to col. 9, I. 17).

81. As per claim 237, <u>Hashimoto</u>, <u>Smith</u>, <u>Kerigan</u>, <u>Ristelhueber</u> and <u>Shinohara</u> teach all the of limitations claim 183 as discussed above, where <u>Hashimoto</u>, <u>Smith</u>, <u>Ristelhueber</u> and <u>Shinohara</u> further teach the ADGPD comprising wherein the ADGPD processor is adapted to, after the at least one parameter has been sent to the PC, execute one or more instruction sets and thereby cause the one or more user-selected files of digitized analog data to be transferred to the PC without requiring the user to have previously loaded the file transfer enabling software on the PC (<u>Hashimoto</u>, Fig. 8; Fig. 9, ref. 52, 54-55; Fig. 14; col. 6, l. 16 to col. 9, l. 54 and col. 10, l. 41 to col. 11, l. 42; <u>Smith</u>, Fig. 2-5; col. 1, ll. 9-22; col. 2, l. 40 to col. 3, l. 8; col. 3, ll. 22-27; col. 3, ll. 53-59;

col. 4, II. 5-34; col. 6, II. 63-62; <u>Ristelhueber</u>, pages 1-3; and <u>Shinohara</u>, col. 1, II. 48-60; col. 3, I. 56 to col. 4, I. 49), wherein the above transferring of data functionality is equivalent to the transferring of user selected image/audio files from the plug-and-play ADGPD's memory card to the PC; furthermore, this equivalency is in accord with applicant's disclosure of the instant invention during the interview dated 2/3/2009 corresponding to "...the end result/outcome of the peripheral device operating in correspondence to plug-and-play, which is action caused by an individual by plugging a portable peripheral device into the computer and play (e.g. transferring data) the portable peripheral device without the need for the individual to load corresponding special driver or other software...".

82. As per claim 238, <u>Hashimoto</u>, <u>Smith</u>, <u>Kerigan</u>, <u>Ristelhueber</u> and <u>Shinohara</u> teach all the of limitations claim 183 as discussed above, where <u>Hashimoto</u>, <u>Smith</u>, <u>Ristelhueber</u> and <u>Shinohara</u> further teach a combination comprising the ADGPD of claim 183 and a PC (e.g. combination of the plug-and-play digital camera with the memory card emulating the hard disk drive and a PC) (<u>Hashimoto</u>, Fig. 8; <u>Smith</u>, Fig. 2-5; col. 1, II. 9-22; col. 2, I. 40 to col. 3, I. 8; col. 3, II. 22-27; col. 3, II. 53-59; col. 4, II. 5-34; col. 6, II. 63-62; <u>Ristelhueber</u>, pages 1-3; and <u>Shinohara</u>, col. 1, II. 48-60; col. 3, I. 56 to col. 4, I. 49).

83. Claims 227-229 are rejected under 35 U.S.C. 103(a) as being unpatentable over <u>Hashimoto et al.</u> (US Patent 6,111,604) in view of <u>Smith et al.</u> (US Patent 5,634,075), <u>Kerigan</u>

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et al. (US Patent 5,948,091), <u>Ristelhueber : "Plug and play is almost here"</u> and <u>Shinohara</u> (US Patent 5,742,934) as applied to claim 183 above, and further in view of <u>Endo et al.</u> (US Patent 4,652,928).

<u>Hashimoto</u>, <u>Smith</u>, <u>Kerigan</u>, <u>Ristelhueber</u> and <u>Shinohara</u> teach all the limitations of claim 183 as discussed above, wherein <u>Hashimoto</u> further teaches the ADGPD comprising wherein the sensor (<u>Hashimoto</u>, Fig. 8, ref. 6, 9) is designed to be operatively coupled to the ADGPD processor (<u>Hashimoto</u>, Fig. 8).

<u>Hashimoto</u>, <u>Smith</u>, <u>Kerigan</u>, <u>Ristelhueber</u> and <u>Shinohara</u> do not expressly teach the ADGPD comprising a plug that is designed to operatively couple the sensor; and wherein the sensor is designed to be de-coupled from the plug.

Endo teaches a digital camera comprising a plug designed to operatively couple and de-coupled (e.g. couple and de-coupled when interchanging) a sensor (e.g. CCD) (col. 1, II. 18-25 and col. 13, II. 57-58).

It would have been obvious for one of ordinary skill in this art, at the time of invention was made to include Endo's interchangeable sensor into Hashimoto, Smith, Kerigan, Ristelhueber and Shinohara's ADGPD for the benefit of adaptively increase the resolution of the camera to obtaining a better quality image (Endo, col. 1, II. 18-20) to obtain the invention as specified in claim 227-229.

84. Claim 236 is rejected under 35 U.S.C. 103(a) as being unpatentable over <u>Hashimoto et</u> <u>al.</u> (US Patent 6,111,604) in view of <u>Smith et al.</u> (US Patent 5,634,075), <u>Kerigan et al.</u> (US Patent 5,948,091), <u>Ristelhueber : "Plug and play is almost here"</u> and <u>Shinohara</u> (US Patent

5,742,934) as applied to claim 183 above, and further in view of <u>Roberts et al.</u> (US Patent 5,576,757).

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Hashimoto, Smith, Kerigan, Ristelhueber and Shinohara teach all the limitations of claim 183 as discussed above, wherein Hashimoto further teaches the ADGPD comprising processing of analog data (Hashimoto, Fig. 1A-1B; Fig. 11-12; Fig. 14-15; col. 1, II. 35-57; col. 3, I. 43 to col. 4, I. 57; col. 5, II. 43-57; col. 6, I. 16 to col. 9, I. 17 and col. 9, I. 46 to col. 10, I. 16).

Hashimoto, Smith, Kerigan, Ristelhueber and Shinohara do not expressly teach the ADGPD comprising a fast Fourier transform.

<u>Roberts</u> teaches a system and a method comprising an electronic still camera processing data utilizing a fast Fourier transform (Abstract and col. 9, I. 60 to col. 10, I. 7).

It would have been obvious for one of ordinary skill in this art, at the time of invention was made to include <u>Roberts</u>'s fast Fourier transform into <u>Hashimoto</u>, <u>Smith</u>, <u>Kerigan</u>, <u>Ristelhueber</u> and <u>Shinohara</u>'s ADGPD for the benefit of having an easier computation for image processing while providing a reasonable visual fidelity (<u>Roberts</u>, col. 10, II. 1-3) to obtain the invention as specified in claim 236.

X. CLOSING COMMENTS

Conclusion

a. STATUS OF CLAIMS IN THE APPLICATION

The following is a summary of the treatment and status of all claims in the application as recommended by **M.P.E.P. 707.07(i)**:

a(1) CLAIMS REJECTED IN THE APPLICATION

Per the instant office action, claims 183-238 have received a first action on the merits and are subject of a first action non-final.

b. DIRECTION OF FUTURE CORRESPONDENCES

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chun-Kuan (Mike) Lee whose telephone number is (571) 272-0671. The examiner can normally be reached on 8AM to 5PM.

IMPORTANT NOTE

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Alford Kindred can be reached on (571) 272-4037. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

February 18, 2009

Chun-Kuan (Mike) Lee Examiner Art Unit 2181

/Chun-Kuan Lee/

Examiner, Art Unit 2181

I hereby certify that this paper (along with any paper referred to as being atta or enclosed) is being transmitted via the Office electronic filing system in	ached
accordance with § 1.6(a)(4). Dated: December 30, 2008 Signature:	e
(affred (annoh)	

Docket No.: 31436/43993 (PATENT)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of: Michael Tasler

Application No.: 11/467,092

Filed: August 24, 2006

Confirmation No.: 3038

Art Unit: 2181

For: ANALOG DATA GENERATING AND PROCESSING DEVICE FOR USE WITH A PERSONAL COMPUTER Examiner: C. K. Lee

PRELIMINARY AMENDMENT

MS Amendment Commissioner for Patents P.O. Box 1450 Alexandria, VA 22313-1450

Dear Sir:

INTRODUCTORY COMMENTS

Please enter this preliminary amendment in connection with the Request for Continued Examination that is being filed herewith. As a response to the Office Action dated October 1, 2008 that contains a final rejection, please amend the above-identified U.S. patent application as follows:

Amendments to the Claims are reflected in the listing of claims which begins on page 2 of this paper.

Remarks/Arguments begin on page 10 of this paper.

AMENDMENTS TO THE CLAIMS

WE CLAIM:

Please cancel claims 1-182 and add new claims 183-238 as noted hereinafter:

1-182. (cancelled).

183. (new) An analog data generating and processing device (ADGPD) for use with a

personal computer (PC) having a multi-purpose interface (MPI) and at least one software driver,

the ADGPD comprising:

an i/o connector designed to be operatively coupled to an MPI of a PC;

a program memory;

a data storage memory;

a sensor designed to generate analog data from one or more analog waves to

which the sensor is exposed;

an ADGPD processor operatively coupled to the i/o connector, the program memory, the data storage memory and the sensor;

wherein the ADGPD is adapted to undergo a data generation process when the i/o connector is not coupled to the MPI of the PC by which the sensor generates analog data, the analog data is processed, and the processed analog data is stored in the data storage memory as one or more files of digitized analog data;

wherein the ADGPD processor is adapted to initiate the data generation process and be involved in an automatic recognition process in which, after the i/o connecter has been operatively coupled to the MPI of the PC, the ADGPD processor executes at least one instruction

set stored in the program memory and thereby causes at least one parameter regarding the ADGPD, which signifies that the ADGPD has the ability to transfer files of digital data in response to commands issued from the at least one software driver, to be automatically sent through the i/o connector and to the MPI of the PC (a) without any type of user intervention at any time by means of the PC and (b) before a time when the PC is able to receive data files that are transferred to it from the ADGPD; and

wherein the ADGPD is adapted to, after the at least one parameter has been sent to the PC, transfer one or more user-selected files of digitized analog data to the PC without requiring a user to have previously loaded file transfer enabling software on the PC.

184. (new) The ADGPD of claim 183, wherein the ADGPD processor is adapted to execute one or more instructions sets stored in the program memory and thereby cause ADGPD file system information to be automatically sent to the PC (a) without any type of user intervention at any time by means of the PC and (b) at a point in time before a time when the PC is able to receive data files that are transferred to it from the ADGPD.

185. (new) The ADGPD of claim 184, wherein the ADGPD processor is adapted to execute one or more instructions sets stored in the program memory in response to commands from the at least one software driver and thereby transfer one or more user-selected files of digitized analog data from the data storage memory without requiring any user intervention by means of the PC after the commands are sent.

186. (new) The ADGPD of claim 185, wherein the at least one parameter is consistent with the ADGPD being a mass storage device.

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187. (new) The ADGPD of claim 186,

wherein the ADGPD processor and the program memory are configured to cause, after the at least one parameter has been sent to the i/o connector, file allocation table information to be sent to the i/o connector,

wherein the ADGPD processor and the program memory are configured to cause a virtual boot sequence to be sent to the i/o connector which includes at least information that is representative of a number of sectors of a storage disk, and

wherein the file allocation table information includes at least a start location of a file allocation table.

188. (new) The ADGPD of claim 187, wherein the at least one parameter is consistent with the ADGPD being adapted to operate in a manner consistent with a hard disk drive.

189. (new) The ADGPD of claim 188, wherein the ADGPD processor is formed in a single chip.

190. (new) The ADGPD of claim 189, wherein the ADGPD processor includes a single central processing unit.

191. (new) The ADGPD of claim 188, wherein the program memory is formed in a single chip.

192. (new) The ADGPD of claim 191, wherein the program memory comprises a single memory device.

193. (new) The ADGPD of claim 188, wherein the data storage memory comprises a single memory device.

194. (new) The ADGPD of claim 184, wherein the ADGPD file system information comprises at least an indication of the type of a file system that is used to store each one of the one or more files of digitized analog data in the data storage memory.

195. (new) The ADGPD of claim 183, further comprising an output device that is operatively coupled to the ADGPD processor, the output device being capable of generating one or more analog waves that are representative of at least some of the analog data that is generated by the sensor.

196. (new) The ADGPD of claim 183, wherein the ADGPD processor and the program memory are configured to initiate a process by which one or more files of digitized analog data stored in the data storage memory are directly transferred to an input/output device by means of the i/o connector.

197. (new) The ADGPD of claim 196, wherein the ADGPD processor and the program memory are adapted to allow an aspect of operation of the ADGPD other than the transfer of at least some of the one or more files of digitized analog data from the data storage memory to the i/o connector to be controlled by means of the PC.

198. (new) The ADGPD of claim 183, wherein the at least one parameter is consistent with the ADGPD being a mass storage device.

199. (new) The ADGPD of claim 183, wherein the at least one parameter is consistent with the ADGPD being responsive to a SCSI command set.

200. (new) The ADGPD of claim 183, wherein the at least one parameter is not consistent with the true nature of the ADGPD.

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201. (new) The ADGPD of claim 183, wherein the at least one parameter does not indicate that the ADGPD includes the sensor.

202. (new) The ADGPD of claim 183, wherein the at least one parameter is consistent with the ADGPD being an input/output device customary in a host device.

203. (new) The ADGPD of claim 202, wherein the at least one parameter is consistent with the ADGPD being a hard disk drive.

204. (new) The ADGPD of claim 183, wherein the ADGPD comprises at least a portion of a medical device.

205. (new) The ADGPD of claim 183, wherein the ADGPD comprises at least a portion of a data acquisition system.

206. (new) The ADGPD of claim 183, wherein the i/o connector comprises a parallel port.

207. (new) The ADGPD of claim 183, wherein the i/o connector comprises a SCSI connector.

208. (new) The ADGPD of claim 183, wherein the i/o connector is adapted to be operatively coupled to a cable.

209. (new) The ADGPD of claim 183, wherein the ADGPD is designed for use with a PC that has an operating system that is designed by a particular software company.

210. (new) The ADGPD of claim 183, the ADGPD processor is formed in a single chip.

211. (new) The ADGPD of claim 183, wherein the ADGPD processor comprises a

single microprocessor.

212. (new) The ADGPD of claim 183, wherein the ADGPD processor comprises a single digital signal processor.

213. (new) The ADGPD of claim 183, wherein the program memory is formed in a single chip.

214. (new) The ADGPD of claim 183, wherein the program memory comprises a single memory device.

215. (new) The ADGPD of claim 183, wherein the data storage memory comprises a single memory device.

216. (new) The ADGPD of claim 183, wherein the data storage memory comprises a semiconductor based memory.

217. (new) The ADGPD of claim 183, wherein the ADGPD includes a flexible interface.

218. (new) The ADGPD of claim 183, wherein the ADGPD includes a universal interface.

219. (new) The ADGPD of claim 183, further comprising an ADGPD interface that is operatively coupled between the i/o connector and the ADGPD processor.

220. (new) The ADGPD of claim 219, wherein the ADGPD interface and the ADGPD processor are not formed in the same chip.

221. (new) The ADGPD of claim 219, wherein the ADGPD interface comprises a SCSI interface.

222. (new) The ADGPD of claim 219, wherein the ADGPD interface comprises a parallel logic circuit.

223. (new) The ADGPD of claim 183, wherein the ADGPD includes a stand-alone interface device.

224. (new) The ADGPD of claim 183, wherein the sensor is designed to have twoway communication with a PC.

225. (new) The ADGPD of claim 183, wherein the sensor comprises a data transmit/receive device.

226. (new) The ADGPD of claim 225, wherein the data transmit/receive device is designed to receive data from the PC.

227. (new) The ADGPD of claim 183, wherein the sensor is designed to be decoupled from the ADGPD processor.

228. (new) The ADGPD of claim 183, further comprising a plug that is designed to operatively couple the sensor to the ADGPD processor.

229. (new) The ADGPD of claim 228, wherein the sensor is designed to be decoupled from the plug.

230. (new) The ADGPD of claim 183, wherein the sensor includes at least first and second transducers that are designed to generate analog data that corresponds to first and second analog waves, respectively, to which the first and second transducers are exposed.

231. (new) The ADGPD of claim 183, wherein the ADGPD processor and the program memory are configured to be involved with the automatic recognition process as a

response to a SCSI inquiry command.

232. (new) The ADGPD of claim 183, wherein the ADGPD processor is adapted to execute the at least one instruction set to thereby directly cause the at least one parameter regarding the ADGPD to be automatically sent to the PC.

233. (new) The ADGPD of claim 232, wherein the ADGPD processor is formed in a single chip.

234. (new) The ADGPD of claim 233, wherein the ADGPD processor includes a single central processing unit (CPU).

235. (new) The ADGPD of claim 233, wherein the program memory comprises a single memory device.

236. (new) The ADGPD of claim 183, wherein the analog data is processed by being subject to a fast Fourier transform.

237. (new) The ADGPD of claim 183, wherein the ADGPD processor is adapted to, after the at least one parameter has been sent to the PC, execute one or more instruction sets and thereby cause one or more user-selected files of digitized analog data to be transferred to the PC without requiring a user to have previously loaded file transfer enabling software on the PC.

238. (new) A combination comprising the ADGPD of claim 183 and a PC.

REMARKS

This responds to the Office Action dated October 1, 2008. Claims 1-182 have been cancelled, and new claims 183-238 have been inserted in their place.

Preliminary Remarks

The Examiner is respectfully requested to consider only the remarks and amendments made in this Preliminary Amendment, as well as any remarks made in any interview that takes place after this document is filed, when considering the patentability of the new claims. Please disregard all remarks and/or amendments made in all other papers filed in any application related to this application or previously filed in this application. Also, please disregard all remarks made in any telephone or e-mail communication or in any interview with the undersigned attorney that took place prior to the filing of this preliminary amendment.

An Information Disclosure Statement is being filed herewith. The Examiner also is respectfully requested to review all of the references identified in the IDS, as well as all other references of record, when considering the patentability of the new claims.

Regarding the new claims, please note that a PC, an MPI and at least one software driver are recited in the preamble of claim 180. While these words do appear in the body of the claim, they are referenced there only for the purpose of better describing the structure of the claimed ADGPD. It is the applicant's specific intention regarding the scope of the new claims that:

- new claims 183-237 read on, for example, an ADGPD that includes structure corresponding to each limitation of each claim,
- new claims 183-237 *do not* read on, for example, the combination of an ADGPD and a personal computer,

- it is not proper to read the "PC," the "MPI" and/or the "at least one software driver" into any of claims 183-237,
- new claims 183-185, 194-197, 199-202 and 204-237 cover but are not limited to an ADGPD that operates in a manner consistent with a mass storage device,
- it is not proper to put a time limitation on the "at least one software driver" to limit the scope of any new claim to cover only an ADGPD that only responds to commands from a particular time limited set of software driver(s),
- the "ADGPD processor" of new claims 183-189, 191, 193-210, 213, 215-233 and 236-237 reads on, for example, a cluster of two or more microprocessors that are formed in a single chip or in physically separate chips,
- new claims 183-226, 228 and 230-237 read on, for example, an ADGPD having a "sensor" that is not designed to be decoupled from the rest of the ADGPD,
- new claim 238 *does* read on, for example, the combination of an ADGPD and a PC,
- none of the new claims should be interpreted in accordance with 35 USC §112, paragraph 6; and
- it is not proper to read the limitation of the "PC" from claim 238 into any of claims 183-237.

The Claimed Invention

All of the new claims positively recite the following claim language:

"wherein the ADGPD processor is adapted to initiate the data generation process and be involved in an automatic recognition process in which, after the i/o connecter has been operatively coupled to the MPI of the PC, the ADGPD processor executes at least one instruction set stored in the program memory and thereby causes at least one parameter regarding the ADGPD, which signifies that the ADGPD has the ability to transfer files of digital data in response to commands issued from the at least one software driver, to be automatically sent through the i/o connector and to the MPI of the PC (a) without any type of user intervention at any time by means of the PC and (b) before a time when the PC is able to receive data files that are transferred to it from the ADGPD."

It is the applicant's specific intention that this language be interpreted as a single claim feature,

which shall be referenced hereinafter as the *multi-use automatic processor* claim feature. However, for ease of explanation, this claim language that describes how the claimed "ADGPD processor" operates is broken down into five individual parts in order for the Examiner to better understand how those parts, when taken together, form exemplary claimed subject matter that is not taught or suggested by the purported combination of references cited in the October 1st Office Action.

First, one aspect of the *multi-use automatic processor* claim feature is:

"wherein the ADGPD processor is adapted to initiate the data generation process and be involved in an automatic recognition process."

In view of this claim language, it can be seen that all of the new claims require that an "ADGPD processor" be a multi-use automatic processor that both initiates the "data generation process" and is involved in an "automatic recognition process." The "data generation process" concerns the generation and storage in a data storage memory of the ADGPD one or more files of digitized analog data. The "automatic recognition process" concerns the ADGPD processor providing the PC with at least one parameter regarding the ADGPD that, when received and processed by the PC, allows the PC to select, for file transfer purposes, at least one software driver already present in the PC when it is purchased by an end user.

Exemplary structure corresponding to the above-quoted claim language is shown, for example, in Figure 2 of the instant application. In accordance with this exemplary embodiment, the DSP 1300 shown in Figure 2 is at least partially involved in an analog "data generation process" by, for example, implementing a fast Fourier transform on the analog data that is acquired from data transmit/receive device 16. The DSP 1300 is a multi-use automatic processor

in that it also is involved in an "automatic recognition process" by which information is provided to the PC that, when received and processed by the PC, allows the PC to select at least one software driver already present in the PC when purchased by an end user to handle file transfers from the Figure 2 device to the PC. The new claims cover but are not limited to this structure.

A first example of a product that does not include structure corresponding to the abovequoted claim language is a device having a "single use" processor that is adapted for a single use such as, for example, the provision of streamed video to a PC by the processor inside of the camera disclosed in U.S. Patent No. 5,948,091 to Kerigan et al. (the "Kerigan patent"). A second example of such a product is the "plug and play" peripheral that the Examiner contends is taught in the background of the invention of U.S. Patent No. 5,634,075 to Smith et al. (the "Smith patent"). The processor contained in such a hypothetical product is not capable of being used to, for example, generate analog data or to process the analog data that is generated.

Second, another aspect of the *multi-use automatic processor* claim feature is the following claim language that specifies that the ADGPD processor

"executes at least one instruction set and thereby causes at least one parameter to be automatically sent from the i/o connector to the MPI of the PC."

This means that it is the execution of the processing steps by the ADGPD processor (not any processing power provided by any program (*e.g.*, the "card services" program) running on a PC) that allows the "ADGPD processor" to be involved in the claimed "automatic recognition process." This also means that it is the execution of the instruction set(s) by the "ADGPD processor" (and not some processor external to the PC or to the ADGPD) that causes the at least

one parameter to be sent.

Exemplary structure corresponding to this claim feature is shown, for example, in Figure 2 of the instant application. In accordance with this exemplary embodiment, DSP 1300 executes one or more instruction sets to cause at least one parameter regarding the Figure 2 device (*e.g.*, a parameter consistent with the Figure 2 device being a mass storage device such as a hard disk drive) to be sent to the PC to which the Figure 2 device is connected. The new claims cover but are not limited to this exemplary structure.

None of the following products include structure corresponding to the above-quoted claim language:

- a) a digital camera built around a memory card that affirmatively requires processing power to be provided by the "card services" program of the PC to which the camera is connected in order for the camera to be able to transfer pictures to it (*e.g.*, the Nikon Coolpix 100 camera and the camera disclosed in JP Publication H8-13072);
- b) a digital camera that is connected to a PC through a box that (i) converts RS-232 voltage levels into voltage levels usable by a camera and that (ii) is kept in standby mode until the camera CPU detects that the PC has sent it a DTR signal which indicates that the PC is ready to have files transferred to it from the camera (*e.g.*, the camera shown in U.S. Patent No. 6,111,604 to Hashimoto et al. (the "Hashimoto patent"); and/or
- c) a "web cam" that streams video to a PC after the web cam has been connected to the PC such as the camera disclosed in the Kerigan patent that is recognized by a PC at least in part by means of a monitor processor (and not a camera processor) sending a digital extended display identification (DEDID) to a PC (col. 3, lines 3-7 of Kerigan).

Third, another aspect of the multi-use automatic processor claim feature is that at least

one parameter regarding the ADGPD is automatically sent to the MPI of the PC

"without any type of user intervention at any time by means of the PC."

The use of the quoted phrase in the new claims means that:

- no user has to load an applications level program or a software driver onto a PC at any time in order to allow a peripheral device to be able to send "at least one parameter regarding the ADGPD" to a PC as quoted in the claims that, when received and processed by the PC, allows the PC to select at least one software driver to handle file transfers from the peripheral device; or
- no user has to interact with a PC (*e.g.*, setting up a file system) at any time in order to allow a peripheral device to be able to send "at least one parameter regarding the ADGPD" to a PC as quoted in the claims that, when received and processed by the PC, allows the PC to select at least one software driver to handle file transfers from the peripheral device.

Exemplary structure corresponding to the above-quoted claim language is shown, for

example, in Figure 2 of the instant application. In this exemplary embodiment, the DSP 1300 is

adapted to respond to a device identification inquiry signal sent from an MPI of a PC by

providing the PC with information that is consistent with the device shown in Figure 2 being, for

example, a mass storage device such as a hard disk drive. The new claims cover but are not

limited to this structure.

None of the following products include structure corresponding to the above-quoted

claim language:

a) a digital camera or scanner that requires a user to interact with a PC (*e.g.*, use the PC to set up a file system in the digital camera or scanner) in order to be able to transfer images from the digital camera or scanner to the PC (see, for example, US Patent No. 6,256,452, which relates to a storage device for an electronic camera, and which requires that the storage device be "beforehand formatted" before it is attached to the camera (column 2, line 59 of the '452 patent)) (see also, for example, US Patent No. 6,088,532, the HDD of which is believed to operate in a manner consistent with the HDD that is used with the camera disclosed in the '452 patent) (see also, for example, US Patent No. 5,506,692 to Murata that requires the user to create a file system on the attached device before the Murata scanner can be used);

- a digital camera or scanner that requires a user to remove a storage device such as a memory card from the digital camera or scanner and then place the memory card in a PC card reader in order to be able to transfer images from the digital camera or scanner to the PC (see, for example, the Figure 4A embodiment of US Patent No. 5,914,748 that was cited by the Examiner in the May, 2008 Office Action);
- c) a digital camera or scanner that requires a user to load a software driver and/or applications level program onto a PC in order to be able to transfer images from the digital camera or scanner to the PC (see, for example, the document attached to Supplemental Notice filed April 22, 2008, in which Casio, Inc. admits that the Casio QV-10 camera and the Kodak DCS200 camera both need "a [user loaded] software driver to retrieve images in the camera's memory") (see also, for example, US Patent No. 5,969,750 that requires a user to load a "vendor specific" driver onto a PC);
- d) a data acquisition system that requires a user to load an applications level program onto a PC in order to be able to transfer digitized analog data to the PC; and
- e) the "camera" disclosed in the Kerigan patent because, in order to use such a camera, a user is required to load software onto a PC to allow the PC to be able to understand what signals are provided on the pins of the connector that is used to implement the interface disclosed and claimed in Kerigan.

Fourth, a still further aspect of the multi-use automatic processor claim feature is that it

requires the execution of an instruction set by an "ADGPD processor" to cause the following

parameter to be sent to the PC:

"at least one parameter regarding the ADGPD, which signifies that the ADGPD has the ability to transfer files of digital data in response to commands from the at least one software driver."

This claim language reads on, for example, the device shown in Figure 2 of the instant

application. In accordance with this exemplary embodiment, while the Figure 2 device is

capable of generating files of digitized analog data, it merely sends information to a PC that is