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(12) United States Patent Hardee

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(54) DUAL SLOPE SENSE CLOCK GENERATOR

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(US)

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patent is extended or adjusted under 35

U.S.C. 154(b) by 0 days.

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Related U.S. Application Data

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(52) **U.S. Cl.** **365/205**; 365/149; 365/194; 327/51

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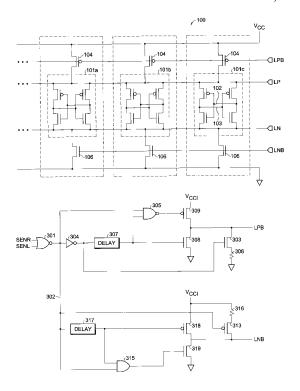
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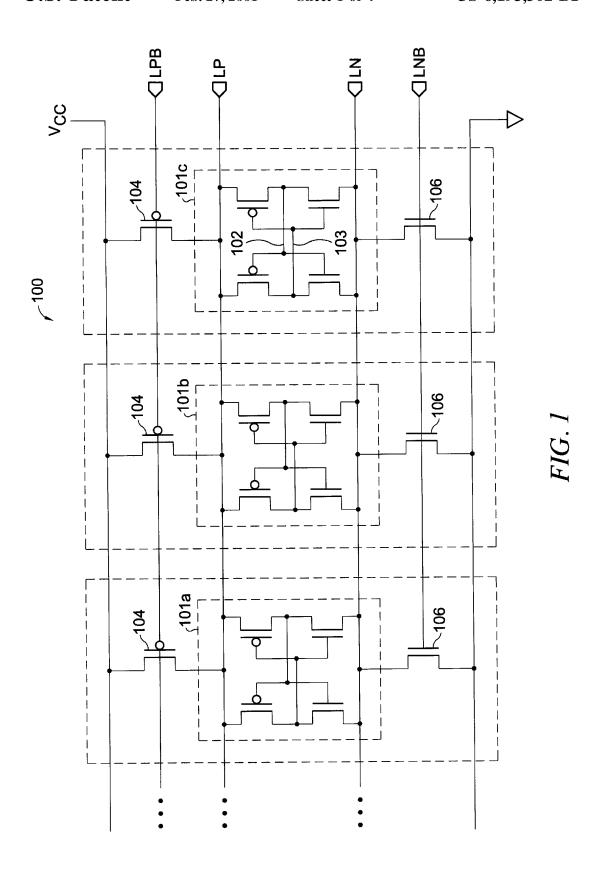
(57) ABSTRACT

A memory device including a plurality of sense amplifiers distributed about an integrated circuit chip, where each sense amplifier has a power node for receiving current. A conductor couples the power nodes of a number of sense amplifiers together. A low-impedance power supply conductor extends to each sense amplifier and a local drive transistor is provided for each sense amplifier. A timer unit generates an output signal controlling the local drive transistors. A first component within the timer unit causes the output to change from a first logic level towards a second logic level at a first rate while a second component within the timer unit causes the output to change at a second rate, wherein the second rate is greater than the first rate.

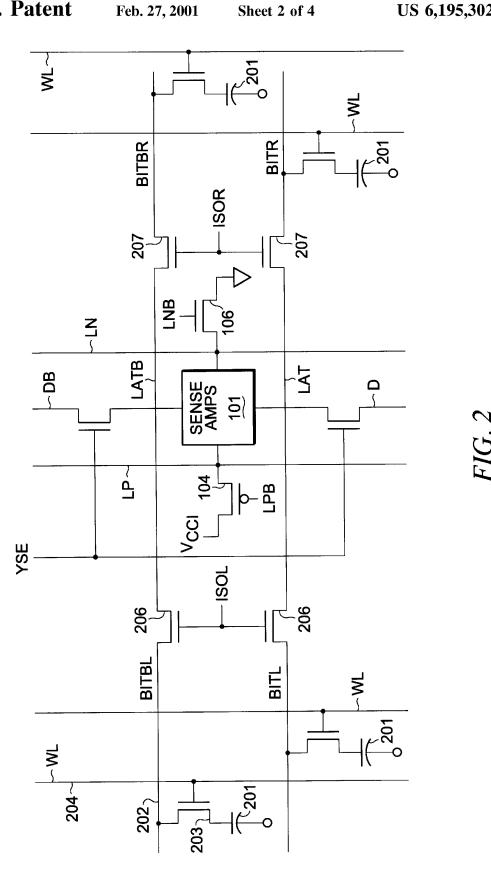
18 Claims, 4 Drawing Sheets



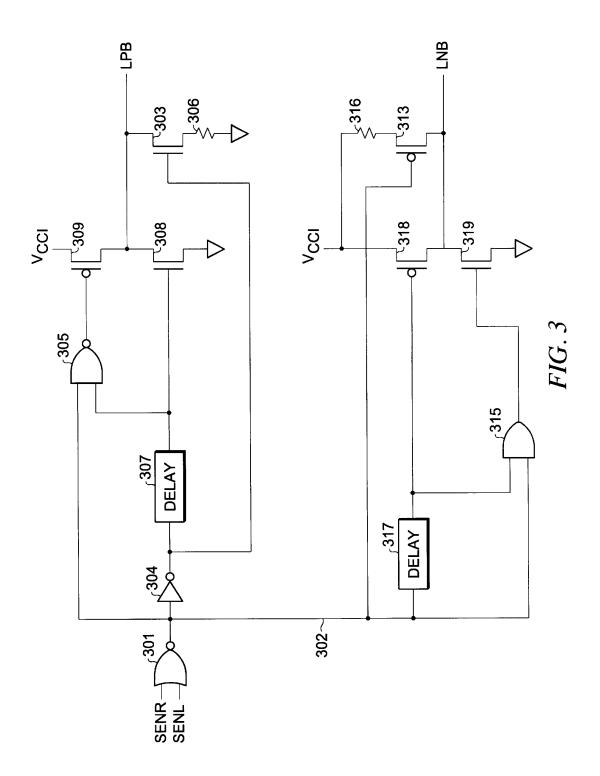




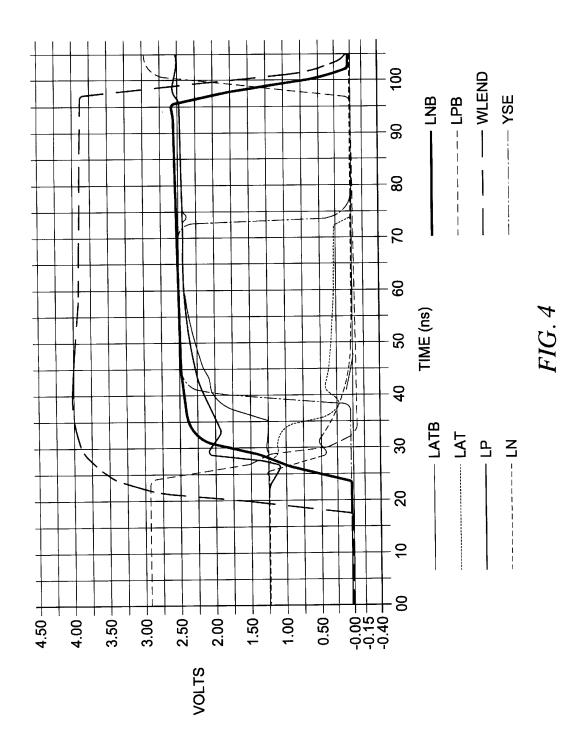
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