ISSUE CLASSIFICATION	Class	Subclass
	710	16

FILED UNDER 35 U.S.C. 371

PATENT NUMBER
6470399
6470399

U.S. UTILITY PATENT APPLICATION

O.I.P.E.	PATENT DATE
SCANNED RM CC2 Q.A. CS2	OCT 22 2002

SECTOR	CLASS	SUBCLASS	ART UNIT	EXAMINER
	710	+ 16	2783	Kee D.

FILED WITH: ☐ DISK (CRF) ☐ FICHE
(Attached in pocket on right inside flap)

5

PREPARED AND APPROVED FOR ISSUE

ISSUING CLASSIFICATION

ORIGINAL		CROSS REFERENCE(S)	
CLASS	SUBCLASS	CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)
710	16	710	62 63

INTERNATIONAL CLASSIFICATION

G 06 F 13/14

☐ Continued on Issue Slip Inside File Jacket

9/12/02 Formal Drawings 2 sheet set 4/3/02

☐ TERMINAL DISCLAIMER	DRAWINGS			CLAIMS ALLOWED	
	Sheets Drwg.	Figs. Drwg.	Print Fig.	Total Claims	Print Claim for O.G.
	2	2	2	15	1

☐ a) The term of this patent subsequent to _____ (date) has been disclaimed.

THUAN DU (Assistant Examiner) 5/15/02 (Date)

NOTICE OF ALLOWANCE MAILED
5-17-02

☐ b) The term of this patent shall not extend beyond the expiration date of U.S Patent. No. _____.

THOMAS LEE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100
(Primary Examiner) 5/16 (Date)

ISSUE FEE
Amount Due: $1280.00
Date Paid: 8-16-02

☐ c) The terminal ____ months of this patent have been disclaimed.

(Legal Instruments Examiner) 5/05 (Date)

ISSUE BATCH NUMBER

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(Rev. 6/98)

(LABEL AREA)

09/331002

PATENT APPLICATION

09331002

EP98/01187

INITIALS 06-25-99-48

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	Date received (Incl. C. of M.) or Date Mailed		Date received (Incl. C. of M.) or Date Mailed
1. Application 9 papers.		42.	
2. 903	26 JUL 1999	43.	
3. Pre-Amdt A	June 14, 1999	44.	
4. Change of address	1-23-01	45.	
5. Suppl IDS	10-9-01	46.	
6. IDS	6-14-99	47.	
7. Req (3 months) EM 3-803	12-18-01	48.	
8. Amdt B	4-3-02	49.	
9. Ex Amdt/C	5-17-02	50.	
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PATENT APPLICATION SERIAL NO. 09-331002

U.S. DEPARTMENT OF COMMERCE
PATENT AND TRADEMARK OFFICE
FEE RECORD SHEET

UNITED STATES PATENT AND TRADEMARK OFFICE

COMMISSIONER FOR PATENTS
UNITED STATES PATENT AND TRADEMARK OFFICE
WASHINGTON, D.C. 20231
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Bib Data Sheet

CONFIRMATION NO. 1117

SERIAL NUMBER	FILING DATE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.
09/331,002	06/14/1999 RULE	710	2185	2055/101

APPLICANTS

MICHAEL TASLER, WURZBURG, GERMANY;

** CONTINUING DATA **********
THIS APPLICATION IS A 371 OF PCT/EP98/01187 03/03/1998

** FOREIGN APPLICATIONS **********
GERMANY 19708755.8 03/04/1997

** SMALL ENTITY **

		STATE OR	SHEETS	TOTAL	INDEPENDENT
Foreign Priority claimed	☐ yes ☐ no	COUNTRY	DRAWING	CLAIMS	CLAIMS
35 USC 119 (a-d) conditions met	☐ yes ☐ no ☐ Met after Allowance	GERMANY	2	16	3
Verified and Acknowledged	Examiner's Signature Initials				

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TITLE
FLEXIBLE INTERFACE FOR COMMUNICATION BETWEEN A HOST AND AN ANALOG I/O DEVICE CONNTECTED TO THE INTERFACE REGARDLESS THE TYPE OF THE I/O DEVICE

FILING FEE RECEIVED 420	FEES: Authority has been given in Paper No. _____ to charge/credit DEPOSIT ACCOUNT No. _____ for following:	☐ All Fees ☐ 1.16 Fees (Filing) ☐ 1.17 Fees (Processing Ext. of time) ☐ 1.18 Fees (Issue) ☐ Other _____ ☐ Credit

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Foreign Priority claimed	STATE OR	SHEETS	TOTAL	INDEPENDENT
☑ yes ☐ no 35 USC 119 (a-d) conditions met ☑ yes ☐ no ☐ Met after Allowance Verified and Acknowledged Examiner's Signature Initials	COUNTRY GERMANY	DRAWING 2	CLAIMS 16	CLAIMS 3

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SERIAL NUMBER	FILING DATE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.
09/331,002	06/14/99	710	2782	2055/101

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CONTINUING DOMESTIC DATA********
VERIFIED

None

371 (NAT'L STAGE) DATA********
VERIFIED THIS APPLN IS A 371 OF PCT/EP98/01187 03/03/98

Yes

FOREIGN APPLICATIONS********
VERIFIED FED REP GERMANY 19708755.8 03/04/97

Yes

IF REQUIRED, FOREIGN FILING LICENSE GRANTED 07/27/99 ** SMALL ENTITY **

Foreign Priority claimed 35 USC 119 (a-d) conditions met	STATE OR COUNTRY	SHEETS DRAWING	TOTAL CLAIMS	INDEPENDENT CLAIMS
☒ yes ☐ no ☒ yes ☐ no ☐ Met after Allowance Verified and Acknowledged _____ Examiner's Initials _____ Initials	DEX	2	16	3

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FLEXIBLE INTERFACE

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418 Rec'd /PTO 14 JUN 1999

Practitioner's Docket No. 5/101

CHAPTER II

09/331002

TRANSMITTAL LETTER TO THE UNITED STATES ELECTED OFFICE (EO/US)

(ENTRY INTO U.S. NATIONAL PHASE UNDER CHAPTER II)

PCT/EP98/01187	03 March 1998 (3.03.98)	04 March 1997 (4.03.97)
International Application Number	**International Filing Date**	**International Earliest Priority Date**

TITLE OF INVENTION: FLEXIBLE INTERFACE
APPLICANT(S): Tasler, Michael

Attention: EO/US
Box PCT
Assistant Commissioner for Patents
Washington DC 20231

1. Applicant herewith submits to the United States Elected Office (EO/US) the following items under 35 U.S.C. §371:

   a. This express request to immediately begin national examination procedures (35 U.S.C. §371(f)).

   b. The U.S. National Fee (35 U.S.C. §371(c)(1)) and other fees (37 C.F.R. §1.492) as indicated below:

CERTIFICATION UNDER 37 C.F.R. 1.10*
*(Express Mail label number is **mandatory**.)*
(Express Mail certification is optional.)

I hereby certify that this correspondence and the documents referred to as attached therein are being deposited with the United States Postal Service on this date June 14, 1999, in an envelope as "Express Mail Post Office to Addressee," Mailing Label Number EL304928607US, addressed to Attention: EO/US, Box PCT, Assistant Commissioner for Patents, Washington, D.C. 20231.

Elaine C. VonSpreckelsen
(type or print name of person mailing paper)

Elaine C. VonSpreckelsen
Signature of person mailing paper

WARNING: *Certificate of mailing (first class) or facsimile transmission procedures of 37 C.F.R. 1.8 cannot be used to obtain a date of mailing or transmission for this correspondence.*

WARNING:* *Each paper or fee filed by "Express Mail" **must have the number of the "Express Mail" mailing label placed thereon prior to mailing. 37 C.F.R. 1.10(b).*
*"Since the filing of correspondence under §1.10 without the Express Mail mailing label thereon is an oversight that can be avoided by the exercise of reasonable care, requests for waiver of this requirement will **not** be granted on petition." Notice of Oct. 24, 1996, 60 Fed. Reg. 56,439, at 56,442.*

2. Fees

CLAIMS FEE*	(1) FOR	(2) NUMBER FILED	(3) NUMBER EXTRA	(4) RATE	(5) CALCULATIONS
	TOTAL CLAIMS	16 -20 =	0	x $18.00 =	$0.00
	INDEPENDENT CLAIMS	3 - 3 =	0	x $78.00 =	$0.00
	MULTIPLE DEPENDENT CLAIM(S) (if applicable) + $260.00				$0.00
BASIC FEE	U.S. PTO WAS NOT INTERNATIONAL PRELIMINARY EXAMINATION AUTHORITY Where no international preliminary examination fee as set forth in §1.482 has been paid to the U.S. PTO, and payment of an international search fee as set forth in §1.445(a)(2) to the U.S. PTO: where a search report on the international application has been prepared by the European Patent Office or the Japanese Patent Office (37 C.F.R. §1.492(a)(5)) $840.00				$840.00
	Total of above Calculations				= $840.00
SMALL ENTITY	Reduction by ½ for filing by small entity, if applicable. Affidavit must be filed. (note 37 CFR §§1.9, 1.27, 1.28)				- $420.00
	Subtotal				$420.00
	Total National Fee				$420.00
	Fee for recording the enclosed assignment document $40.00 (37 C.F.R. §1.21(h)). See attached "ASSIGNMENT COVER SHEET".				$0.00
TOTAL	Total Fees enclosed				$420.00

*See attached Preliminary Amendment Reducing the Number of Claims.

A check in the amount of $420.00 to cover the above fees is enclosed.

3. A copy of the International application as filed (35 U.S.C. §371(c)(2)) is transmitted herewith.

4. A translation of the International application into the English language (35 U.S.C. §371(c)(2)) is transmitted herewith.

5. A copy of the international examination report (PCT/IPEA/409) is transmitted herewith.

6. There were no annex(es) to the international preliminary examination report.

7. A translation of the annexes to the international preliminary examination report is not required as there were no annexes.

8. An oath or declaration of the inventor (35 U.S.C. §371(c)(4)) complying with 35 U.S.C. §115 is submitted herewith, and such oath or declaration is attached to the application.

II. Other document(s) or information included:

9. An International Search Report (PCT/ISA/210) or Declaration under PCT Article 17(2)(a) is transmitted herewith.

10. An Information Disclosure Statement under 37 C.F.R. §§1.97 and 1.98 is transmitted herewith. Also transmitted herewith are Forms PTO-1449 PTO/SB/08A and 08B, Explanation of documents cited in the examination proceedings of corresponding foreign and international applications, and copies of citations listed.

11. Additional documents:

    a. Preliminary amendment (37 C.F.R. §1.121)
    b. Verified Statement (Declaration) Claiming Small Entity Status
    c. Express Mail Certificate
    d. Return Postcard

12. The above items are being transmitted before 30 months from any claimed priority date.

AUTHORIZATION TO CHARGE ADDITIONAL FEES

The Commissioner is hereby authorized to charge the following additional fees that may be required by this paper and during the entire pendency of this application to Account No.: 04-1697

37 C.F.R. §1.492(a)(1), (2), (3), and (4) (filing fees)
37 C.F.R. §1.492(b), (c), and (d) (presentation of extra claims)
37 C.F.R. §1.17 (application processing fees)
37 C.F.R. §1.17(a)(1)-(5) (extension fees pursuant to 1.136(a))
37 C.F.R. §1.492(e) and (f) (surcharge fees for filing the declaration and/or filing an English translation of an International Application later than 30 months after the priority date).

Date: June 14, 1999

Reg. No. 28,494
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SIGNATURE OF PRACTITIONER

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Practitioner's Docket No. 2055/101 *PATENT*

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:	Tasler, Michael		
Application No.:	Applied For	Group No.:	Unknown
Filed:	Herewith	Examiner:	Unknown
For:	FLEXIBLE INTERFACE		

Attention: EO/US
Box PCT
Assistant Commissioner for Patents
Washington, DC 20231

EXPRESS MAIL CERTIFICATE

"Express Mail" Label Number: EL304928607US
Date of Deposit: 06/14/99

I hereby state that the following attached papers or fee:

1. Check No. 5994 in the amount of $420.00
2. Transmittal Letter to the United States Elected Office (EO/US) (Entry into U.S. National Phase Under Chapter II (3 pages)
3. Copy of German Application filed with the PCT (36 pages)
4. Translation of PCT Application PCT/EP98/01187 as originally filed (26 pages)
5. Copy of the IPER (6 pages)
6. First Preliminary Amendment and Remarks (2 pages)
7. Final version of PCT/EP98/01187 for the prosecution at the USPTO to be filed as first preliminary amendment (28 pages)
8. Declaration and Power of Attorney For Patent Application (28 pages)
9. Verified Statement (Declaration) Claiming Small Entity Status - Independent Inventor (1 page)
10. Copy of International Search Report (7 pages)
11. IDS Transmittal (1 page)
12. IDS Form PTO/SB/08A and 08B (2 pages)
13. Concise explanation of documents cited in examination proceedings of corresponding foreign and international applications (4 pages)
14. IDS References (7 for a total of 92 pages)

are being deposited with the United States Postal Service "Express Mail Post Office to Addressee" service under 37 CFR 1.10, on the date indicated above and is addressed to Attention: EO/US, Box PCT, Assistant Commissioner for Patents, Washington, DC 20231.

Elaine C. VonSpreckelsen

Elaine C. VonSpreckelsen

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2PRTS

09/331002

510 Rec'd PCT/PTO 14 JUN 1999

Flexible Interface

Description

The present invention relates to the transfer of data and in particular to interface devices for communication between a computer or host device and a data transmit/receive device from which data is to be acquired or with which two-way communication is to take place.

Existing data acquisition systems for computers are very limited in their areas of application. Generally such systems can be classified into two groups.

In the first group host devices or computer systems are attached by means of an interface to a device whose data is to be acquired. The interfaces of this group are normally standard interfaces which, with specific driver software, can be used with a variety of host systems. An advantage of such interfaces is that they are largely independent of the host device. However, a disadvantage is that they generally require very sophisticated drivers which are prone to malfunction and which limit data transfer rates between the device connected to the interface and the host device and vice versa. Further, it is often very difficult to implement such interfaces for portable systems and they offer few possibilities for adaptation with the result that such systems offer little flexibility.

The devices from which data is to be acquired cover the entire electrical engineering spectrum. In a typical case, it is assumed that a customer who operates, for example, a diagnostic radiology system in a medical engineering environment reports a fault. A field service technician of the system manufacturer visits the customer and reads system log files generated by the diagnostic radiology system by means a portable computer or laptop for example. If the fault cannot be localized or if the fault is intermittent, it will be necessary for the service technician to read not only an error log file but also data from current operation. It is apparent that in this case fast data transfer and rapid data analysis are necessary.

Another case requiring the use of an interface could be, for example, when an electronic measuring device, e.g. a multimeter, is attached to a computer system to transfer the data measured by the multimeter to the computer. Particularly when long-term measurements or large volumes of data are involved is it necessary for the interface to support a high data transfer rate.

From these randomly chosen examples it can be seen that an interface may be put to totally different uses. It is therefore desirable that an interface be sufficiently flexible to permit attachment of very different electrical or electronic systems to a host device by means of the interface. To prevent operator error, it is also desirable that a service technician is not required to operate different interfaces in different ways for different applications but that, if possible, a universal method of operating the interface be provided for a large number of applications.

To increase the data transfer rates across an interface, the route chosen in the second group of data acquisition systems for the interface devices was to specifically match the interface very closely to individual host systems or computer systems. The advantage of this solution is that high data transfer rates are possible. However, a disadvantage is that the drivers for the interfaces of the second group are very closely matched to a single host system with the result that they generally cannot be used with other host systems or their use is very ineffective. Further, such types of interface have the disadvantage that they must be installed inside the computer casing to achieve maximum data transfer rates as they access the internal host bus system. They are therefore generally not suitable for portable host systems in the form of laptops whose minimum possible size leaves little internal space to plug in an interface card.

A solution to this problem is offered by the interface devices of IOtech (business address: 25971 Cannon Road, Cleveland, Ohio 44146, USA) which are suitable for laptops such as the WaveBook/512 (registered trademark). The interface devices are connected by means of a plug-in card, approximately the size of a credit card, to the PCMCIA interface which is now a standard feature in laptops. The plug-in card converts the PCMCIA interface into an interface known in the art as IEEE 1284. The said plug-in card provides a special printer interface which is enhanced as regards the data transfer rate and delivers a data transfer rate of approximately 2 MBps as

compared with a rate of approx. 1 MBps for known printer interfaces. The known interface device generally consists of a driver component, a digital signal processor, a buffer and a hardware module which terminates in a connector to which the device whose data is to be acquired is attached. The driver component is attached directly to the enhanced printer interface thus permitting the known interface device to establish a connection between a computer and the device whose data is to be acquired.

In order to work with the said interface, an interface-specific driver must be installed on the host device so that the host device can communicate with the digital signal processor of the interface card. As described above, the driver must be installed on the host device. If the driver is a driver developed specifically for the host device, a high data transfer rate is achieved but the driver cannot be easily installed on a different host system. However, if the driver is a general driver which is as flexible as possible and which can be used on many host devices, compromises must be accepted with regard to the data transfer rate.

Particularly in an application for multi-tasking systems in which several different tasks such as data acquisition, data display and editing are to be performed quasi-simultaneously, each task is normally assigned a certain priority by the host system. A driver supporting a special task requests the central processing system of the host device for processor resources in order to perform its task. Depending on the particular priority assignment method and on the driver implementation, a particular share of processor resources is assigned to a special task in particular time slots. Conflicts arise if one or more drivers are implemented in such a way that they have the highest priority by default, i.e. they are incompatible, as happens in practice in many applications. It may occur that both drivers are set to highest priority which, in the worst case, can result in a system crash.

EP 0685799 A1 discloses an interface by means of which several peripheral devices can be attached to a bus. An interface is connected between the bus of a host device and various peripheral devices. The interface comprises a finite state machine and several branches each of which is assigned to a peripheral device. Each branch comprises a data manager, cycle control, user logic and a buffer. This known interface

device provides optimal matching between a host device and a specific peripheral device.

The specialist publication IBM Technical Disclosure Bulletin, Vol. 38, No. 05, page 245; "Communication Method between Devices through FDD Interface" discloses an interface which connects a host device to a peripheral device via a floppy disk drive interface. The interface consists in particular of an address generator, an MFM encoder/decoder, a serial/parallel adapter and a format signal generator. The interface makes it possible to attach not only a floppy disk drive but also a further peripheral device to the FDD host controller of a host device. The host device assumes that a floppy disk drive is always attached to its floppy disk drive controller and communication is initiated if the address is correct. However, this document contains no information as to how communication should be possible if the interface is connected to a multi-purpose interface instead of to a floppy disk drive controller.

It is the object of the present invention to provide an interface device for communication between a host device and a data transmit/receive device whose use is host device-independent and which delivers a high data transfer rate.

This object is achieved by an interface device according to claim 1 or 12 and by a method according to claim 15.

The present invention is based on the finding that both a high data transfer rate and host device-independent use can be achieved if a driver for an input/output device customary in a host device, normally present in most commercially available host devices, is utilized. Drivers for input/output devices customary in a host device which are found in practically all host devices are, for example, drivers for hard disks, for graphics devices or for printer devices. As however the hard disk interfaces in common host devices which can be, for example, IBM PCs, IBM-compatible PCs, Commodore PCs, Apple computers or even workstations, are the interfaces with the highest data transfer rate, the hard disk driver is utilized in the preferred embodiment of the interface device of the present invention. Drivers for other storage devices such as floppy disk drives, CD-ROM drives or tape drives could also be utilized in order to implement the interface device according to the present invention.

As described in the following, the interface device according to the present invention is to be attached to a host device by means of a multi-purpose interface of the host device which can be implemented, for example, as an SCSI interface or as an enhanced printer interface. Multi-purpose interfaces comprise both an interface card and specific driver software for the interface card. The driver software can be designed so that it can replace the BIOS driver routines. Communication between the host device and the devices attached to the multi-purpose interface then essentially takes place by means of the specific driver software for the multi-purpose interface and no longer primarily by means of BIOS routines of the host device. Recently however drivers for multi-purpose interfaces can also already be integrated in the BIOS system of the host device as, alongside classical input/output interfaces, multi-purpose interfaces are becoming increasingly common in host devices. It is of course also possible to use BIOS routines in parallel with the specific driver software for the multi-purpose interface, if this is desired.

The interface device according to the present invention comprises a processor means, a memory means, a first connecting device for interfacing the host device with the interface device, and a second connecting device for interfacing the interface device with the data transmit/receive device. The interface device is configured by the processor means and the memory means in such a way that the interface device, when receiving an inquiry from the host device via the first connecting device as to the type of a device attached to the host device, sends a signal, regardless of the type of the data transmit/receive device, to the host device via the first connecting device which signals to the host device that it is communicating with an input/output device. The interface device according to the present invention therefore simulates, both in terms of hardware and software, the way in which a conventional input/output device functions, preferably that of a hard disk drive. As support for hard disks is implemented as standard in all commercially available host systems, the simulation of a hard disk, for example, can provide host device-independent use. The interface device according to the present invention therefore no longer communicates with the host device or computer by means of a specially designed driver but by means of a program which is present in the BIOS system (Basic Input/Output System) and is normally precisely matched to the specific computer system on which it is installed,

or by means of a specific program for the multi-purpose interface. Consequently, the interface device according to the present invention combines the advantages of both groups. On the one hand, communication between the computer and the interface takes place by means of a host device-specific BIOS program or by means of a driver program which is matched to the multi-purpose interface and which could be regarded as a "device-specific driver". On the other hand, the BIOS program or a corresponding multi-purpose interface program which operates one of the common input/output interfaces in host systems is therefore present in all host systems so that the interface device according to the present invention is host device-independent.

In the following, preferred embodiments of the present invention will be explained in more detail with reference to the drawings enclosed, in which:

Fig. 1 shows a general block diagram of the interface device according to the present invention; and

Fig. 2 shows a detailed block diagram of an interface device according to a preferred embodiment of the present invention.

Fig. 1 shows a general block diagram of an interface device 10 according to the present invention. A first connecting device 12 of the interface device 10 can be attached to a host device (not shown) via a host line 11. The first connecting device is attached both to a digital signal processor 13 and to a memory means 14. The digital signal processor 13 and the memory means 14 are also attached to a second connecting device 15 by means of bi-directional communication lines (shown for all lines by means of two directional arrows). The second connecting device can be attached by means of an output line 16 to a data transmit/receive device which is to receive data from the host device or from which data is to be read, i.e. acquired, and transferred to the host device. The data transmit/receive device itself can also communicate actively with the host device via the first and second connecting device, as described in more detail in the following.

Communication between the host system or host device and the interface device is based on known standard access commands as supported by all known operating

systems (e.g. DOS, Windows, Unix). Preferably, the interface device according to the present invention simulates a hard disk with a root directory whose entries are "virtual" files which can be created for the most varied functions. When the host device system with which the interface device according to the present invention is connected is booted and a data transmit/receive device is also attached to the interface device 10, usual BIOS routines or multi-purpose interface programs issue an instruction, known by those skilled in the art as the INQUIRY instruction, to the input/output interfaces in the host device. The digital signal processor 13 receives this inquiry instruction via the first connecting device and generates a signal which is sent to the host device (not shown) again via the first connecting device 12 and the host line 11. This signal indicates to the host device that, for example, a hard disk drive is attached at the interface to which the INQUIRY instruction was sent. Optionally, the host device can send an instruction, known by those skilled in the art as "Test Unit Ready", to the interface device to request more precise details regarding the queried device.

Regardless of which data transmit/receive device at the output line 16 is attached to the second connecting device, the digital signal processor 13 informs the host device that it is communicating with a hard disk drive. If the host device receives the response that a drive is present, it then sends a request to the interface device 10 to read the boot sequence which, on actual hard disks, normally resides on the first sectors of the disk. The digital signal processor 13, whose operating system in stored in the memory means 14, responds to this instruction by sending to the host device a virtual boot sequence which, in the case of actual drives, includes the drive type, the starting position and the length of the file allocation table (FAT), the number of sectors, etc., known to those skilled in the art. Once the host device has received this data, it assumes that the interface device 10 according to a preferred embodiment of the present invention is a hard disk drive. In reply to an instruction from the host device to display the directory of the "virtual" hard disk drive simulated by the interface device 10 with respect to the host device, the digital signal processor can respond to the host device in exactly the same way as a conventional hard disk would, namely by reading on request the file allocation table or FAT on a sector specified in the boot sequence, normally the first writable sector, and transferring it to the host device, and subsequently by transferring the directory structure of the virtual hard

disk. Further, it is possible that the FAT is not read until immediately prior to reading or storing the data of the "virtual" hard disk and not already at initialization.

In a preferred embodiment of the present invention, the digital signal processor 13, which need not necessarily be implemented as a digital signal processor but may be any other kind of microprocessor, comprises a first and a second command interpreter. The first command interpreter carries out the steps described above whilst the second command interpreter carries out the read/write assignment to specific functions. If the user now wishes to read data from the data transmit/receive device via the line 16, the host device sends a command, for example "read file xy", to the interface device. As described above, the interface device appears to the host device as a hard disk. The second command interpreter of the digital signal processor now interprets the read command of the host processor as a data transfer command, by decoding whether "xy" denotes, for example, a "real-time input" file, a "configuration" file or an executable file, whereby the same begins to transfer data from the data transmit/receive device via the second connecting device to the first connecting device and via the line 11 to the host device.

Preferably, the volume of data to be acquired by a data transmit/receive device is specified in a configuration file described in the following by the user specifying in the said configuration file that a measurement is to last, for example, five minutes. To the host device the "real-time input" file then appears as a file whose length corresponds to the anticipated volume of data in those five minutes. Those skilled in the art know that communication between a processor and a hard disk consists of the processor transferring to the hard disk the numbers of the blocks or clusters or sectors whose contents it wishes to read. By reference to the FAT the processor knows which information is contained in which block. In this case, communication between the host device and the interface device according to the present invention therefore consists of the very fast transfer of block numbers and preferably of block number ranges because a virtual "real-time input" file will not be fragmented. If the host device now wants to read the "real-time input" file, it transfers a range of block numbers to the interface device, whereupon data commences to be received via the second connecting device and data commences to be sent to the host device via the first connecting device.

In addition to the digital signal processor instruction memory, which comprises the operating system of the digital signal processor and can be implemented as an EPROM or EEPROM, the memory means 14 can have an additional buffer for purposes of synchronizing data transfer from the data transmit/receive device to the interface device 10 and data transfer from the interface device 10 to the host device.

Preferably, the buffer is implemented as a fast random access memory or RAM buffer.

Further, from the host device the user can also create a configuration file, whose entries automatically set and control various functions of the interface device 10, on the interface device 10 which appears to the host device as a hard disk. These settings can be, for example, gain, multiplex or sampling rate settings. By creating and editing a configuration file, normally a text file which is simple to understand with little prior knowledge, users of the interface device 10 are able to perform essentially identical operator actions for almost any data transmit/receive devices which can be attached to the second connecting device via the line 16, thus eliminating a source of error arising from users having to know many different command codes for different applications. In the case of the interface device 10 according to the present invention it is necessary for users to note the conventions of the configuration file once only in order to be able to use the interface device 10 as an interface between a host device and almost any data transmit/receive device.

As a result of the option of storing any files in agreed formats in the memory means 14 of the interface device 10, taking into account the maximum capacity of the memory means, any enhancements or even completely new functions of the interface device 10 can be quickly implemented. Even files executable by the host device, such as batch files or executable files (BAT or EXE files), and also help files can be implemented in the interface device, thus achieving independence of the interface device 10 from any additional software (with the exception of the BIOS routines) of the host device. On the one hand, this avoids licensing and/or registration problems and, on the other hand, installation of certain routines which can be frequently used, for example an FFT routine to examine acquired time-domain data in the frequency

domain, is rendered unnecessary as the EXE files are already installed on the interface device 10 and appear in the virtual root directory, by means of which the host device can access all programs stored on the interface device 10.

In a preferred embodiment of the present invention in which the interface device 10 simulates a hard disk to the host device, the interface device is automatically detected and readied for operation when the host system is powered up or booted. This corresponds to the plug-and-play standard which is currently finding increasingly widespread use. The user is no longer responsible for installing the interface device 10 on the host device by means of specific drivers which must also be loaded; instead the interface device 10 is automatically readied for operation when the host system is booted.

For persons skilled in the art it is however obvious that the interface device 10 is not necessarily signed on when the computer system is powered up but that a special BIOS routine or a driver for a multi-purpose interface can also be started on the host device during current operation of the computer system in order to sign on or mount the interface device 10 as an additional hard disk. This embodiment is suitable for larger workstation systems which are essentially never powered down as they perform, e.g. mail functions or monitor processes which run continuously, for example, in multi-tasking environments.

In the interface device according to the present invention an enormous advantage is to be gained, as apparent in the embodiment described in the following, in separating the actual hardware required to attach the interface device 10 to the data transmit/receive device from the communication unit, which is implemented by the digital signal processor 13, the memory means 14 and the first connecting device 12, as this allows a plurality of dissimilar device types to be operated in parallel in identical manner. Accordingly, many interface devices 10 can be connected to a host device which then sees many different "virtual" hard disks. In addition, any modification of the specific hardware symbolized by the second connecting device 15 can be implemented essentially without changing the operation of the interface device according to the present invention. Further, an experienced user can intervene at any time on any level of the existing second connecting device by making use of the above mentioned

option of creating a configuration file or adding or storing new program sections for the second connecting device.

An important advantage of the interface device 10 of the present invention is that it also permits extremely high data transfer rates by using, for data interchange, the host device-own BIOS routines which are optimized for each host device by the host device manufacturer or BIOS system manufacturer, or by using driver programs which are normally optimized and included by the manufacturers of multi-purpose interfaces. Furthermore, due to the simulation of a virtual mass storage device, the data is managed and made available in such a way that it can be transferred directly to other storage media, e.g. to an actual hard disk of the host device without, as it were, intervention of the host device processor. The only limitation to long-term data transfer at high speed is therefore imposed exclusively by the speed and the size of the mass storage device of the host device. This is the case as the digital signal processor 13 already formats the data read by the data transmit/receive device via the second connecting device 15 into block sizes suitable for a hard disk of the host device, whereby the data transfer speed is limited only by the mechanical latency of the hard disk system of the host device. At this point, it should be noted that normally data flow from a host device must be formatted in blocks to permit writing to a hard disk and subsequent reading from a hard disk, as known by those skilled in the art.

The said data transfer rate can be increased further by setting up a direct memory access (DMA) or RAM drive in the host system. As those skilled in the art know, the setting up of a RAM drive requires processor resources of the host device, with the result that the advantage of writing the data to a hard disk drive of the host device essentially without the need for processor resources is lost.

As described above, a data buffer can be implemented in the memory means 14 to permit independence in terms of time of the data transmit/receive device attached to the second connecting device from the host device attached to the first connecting device. This guarantees error-free operation of the interface device 10 even for time-critical applications in multi-tasking host systems.

Fig. 2 shows a detailed block diagram of an interface device 10 according to the present invention.

A digital signal processor (DSP) 1300 is, in a manner of speaking, the heart of the interface device 10. The DSP can be any DSP but preferably has a 20-MB on-chip random access memory (RAM). Certain instruction sets, for example, can be stored in the RAM already integrated in the DSP. An 80-MHz clock generator is attached to the DSP 1300 in order to synchronize the DSP. The DSP implements a fast Fourier transformation (FFT) in real time and also optional data compression of the data to be transferred from the data transmit/receive device to the host device in order to achieve greater efficiency and to permit interoperation with host devices which have a smaller memory.

In the preferred embodiment of the interface device 10 shown in Fig. 2, the first connecting device 12 of Fig. 1 contains the following components: an SCSI interface 1220 and a 50-pin SCSI connector 1240 for attachment to an SCSI interface present on most host devices or laptops. The SCSI (small computer system interface) interface 1220 translates the data received via the SCSI connector 1240 into data understood by the DSP 1300, as known by those skilled in the art. Further, the first connecting device 12 comprises an EPP (enhanced parallel port) with a data transfer rate of approx. 1 MBps which delivers a more moderate data transfer rate of 1 MBps by comparison to the data transfer rate of 10 MBps of the SCSI interface. The EPP 1260 is connected to a 25-pin D-shell connector 1280 to permit attachment to a printer interface of a host device for example. Optionally, the first connecting device 12 also comprises a 25-pin connector 1282 which permits the attachment of 8 digital outputs and 8 digital inputs 1284 at a host device.

Preferably, the second connecting device comprises 8 BNC inputs with the calibration relay 1505, a block 1510 with 8 device amplifiers with an overvoltage protection of ±75 V, this block being connected in turn to 8 sample/hold (S&H) circuits 1515. The calibration relays are relays which permit controlled changeover between a test voltage and a calibration reference voltage. Each sample/hold circuit is connected to a corresponding input of an 8-channel multiplexer 1520 which feeds its output signals

via a programmable amplifier 1525 into an analog/digital converter (ADC) with 12 bit and 1.25 MHz 1530 and to the DSP 1300. The ADC 1530 is controlled by means of a 20-bit timer 1535, as known by persons skilled in the art. The programmable amplifier 1525 and the 8-channel multiplexer 1520 are controlled via an amplifier channel selection circuit 1540 which is in turn controlled by the DSP 1300.

The complete interface device 10 is supplied with power by an external AC/DC converter 1800 which delivers a digital supply voltage of ±5 V and is attached to a DC/DC converter 1810 which can deliver analog supply voltages of ±5 V and ±15 V as required for the interface device 10. Further, the DC/DC converter controls a precision voltage reference 1820 which controls the 8 BNC inputs 1505 and the ADC 1530 as well as a digital/analog converter (DAC) 1830 which permits, via an output amplifier block with 4 output amplifiers 1840 and a 9-pin connector 1850, analog output direct from the DSP 1300 to an output device, e.g. printer device or monitor device, which can be attached via the 9-pin connector 1850, thus providing the option of monitoring the data transferred to the host device or also, for example, of viewing an FFT to obtain rapid and comprehensive data analysis without using processor time of the host device.

In Fig. 2 the memory means 14 of Fig. 1 is implemented by an EPROM 1400 which, in a preferred embodiment of the present invention, contains the operating system of the digital signal processor 1300. A random access memory with an access time of 15 ns and a size of 512 KB or optionally 1024 KB 1420 serves as a data buffer to achieve independence in terms of time of the output line 16 from the output lines 11a, 11b and 11c to the data transmit/receive device and to the host device respectively. As described above, in a preferred embodiment of the present invention the digital signal processor 1300 already contains a 20-KB on-chip RAM 1440 which can store certain instruction sets, functions and also smaller application software units.

The connection, symbolized by the line 16, of the interface device 10 to any data transmit/receive device implements, by means of the blocks 1505 – 1535, an analog input with a sampling rate of 1.25 MHz and quantization of 12 bits. There are 8 channels with an overvoltage protection of ± 75 V. By means of the programmable

amplifier 1525 the channels can be programmed independently of each other in voltage ranges up to a maximum of ± 10 V. Unused channels can be grounded internally to reduce channel intermodulation. The block 1515 is implemented as a monolithic high-precision, high-speed sample/hold amplifier for simultaneous sampling of all channels. The precision voltage reference 1820 provides a high-precision, temperature-compensated monolithic energy gap voltage reference for auto-calibration of each channel and each gain. Further, offset fine adjustment for each channel is implemented by the same.

The blocks 1830, 1840 and 1850 implement a direct analog output for the digital signal processor 1300, and the DAC 1830 provides a data transfer rate of 625 kHz and a quantization of 12 bits. The block 1840 comprises 4 channels with a common output latch.

Further, the interface device 10 comprises a digital input/output device implemented by the blocks 1284 and 1282. Here there are 8 digital inputs, 8 digital outputs with a common latch, and the digital port can be attached preferably to a side panel of the interface device 10 so that the port itself can easily be accessed.

The digital signal processor 1300 provides on-board digital data processing. In particular, it is a high-performance DSP with a clock speed of 80 MHz and a 20-bit timer 1535.

As described above, the first connecting device 12 comprises the SCSI interface 1220 with a peak transfer rate of 10 MBps. An optional PCMCIA-to-SCSI adapter permits high-speed communication with laptop computers which are desirable and in widespread use, particularly by mobile service technicians. The EPP 1260 with its associated connector 1280 permits data transfer at a more moderate rate.

As described above, the interface device 10 is supplied with power by means of an external AC/DC adapter which has a universal power input (85 – 264 VAC, 47 – 63 Hz). Interference suppression complies with the standards EN 55022, curve B and FFC, Class B). Further, it is also in accordance with international safety regulations

(TÜV, UL, CSA). The interface device 10 is externally shielded and achieves a value of 55 dB at 30 – 60 MHz and a value of approximately 40 dB at 1 GHz, and therefore complies with the MILSTD 285-1 standard.

As described above, communication between the host device and the multi-purpose interface can take place not only via drivers for input/output device customary in a host device which reside in the BIOS system of the host device but also via specific interface drivers which, in the case of SCSI interfaces, are known as multi-purpose interface ASPI (advanced SCSI programming interface) drivers. This ASPI driver, which can also be referred to as an ASPI manager, is specific to a special SCSI host adapter, i.e. to a special multi-purpose interface, and is normally included by the manufacturer of the multi-purpose interface. Generally speaking, this multi-purpose interface driver has the task of moving precisely specified SCSI commands from the host system program to the host system SCSI adapter. For this reason, the command set is almost identical to that of the SCSI interface itself. Essentially, only status and reset commands for the host adapter have been added.

The ASPI driver can be used if the hard disk was not already addressable at boot time or if the SCSI-related BIOS routines of the host computer were still disabled. Here too, the steps needed to initialize the interface device, preferably as a virtual hard disk, are similar to the steps taken when initializing at boot time.

In general terms, the ASPI manager comprises two sides. One side is the proprietary, hardware-oriented side. It is responsible for converting all commands into a form required by the corresponding multi-purpose interface. The hardware-oriented side of the ASPI driver is therefore matched to a very specific type of multi-purpose interface or SCSI interface. The other side is known as the user software side. This side is totally independent of the proprietary operating characteristics of the SCSI adapter and is therefore identical for all SCSI interfaces. This permits SCSI programming which is however independent of the individual SCSI adapter types.

In contrast to communication between the host device and the interface device according to the present invention on the basis of a BIOS driver, the use of such an ASPI driver for communication between the host device and the interface device

according to the present invention allows various further possibilities of the SCSI multi-purpose interface to be exploited. In the case described above, the interface device which preferably signs on and behaves as a virtual hard disk is detected by the BIOS driver of the host computer at boot time and is configured as a hard disk. This step does not however support active requests sent by the interface device to the host computer. If however the virtual hard disk wishes to write data actively to, for example, a hard disk of the host computer or wishes to initiate communication with the processor of the host computer, the host computer must recognize the request of the virtual hard disk and tolerate a further issuer of instructions on its bus. If the interface device behaves solely like a virtual hard disk, it would always receive and never issue commands. The BIOS has no objections to an additional issuer of commands that actively wishes to place data on the bus of the host device but the BIOS does not support the host device in recognizing corresponding requests of the interface device or in granting the interface device permission to access the bus.

Using the ASPI manager the interface device according to the present invention can now obtain active access to an SCSI hard disk of the host device connected to the same SCSI bus which, in contrast to the interface device, cannot be a virtual but a real SCSI mass storage device or also a further interface device according to the present invention. Thereupon, the interface device according to the present invention can write the desired data to the SCSI hard disk of the host computer totally independently of the host computer or can communicate with the same in some other manner. The interface device according to the present invention therefore initially behaves passively as a virtual hard disk and then, as required and using the driver software for the multi-purpose interface, actively on the same SCSI bus. This means however that the interface device according to the present invention, using a driver software for the multi-purpose interface which comprises the BIOS routines customary in host devices and simultaneously provides the option of active participation, can, regardless of the type of the data transmit/receive device attached to the second connecting device, behave initially as a virtual and at the same time passive hard disk but can, as required, participate actively on the bus so as to be able to initiate communication directly with other SCSI hard disks of the host device by bypassing the processor of the host device.

Using a standard interface of a host device, the interface device according to the present invention permits communication with any host device. By simulating an input/output device to the host device and, in a preferred embodiment, by simulating a virtual mass storage device, the interface device 10 is automatically supported by all known host systems without any additional sophisticated driver software. The simulation of a freely definable file structure on the "virtual" hard disk provides simple operation and expansion options and, through the implementation of any programs, independence from special software implemented on the host device. Help files included on the interface device 10 and plug-and-play support ensure ease of use even in portable, flexible host devices. Despite the very simple user interface, experienced users are free at any time to intervene in the functions of the interface device 10 on system level. The interface device 10 thus provides a universal solution which can cover the entire spectrum of possible data transmit/receive devices.

Claims

Sub A1

1. An interface device (10) for communication between a host device, which comprises drivers for input/output devices customary in a host device and a multi-purpose interface, and a data transmit/receive device comprising the following features:

a processor means (13; 1300, 1320);

a memory means (14; 1400, 1420, 1440);

a first connecting device (12; 1220, 1240, 1260, 1280) for interfacing the host device with the interface device (10) via the multi-purpose interface of the host device; and

a second connecting device (15; 1505 – 1535) for interfacing the interface device (10) with the data transmit/receive device,

wherein the interface device (10) is configured by the processor means (13; 1300, 1320) and the memory means (14; 1400, 1420, 1440) in such a way that the interface device, when receiving an inquiry from the host device as to the type of a device attached to the multi-purpose interface of the host device, sends a signal, regardless of the type of the data transmit/receive device attached to the second connecting device (15; 1505 – 1535) of the interface device (10), to the host device which signals to the host device that it is an input/output device customary in a host device, whereupon the host device communicates with the interface device (10) by means of the driver for the input/output device customary in a host device.

2. An interface device (10) according to claim 1,

wherein the drivers for input/output drivers customary in a host device comprise a

hard disk driver, and the signal indicates to the host device that the host device is communicating with a hard disk.

3. An interface device (10) according to claim 1 or 2,

wherein the memory means comprises a buffer (1420) to buffer data to be transferred between the data transmit/receive device and the host device.

4. An interface device (10) according to one of the preceding claims,

wherein the multi-purpose interface of the host device is an SCSI interface and the first connecting device also comprises an SCSI interface (1220).

5. An interface device (10) according to one of the preceding claims,

wherein the second connecting device comprises an analog input (1505) with a subsequent A/D converter (1530) in order to transfer analog data to the host device from a data transmit/receive device connectable to the analog device (1505).

6. An interface device (10) according to one of the preceding claims,

wherein the processor means (13) is a digital signal processor (1300).

7. An interface device (10) according to one of the claims 2 to 6,

wherein the data to be transferred from the data transmit/receive device to the host device in the interface device (10) is formatted in a suitable format for a hard disk present in the host device.

8. An interface device (10) according to one of the claims 2 to 7,

which further comprises a root directory and virtual files which are present on the

signaled hard disk drive and which can be accessed from the host device.

9. An interface device (10) according to claim 8,

wherein the virtual files comprise a configuration file in text format which are stored in the memory means (14) and using which the user can configure the interface device (10) for a specific data transmit/receive device.

10. An interface device (10) according to claim 8 or 9,

wherein the virtual files comprise batch files or executable files for the microprocessor means which are stored in the interface device (10) in order to perform data processing, independently of the host device, of data received via the second connecting device (15; 1505 – 1535).

11. An interface device (10) according to claim 8 or 9,

wherein the virtual files comprise batch files or executable files for the host device which are stored in the interface device (10).

sub A2 > 12. An interface device (10) for communication between a host device, which comprises a multi-purpose interface and a specific driver for this interface, and a data transmit/receive device comprising the following features:

a processor means (13; 1300, 1320);

a memory means (14; 1400, 1420, 1440);

a first connecting device (12; 1220, 1240, 1260, 1280) for interfacing the host device with the interface device (10) via the multi-purpose interface of the host device; and

a second connecting device (15; 1505 – 1535) for interfacing the interface device (10) with the data transmit/receive device,

where the interface device (10) is configured using the processor means (13; 1300, 1320) and the memory means (14; 1400, 1420, 1440) in such a way that the interface device, when receiving an inquiry from the host device as to the type of a device attached at the multi-purpose interface of the host device, sends a signal, regardless of the type of the data transmit/receive device attached to the second connecting device (15; 1505 – 1535) of the interface device (10), to the host device which signals to the host device that it is an input/output device customary in a host device, whereupon the host device communicates with the interface device (10) by means of the specific driver for the multi-purpose interface.

A2

13. An interface device according to claim 12,

wherein, in addition to the first connecting device of the interface device, there is a further input/output device at the multi-purpose interface of the host device, and wherein the interface device can communicate directly with the hard disk via the specific driver for the multi-purpose interface.

14. An interface device according to claim 12 or 13,

wherein the multi-purpose interface is an SCSI interface, and wherein the specific driver for the multi-purpose interface is an ASPI manager.

Sub A3

15. A method of communication between a host device, which comprises drivers for input/output devices customary in a host device and a multi-purpose interface, and a data transmit/receive device via an interface device (10) comprising the following steps:

interfacing of the host device with a first connecting device (12; 1220, 1240, 1260, 1280) of the interface device (10) via the multi-purpose interface of the host device;

interfacing of the data transmit/receive device with a second connecting device (15; 1505 – 1535) of the interface device (10);

inquiring by the host device at the interface device (10) as to the type of device to which the multi-purpose interface of the host device is attached;

regardless of the type of the data transmit/receive device attached to the second connecting device of the interface device (10), responding to the inquiry from the host device by the interface device (10) in such a way that it is an input/output device customary in a host device, whereupon the host device communicates with the interface device (10) by means of the usual driver for the input/output device.

16. A method according to claim 15,

wherein the drivers for input/output devices customary in a host device comprise a driver for a storage device and in particular for a hard disk drive.

09/331002

Flexible Interface

ABSTRACT

An interface device (10) provides fast data communication between a host device with input/output interfaces and a data transmit/receive device, wherein the interface device (10) comprises a processor means (13), a memory means (14), a first connecting device (12) for interfacing the host device with the interface device, and a second connecting device (15) for interfacing the interface device (10) with the data transmit/receive device. The interface device (10) is configured by the processor means (13) and the memory means (14) in such a way that, when receiving an inquiry from the host device via the first connecting device (12) as to the type of a device attached to the host device, regardless of the type of the data transmit/receive device, the interface device sends a signal to the host device via the first connecting device (12) which signals to the host device that it is communicating with an input/output device.

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			Priority Claimed	
19708755.8 (Number) (Nummer)	Germany (Country) (Land)	04/3/97 (March 4, 1997) (Day/Month/Year Filed) (Tag/Monat/Jahr eingereicht)	[X] Yes Ja	☐ No Nein
PCT/EP98/01187 (Number) (Nummer)	Germany (Country) (Land)	03/03/98 (March 3, 1998) (Day/Month/Year Filed) (Tag/Monat/Jahr eingereicht)	[X] Yes Ja	☐ No Nein
(Number) (Nummer)	(Country) (Land)	(Day/Month/Year Filed) (Tag/Monat/Jahr eingereicht)	☐ Yes Ja	☐ No Nein

Ich beanspruche hiermit gemäss Absatz 35 der Zivilprozessordnung der Vereinigten Staaten, Paragraph 120, den Vorzug aller unten aufgeführten Anmeldungen und falls der Gegenstand aus jedem Anspruch dieser Anmeldung nicht in einer früheren amerikanischen Patentanmeldung laut dem ersten Paragraphen des Absatzes 35 der Zivilprozessordnung der Vereinigten Staaten, Paragraph 112 offenbart ist, erkenne ich gemäss Absatz 37, Bundesgesetzbuch, Paragraph 1.56(a) meine Pflicht zur Offenbarung von Informationen an, die zwischen dem Anmeldedatum der früheren Anmeldung und dem nationalen oder PCT internationalen Anmeldedatum dieser Anmeldung bekannt geworden sind.

I hereby claim the benefit under Title 35, United States Code, §120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, §112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, §1.56(a) which occurred between the filing date of the prior application and the national or PCT international filing date of this application:

(Application Serial No.) (Anmeldeseriennummer)	(Filing Date) (Anmeldedatum)	(Status) (patentiert, anhängig, aufgegeben)	(Status) (patented, pending, abandoned)
(Application Serial No.) (Anmeldeseriennummer)	(Filing Date) (Anmeldedatum)	(Status) (patentiert, anhängig, aufgegeben)	(Status) (patented, pending, abandoned)

Ich erkläre hiermit, dass alle von mir in der vorliegenden Erklärung gemachten Angaben nach meinem besten Wissen und Gewissen der vollen Wahrheit entsprechen, und dass ich diese eidesstattliche Erklärung in Kenntnis dessen abgebe, dass wissentlich und vorsätzlich falsche Angaben gemäss Paragraph 1001, Absatz 18 der Zivilprozessordnung der Vereinigten Staaten von Amerika mit Geldstrafe belegt und/oder Gefängnis bestraft werden koennen, und dass derartig wissentlich und vorsätzlich falsche Angaben die Gültigkeit der vorliegenden Patentanmeldung oder eines darauf erteilten Patentes gefährden können.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

German Language Declaration

VERTRETUNGSVOLLMACHT: Als benannter Erfinder beauftrage ich hiermit den nachstehend benannten Patentanwalt (oder die nachstehend benannten Patentanwälte) und/oder Patent-Agenten mit der Verfolgung der vorliegenden Patentanmeldung sowie mit der Abwicklung aller damit verbundenen Geschäfte vor dem Patent-und Warenzeichenamt: *(Name und Registrationsnummer anführen)*

POWER OF ATTORNEY: As a named inventor, I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith. *(list name and registration number)*

Donald M. Duft	~~17,484~~	William P. Wilbar	43,265
James M. Graziano	~~28,300~~ 28,300	Thomas Swenson	36,696
Carl A. Forest	~~28,494~~	Curtis A. Vock	38,356
Dan Cleveland, Jr.	~~36,106~~ 36,106	Kirk D. Williams	42,229
Michael J. Setter	37,936	Steven W. Weinrieb	~~26,520~~ 26,520

10

Telefongespräche bitte richten an: *(Name und Telefonnummer)*

Direct Telephone Calls to: *(name and telephone number)*

Postanschrift:

Send Correspondence to:
Carl A. Forest, Ph.D.
c/o DUFT, GRAZIANO & FOREST, P.C.
1790-30th Street
- Suite 140 -
Boulder, Colorado 80301-1018, U.S.A.

Voller Name des einzigen oder ursprünglichen Erfinders:	Full name of sole or first inventor: Michael TASLER
Unterschrift des Erfinders Datum	Inventor's signature Michael Tasler Date April 27, 1999
Wohnsitz	Residence Würzburg, Germany
Staatsangehörigkeit	Citizenship German DEX
Postanschrift	Post Office Address Cronthalstraße 6c
	D-97074 Würzburg, Germany
Voller Name des zweiten Miterfinders (falls zutreffend)	Full name of second joint inventor, if any
Unterschrift des Erfinders Datum	Second Inventor's signature Date
Wohnsitz	Residence
Staatsangehörigkeit	Citizenship
Postanschrift	Post Office Address

(Bitte entsprechende Informationen und Unterschriften im Falle von dritten und weiteren Miterfindern angeben).

(Supply similar information and signature for third and subsequent joint inventors.)

Applicant or Patentee: TASLER, el
Serial or Patent No.:
Filed or Issued:
For: Flexible Interface

VERIFIED STATEMENT (DECLARATION) CLAIMING SMALL ENTITY STATUS
(37 CFR 1.9 (F) and 1.27 (B)) - INDEPENDENT INVENTOR

As a below named inventor, I hereby declare that I qualify as an independent inventor as defined in 37 CFR 1.9 (c) for purposes of paying reduced fees under section 41(a) and (b) of Title 35, United States Code, to the Patent and Trademark Office with regard to the invention entitled Flexible Interface described in:

(X) the specification filed herewith
( ) application serial no. ....., filed .....
( ) patent no. ....., issued .....

I have not assigned, granted, conveyed or licensed and am under no obligation under contract or law to assign, grant, convey or license, any rights in the invention to any person who could not be classified as an independent inventor under 37 CFR 1.9(c) if that person had made the invention, or to any concern which would not qualify as a small business concern under 37 CFR 1.9(d) or a nonprofit organization under 37 CFR 1.9(e).

Each person, concern or organization to which I have assigned, granted conveyed, or licensed or am under an obligation under contract or law to assign, grant, convey, or license any rights in the invention listed below:

(X) no such person, concern, organization
( ) persons, concerns or organizations listed below*

*NOTE: Separate verified statements are required from each named person, concern or organization having rights to the invention averring to their status as small entities. (37 CFR 1.27)

FULL NAME .....Name des deutschen Anmelders.....
ADDRESS .....Adresse.....
( ) INDIVIDUAL ( ) SMALL BUSINESS CONCERN ( ) NONPROFIT ORGANIZATION

FULL NAME _____
ADDRESS _____
( ) INDIVIDUAL ( ) SMALL BUSINESS CONCERN ( ) NONPROFIT ORGANIZATION

I acknowledge the duty to file, in this application or patent, notification of any change in status resulting in loss of entitlement to small entity status prior to paying, or at the time of paying , the earliest of the issue fee or any maintenance fee due after the date on which status as a small entity in no longer appropriate. (37 CFR 1.28 (b))

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application, any patent issuing thereon, or any patent to which this verified statement is directed.

Michael TASLER
NAME OF INVENTOR

Michael Tasler
Signature of Inventor

April 27, 1999
DATE

09/331002

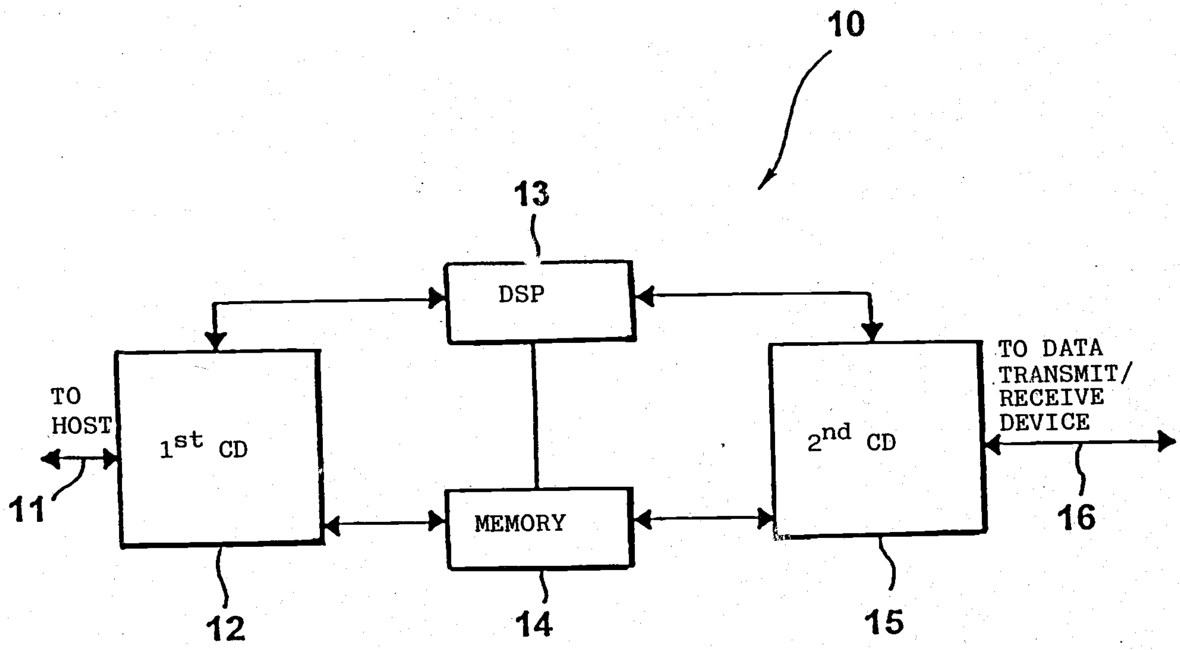

FIG.1

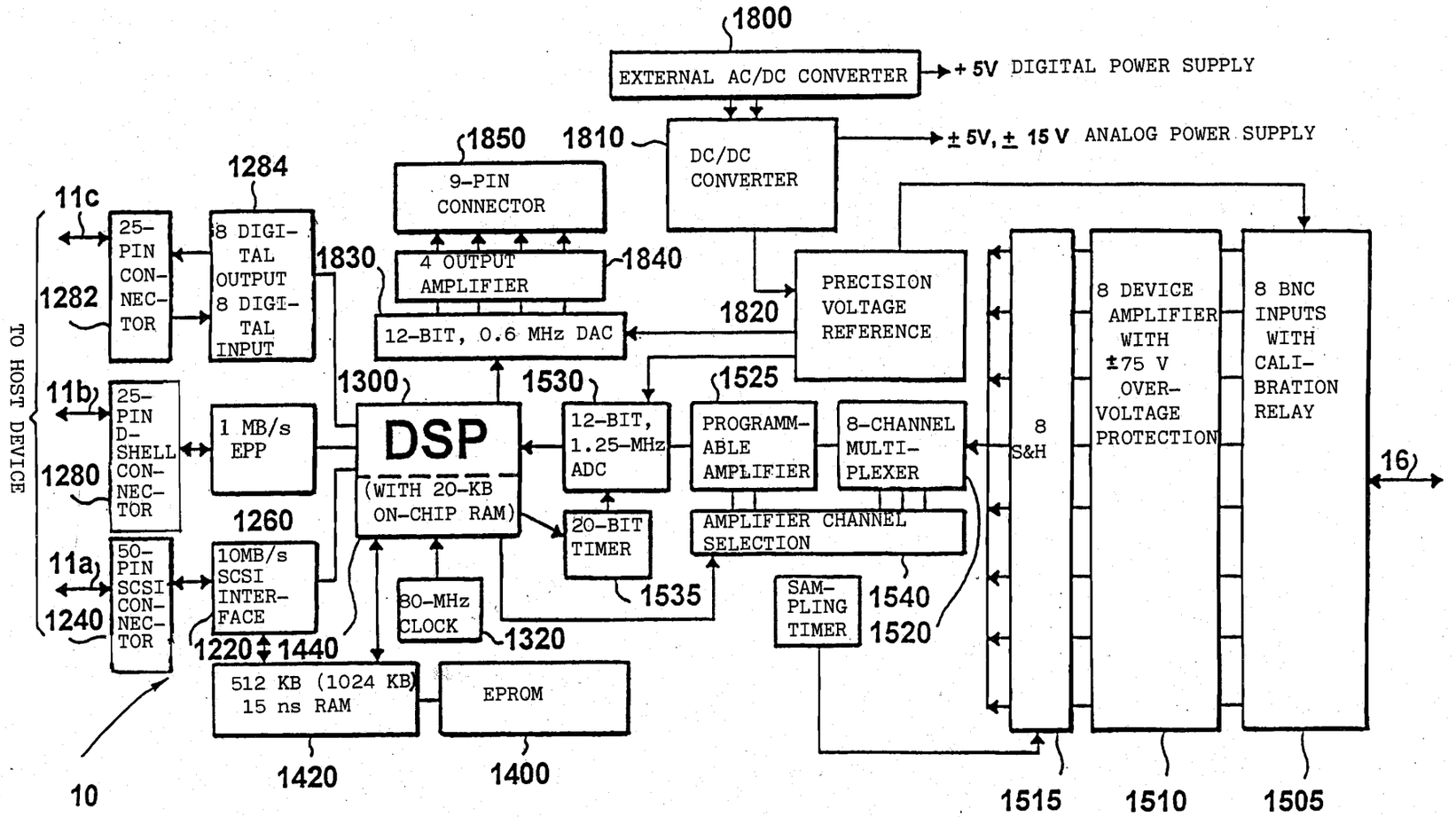

FIG.2

PRINT OF DRAWINGS
AS ORIGINALLY FILED

09/331002

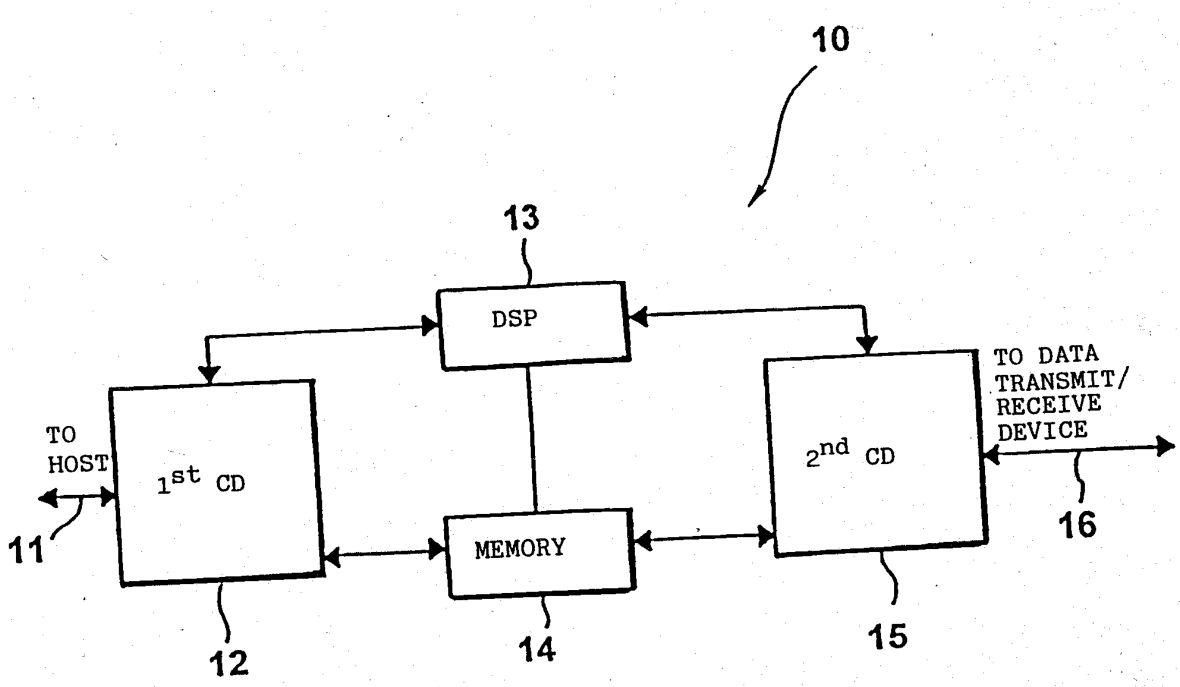

FIG. 1

PRINT OF DRAWINGS
AS ORIGINALLY FILED

09/331002

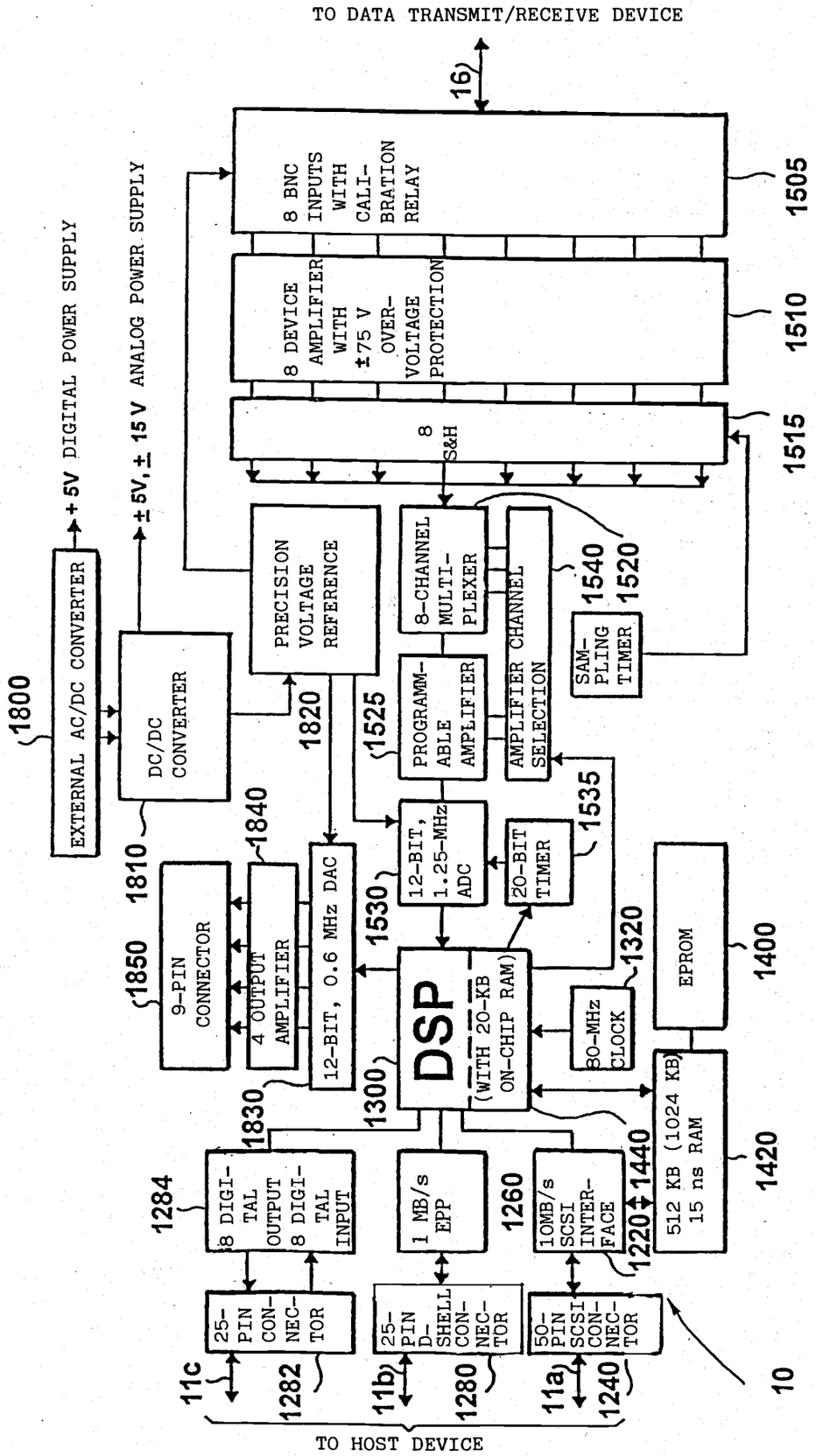

FIG.2

VERTRAG ÜBER DIE INTERNATIONALE ZUSAMMENARBEIT
AUF DEM GEBIET DES PATENTWESENS

PCT

INTERNATIONALER RECHERCHENBERICHT

(Artikel 18 sowie Regeln 43 und 44 PCT)

Aktenzeichen des Anmelders oder Anwalts	**WEITERES VORGEHEN**	siehe Mitteilung über die Übermittlung des internationalen Recherchenberichts (Formblatt PCT/ISA/220) sowie, soweit zutreffend, nachstehender Punkt 5
1482-PCT		
Internationales Aktenzeichen	Internationales Anmeldedatum *(Tag/Monat/Jahr)*	(Frühestes) Prioritätsdatum *(Tag/Monat/Jahr)*
PCT/DE 98/ 01187	29/04/1998	30/04/1997
Anmelder		
LEMUTH PRÄZISIONSTEILE GMBH et al.		

Dieser internationale Recherchenbericht wurde von der Internationalen Recherchenbehörde erstellt und wird dem Anmelder gemäß Artikel 18 übermittelt. Eine Kopie wird dem Internationalen Büro übermittelt.

Dieser internationale Recherchenbericht umfaßt insgesamt 2 Blätter.

[X] Darüber hinaus liegt ihm jeweils eine Kopie der in diesem Bericht genannten Unterlagen zum Stand der Technik bei.

1. [ ] **Bestimmte Ansprüche haben sich als nichtrecherchierbar erwiesen** (siehe Feld I).

2. [ ] **Mangelnde Einheitlichkeit der Erfindung**(siehe Feld II).

3. [ ] In der internationalen Anmeldung ist **ein Protokoll einer Nucleotid- und/oder Aminosäuresequenz** offenbart; die internationale Recherche wurde auf der Grundlage des Sequenzprotokolls durchgeführt,
   - [ ] das zusammen mit der internationalen Anmeldung eingereicht wurde.
   - [ ] das vom Anmelder getrennt von der internationalen Anmeldung vorgelegt wurde,
     - [ ] dem jedoch keine Erklärung beigefügt war, daß der Inhalt des Protokolls nicht über den Offenbarungsgehalt der internationalen Anmeldung in der eingereichten Fassung hinausgeht.
   - [ ] das von der Internationalen Recherchenbehörde in die ordnungsgemäße Form übertragen wurde.

4. Hinsichtlich der **Bezeichnung der Erfindung**
   - [X] wird der vom Anmelder eingereichte Wortlaut genehmigt.
   - [ ] wurde der Wortlaut von der Behörde wie folgt festgesetzt.

5. Hinsichtlich der **Zusammenfassung**
   - [X] wird der vom Anmelder eingereichte Wortlaut genehmigt.
   - [ ] wurde der Wortlaut nach Regel 38.2b) in der Feld III angegebenen Fassung von dieser Behörde festgesetzt. Der Anmelder kann der Internationalen Recherchenbehörde innerhalb eines Monats nach dem Datum der Absendung dieses internationalen Recherchenberichts eine Stellungnahme vorlegen.

6. Folgende Abbildung der **Zeichnungen** ist mit der Zusammenfassung zu veröffentlichen:
   Abb. Nr. 2
   - [ ] wie vom Anmelder vorgeschlagen
   - [X] weil der Anmelder selbst keine Abbildung vorgeschlagen hat.
   - [ ] weil diese Abbildung die Erfindung besser kennzeichnet.
   - [ ] keine der Abb.

INTERNATIONALER RECHERCHENBERICHT

nationales Aktenzeichen
T/DE 98/01187

A. KLASSIFIZIERUNG DES ANMELDUNGSGEGENSTANDES
IPK 6 G05B19/414 G05B19/418

Nach der Internationalen Patentklassifikation (IPK) oder nach der nationalen Klassifikation und der IPK

B. RECHERCHIERTE GEBIETE

Recherchierter Mindestprüfstoff (Klassifikationssystem und Klassifikationssymbole)
IPK 6 G05B B23K G02B

Recherchierte aber nicht zum Mindestprüfstoff gehörende Veröffentlichungen, soweit diese unter die recherchierten Gebiete fallen

Während der internationalen Recherche konsultierte elektronische Datenbank (Name der Datenbank und evtl. verwendete Suchbegriffe)

C. ALS WESENTLICH ANGESEHENE UNTERLAGEN

Kategorie°	Bezeichnung der Veröffentlichung, soweit erforderlich unter Angabe der in Betracht kommenden Teile	Betr. Anspruch Nr.
A	US 5 268 975 A (YOSHITANI KATSUMI ET AL) 7. Dezember 1993 siehe Spalte 6, Zeile 6 - Spalte 8, Zeile 31; Abbildungen 1-3 ---	1-6
A	EP 0 530 973 A (HITACHI LTD) 10. März 1993 siehe Spalte 2, Zeile 55 - Spalte 8, Zeile 36 -----	1-6

☐ Weitere Veröffentlichungen sind der Fortsetzung von Feld C zu entnehmen

☒ Siehe Anhang Patentfamilie

° Besondere Kategorien von angegebenen Veröffentlichungen :
"A" Veröffentlichung, die den allgemeinen Stand der Technik definiert, aber nicht als besonders bedeutsam anzusehen ist
"E" älteres Dokument, das jedoch erst am oder nach dem internationalen Anmeldedatum veröffentlicht worden ist
"L" Veröffentlichung, die geeignet ist, einen Prioritätsanspruch zweifelhaft erscheinen zu lassen, oder durch die das Veröffentlichungsdatum einer anderen im Recherchenbericht genannten Veröffentlichung belegt werden soll oder die aus einem anderen besonderen Grund angegeben ist (wie ausgeführt)
"O" Veröffentlichung, die sich auf eine mündliche Offenbarung, eine Benutzung, eine Ausstellung oder andere Maßnahmen bezieht
"P" Veröffentlichung, die vor dem internationalen Anmeldedatum, aber nach dem beanspruchten Prioritätsdatum veröffentlicht worden ist
"T" Spätere Veröffentlichung, die nach dem internationalen Anmeldedatum oder dem Prioritätsdatum veröffentlicht worden ist und mit der Anmeldung nicht kollidiert, sondern nur zum Verständnis des der Erfindung zugrundeliegenden Prinzips oder der ihr zugrundeliegenden Theorie angegeben ist
"X" Veröffentlichung von besonderer Bedeutung; die beanspruchte Erfindung kann allein aufgrund dieser Veröffentlichung nicht als neu oder auf erfinderischer Tätigkeit beruhend betrachtet werden
"Y" Veröffentlichung von besonderer Bedeutung; die beanspruchte Erfindung kann nicht als auf erfinderischer Tätigkeit beruhend betrachtet werden, wenn die Veröffentlichung mit einer oder mehreren anderen Veröffentlichungen dieser Kategorie in Verbindung gebracht wird und diese Verbindung für einen Fachmann naheliegend ist
"&" Veröffentlichung, die Mitglied derselben Patentfamilie ist

Datum des Abschlusses der internationalen Recherche	Absendedatum des internationalen Recherchenberichts
23. Oktober 1998	30/10/1998
Name und Postanschrift der Internationalen Recherchenbehörde Europäisches Patentamt, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	**Bevollmächtigter Bediensteter** Nettesheim, J

1

Formblatt PCT/ISA/210 (Blatt 2) (Juli 1992)

INTERNATIONAL SEARCH REPORT

Information on patent family members

National Application No
PCT/DE 98/01187

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 5268975 A	07-12-1993	JP 5212574 A	24-08-1993
		JP 5157978 A	25-06-1993
		JP 5107486 A	30-04-1993
		CA 2066909 A	27-10-1992
		DE 4213424 A	29-10-1992
		GB 2255653 A,B	11-11-1992
EP 0530973 A	10-03-1993	JP 5067669 A	19-03-1993
		DE 69224568 D	09-04-1998
		US 5663884 A	02-09-1997
		US 5448470 A	05-09-1995

VERTRAG BER DIE INTERNATIONALE ZUS MENARBEIT
AUF DEM GEBIET DES PATENTWESENS

PCT

INTERNATIONALER RECHERCHENBERICHT

(Artikel 18 sowie Regeln 43 und 44 PCT)

Aktenzeichen des Anmelders oder Anwalts	**WEITERES VORGEHEN**	siehe Mitteilung über die Übermittlung des internationalen Recherchenberichts (Formblatt PCT/ISA/220) sowie, soweit zutreffend, nachstehender Punkt 5	
TA980301PCT			
Internationales Aktenzeichen	Internationales Anmeldedatum *(Tag/Monat/Jahr)*		(Frühestes) Prioritätsdatum *(Tag/Monat/Jahr)*
PCT/EP 98/ 01187	03/03/1998		04/03/1997
Anmelder			
TASLER, Michael			

Dieser internationale Recherchenbericht wurde von der Internationalen Recherchenbehörde erstellt und wird dem Anmelder gemäß Artikel 18 übermittelt. Eine Kopie wird dem Internationalen Büro übermittelt.

Dieser internationale Recherchenbericht umfaßt insgesamt 3 Blätter.

[X] Darüber hinaus liegt ihm jeweils eine Kopie der in diesem Bericht genannten Unterlagen zum Stand der Technik bei.

1. [ ] **Bestimmte Ansprüche haben sich als nichtrecherchierbar erwiesen** (siehe Feld I).

2. [ ] **Mangelnde Einheitlichkeit der Erfindung** (siehe Feld II).

3. [ ] In der internationalen Anmeldung ist **ein Protokoll einer Nucleotid- und/oder Aminosäuresequenz** offenbart; die internationale Recherche wurde auf der Grundlage des Sequenzprotokolls durchgeführt,
   - [ ] das zusammen mit der internationalen Anmeldung eingereicht wurde.
   - [ ] das vom Anmelder getrennt von der internationalen Anmeldung vorgelegt wurde,
     - [ ] dem jedoch keine Erklärung beigefügt war, daß der Inhalt des Protokolls nicht über den Offenbarungsgehalt der internationalen Anmeldung in der eingereichten Fassung hinausgeht.
   - [ ] das von der Internationalen Recherchenbehörde in die ordnungsgemäße Form übertragen wurde.

4. Hinsichtlich der **Bezeichnung der Erfindung**
   - [X] wird der vom Anmelder eingereichte Wortlaut genehmigt.
   - [ ] wurde der Wortlaut von der Behörde wie folgt festgesetzt.

5. Hinsichtlich der **Zusammenfassung**
   - [X] wird der vom Anmelder eingereichte Wortlaut genehmigt.
   - [ ] wurde der Wortlaut nach Regel 38.2b) in der Feld III angegebenen Fassung von dieser Behörde festgesetzt. Der Anmelder kann der Internationalen Recherchenbehörde innerhalb eines Monats nach dem Datum der Absendung dieses internationalen Recherchenberichts eine Stellungnahme vorlegen.

6. Folgende Abbildung der **Zeichnungen** ist mit der Zusammenfassung zu veröffentlichen:
   Abb. Nr. 1
   - [X] wie vom Anmelder vorgeschlagen
   - [ ] weil der Anmelder selbst keine Abbildung vorgeschlagen hat.
   - [ ] weil diese Abbildung die Erfindung besser kennzeichnet.
   - [ ] keine der Abb.

INTERNATIONALER RECHERCHENBERICHT

nationales Aktenzeichen
T/EP 98/01187

A. KLASSIFIZIERUNG DES ANMELDUNGSGEGENSTANDES
IPK 6 G06F13/38

Nach der Internationalen Patentklassifikation (IPK) oder nach der nationalen Klassifikation und der IPK

B. RECHERCHIERTE GEBIETE

Recherchierter Mindestprüfstoff (Klassifikationssystem und Klassifikationssymbole)
IPK 6 G06F G05B

Recherchierte aber nicht zum Mindestprüfstoff gehörende Veröffentlichungen, soweit diese unter die recherchierten Gebiete fallen

Während der internationalen Recherche konsultierte elektronische Datenbank (Name der Datenbank und evtl. verwendete Suchbegriffe)

C. ALS WESENTLICH ANGESEHENE UNTERLAGEN

Kategorie°	Bezeichnung der Veröffentlichung, soweit erforderlich unter Angabe der in Betracht kommenden Teile	Betr. Anspruch Nr.
Y A	US 5 487 154 A (GUNJI KEITA) 23.Januar 1996 siehe Spalte 1, Zeile 24 - Spalte 2, Zeile 16 siehe Spalte 3, Zeile 46 - Spalte 4, Zeile 4 siehe Spalte 4, Zeile 47 - Spalte 5, Zeile 2 siehe Zusammenfassung; Ansprüche 1-3; Abbildungen 1,4,5 ---	1,12,15 2-11,13, 14,16
Y	US 5 510 775 A (LONCLE JEAN-PIERRE) 23.April 1996 siehe Spalte 4, Zeile 56 - Zeile 61 siehe Spalte 6, Zeile 27 - Spalte 7, Zeile 21 siehe Zusammenfassung; Abbildung 1 --- -/--	1,12,15

[X] Weitere Veröffentlichungen sind der Fortsetzung von Feld C zu entnehmen

[X] Siehe Anhang Patentfamilie

° Besondere Kategorien von angegebenen Veröffentlichungen :
"A" Veröffentlichung, die den allgemeinen Stand der Technik definiert, aber nicht als besonders bedeutsam anzusehen ist
"E" älteres Dokument, das jedoch erst am oder nach dem internationalen Anmeldedatum veröffentlicht worden ist
"L" Veröffentlichung, die geeignet ist, einen Prioritätsanspruch zweifelhaft erscheinen zu lassen, oder durch die das Veröffentlichungsdatum einer anderen im Recherchenbericht genannten Veröffentlichung belegt werden soll oder die aus einem anderen besonderen Grund angegeben ist (wie ausgeführt)
"O" Veröffentlichung, die sich auf eine mündliche Offenbarung, eine Benutzung, eine Ausstellung oder andere Maßnahmen bezieht
"P" Veröffentlichung, die vor dem internationalen Anmeldedatum, aber nach dem beanspruchten Prioritätsdatum veröffentlicht worden ist
"T" Spätere Veröffentlichung, die nach dem internationalen Anmeldedatum oder dem Prioritätsdatum veröffentlicht worden ist und mit der Anmeldung nicht kollidiert, sondern nur zum Verständnis des der Erfindung zugrundeliegenden Prinzips oder der ihr zugrundeliegenden Theorie angegeben ist
"X" Veröffentlichung von besonderer Bedeutung; die beanspruchte Erfindung kann allein aufgrund dieser Veröffentlichung nicht als neu oder auf erfinderischer Tätigkeit beruhend betrachtet werden
"Y" Veröffentlichung von besonderer Bedeutung; die beanspruchte Erfindung kann nicht als auf erfinderischer Tätigkeit beruhend betrachtet werden, wenn die Veröffentlichung mit einer oder mehreren anderen Veröffentlichungen dieser Kategorie in Verbindung gebracht wird und diese Verbindung für einen Fachmann naheliegend ist
"&" Veröffentlichung, die Mitglied derselben Patentfamilie ist

Datum des Abschlusses der internationalen Recherche	Absendedatum des internationalen Recherchenberichts
21.Juli 1998	28/07/1998

Name und Postanschrift der Internationalen Recherchenbehörde	Bevollmächtigter Bediensteter
Europäisches Patentamt, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Nguyen Xuan Hiep, C

1

INTERNATIONALER RECHERCHENBERICHT

ationales Aktenzeichen
PCT/EP 98/01187

C.(Fortsetzung) ALS WESENTLICH ANGESEHENE UNTERLAGEN

Kategorie°	Bezeichnung der Veröffentlichung, soweit erforderlich unter Angabe der in Betracht kommenden Teile	Betr. Anspruch Nr.
A	US 5 444 644 A (DIVJAK AUGUST A) 22.August 1995 siehe Zusammenfassung; Abbildung 1 ---	1-16
A	US 5 291 611 A (DAVIS ALAN J ET AL) 1.März 1994 siehe Zusammenfassung; Abbildung 1 -----	1-16

1

INTERNATIONAL SEARCH REPORT

ıation on patent family members

·national Application No
, ,T/EP 98/01187

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 5487154 A	23-01-1996	JP 5030112 A	05-02-1993
		DE 4223454 A	21-01-1993
US 5510775 A	23-04-1996	FR 2659457 A	13-09-1991
		DE 69118994 D	30-05-1996
		DE 69118994 T	31-10-1996
		WO 9114213 A	19-09-1991
		EP 0471806 A	26-02-1992
		JP 7031653 B	10-04-1995
		JP 4503728 T	02-07-1992
US 5444644 A	22-08-1995	NONE	
US 5291611 A	01-03-1994	NONE	

VERTRAG Ü R DIE INTERNATIONALE ZUSAM ENARBEIT
AU. DEM GEBIET DES PATENTWESENS

PCT

INTERNATIONALER RECHERCHENBERICHT

(Artikel 18 sowie Regeln 43 und 44 PCT)

Aktenzeichen des Anmelders oder Anwalts	**WEITERES VORGEHEN**	siehe Mitteilung über die Übermittlung des internationalen Recherchenberichts (Formblatt PCT/ISA/220) sowie, soweit zutreffend, nachstehender Punkt 5	
TA980301PCT			
Internationales Aktenzeichen	Internationales Anmeldedatum *(Tag/Monat/Jahr)*	(Frühestes) Prioritätsdatum *(Tag/Monat/Jahr)*	
PCT/EP 98/ 01187	03/03/1998	04/03/1997	
Anmelder			
TASLER, Michael			

Dieser internationale Recherchenbericht wurde von der Internationalen Recherchenbehörde erstellt und wird dem Anmelder gemäß Artikel 18 übermittelt. Eine Kopie wird dem Internationalen Büro übermittelt.

Dieser internationale Recherchenbericht umfaßt insgesamt 3 Blätter.

[X] Darüber hinaus liegt ihm jeweils eine Kopie der in diesem Bericht genannten Unterlagen zum Stand der Technik bei.

1. [ ] **Bestimmte Ansprüche haben sich als nichtrecherchierbar erwiesen** (siehe Feld I).

2. [ ] **Mangelnde Einheitlichkeit der Erfindung** (siehe Feld II).

3. [ ] In der internationalen Anmeldung ist **ein Protokoll einer Nucleotid- und/oder Aminosäuresequenz** offenbart; die internationale Recherche wurde auf der Grundlage des Sequenzprotokolls durchgeführt,
   - [ ] das zusammen mit der internationalen Anmeldung eingereicht wurde.
   - [ ] das vom Anmelder getrennt von der internationalen Anmeldung vorgelegt wurde,
     - [ ] dem jedoch keine Erklärung beigefügt war, daß der Inhalt des Protokolls nicht über den Offenbarungsgehalt der internationalen Anmeldung in der eingereichten Fassung hinausgeht.
   - [ ] das von der Internationalen Recherchenbehörde in die ordnungsgemäße Form übertragen wurde.

4. Hinsichtlich der **Bezeichnung der Erfindung**
   - [X] wird der vom Anmelder eingereichte Wortlaut genehmigt.
   - [ ] wurde der Wortlaut von der Behörde wie folgt festgesetzt.

5. Hinsichtlich der **Zusammenfassung**
   - [X] wird der vom Anmelder eingereichte Wortlaut genehmigt.
   - [ ] wurde der Wortlaut nach Regel 38.2b) in der Feld III angegebenen Fassung von dieser Behörde festgesetzt. Der Anmelder kann der Internationalen Recherchenbehörde innerhalb eines Monats nach dem Datum der Absendung dieses internationalen Recherchenberichts eine Stellungnahme vorlegen.

6. Folgende Abbildung der **Zeichnungen** ist mit der Zusammenfassung zu veröffentlichen:
   Abb. Nr. 1
   - [X] wie vom Anmelder vorgeschlagen
   - [ ] weil der Anmelder selbst keine Abbildung vorgeschlagen hat.
   - [ ] weil diese Abbildung die Erfindung besser kennzeichnet.
   - [ ] keine der Abb.

INTERNATIONALER RECHERCHENBERICHT

Internales Aktenzeichen
PC., EP 98/01187

A. KLASSIFIZIERUNG DES ANMELDUNGSGEGENSTANDES
IPK 6 G06F13/38

Nach der Internationalen Patentklassifikation (IPK) oder nach der nationalen Klassifikation und der IPK

B. RECHERCHIERTE GEBIETE

Recherchierter Mindestprüfstoff (Klassifikationssystem und Klassifikationssymbole)
IPK 6 G06F G05B

Recherchierte aber nicht zum Mindestprüfstoff gehörende Veröffentlichungen, soweit diese unter die recherchierten Gebiete fallen

Während der internationalen Recherche konsultierte elektronische Datenbank (Name der Datenbank und evtl. verwendete Suchbegriffe)

C. ALS WESENTLICH ANGESEHENE UNTERLAGEN

Kategorie°	Bezeichnung der Veröffentlichung, soweit erforderlich unter Angabe der in Betracht kommenden Teile	Betr. Anspruch Nr.
Y A	US 5 487 154 A (GUNJI KEITA) 23.Januar 1996 siehe Spalte 1, Zeile 24 - Spalte 2, Zeile 16 siehe Spalte 3, Zeile 46 - Spalte 4, Zeile 4 siehe Spalte 4, Zeile 47 - Spalte 5, Zeile 2 siehe Zusammenfassung; Ansprüche 1-3; Abbildungen 1,4,5	1,12,15 2-11,13, 14,16
Y	US 5 510 775 A (LONCLE JEAN-PIERRE) 23.April 1996 siehe Spalte 4, Zeile 56 - Zeile 61 siehe Spalte 6, Zeile 27 - Spalte 7, Zeile 21 siehe Zusammenfassung; Abbildung 1	1,12,15

-/--

[X] Weitere Veröffentlichungen sind der Fortsetzung von Feld C zu entnehmen

[X] Siehe Anhang Patentfamilie

° Besondere Kategorien von angegebenen Veröffentlichungen :
"A" Veröffentlichung, die den allgemeinen Stand der Technik definiert, aber nicht als besonders bedeutsam anzusehen ist
"E" älteres Dokument, das jedoch erst am oder nach dem internationalen Anmeldedatum veröffentlicht worden ist
"L" Veröffentlichung, die geeignet ist, einen Prioritätsanspruch zweifelhaft erscheinen zu lassen, oder durch die das Veröffentlichungsdatum einer anderen im Recherchenbericht genannten Veröffentlichung belegt werden soll oder die aus einem anderen besonderen Grund angegeben ist (wie ausgeführt)
"O" Veröffentlichung, die sich auf eine mündliche Offenbarung, eine Benutzung, eine Ausstellung oder andere Maßnahmen bezieht
"P" Veröffentlichung, die vor dem internationalen Anmeldedatum, aber nach dem beanspruchten Prioritätsdatum veröffentlicht worden ist
"T" Spätere Veröffentlichung, die nach dem internationalen Anmeldedatum oder dem Prioritätsdatum veröffentlicht worden ist und mit der Anmeldung nicht kollidiert, sondern nur zum Verständnis des der Erfindung zugrundeliegenden Prinzips oder der ihr zugrundeliegenden Theorie angegeben ist
"X" Veröffentlichung von besonderer Bedeutung; die beanspruchte Erfindung kann allein aufgrund dieser Veröffentlichung nicht als neu oder auf erfinderischer Tätigkeit beruhend betrachtet werden
"Y" Veröffentlichung von besonderer Bedeutung; die beanspruchte Erfindung kann nicht als auf erfinderischer Tätigkeit beruhend betrachtet werden, wenn die Veröffentlichung mit einer oder mehreren anderen Veröffentlichungen dieser Kategorie in Verbindung gebracht wird und diese Verbindung für einen Fachmann naheliegend ist
"&" Veröffentlichung, die Mitglied derselben Patentfamilie ist

Datum des Abschlusses der internationalen Recherche	Absendedatum des internationalen Recherchenberichts
21.Juli 1998	28/07/1998

Name und Postanschrift der Internationalen Recherchenbehörde	Bevollmächtigter Bediensteter
Europäisches Patentamt, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Nguyen Xuan Hiep, C

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Formblatt PCT/ISA/210 (Blatt 2) (Juli 1992)

INTERNATIONALER RECHERCHENBERICHT

Internales Aktenzeichen
PC[illegible]P 98/01187

C.(Fortsetzung) ALS WESENTLICH ANGESEHENE UNTERLAGEN

Kategorie°	Bezeichnung der Veröffentlichung, soweit erforderlich unter Angabe der in Betracht kommenden Teile	Betr. Anspruch Nr.
A	US 5 444 644 A (DIVJAK AUGUST A) 22.August 1995 siehe Zusammenfassung; Abbildung 1	1-16
A	US 5 291 611 A (DAVIS ALAN J ET AL) 1.März 1994 siehe Zusammenfassung; Abbildung 1	1-16

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INTERNATIONALER RECHERCHENBERICHT

Angaben zu Veröffentlichungen, die ...lben Patentfamilie gehören

Interr ...ales Aktenzeichen
PC... ...P 98/01187

Im Recherchenbericht angeführtes Patentdokument	Datum der Veröffentlichung	Mitglied(er) der Patentfamilie	Datum der Veröffentlichung
US 5487154 A	23-01-1996	JP 5030112 A	05-02-1993
		DE 4223454 A	21-01-1993
US 5510775 A	23-04-1996	FR 2659457 A	13-09-1991
		DE 69118994 D	30-05-1996
		DE 69118994 T	31-10-1996
		WO 9114213 A	19-09-1991
		EP 0471806 A	26-02-1992
		JP 7031653 B	10-04-1995
		JP 4503728 T	02-07-1992
US 5444644 A	22-08-1995	KEINE	
US 5291611 A	01-03-1994	KEINE	

Formblatt PCT/ISA/210 (Anhang Patentfamilie)(Juli 1992)

INTERNATIONAL SEARCH REPORT

Inte onal Application No
PCT/EP 98/01187

A. CLASSIFICATION OF SUBJECT MATTER
IPC 6 G06F13/38

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 6 G06F G05B

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 5 487 154 A (GUNJI KEITA) 23 January 1996	1,12,15
A	see column 1, line 24 - column 2, line 16 see column 3, line 46 - column 4, line 4 see column 4, line 47 - column 5, line 2 see abstract; claims 1-3; figures 1,4,5	2-11,13, 14,16
Y	US 5 510 775 A (LONCLE JEAN-PIERRE) 23 April 1996 see column 4, line 56 - line 61 see column 6, line 27 - column 7, line 21 see abstract; figure 1	1,12,15
A	US 5 444 644 A (DIVJAK AUGUST A) 22 August 1995 see abstract; figure 1	1-16

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[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

° Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
21 July 1998	28/07/1998

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Nguyen Xuan Hiep, C

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Form PCT/ISA/210 (second sheet) (July 1992)

INTERNATIONAL SEARCH REPORT

International Application No
PCT/EP 98/01187

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication,where appropriate, of the relevant passages	Relevant to claim No.
A	US 5 291 611 A (DAVIS ALAN J ET AL) 1 March 1994 see abstract; figure 1	1-16

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Form PCT/ISA/210 (continuation of second sheet) (July 1992)

INTERNATIONAL SEARCH REPORT

Information on patent family members

Int ional Application No
PCT/EP 98/01187

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 5487154 A	23-01-1996	JP 5030112 A	05-02-1993
		DE 4223454 A	21-01-1993
US 5510775 A	23-04-1996	FR 2659457 A	13-09-1991
		DE 69118994 D	30-05-1996
		DE 69118994 T	31-10-1996
		WO 9114213 A	19-09-1991
		EP 0471806 A	26-02-1992
		JP 7031653 B	10-04-1995
		JP 4503728 T	02-07-1992
US 5444644 A	22-08-1995	NONE	
US 5291611 A	01-03-1994	NONE	

Form PCT/ISA/210 (patent family annex) (July 1992)

INTERNATIONALER 'CHERCHENBERICHT

....ionales Aktenzeichen
PCT/EP 98/01187

C.(Fortsetzung) ALS WESENTLICH ANGESEHENE UNTERLAGEN

Kategorie°	Bezeichnung der Veröffentlichung, soweit erforderlich unter Angabe der in Betracht kommenden Teile	Betr. Anspruch Nr.
A	US 5 444 644 A (DIVJAK AUGUST A) 22.August 1995 siehe Zusammenfassung; Abbildung 1	1-16
A	US 5 291 611 A (DAVIS ALAN J ET AL) 1.März 1994 siehe Zusammenfassung; Abbildung 1	1-16

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INTERNATIONALER R HERCHENBERICHT

Inte ionales Aktenzeichen
PCT/EP 98/01187

A. KLASSIFIZIERUNG DES ANMELDUNGSGEGENSTANDES
IPK 6 G06F13/38

Nach der Internationalen Patentklassifikation (IPK) oder nach der nationalen Klassifikation und der IPK

B. RECHERCHIERTE GEBIETE

Recherchierter Mindestprüfstoff (Klassifikationssystem und Klassifikationssymbole)
IPK 6 G06F G05B

Recherchierte aber nicht zum Mindestprüfstoff gehörende Veröffentlichungen, soweit diese unter die recherchierten Gebiete fallen

Während der internationalen Recherche konsultierte elektronische Datenbank (Name der Datenbank und evtl. verwendete Suchbegriffe)

C. ALS WESENTLICH ANGESEHENE UNTERLAGEN

Kategorie*	Bezeichnung der Veröffentlichung, soweit erforderlich unter Angabe der in Betracht kommenden Teile	Betr. Anspruch Nr.
Y	US 5 487 154 A (GUNJI KEITA) 23.Januar 1996	1,12,15
A	siehe Spalte 1, Zeile 24 - Spalte 2, Zeile 16 siehe Spalte 3, Zeile 46 - Spalte 4, Zeile 4 siehe Spalte 4, Zeile 47 - Spalte 5, Zeile 2 siehe Zusammenfassung; Ansprüche 1-3; Abbildungen 1,4,5	2-11,13, 14,16
Y	US 5 510 775 A (LONCLE JEAN-PIERRE) 23.April 1996 siehe Spalte 4, Zeile 56 - Zeile 61 siehe Spalte 6, Zeile 27 - Spalte 7, Zeile 21 siehe Zusammenfassung; Abbildung 1	1,12,15

-/--

[X] Weitere Veröffentlichungen sind der Fortsetzung von Feld C zu entnehmen

[X] Siehe Anhang Patentfamilie

* Besondere Kategorien von angegebenen Veröffentlichungen :

"A" Veröffentlichung, die den allgemeinen Stand der Technik definiert, aber nicht als besonders bedeutsam anzusehen ist

"E" älteres Dokument, das jedoch erst am oder nach dem internationalen Anmeldedatum veröffentlicht worden ist

"L" Veröffentlichung, die geeignet ist, einen Prioritätsanspruch zweifelhaft erscheinen zu lassen, oder durch die das Veröffentlichungsdatum einer anderen im Recherchenbericht genannten Veröffentlichung belegt werden soll oder die aus einem anderen besonderen Grund angegeben ist (wie ausgeführt)

"O" Veröffentlichung, die sich auf eine mündliche Offenbarung, eine Benutzung, eine Ausstellung oder andere Maßnahmen bezieht

"P" Veröffentlichung, die vor dem internationalen Anmeldedatum, aber nach dem beanspruchten Prioritätsdatum veröffentlicht worden ist

"T" Spätere Veröffentlichung, die nach dem internationalen Anmeldedatum oder dem Prioritätsdatum veröffentlicht worden ist und mit der Anmeldung nicht kollidiert, sondern nur zum Verständnis des der Erfindung zugrundeliegenden Prinzips oder der ihr zugrundeliegenden Theorie angegeben ist

"X" Veröffentlichung von besonderer Bedeutung; die beanspruchte Erfindung kann allein aufgrund dieser Veröffentlichung nicht als neu oder auf erfinderischer Tätigkeit beruhend betrachtet werden

"Y" Veröffentlichung von besonderer Bedeutung; die beanspruchte Erfindung kann nicht als auf erfinderischer Tätigkeit beruhend betrachtet werden, wenn die Veröffentlichung mit einer oder mehreren anderen Veröffentlichungen dieser Kategorie in Verbindung gebracht wird und diese Verbindung für einen Fachmann naheliegend ist

"&" Veröffentlichung, die Mitglied derselben Patentfamilie ist

Datum des Abschlusses der internationalen Recherche	Absendedatum des internationalen Recherchenberichts
21.Juli 1998	28/07/1998

Name und Postanschrift der Internationalen Recherchenbehörde	Bevollmächtigter Bediensteter
Europäisches Patentamt, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Nguyen Xuan Hiep, C

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INTERNATIONALER RE(RCHENBERICHT

Angaben zu Veröffentlichu...gen, die zur selben Patentfamilie gehören

Int(onales Aktenzeichen
PCT/EP 98/01187

Im Recherchenbericht angeführtes Patentdokument		Datum der Veröffentlichung	Mitglied(er) der Patentfamilie		Datum der Veröffentlichung
US 5487154	A	23-01-1996	JP	5030112 A	05-02-1993
			DE	4223454 A	21-01-1993
US 5510775	A	23-04-1996	FR	2659457 A	13-09-1991
			DE	69118994 D	30-05-1996
			DE	69118994 T	31-10-1996
			WO	9114213 A	19-09-1991
			EP	0471806 A	26-02-1992
			JP	7031653 B	10-04-1995
			JP	4503728 T	02-07-1992
US 5444644	A	22-08-1995	KEINE		
US 5291611	A	01-03-1994	KEINE		

VERTRAG Ü R DIE INTERNATIONALE ZUSAI ENARBEIT
AU. DEM GEBIET DES PATENTWESENS

Absender: INTERNATIONALE RECHERCHENBEHÖRDE

PCT

MITTEILUNG ÜBER DIE ÜBERMITTLUNG DES INTERNATIONALEN RECHERCHENBERICHTS ODER DER ERKLÄRUNG

(Regel 44.1 PCT)

An
SCHOPPE & ZIMMERMANN
z.H. Schoppe, Fritz
Postfach 71 08 67
D-81458 München
GERMANY

EINGEGANGEN
30. JULI 1998

	Absendedatum *(Tag/Monat/Jahr)* 28/07/1998
Aktenzeichen des Anmelders oder Anwalts TA980301PCT	**WEITERES VORGEHEN** siehe Punkt 1 und 4 unten
Internationales Aktenzeichen PCT/EP 98/ 01187	Internationales Anmeldedatum *(Tag/Monat/Jahr)* 03/03/1998
Anmelder TASLER, Michael	

1. [X] Dem Anmelder wird mitgeteilt, daß der internationale Recherchenbericht erstellt wurde und ihm hiermit übermittelt wird.

Einreichung von Änderungen und einer Erklärung nach Artikel 19:
Der Anmelder kann auf eigenen Wunsch die Ansprüche der internationalen Anmeldung ändern (siehe Regel 46):

Bis wann sind Änderungen einzureichen?

Die Frist zur Einreichung solcher Änderungen beträgt üblicherweise zwei Monate ab der Übermittlung des internationalen Recherchenberichts; weitere Einzelheiten sind den Anmerkungen auf dem Beiblatt zu entnehmen.

Wo sind die Änderungen einzureichen?

Unmittelbar beim Internationalen Büro der WIPO, 34, CHEMIN des Colombettes, CH-1211 Genf 20, Telefaxnr.: (41-22) 740.14.35

Nähere Hinweise sind den Anmerkungen auf dem Beiblatt zu entnehmen.

2. [ ] Dem Anmelder wird mitgeteilt, daß kein internationaler Recherchenbericht erstellt wird und daß ihm hiermit die Erklärung nach Artikel 17(2)a) übermittelt wird.

3. [ ] **Hinsichtlich des Widerspruchs** gegen die Entrichtung einer zusätzlichen Gebühr (zusätzlicher Gebühren) nach Regel 40.2 wird dem Anmelder mitgeteilt, daß

[ ] der Widerspruch und die Entscheidung hierüber zusammen mit seinem Antrag auf Übermittlung des Wortlauts sowohl des Widerspruchs als auch der Entscheidung hierüber an die Bestimmungsämter dem Internationalen Büro übermittelt worden sind.

[ ] noch keine Entscheidung über den Widerspruch vorliegt; der Anmelder wird benachrichtigt, sobald eine Entscheidung getroffen wurde.

4. **Weiteres Vorgehen:** Der Anmelder wird auf folgendes aufmerksam gemacht:

Kurz nach Ablauf von **18 Monaten** seit dem Prioritätsdatum wird die internationale Anmeldung vom Internationalen Büro veröffentlicht. Will der Anmelder die Veröffentlichung verhindern oder auf einen späteren Zeitpunkt verschieben, so muß gemäß Regel 90 ^{bis}.1 bzw. 90 ^{bis}.3 vor Abschluß der technischen Vorbereitungen für die internationale Veröffentlichung eine Erklärung über die Zurücknahme der internationalen Anmeldung oder des Prioritätsanspruchs beim Internationalen Büro eingehen.

Innerhalb von **19 Monaten** seit dem Prioritätsdatum ist ein Antrag auf internationale vorläufige Prüfung einzureichen, wenn der Anmelder den Eintritt in die nationale Phase bis zu 30 Monaten seit dem Prioritätsdatum (in manchen Ämtern sogar noch länger) verschieben möchte.

Innerhalb von **20 Monaten** seit dem Prioritätsdatum muß der Anmelder die für den Eintritt in die nationale Phase vorgeschriebenen Handlungen vor allen Bestimmungsämtern vornehmen, die nicht innerhalb von 19 Monaten seit dem Prioritätsdatum in der Anmeldung oder einer nachträglichen Auswahlerklärung ausgewählt wurden oder nicht ausgewählt werden konnten, da für sie Kapitel II des Vertrages nicht verbindlich ist.

Name und Postanschrift der Internationalen Recherchenbehörde Europäisches Patentamt, P.B. 5818 Patentlaan 2 NL-2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Bevollmächtigter Bediensteter Marjory Sastropawiro

Formblatt PCT/ISA/220 (Januar 1994)

ANMERKUNGEN ZU FORMBLATT PCT/ISA/220

Diese Anmerkungen sollen grundlegende Hinweise zur Einreichung von Änderungen gemäß Artikel 19 geben. Diesen Anmerkungen liegen die Erfordernisse des Vertrags über die internationale Zusammenarbeit auf dem Gebiet des Patentwesens (PCT), der Ausführungsordnung und der Verwaltungsrichtlinien zu diesem Vertrag zugrunde. Bei Abweichungen zwischen diesen Anmerkungen und obengenannten Texten sind letztere maßgebend. Nähere Einzelheiten sind dem PCT-Leitfaden für Anmelder, einer Veröffentlichung der WIPO, zu entnehmen.
Die in diesen Anmerkungen verwendeten Begriffe "Artikel", "Regel" und "Abschnitt" beziehen sich jeweils auf die Bestimmungen des PCT-Vertrags, der PCT-Ausführungsordnung bzw. der PCT-Verwaltungsrichtlinien.

HINWEISE ZU ÄNDERUNGEN GEMÄSS ARTIKEL 19

Nach Erhalt des internationalen Recherchenberichts hat der Anmelder die Möglichkeit, einmal die Ansprüche der internationalen Anmeldung zu ändern. Es ist jedoch zu betonen, daß, da alle Teile der internationalen Anmeldung (Ansprüche, Beschreibung und Zeichnungen) während des internationalen vorläufigen Prüfungsverfahrens geändert werden können, normalerweise keine Notwendigkeit besteht, Änderungen der Ansprüche nach Artikel 19 einzureichen, außer wenn der Anmelder z.B. zum Zwecke eines vorläufigen Schutzes die Veröffentlichung dieser Anspruche wünscht oder ein anderer Grund für eine Änderung der Ansprüche vor ihrer internationalen Veröffentlichung vorliegt. Weiterhin ist zu beachten, daß ein vorläufiger Schutz nur in einigen Staaten erhältlich ist.

Welche Teile der internationalen Anmeldung können geändert werden?

Im Rahmen von Artikel 19 können nur die Ansprüche geändert werden.

In der internationalen Phase können die Ansprüche auch nach Artikel 34 vor der mit der internationalen vorläufigen Prüfung beauftragten Behörde geändert (oder nochmals geändert) werden. Die Beschreibung und die Zeichnungen können nur nach Artikel 34 vor der mit der internationalen vorläufigen Prüfung beauftragten Behörde geändert werden.

Beim Eintritt in die nationale Phase können alle Teile der internationalen Anmeldung nach Artikel 28 oder gegebenenfalls Artikel 41 geändert werden.

Bis wann sind Änderungen einzureichen?

Innerhalb von zwei Monaten ab der Übermittlung des internationalen Recherchenberichts oder innerhalb von sechzehn Monaten ab dem Prioritätsdatum, je nachdem, welche Frist später abläuft. Die Änderungen gelten jedoch als rechtzeitig eingereicht, wenn sie dem Internationalen Büro nach Ablauf der maßgebenden Frist, aber noch vor Abschluß der technischen Vorbereitungen für die internationale Veröffentlichung (Regel 46.1) zugehen.

Wo sind die Änderungen nicht einzureichen?

Die Änderungen können nur beim Internationalen Büro, nicht aber beim Anmeldeamt oder der Internationalen Recherchenbehörde eingereicht werden (Regel 46.2).

Falls ein Antrag auf internationale vorläufige Prüfung eingereicht wurde/wird, siehe unten.

In welcher Form können Änderungen erfolgen?

Eine Änderung kann erfolgen durch Streichung eines oder mehrerer ganzer Ansprüche, durch Hinzufügung eines oder mehrerer neuer Ansprüche oder durch Änderung des Wortlauts eines oder mehrerer Ansprüche in der eingereichten Fassung.

Für jedes Anspruchsblatt, das sich aufgrund einer oder mehrerer Änderungen von dem ursprünglich eingereichten Blatt unterscheidet, ist ein Ersatzblatt einzureichen.

Alle Ansprüche, die auf einem Ersatzblatt erscheinen, sind mit arabischen Ziffern zu numerieren. Wird ein Anspruch gestrichen, so brauchen, die anderen Ansprüche nicht neu numeriert zu werden. Im Fall einer Neunumerierung sind die Ansprüche fortlaufend zu numerieren (Verwaltungsrichtlinien, Abschnitt 205 b)).

Die Änderungen sind in der Sprache abzufassen, in der dieinternationale Anmeldung veröffentlicht wird.

Welche Unterlagen sind den Änderungen beizufügen?

Begleitschreiben (Abschnitt 205 b)):

Die Änderungen sind mit einem Begleitschreiben einzureichen.

Das Begleitschreiben wird nicht zusammen mit der internationalen Anmeldung und den geänderten Ansprüchen veröffentlicht. Es ist nicht zu verwechseln mit der "Erklärung nach Artikel 19(1)" (siehe unten, "Erklärung nach Artikel 19 (1)").

Das Begleitschreiben ist nach Wahl des Anmelders in englischer oder französischer Sprache abzufassen. Bei englischsprachigen internationalen Anmeldungen ist das Begleitschreiben aber ebenfalls in englischer, bei französischsprachigen internationalen Anmeldungen in französischer Sprache abzufassen.

ANMERKUNGEN ZU FORMBLATT PCT/ISA/220 (Fortsetzung)

Im Begleitschreiben sind die Unterschiede zwischen den Ansprüchen in der eingereichten Fassung und den geänderten Ansprüchen anzugeben. So ist insbesondere zu jedem Anspruch in der internationalen Anmeldung anzugeben (gleichlautende Angaben zu verschiedenen Ansprüchen können zusammengefaßt werden), ob

i) der Anspruch unverändert ist;

ii) der Anspruch gestrichen worden ist;

iii) der Anspruch neu ist;

iv) der Anspruch einen oder mehrere Ansprüche in der eingereichten Fassung ersetzt;

v) der Anspruch auf die Teilung eines Anspruchs in der eingereichten Fassung zurückzuführen ist.

Im folgenden sind Beispiele angegeben, wie Änderungen im Begleitschreiben zu erläutern sind:

1. [Wenn anstelle von ursprünglich 48 Ansprüchen nach der Änderung einiger Ansprüche 51 Ansprüche existieren]:
"Die Ansprüche 1 bis 29, 31, 32, 34, 35, 37 bis 48 werden durch geänderte Ansprüche gleicher Numerierung ersetzt; Ansprüche 30, 33 und 36 unverändert; neue Ansprüche 49 bis 51 hinzugefügt."

2. [Wenn anstelle von ursprünglich 15 Ansprüchen nach der Änderung aller Ansprüche 11 Ansprüche existieren]:
"Geänderte Ansprüche 1 bis 11 treten an die Stelle der Ansprüche 1 bis 15."

3. [Wenn ursprünglich 14 Ansprüche existierten und die Änderungen darin bestehen, daß einige Ansprüche gestrichen werden und neue Ansprüche hinzugefügt werden]:
Ansprüche 1 bis 6 und 14 unverändert; Ansprüche 7 bis 13 gestrichen; neue Ansprüche 15, 16 und 17 hinzugefügt."Oder" Ansprüche 7 bis 13 gestrichen; neue Ansprüche 15, 16 und 17 hinzugefügt; alle übrigen Ansprüche unverändert."

4. [Wenn verschiedene Arten von Änderungen durchgeführt werden]:
"Ansprüche 1-10 unverändert; Ansprüche 11 bis 13, 18 und 19 gestrichen; Ansprüche 14, 15 und 16 durch geänderten Anspruch 14 ersetzt; Anspruch 17 in geänderte Ansprüche 15, 16 und 17 unterteilt; neue Ansprüche 20 und 21 hinzugefügt."

"Erklärung nach Artikel 19(1)" (Regel 46.4)

Den Änderungen kann eine Erklärung beigefügt werden, mit der die Änderungen erläutert und ihre Auswirkungen auf die Beschreibung und die Zeichnungen dargelegt werden (die nicht nach Artikel 19 (1) geändert werden können).

Die Erklärung wird zusammen mit der internationalen Anmeldung und den geänderten Ansprüchen veröffentlicht.

Sie ist in der Sprache abzufassen, in der die internationale Anmeldung veröffentlicht wird.

Sie muß kurz gehalten sein und darf, wenn in englischer Sprache abgefaßt oder ins Englische übersetzt, nicht mehr als 500 Wörter umfassen

Die Erklärung ist nicht zu verwechseln mit dem Begleitschreiben, das auf die Unterschiede zwischen den Ansprüchen in der eingereichten Fassung und den geänderten Ansprüchen hinweist, und ersetzt letzteres nicht. Sie ist auf einem gesonderten Blatt einzureichen und in der Überschrift als solche zu kennzeichnen, vorzugsweise mit den Worten "Erklärung nach Artikel 19 (1)".

Die Erklärung darf keine herabsetzenden Äußerungen über den internationalen Recherchenbericht oder die Bedeutung von in dem Bericht angeführten Veröffentlichungen enthalten. Sie darf auf im internationalen Recherchenbericht angeführte Veröffentlichungen, die sich auf einen bestimmten Anspruch beziehen, nur im Zusammenhang mit einer Änderung dieses Anspruchs Bezug nehmen.

Auswirkungen eines bereits gestellten Antrags auf internationale vorläufige Prüfung

Ist zum Zeitpunkt der Einreichung von Änderungen nach Artikel 19 bereits ein Antrag auf internationale vorläufige Prüfung gestellt worden, so sollte der Anmelder in seinem Interesse gleichzeitig mit der Einreichung der Änderungen beim Internationalen Büro auch eine Kopie der Änderungen bei der mit der internationalen vorläufigen Prüfung beauftragen Behörde einreichen (siehe Regel 62.2 a), erster Satz).

Auswirkungen von Änderungen hinsichtlich der Übersetzung der internationalen Anmeldung beim Eintritt in die nationale Phase

Der Anmelder wird darauf hingewiesen, daß bei Eintritt in die nationale Phase möglicherweise anstatt oder zusätzlich zu der Übersetzung der Ansprüche in der eingereichten Fassung eine Übersetzung der nach Artikel 19 geänderten Ansprüche an die bestimmten/ausgewählten Ämter zu übermitteln ist.

Nähere Einzelheiten über die Erfordernisse jedes bestimmten/ausgewählten Amts sind Band II des PCT-Leitfadens für Anmelder zu entnehmen.

PATENT COOPERATION TREATY

From the INTERNATIONAL BUREAU

PCT

NOTIFICATION OF ELECTION

(PCT Rule 61.2)

To:

United States Patent and Trademark Office
(Box PCT)
Crystal Plaza 2
Washington, DC 20231
ÉTATS-UNIS D'AMÉRIQUE

in its capacity as elected Office

Date of mailing (day/month/year) 20 October 1998 (20.10.98)	
International application No. PCT/EP98/01187	**Applicant's or agent's file reference** TA980301PCT
International filing date (day/month/year) 03 March 1998 (03.03.98)	**Priority date** (day/month/year) 04 March 1997 (04.03.97)
Applicant TASLER, Michael	

1. The designated Office is hereby notified of its election made:

[X] in the demand filed with the International Preliminary Examining Authority on:

01 October 1998 (01.10.98)

[ ] in a notice effecting later election filed with the International Bureau on:

2. The election [X] was

[ ] was not

made before the expiration of 19 months from the priority date or, where Rule 32 applies, within the time limit under Rule 32.2(b).

The International Bureau of WIPO **34, chemin des Colombettes** **1211 Geneva 20, Switzerland**	Authorized officer Nicola Wolff
Facsimile No.: (41-22) 740.14.35	Telephone No.: (41-22) 338.83.38

Form PCT/IB/331 (July 1992) 2292582

VERTRAG ÜBER DIE INTERNATIONALE ZUSAMMENARBEIT AUF DEM GEBIET DES PATENTWESENS

Absender: MIT DER INTERNATIONALEN VORLÄUFIGEN PRÜFUNG BEAUFTRAGTE BEHÖRDE

An:

SCHOPPE, Fritz
Kanzlei Schoppe & Zimmermann
Postfach 71 08 67
D-81458 München
ALLEMAGNE

PCT

MITTEILUNG ÜBER DIE ÜBERSENDUNG DES INTERNATIONALEN VORLÄUFIGEN PRÜFUNGSBERICHTS

(Regel 71.1 PCT)

Absendedatum *(Tag/Monat/Jahr)*	11. 12. 98

Aktenzeichen des Anmelders oder Anwalts	WICHTIGE MITTEILUNG
TA980301PCT	

Internationales Aktenzeichen	Internationales Anmeldedatum *(Tag/Monat/Jahr)*	Prioritätsdatum *(Tag/Monat/Jahr)*
PCT/EP98/01187	03/03/1998	04/03/1997

Anmelder
TASLER, Michael

1. Dem Anmelder wird mitgeteilt, daß ihm die mit der internationalen vorläufigen Prüfung beauftragte Behörde hiermit den zu der internationalen Anmeldung erstellten internationalen vorläufigen Prüfungsbericht, gegebenenfalls mit den dazugehörigen Anlagen, übermittelt.

2. Eine Kopie des Berichts wird - gegebenenfalls mit den dazugehörigen Anlagen - dem Internationalen Büro zur Weiterleitung an alle ausgewählten Ämter übermittelt.

3. Auf Wunsch eines ausgewählten Amts wird das Internationale Büro eine Übersetzung des Berichts (jedoch nicht der Anlagen) ins Englische anfertigen und diesem Amt übermitteln.

4. **ERINNERUNG**

Zum Eintritt in die nationale Phase hat der Anmelder vor jedem ausgewählten Amt innerhalb von 30 Monaten ab dem Prioritätsdatum (oder in manchen Ämtern noch später) bestimmte Handlungen (Einreichung von Übersetzungen und Entrichtung nationaler Gebühren) vorzunehmen (Artikel 39 (1)) (siehe auch die durch das Internationale Büro im Formblatt PCT/IB/301 übermittelte Information).

Ist einem ausgewählten Amt eine Übersetzung der internationalen Anmeldung zu übermitteln, so muß diese Übersetzung auch Übersetzungen aller Anlagen zum internationalen vorläufigen Prüfungsbericht enthalten. Es ist Aufgabe des Anmelders, solche Übersetzungen anzufertigen und den betroffenen ausgewählten Ämtern direkt zuzuleiten.

Weitere Einzelheiten zu den maßgebenden Fristen und Erfordernissen der ausgewählten Ämter sind Band II des PCT-Leitfadens für Anmelder zu entnehmen.

Name und Postanschrift der mit der internationalen Prüfung beauftragten Behörde	Bevollmächtigter Bediensteter
Europäisches Patentamt D-80298 München Tel. (+49-89) 2399-0, Tx: 523656 epmu d Fax: (+49-89) 2399-4465	Maier, E Tel. (+49-89) 2399-2709

Formblatt PCT/IPEA/416 (Juli 1992)

VERTRAG ÜBER DIE INTERNATIONALE ZUSAMMENARBEIT AUF DEM GEBIET DES PATENTWESENS

PCT

INTERNATIONALER VORLÄUFIGER PRÜFUNGSBERICHT

(Artikel 36 und Regel 70 PCT)

Aktenzeichen des Anmelders oder Anwalts	**WEITERES VORGEHEN** siehe Mitteilung über die Übersendung des internationalen vorläufigen Prüfungsberichts (Formblatt PCT/IPEA/416)	
TA980301PCT		
Internationales Aktenzeichen	Internationales Anmeldedatum *(Tag/Monat/Jahr)*	Priority date *(Tag/Monat/Jahr)*
PCT/EP98/01187	03/03/1998	04/03/1997
Internationale Patentklassifikation (IPK) oder nationale Klassifikation und IPK		
G06F13/38		
Anmelder		
TASLER, Michael		

1. Dieser internationale vorläufige Prüfungsbericht wurde von der mit der internationalen vorläufigen Prüfung beauftragten Behörde erstellt und wird dem Anmelder gemäß Artikel 36 übermittelt.

2. Dieser BERICHT umfaßt insgesamt 5 Blätter einschließlich dieses Deckblatts.

   ☐ Außerdem liegen dem Bericht ANLAGEN bei; dabei handelt es sich um Blätter mit Beschreibungen, Ansprüchen und/oder Zeichnungen, die geändert wurden und diesem Bericht zugrunde liegen, und/oder Blätter mit vor dieser Behörde vorgenommenen Berichtigungen (siehe Regel 70.16 und Abschnitt 607 der Verwaltungsrichtlinien zum PCT).

   Diese Anlagen umfassen insgesamt Blätter.

3. Dieser Bericht enthält Angaben zu folgenden Punkten:

I	☒	Grundlage des Berichts
II	☐	Priorität
III	☐	Keine Erstellung eines Gutachtens über Neuheit, erfinderische Tätigkeit und gewerbliche Anwendbarkeit
IV	☐	Mangelnde Einheitlichkeit der Erfindung
V	☒	Begründete Feststellung nach Artikel 35(2) hinsichtlich der Neuheit, der erfinderischen Tätigkeit und der gewerblichen Anwendbarkeit; Unterlagen und Erklärungen zur Stützung dieser Feststellung
VI	☐	Bestimmte angeführte Unterlagen
VII	☐	Bestimmte Mängel der internationalen Anmeldung
VIII	☒	Bestimmte Bemerkungen zur internationalen Anmeldung

Datum der Einreichung des Antrags	Datum der Fertigstellung dieses Berichts
01/10/1998	11. 12. 98
Name und Postanschrift der mit der internationalen vorläufigen Prüfung beauftragten Behörde	Bevollmächtigter Bediensteter
Europäisches Patentamt D-80298 München Tel. (+49-89) 2399-0, Tx: 523656 epmu d Fax: (+49-89) 2399-4465	Meis, M Telefon (+49-89) 2399-2121

Formblatt PCT/IPEA/409 (Deckblatt) (Januar 1994)

I. Grundlage des Berichts

1. Dieser Bericht wurde erstellt auf der Grundlage (*Ersatzblätter, die dem Anmeldeamt auf eine Aufforderung nach Artikel 14 hin vorgelegt wurden, gelten im Rahmen dieses Berichts als "ursprünglich eingereicht" und sind ihm nicht beigefügt, weil sie keine Änderungen enthalten.*):

Beschreibung, Seiten:

1-23 ursprüngliche Fassung

Patentansprüche, Nr.:

1-16 ursprüngliche Fassung

Zeichnungen, Blätter:

1/2-2/2 ursprüngliche Fassung

2. Aufgrund der Änderungen sind folgende Unterlagen fortgefallen:

☐ Beschreibung, Seiten:
☐ Ansprüche, Nr.:
☐ Zeichnungen, Blatt:

3. ☐ Dieser Bericht ist ohne Berücksichtigung (von einigen) der Änderungen erstellt worden, da diese aus den angegebenen Gründen nach Auffassung der Behörde über den Offenbarungsgehalt in der ursprünglich eingereichten Fassung hinausgehen (Regel 70.2(c)):

4. Etwaige zusätzliche Bemerkungen:

V. Begründete Feststellung nach Artikel 35(2) hinsichtlich der Neuheit, der erfinderischen Tätigkeit und der gewerblichen Anwendbarkeit; Unterlagen und Erklärungen zur Stützung dieser Feststellung

1. Feststellung

Neuheit (N)	Ja:	Ansprüche	1-16
	Nein:	Ansprüche	
Erfinderische Tätigkeit (ET)	Ja:	Ansprüche	1-16
	Nein:	Ansprüche	
Gewerbliche Anwendbarkeit (GA)	Ja:	Ansprüche	1-16
	Nein:	Ansprüche	

2. Unterlagen und Erklärungen

siehe Beiblatt

VIII. Bestimmte Bemerkungen zur internationalen Anmeldung

Zur Klarheit der Patentansprüche, der Beschreibung und der Zeichnungen oder zu der Frage, ob die Ansprüche in vollem Umfang durch die Beschreibung gestützt werden, ist folgendes zu bemerken:

siehe Beiblatt

PUNKT V

1. Die Anmeldung bezieht sich auf eine Schnittstellen-Schnittstelle und ein Verfahren zum Betreiben einer solchen Schnittstelle.
2. Siehe die Beschreibung, S. 1 - S. 5, Ab 2 für eine Beschreibung des Standes der Technik, S. 5, Ab. 3 für die vorliegender Anmeldung zugrundeliegende Aufgabe, S. 5, letzter Ab. - S. 6 und die A. 1 und 12 (Schnittstellengerät) und 15 (Verfahren) für die Erfindung und S. 14 für den durch die Erfindung erzielten technischen Vorteil.
   Bei der Erfindung geht es darum, eine Datensende/Empfangseinrichtung über ein erfindungsgemäßes Schnittstellengerät an einer Vielzweckschnittstelle (SCSI) eines Hostgerät (Rechner) zu betreiben, wobei das Schnittstellegerät sich dem Vielzweckschnittstellentreiber (ASPI, BIOS) des Hostgerätes als Hostgerät-übliches Ein/Ausgabegerät (Festplatte) ausgibt und auch als solches mit dem Treiber kommuniziert. Der wesentliche Vorteil ist der, daß keine speziellen Treiber zum Betreiben des Schnittstellengeräts benötigt werden.
3. Die beanspruchten Schnittstellengeräte und das beanspruchte Verfahren und insbesondere eine Host-Treiber-Schnittstellen-Kombination im Sinne der Anmeldung mit darin anschließbarer Schnittstellen-Schnittstelle, sind weder bekannt, noch offensichtlich aus dem Stand der Technik wie er aus den im internationalen Recherchebericht zitierten Druckschriften hervorgeht und die Erfordernisse der Art. 33(2) und (3) PCT sind erfüllt.

   US 5 487 154 A (GUNJI KEITA) 23.Januar 1996 (Y,A) offenbart ein Signalverarbeitungssystem bei dem eine CPU über einen Adressenbus mit einem DSP, einem Speicher und einer DMA-Steuerung verbunden ist und der DSP, der Speicher und die DMA-Steuerung mit einem Datenbus, einem Ein/Ausgabegerät und, über ein Latch mit einem A/D-Wandler verbunden sind. Die CPU berechnet die Ein/Ausgabedauer des A/D-Wandlers und, falls kleiner als die Berechnungszeit des DSPs, wird DMA zur Datenübertragung vom A/D-Wandler verwendet, ansonsten findet die Datenübertragung per DSP statt.

   US 5 510 775 A (LONCLE JEAN-PIERRE) 23.April 1996 (Y) offenbart ein Verfahren zum personalisieren eines elektronischen Moduls und eine Schaltung dazu, wobei das Modul zum Betreiben an einem seriellen Fahrzeugbus ist und ebenfalls, über die dafür vorgesehene Schnittstelle personalisiert wird.

   US 5 444 644 A (DIVJAK AUGUST A) 22.August 1995 (A) offenbart ein

Datenübertragungsgerät mit, an einen Mikroprozessor angeschossenen analogen Schnittstelle welche automatisch konfigurierbar ist.

US 5 291 611 A (DAVIS ALAN J ET AL) 1.März 1994 (A) betrifft eine modulare Signalverarbeitungseinheit bei der Einzelchip-DSPs beliebig parallel und/oder seriell kombiniert werden können.

4. Die A. 2 - 11, 13 - 14 und 16 beziehen sich beziehungsweise auf spezielle Ausführungsformen der Schnittstellengeräte gemäß den A. 1 und 12 und dem Verfahren gemäß A. 15.
7. Die beanspruchten Schnittstellengeräte und das beanspruchte Verfahren sind zum Datenaustausch gewerblich anwendbar.

PUNKT VIII

1. Es ist nicht klar (Art. 6 PCT) in A. 13, welche Festplatte gemeint ist weil vorher keine Festplatte definiert wurde.

T2C

VERTRAG ÜBER DIE INTERNATIONALE ZUSAMMENARBEIT AUF DEM GEBIET DES PATENTWESENS

PCT

INTERNATIONALER VORLÄUFIGER PRÜFUNGSBERICHT

(Artikel 36 und Regel 70 PCT)

Aktenzeichen des Anmelders oder Anwalts TA980301PCT	**WEITERES VORGEHEN** siehe Mitteilung über die Übersendung des internationalen vorläufigen Prüfungsberichts (Formblatt PCT/IPEA/416)	
Internationales Aktenzeichen PCT/EP98/01187	Internationales Anmeldedatum *(Tag/Monat/Jahr)* 03/03/1998	Priority date *(Tag/Monat/Jahr)* 04/03/1997
Internationale Patentklassifikation (IPK) oder nationale Klassifikation und IPK G06F13/38		
Anmelder TASLER, Michael		

1. Dieser internationale vorläufige Prüfungsbericht wurde von der mit der internationalen vorläufigen Prüfung beauftragten Behörde erstellt und wird dem Anmelder gemäß Artikel 36 übermittelt.

2. Dieser BERICHT umfaßt insgesamt 5 Blätter einschließlich dieses Deckblatts.

   ☐ Außerdem liegen dem Bericht ANLAGEN bei; dabei handelt es sich um Blätter mit Beschreibungen, Ansprüchen und/oder Zeichnungen, die geändert wurden und diesem Bericht zugrunde liegen, und/oder Blätter mit vor dieser Behörde vorgenommenen Berichtigungen (siehe Regel 70.16 und Abschnitt 607 der Verwaltungsrichtlinien zum PCT).

   Diese Anlagen umfassen insgesamt Blätter.

3. Dieser Bericht enthält Angaben zu folgenden Punkten:

I	☒	Grundlage des Berichts
II	☐	Priorität
III	☐	Keine Erstellung eines Gutachtens über Neuheit, erfinderische Tätigkeit und gewerbliche Anwendbarkeit
IV	☐	Mangelnde Einheitlichkeit der Erfindung
V	☒	Begründete Feststellung nach Artikel 35(2) hinsichtlich der Neuheit, der erfinderischen Tätigkeit und der gewerblichen Anwendbarkeit; Unterlagen und Erklärungen zur Stützung dieser Feststellung
VI	☐	Bestimmte angeführte Unterlagen
VII	☐	Bestimmte Mängel der internationalen Anmeldung
VIII	☒	Bestimmte Bemerkungen zur internationalen Anmeldung

Datum der Einreichung des Antrags	Datum der Fertigstellung dieses Berichts
01/10/1998	11. 12. 98
Name und Postanschrift der mit der internationalen vorläufigen Prüfung beauftragten Behörde Europäisches Patentamt D-80298 München Tel. (+49-89) 2399-0, Tx: 523656 epmu d Fax: (+49-89) 2399-4465	Bevollmächtigter Bediensteter Meis, M Telefon (+49-89) 2399-2121

Formblatt PCT/IPEA/409 (Deckblatt) (Januar 1994)

INTERNATIONALER VORLÄUFIGER PRÜFUNGSBERICHT

Internationales Aktenzeichen PCT/EP98/01187

I. Grundlage des Berichts

1. Dieser Bericht wurde erstellt auf der Grundlage (*Ersatzblätter, die dem Anmeldeamt auf eine Aufforderung nach Artikel 14 hin vorgelegt wurden, gelten im Rahmen dieses Berichts als "ursprünglich eingereicht" und sind ihm nicht beigefügt, weil sie keine Änderungen enthalten.*):

Beschreibung, Seiten:

1-23 ursprüngliche Fassung

Patentansprüche, Nr.:

1-16 ursprüngliche Fassung

Zeichnungen, Blätter:

1/2-2/2 ursprüngliche Fassung

2. Aufgrund der Änderungen sind folgende Unterlagen fortgefallen:

☐ Beschreibung, Seiten:
☐ Ansprüche, Nr.:
☐ Zeichnungen, Blatt:

3. ☐ Dieser Bericht ist ohne Berücksichtigung (von einigen) der Änderungen erstellt worden, da diese aus den angegebenen Gründen nach Auffassung der Behörde über den Offenbarungsgehalt in der ursprünglich eingereichten Fassung hinausgehen (Regel 70.2(c)):

4. Etwaige zusätzliche Bemerkungen:

V. Begründete Feststellung nach Artikel 35(2) hinsichtlich der Neuheit, der erfinderischen Tätigkeit und der gewerblichen Anwendbarkeit; Unterlagen und Erklärungen zur Stützung dieser Feststellung

1. Feststellung

Neuheit (N)	Ja:	Ansprüche	1-16
	Nein:	Ansprüche	
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	Nein:	Ansprüche	
Gewerbliche Anwendbarkeit (GA)	Ja:	Ansprüche	1-16
	Nein:	Ansprüche	

2. Unterlagen und Erklärungen

siehe Beiblatt

VIII. Bestimmte Bemerkungen zur internationalen Anmeldung

Zur Klarheit der Patentansprüche, der Beschreibung und der Zeichnungen oder zu der Frage, ob die Ansprüche in vollem Umfang durch die Beschreibung gestützt werden, ist folgendes zu bemerken:

siehe Beiblatt

PUNKT V

1. Die Anmeldung bezieht sich auf eine Schnittstellen-Schnittstelle und ein Verfahren zum Betreiben einer solchen Schnittstelle.
2. Siehe die Beschreibung, S. 1 - S. 5, Ab 2 für eine Beschreibung des Standes der Technik, S. 5, Ab. 3 für die vorliegender Anmeldung zugrundeliegende Aufgabe, S. 5, letzter Ab. - S. 6 und die A. 1 und 12 (Schnittstellengerät) und 15 (Verfahren) für die Erfindung und S. 14 für den durch die Erfindung erzielten technischen Vorteil.

   Bei der Erfindung geht es darum, eine Datensende/Empfangseinrichtung über ein erfindungsgemäßes Schnittstellengerät an einer Vielzweckschnittstelle (SCSI) eines Hostgerät (Rechner) zu betreiben, wobei das Schnittstellegerät sich dem Vielzweckschnittstellentreiber (ASPI, BIOS) des Hostgerätes als Hostgerät-übliches Ein/Ausgabegerät (Festplatte) ausgibt und auch als solches mit dem Treiber kommuniziert. Der wesentliche Vorteil ist der, daß keine speziellen Treiber zum Betreiben des Schnittstellengeräts benötigt werden.
3. Die beanspruchten Schnittstellengeräte und das beanspruchte Verfahren und insbesondere eine Host-Treiber-Schnittstellen-Kombination im Sinne der Anmeldung mit darin anschließbarer Schnittstellen-Schnittstelle, sind weder bekannt, noch offensichtlich aus dem Stand der Technik wie er aus den im internationalen Recherchebericht zitierten Druckschriften hervorgeht und die Erfordernisse der Art. 33(2) und (3) PCT sind erfüllt.

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   US 5 444 644 A (DIVJAK AUGUST A) 22.August 1995 (A) offenbart ein

Datenübertragungsgerät mit, an einen Mikroprozessor angeschossenen analogen Schnittstelle welche automatisch konfigurierbar ist.

US 5 291 611 A (DAVIS ALAN J ET AL) 1.März 1994 (A) betrifft eine modulare Signalverarbeitungseinheit bei der Einzelchip-DSPs beliebig parallel und/oder seriell kombiniert werden können.

4. Die A. 2 - 11, 13 - 14 und 16 beziehen sich beziehungsweise auf spezielle Ausführungsformen der Schnittstellengeräte gemäß den A. 1 und 12 und dem Verfahren gemäß A. 15.

7. Die beanspruchten Schnittstellengeräte und das beanspruchte Verfahren sind zum Datenaustausch gewerblich anwendbar.

PUNKT VIII

1. Es ist nicht klar (Art. 6 PCT) in A. 13, welche Festplatte gemeint ist weil vorher keine Festplatte definiert wurde.

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PATENT COOPERATION TREATY

PCT

INTERNATIONAL PRELIMINARY EXAMINATION REPORT

(PCT Article 36 and Rule 70)

Applicant's or agent's file reference TA980301PCT	FOR FURTHER ACTION See Notification of Transmittal of International Preliminary Examination Report (Form PCT/IPEA/416)	
International application No. PCT/EP98/01187	International filing date (*day/month/year*) 03 March 1998 (03.03.1998)	Priority date (*day/month/year*) 04 March 1997 (04.03.1997)
International Patent Classification (IPC) or national classification and IPC G06F 13/38		
Applicant TASLER, Michael		

1. This international preliminary examination report has been prepared by this International Preliminary Examining Authority and is transmitted to the applicant according to Article 36.

2. This REPORT consists of a total of 5 sheets, including this cover sheet.

☐ This report is also accompanied by ANNEXES, i.e., sheets of the description, claims and/or drawings which have been amended and are the basis for this report and/or sheets containing rectifications made before this Authority (see Rule 70.16 and Section 607 of the Administrative Instructions under the PCT).

These annexes consist of a total of _____ sheets.

3. This report contains indications relating to the following items:

- I ☒ Basis of the report
- II ☐ Priority
- III ☐ Non-establishment of opinion with regard to novelty, inventive step and industrial applicability
- IV ☐ Lack of unity of invention
- V ☒ Reasoned statement under Article 35(2) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement
- VI ☐ Certain documents cited
- VII ☐ Certain defects in the international application
- VIII ☒ Certain observations on the international application

Date of submission of the demand	Date of completion of this report
01 October 1998 (01.10.1998)	11 December 1998 (11.12.1998)
Name and mailing address of the IPEA/EP European Patent Office D-80298 Munich, Germany Facsimile No. 49-89-2399-4465	Authorized officer Telephone No. 49-89-2399-0

Form PCT/IPEA/409 (cover sheet) (January 1994)

INTERNATIONAL PRELIMINARY EXAMINATION REPORT

International application No.
PCT/EP98/01187

I. Basis of the report

1. This report has been drawn on the basis of (*Replacement sheets which have been furnished to the receiving Office in response to an invitation under Article 14 are referred to in this report as "originally filed" and are not annexed to the report since they do not contain amendments.*):

☐ the international application as originally filed.

☒ the description, pages 1-23, as originally filed,
pages _____, filed with the demand,
pages _____, filed with the letter of _____,
pages _____, filed with the letter of _____.

☒ the claims, Nos. 1-16, as originally filed,
Nos. _____, as amended under Article 19,
Nos. _____, filed with the demand,
Nos. _____, filed with the letter of _____,
Nos. _____, filed with the letter of _____.

☒ the drawings, sheets/fig 1/2-2/2, as originally filed,
sheets/fig _____, filed with the demand,
sheets/fig _____, filed with the letter of _____,
sheets/fig _____, filed with the letter of _____.

2. The amendments have resulted in the cancellation of:

☐ the description, pages _____
☐ the claims, Nos. _____
☐ the drawings, sheets/fig _____

3. ☐ This report has been established as if (some of) the amendments had not been made, since they have been considered to go beyond the disclosure as filed, as indicated in the Supplemental Box (Rule 70.2(c)).

4. Additional observations, if necessary:

Form PCT/IPEA/409 (Box I) (January 1994)

INTERNATIONAL PRELIMINARY EXAMINATION REPORT

International application No.
PCT/EP 98/01187

V. Reasoned statement under Article 35(2) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement

1. Statement

Novelty (N)	Claims	1 - 16	**YES**
	Claims		**NO**
Inventive step (IS)	Claims	1 - 16	**YES**
	Claims		**NO**
Industrial applicability (IA)	Claims	1 - 16	**YES**
	Claims		**NO**

2. Citations and explanations

1. The application pertains to an input-output interface and a process for operating the same.
2. See the description, page 1 - page 5, second paragraph, for a description of the prior art, page 5, third paragraph, for the problem addressed by the present application, page 5, last paragraph - page 6 and Claims 1 and 12 (interface device) and 15 (process) for the invention and page 14 for the technical advantage achieved through the invention. The object of the invention is to operate a data transceiver via an interface device as per the invention at a multipurpose interface (SCSI) of a host device (computer), the interface device behaving towards the multipurpose interface driver (ASPI, BIOS) of the host device as a conventional host device input/output device (hard disk) and also communicating as such with the driver. The principal advantage is that no special drivers are required for operating the interface device.
3. The claimed interface devices and the claimed process and, in particular, a host-driver-interface combination within the meaning of the application with an input-output interface connectable therein are neither known nor obvious from the prior art

.../...

(Continuation of V.2)

disclosed in the documents cited in the international search report, and the requirements of PCT Article 33(2) and (3) are satisfied.

US-A-5 487 154 (GUNJI KEITA) 23 January 1996 (Y,A) discloses a signal-processing system in which a CPU is connected via an address bus to a DSP, a memory and a DMA control system, and the DSP, the memory and the DMA control system are connected via a data bus to an input/output device and via a latch to an A/D converter. The CPU calculates the duration of input/output of the A/D converter and, if this duration is less than the calculation time of the DSP, DMA is used to transmit data from the A/D converter; otherwise the data are transmitted by the DSP.

US-A-5 510 775 (LONCLE JEAN-PIERRE) 23 April 1996 (Y) discloses a process for personalizing an electronic module and a circuit therefor, the module is designed to operate on a serial vehicle bus and is likewise personalized via the interface provided therefor.

US-A-5 444 644 (DIVJAK AUGUST A) 22 August 1995 (A) discloses a data-transfer device with an analog interface which is connected to a microprocessor and which can be automatically configured.

US-A-5 291 611 (DAVIS ALAN J ET AL) 1 March 1994 (A) pertains to a modular signal-processing unit in which the single-chip DSPs can be combined in parallel and/or in series, as desired.

4. Claims 2 - 11, 13 and 14 and 16 pertain respectively to particular embodiments of the interface devices according to Claims 1 and 12 and of the process according to Claim 15.

5. The claimed interface devices and the claimed process are industrially applicable for data exchange.

VIII. Certain observations on the international application

The following observations on the clarity of the claims, description, and drawings or on the question whether the claims are fully supported by the description, are made:

1. It is not clear (PCT Article 6) in Claim 13 which hard disk is meant, because no hard disk has been defined beforehand.

BUNDESREPUBLIK DEUTSCHLAND

Bescheinigung

Herr Michael T a s l e r in Goldbach/Deutschland hat eine Patentanmeldung unter der Bezeichnung

"Flexible Schnittstelle"

am 4. März 1997 beim Deutschen Patentamt eingereicht.

Die angehefteten Stücke sind eine richtige und genaue Wiedergabe der ursprünglichen Unterlagen dieser Patentanmeldung.

Die Anmeldung hat im Deutschen Patentamt vorläufig das Symbol G 06 F 13/12 der Internationalen Patentklassifikation erhalten.

München, den 19. März 1998
Der Präsident des Deutschen Patentamts
Im Auftrag

Wehner

enzeichen: 197 08 755.8

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(EVA-L)
04/94

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Flexible Schnittstelle

Flexible Schnittstelle

Beschreibung

Die vorliegende Erfindung bezieht sich auf die Übertragung von Daten und insbesondere auf Schnittstellengeräte zur Kommunikation zwischen einem Computer oder Hostgerät und einer Datensende/Empfangseinrichtung, von der Daten erfaßt werden sollen, bzw. mit der kommuniziert werden soll.

Bisherige Datenerfassungssysteme für Computer sind sehr stark in ihrem Einsatzbereich limitiert. Allgemein können dieselben in zwei Gruppen eingeteilt werden.

Bei der ersten Gruppe werden Hostgeräte oder Computersysteme mittels einer Schnittstelle mit einem Gerät verbunden, dessen Daten erfaßt werden sollen. Die Schnittstellen dieser Gruppe sind üblicherweise Standardschnittstellen, die mit spezieller Treibersoftware für verschiedene Hostsysteme einsetzbar sind. Ein Vorteil dieser Schnittstellengeräte besteht darin, daß sie vom Hostgerät weitgehend unabhängig sind. Nachteilig ist jedoch, daß sie im allgemeinen sehr aufwendige Treiber benötigen, die störungsanfällig sind und die Datenübertragungsraten zwischen dem mit der Schnittstelle verbundenen Gerät und dem Hostgerät und umgekehrt limitieren. Ferner sind Implementationen dieser Schnittstellen für tragbare Systeme teilweise nur schwer möglich und die Anpassungsmöglichkeiten sind gering, weshalb diese Systeme eine geringe Flexibilität besitzen.

Die Geräte, von denen Daten zu erfassen sind, besetzen die ganze Bandbreite der Elektrotechnik. So ist bei einem typischen Szenario davon auszugehen, daß ein Kunde, der beispielsweise im medizintechnischen Bereich eine Röntgendiagnoseanlage betreibt, über einen Fehler berichtet. Ein Servicemitarbeiter des Geräteherstellers wird dann zu dem Kunden gehen und von dem Röntgendiagnosegerät erstellte

Systemprotokolldateien beispielsweise mittels eines tragbaren Computer oder Laptops auslesen. Wenn der Fehler dann nicht zu lokalisieren ist, oder wenn ein Fehler nur sporadisch auftritt, wird es erforderlich sein, daß der Servicemitarbeiter nicht nur eine Fehlerprotokolldatei sondern auch Daten aus dem laufenden Betrieb auslesen muß. Es ist offensichtlich, daß hier eine schnelle Datenübertragung sowie eine schnelle Datenanalyse notwendig ist.

Ein anderer Fall zum Einsatz einer Schnittstelle kann beispielsweise das Verbinden eines elektronischen Meßgeräts, z. B. eines Multimeters, mit einem Computersystem sein, um von dem Multimeter gemessene Daten auf den Computer zu übertragen. Insbesondere bei Langzeitmessungen oder beim Auftreten großer Datenmengen ist es erforderlich, daß die Schnittstelle eine hohe Datenübertragungsrate ermöglicht.

Aus diesen zufällig gewählten Beispielen ist zu sehen, daß die Einsatzmöglichkeiten einer Schnittstelle völlig voneinander unterschiedlich sein können. Es ist daher wünschenswert, daß eine Schnittstelle derart flexibel ist, daß mittels einer Schnittstelle sehr unterschiedliche elektrische oder elektronische Systeme mit einem Hostgerät verbunden werden können. Um Fehlbedienungen zu vermeiden, ist es ferner wünschenswert, daß ein Servicemitarbeiter nicht für jede unterschiedliche Anwendung unterschiedliche Schnittstellen auf unterschiedliche Art und Weise bedienen muß, sondern daß möglichst eine universelle Schnittstellenbedienung für eine große Anzahl von Einsatzmöglichkeiten geschaffen wird.

Um die Datenübertragungsraten über eine Schnittstelle zu erhöhen, wurde bei der zweiten Gruppe von Schnittstellengeräten der Weg beschritten, die Schnittstelle sehr stark an individuelle Hostsysteme oder Computersysteme einzeln anzupassen. Der Vorteil dieser Lösung besteht darin, daß hohe Transferraten möglich sind. Ein Nachteil ist jedoch, daß die Treiber für die Schnittstellen der zweiten Gruppe sehr stark

an ein einziges Hostsystem angepaßt sind, weshalb sie im allgemeinen nicht oder nur sehr uneffektiv für andere Hostsysteme einsetzbar sind. Ferner weisen diese Typen von Schnittstellen den Nachteil auf, daß sie im Computergehäuse montiert werden müssen, da sie auf das interne Hostbussystem zugreifen, um maximale Datenübertragungsraten zu erreichen. Sie sind daher im allgemeinen nicht für tragbare Hostsysteme in Form von Laptops geeignet, die aufgrund ihrer möglichst geringen Größe kein freies Innenvolumen zum Einstecken einer Schnittstellenkarte besitzen.

Eine Lösung für dieses Problem bieten Schnittstellengeräte der Firma IOtech (Geschäftsadresse: 25971 Cannon Road, Cleveland, Ohio 44146, USA), die für Laptops geeignet sind, wie z. B. das Modell WaveBook/512 (eingetragenens Warenzeichen). Die Schnittstellengeräte werden mittels einer steckbaren, etwa scheckkartengroßen Einsteckkarte mit der PCMCIA-Schnittstelle, die mittlerweile an Laptops standardmäßig vorgesehen sind, verbunden. Die Einsteckkarte bewirkt eine Transformation der PCMCIA-Schnittstelle zu einer in der Technik bekannten Schnittstelle IEEE 1284. Die genannte Steckkarte schafft eine bezüglich der Datenrate erweiterte Spezial-Druckerschnittstelle, die eine Datenübertragungsrate von etwa 2 MB/s im Gegensatz zu einer Rate von etwa 1MB/s bei bekannten Druckerschnittstellen liefert. Das bekannte Schnittstellengerät besteht im allgemeinen aus einem Treiberbaustein, einem digitalen Signalprozessor, einem Puffer und einer Hardwarebaugruppe, die in einem Verbinder mündet, an dem das Gerät angeschlossen wird, dessen Daten zu erfassen sind. Der Treiberbaustein ist direkt mit der erweiterten Druckerschnittstelle verbunden, wodurch die bekannte Schnittstelleneinrichtung eine Verbindung zwischen einem Computer und dem Gerät herstellt, dessen Daten erfaßt werden sollen.

Um mit der genannten Schnittstelle zu arbeiten, muß ein schnittstellenspezifischer Treiber in dem Hostgerät installiert werden, damit das Hostgerät mit dem digitalen

Signalprozessor der Schnittstellenkarte kommunizieren kann. Wie es bereits erwähnt wurde, muß der Treiber auf dem Hostgerät installiert werden. Ist der Treiber ein speziell für das Hostgerät entworfener Treiber, so wird zwar eine schnelle Datenübertragung ermöglicht, der Treiber kann jedoch nicht ohne weiteres auf einem anderen Hostsystem installiert werden. Ist der Treiber jedoch ein möglichst flexibler allgemeiner Treiber, der für viele Hostgeräte einsetzbar ist, dann müssen Kompromisse bezüglich der Datenübertragungsrate in Kauf genommen werden.

Speziell bei einer Anwendung für Multi-Tasking-Systeme, bei denen mehrere verschiedene Aufgaben, wie z. B. eine Datenerfassung, eine Datendarstellung oder ein Editieren im wesentlichen gleichzeitig zu bearbeiten sind, wird üblicherweise jeder Aufgabe vom Hostsystem eine gewisse Priorität zugeordnet. Ein Treiber, der eine spezielle Aufgabe unterstützt, fragt im zentralen Verarbeitungssystem des Hostgeräts an, ob er Prozessorresourcen haben kann, um seine Aufgabe zu erledigen. Abhängig vom jeweiligen Prioritätszuweisungsverfahren und abhängig von der Implementation des Treibers wird eine spezielle Aufgabe einen bestimmten Anteil der Prozessorresourcen in bestimmten Zeitschlitzen erhalten. Konflikte ergeben sich dann, wenn einer oder mehrere Treiber derart implementiert sind, daß sie standardmäßig die höchste Priorität haben, d. h. daß sie inkompatibel sind, wie es bei vielen Anwendungen in der Praxis der Fall ist. So kann es vorkommen, daß beide Treiber eingestellt sind, um die höchste Priorität zu haben, was im schlimmsten Fall sogar zu einem Systemabsturz führen kann.

Die Aufgabe der vorliegenden Erfindung besteht darin, ein Schnittstellengerät zur Kommunikation zwischen einem Hostgerät und einer Datensende/Empfangseinrichtung zu schaffen, das unabhängig vom Hostgerät einsetzbar ist und eine hohe Datenübertragungsrate ermöglicht.

Diese Aufgabe wird durch ein Schnittstellengerät gemäß An-

spruch 1 sowie durch ein Verfahren gemäß Anspruch 12 gelöst.

Der vorliegenden Erfindung liegt die Erkenntnis zugrunde, daß sowohl eine hohe Datenübertragungsrate als auch eine vom Hostgerät unabhängige Einsetzbarkeit erreicht werden können, wenn auf eine Eingabe/Ausgabe-Schnittstelle des Hostgeräts zurückgegriffen wird, die üblicherweise in den allaermeisten auf dem Markt verfügbaren Hostgeräten vorhanden ist. Eingabe/Ausgabe-Schnittstellen, die praktisch in jedem Hostgerät vorhanden sind, sind beispielsweise Festplattenschnittstellen, Graphikschnittstellen oder Druckerschnittstellen. Da jedoch die Festplattenschnittstellen bei den üblichen Hostgeräten, die beispielsweise IBM-PCs, IBM-kompatible-PCs, Commodore-PCs, Apple-Computer oder auch Workstations sein können, die Schnittstellen mit der schnellsten Datenübertragungsrate sind, wird bei dem bevorzugten Ausführungsbeispiel des Schnittstellengeräts der vorliegenden Erfindung auf die Festplattenschnittstelle zurückgegriffen. Auf andere Speicherschnittstellen, wie z. B. Diskettenlaufwerke, CD-ROM-Laufwerke oder Bandlaufwerke, könnte jedoch ebenfalls zurückgegriffen werden, um das Schnittstellengerät gemäß der vorliegenden Erfindung zu implementieren.

Das Schnittstellengerät gemäß der vorliegenden Erfindung umfaßt eine Prozessoreinrichtung, eine Speichereinrichtung, eine erste Verbindungseinrichtung zum schnittstellenmäßigen Verbinden des Hostgeräts mit dem Schnittstellengerät und eine zweite Verbindungseinrichtung zum schnittstellenmäßigen Verbinden des Schnittstellengeräts mit der Datensende/Empfangseinrichtung. Das Schnittstellengerät wird durch die Prozessoreinrichtung und die Speichereinrichtung derart konfiguriert, daß das Schnittstellengerät bei einer Anfrage des Hostgeräts über die erste Verbindungseinrichtung, die die Art eines Geräts betrifft, das mit dem Hostgerät verbunden ist, unabhängig von dem Typ der Datensende/Empfangseinrichtung ein Signal über die erste Verbindungseinrichtung zum Hostgerät sendet, das dem Hostgerät signalisiert, daß es mit einem Eingabe/Ausgabe-Gerät kommuniziert. Das Schnitt-

stellensystem gemäß der vorliegenden Erfindung simuliert somit sowohl hardware- als aus auch softwaretechnisch die Funktionsweise eines üblichen Eingabe/Ausgabe-Geräts und vorzugsweise eines Festplattenlaufwerks. Da die Unterstützung von Festplatten in allen verfügbaren Hostsystemen standardmäßig implementiert ist, kann beispielsweise die Simulation einer Festplatte die Unabhängigkeit vom verwendeten Hostsystem erreichen. Das erfindungsgemäße Schnittstellengerät kommuniziert somit mit dem Hostgerät oder Computer nicht mehr über einen speziell entworfenen Treiber sondern über einen in dem BIOS-System (BIOS = Basic Input/Output System = Grund Eingabe/Ausgabe System) vorhandenes Programm, das üblicherweise genau auf das spezielle Computersystem abgestimmt ist, auf dem es installiert ist. Somit vereinigt das Schnittstellengerät gemäß der vorliegenden Erfindung die Vorteile beider Gruppen. Zum einen findet die Datenkommunikation zwischen dem Computer und der Schnittstelle über ein Hostgerät-spezifisches BIOS-Programm statt, das als "gerätespezifischer Treiber" angesehen werden könnte. Zum anderen ist das BIOS-Programm, das eine der üblichen Eingabe/Ausgabe-Schnittstellen in Hostsystemen bedient, in eben jedem Hostsystem vorhanden, weshalb das Schnittstellengerät gemäß der vorliegenden Erfindung Hostgerät-unabhängig ist.

Bevorzugte Ausführungsbeispiele der vorliegenden Erfindung werden nachfolgend bezugnehmend auf die beiliegenden Zeichnungen detaillierter erläutert. Es zeigen:

Fig. 1 ein prinzipielles Blockschaltbild des Schnittstellengeräts gemäß der vorliegenden Erfindung; und

Fig. 2 ein detailliertes Blockschaltbild eines Schnittstellengeräts gemäß einem bevorzugten Ausführungsbeispiel der vorliegenden Erfindung.

Fig. 1 zeigt ein prinzipielles Blockschaltbild eines Schnittstellengeräts 10 gemäß der vorliegenden Erfindung.

Über eine Hostleitung 11 ist eine erste Verbindungseinrichtung 12 des Schnittstellengeräts 10 mit einem Hostgerät (nicht gezeigt) verbindbar. Die erste Verbindungseinrichtung ist sowohl an einen digitalen Signalprozessor 13 als auch an einen Speicher 14 angeschlossen. Der digitale Signalprozessor 13 sowie der Speicher 14 sind ferner mittels bidirektionaler Kommunikationsleitungen (bei allen Leitungen durch zwei Richtungspfeile angezeigt) mit einer zweiten Verbindungseinrichtung 15 gekoppelt. Mittels einer Ausgangsleitung 16 kann die zweite Verbindungseinrichtung mit einer Sende/Empfangseinrichtung gekoppelt werden, die Daten von dem Hostgerät empfangen soll oder von der Daten ausgelesen, d. h. erfaßt, und zu dem Hostgerät übertragen werden sollen.

Die Kommunikation mit dem Hostsystem oder Hostgerät basiert auf bekannten Standard-Zugriffsbefehlen, wie sie von allen bekannten Betriebssystemen (z. B. DOS, Windows, Unix) unterstützt werden. Vorzugsweise simuliert das Schnittstellengerät gemäß der vorliegenden Erfindung eine Festplatte mit einem Wurzelverzeichnis oder "Root-Directory", dessen Einträge "virtuelle" Dateien sind, die für verschiedenste Funktionen angelegt werden können. Wenn das Hostgerätsystem, mit dem das Schnittstellengerät gemäß der vorliegenden Erfindung verbunden ist, wobei mit dem Schnittstellengerät 10 ferner eine Sende/Empfangseinrichtung verbunden ist, hochgefahren wird, geben übliche BIOS-Routinen an jede in dem Hostgerät vorhandene Eingabe/Ausgabe-Schnittstelle einen Befehl aus, der in der Fachwelt als Befehl "INQUIRY" ("Erkundigung") bekannt ist. Über die erste Verbindungseinrichtung wird der digitale Signalprozessor 13 diese Anfrage empfangen und ein Signal erzeugen, das wiederum über die erste Verbindungseinrichtung 12 und die Hostleitung 11 zum Hostgerät (nicht gezeigt) gesendet wird. Dieses Signal wird dem Hostgerät signalisieren, daß an der betreffenden Schnittstelle, zu der der Befehl INQUIRY gesendet wurde, ein Festplattenlaufwerk angeschlossen ist. Optional kann das Hostgerät einen für Fachleute bekannten Befehl "Test Unit Ready" zum Schnittstellengerät senden, der genauere Details bezüglich des

angefragten Geräts wünscht.

Unabhängig davon, welche Sende/Empfangseinrichtung an der Ausgangsleitung 16 mit der zweiten Verbindungseinrichtung verbunden ist, teilt der digitale Signalprozessor 13 dem Hostgerät mit, daß das Hostgerät mit einem Festplattenlaufwerk kommuniziert. Empfängt das Hostgerät die Antwort, daß ein Laufwerk vorhanden ist, wird es nun die Aufforderung zum Schnittstellengerät 10 schicken, die Boot-Sequenz, die sich üblicherweise bei tatsächlichen Festplatten auf den ersten Sektoren derselben befindet, zu lesen. Der digitale Signalprozessor 13, dessen Betriebssystem in der Speichereinrichtung 14 gespeichert ist, wird diesen Befehl beantworten, indem er eine virtuelle Boot-Sequenz zum Hostgerät sendet, die bei tatsächlichen Laufwerken den Typ, die Startposition und die Länge der FAT (FAT = File Allocation Table = Dateipositionstabelle), die Anzahl der Sektoren, usw. enthält, wie es für Fachleute bekannt ist. Wenn das Hostgerät diese Daten empfangen hat, geht es davon aus, daß das Schnittstellengerät 10 gemäß einem bevorzugten Ausführungsbeispiel der vorliegenden Erfindung ein Festplattenlaufwerk ist. Auf einen Befehl vom Hostgerät, das Verzeichnis des "virtuellen" Festplattenlaufwerks, das von der Schnittstelleneinrichtung 10 dem Hostgerät gegenüber simuliert wird, anzuzeigen, kann der digitale Signalprozessor dem Hostgerät genauso antworten, wie es eine herkömmliche Festplatte tun würde, nämlich indem die Dateipositionstabelle oder FAT auf einem in der Bootsequenz bestimmten Sektor, der im allgemeinen der erste beschreibbare Sektor ist, gelesen wird und zum Hostgerät übertragen wird. Es ist ferner möglich, daß die FAT erst direkt vor dem Lesen oder Speichern von Daten der "virtuellen" Festplatte gelesen wird und nicht bereits beim Initialisieren.

Bei einem bevorzugten Ausführungsbeispiel der vorliegenden Erfindung umfaßt der digitale Signalprozessor 13, der nicht unbedingt als digitaler Signalprozessor sondern auch als beliebiger anderer Mikroprozessor ausgeführt sein kann,

einen ersten und einen zweiten Befehlsinterpretierer. Der erste Befehlsinterpretierer führt die gerade genannten Schritte durch, während der zweite Befehlsinterpretierer die Lese/Schreib-Zuordnung zu bestimmten Funktionen durchführt. Besteht nun der Wunsch des Benutzers, von der Sende/Empfangseinrichtung über die Leitung 16 Daten zu lesen, so schickt das Hostgerät einen Befehl zur Schnittstelleneinrichtung, der beispielsweise "Lese Datei xy" lauten könnte. Wie es bereits erwähnt wurde, erscheint die Schnittstelleneinrichtung dem Hostgerät gegenüber wie eine Festplatte. Die zweite Interpretiereinrichtung des digitalen Signalprozessors interpretiert nun den Lesen-Befehl des Hostprozessors durch Entschlüsseln, ob "xy" beispielsweise eine Datei "Echtzeiteingabe", "Konfiguration" oder eine ausführbare Datei bezeichnet, als Datenübertragungsbefehl, wodurch derselbe beginnt, von der Sende/Empfangseinrichtung über die zweite Verbindungseinrichtung Daten zur ersten Verbindungseinrichtung und über die Leitung 11 zum Hostgerät zu übertragen.

Vorzugsweise wird in einer nachfolgend beschriebenen Konfigurationsdatei die Menge von von einer Datensende/Empfangseinrichtung zu erfassenden Daten angegeben, indem der Benutzer in der Konfigurationsdatei angibt, daß sich eine Messung z. B. über fünf Minuten erstrecken soll. Für das Hostgerät wird dann die Datei "Echtzeiteingabe" wie eine Datei erscheinen, deren Länge der in den fünf Minuten erwarteten Datenmenge entspricht. Für Fachleute ist es bekannt, daß die Kommunikation zwischen einem Prozessor und einer Festplatte darin besteht, daß der Prozessor der Festplatte Nummern von Blöcken oder Clustern oder Sektoren übermittelt, deren Inhalt er lesen möchte. Aus der FAT weiß der Prozessor, welche Informationen in welchem Block stehen. Die Kommunikation von dem Hostgerät zu dem Schnittstellengerät der vorliegenden Erfindung besteht also bei diesem Szenario in der sehr schnellen Übertragung von Blocknummern und vorzugsweise von Blocknummernbereichen, da eine "virtuelle" Datei "Echtzeiteingabe" nicht fragmentiert sein wird. Will nun das Hostge-

rät die Datei "Echtzeiteingabe" lesen, so übermittel es einen Bereich von Blocknummern zur Schnittstelleneinrichtung, woraufhin damit begonnen wird, daß über die zweite Verbindungseinrichtung Daten empfangen und über die erste Verbindungseinrichtung zu dem Hostgerät gesendet werden.

Die Speichereinrichtung 14 kann neben dem Befehlsspeicher für den digitalen Signalprozessor, der das Betriebssystem desselben umfaßt und als EPROM oder EEPROM ausgeführt sein kann, einen zusätzlichen Puffer aufweisen, der zu Synchronisationszwecken zwischen der Datenübertragung von der Sende/Empfangseinrichtung zur Schnittstelleneinrichtung 10 und der Datenübertragung von der Schnittstelleneinrichtung 10 zum Hostgerät dient.

Vorzugsweise ist der Puffer als schneller Direktzugriffsspeicher oder RAM-Puffer ausgeführt.

Der Benutzer kann ferner vom Hostgerät aus auf der Schnittstelleneinrichtung 10, die dem Hostgerät gegenüber wie eine Festplatte erscheint, eine Konfigurationsdatei erstellen, deren Einträge automatisch verschiedene Funktionen des Schnittstellengeräts 10 einstellen und steuern. Dies können beispielsweise Verstärkungs-, Multiplex- oder Abtastrateneinstellungen sein. Durch das Erstellen und Editieren einer Konfigurationsdatei, welche üblicherweise eine Textdatei ist, die ohne große Vorkenntnis einfach verständlich ist, kann der Benutzer der Schnittstelleneinrichtung 10 für nahezu beliebiege Sende/Empfangseinrichtungen, die über die Leitung 16 mit der zweiten Verbindungseinrichtung koppelbar sind, die im wesentlichen gleichen Bedienhandlungen durchführen, wodurch eine Fehlerquelle beseitigt wird, die daraus entsteht, daß ein Benutzer für verschiedene Anwendungen viele verschiedene Befehlcodes kennen muß. Bei der Schnittstelleneinrichtung 10 gemäß der vorliegenden Erfindung ist es lediglich notwendig, daß der Benutzer einmal die Konventionen der Konfigurationsdatei notiert, wonach er die Schnittstelleneinrichtung 10 als Schnittstelle zwischen einem

Hostgerät und einem nahezu beliebigen Sende/Empfangsgerät verwenden kann.

Durch die Möglichkeit, beliebige Dateien in vereinbarten Formaten unter Berücksichtigung der maximalen Speicherkapazität der Speichereinrichtung auf der Schnittstelleneinrichtung 10 in der Speichereinrichtung 14 abzuspeichern, sind beliebige Erweiterungen oder sogar gänzlich neue Funktionen der Schnittstelleneinrichtung 10 ohne Zeitverlust zu realisieren. Selbst vom Hostgerät ausführbare Dateien, wie z. B. Stapeldateien oder ausführbare Dateien (BAT-Dateien oder EXE-Dateien) oder auch Hilfedateien können in der Schnittstelleneinrichtung implementiert werden und somit die Unabhängikeit der Schnittstelleneinrichtung 10 von jeglicher zusätzlicher Software (abgesehen von den BIOS-Routinen) des Hostgeräts erreichen. Dies vermeidet zum einen Lizenz- bzw. Anmeldungsprobleme. Zum anderen werden Installationen von bestimmten Routinen, die oft verwendet werden können, wie z. B. eine FFT-Routine, um beispielsweise erfaßte Zeitbereichsdaten im Frequenzbereich betrachten zu können, hinfällig, da diese EXE-Dateien bereits auf der Schnittstelleneinrichtung 10 installiert sind und in dem virtuellen Wurzel-Verzeichnis erscheinen, durch das das Hostgerät auf alle beliebigen auf der Schnittstelleneinrichtung 10 gespeicherten Programme zugreifen kann.

Bei einem bevorzugten Ausführungsbeispiel der vorliegenden Erfindung, bei dem die Schnittstelleneinrichtung 10 dem Hostgerät gegenüber ein Festplattenlaufwerk simuliert, wird dieselbe bereits beim Einschalten oder Hochfahren des Hostsystems automatisch erkannt und zum Betrieb bereitgestellt. Dies entspricht dem derzeit immer weiter verbreiteten "Plug-and-Play"-Standard. Der Benutzer muß sich nicht mehr um die Installation der Schnittstelleneinrichtung 10 auf dem Hostgerät durch spezielle zu ladende Treiber kümmern, sondern die Schnittstelleneinrichtung 10 wird beim Hochfahren des Hostsystems automatisch zum Betrieb bereitgestellt.

Für Fachleute ist es jedoch offensichtlich, daß die Schnittstelleneinrichtung 10 nicht notwendigerweise beim Einschalten des Rechners angemeldet wird, sondern daß auf dem Hostgerät auch eine spezielle BIOS-Routine während des Laufs des Rechners gestartet werden kann, um die Schnittstelleneinrichtung 10 als zusätzliche Festplatte anzubinden oder zu "mounten". Dieses Ausführungsbeispiel ist für größere Workstation-Systeme geeignet sein, welche im wesentlichen nie ausgeschaltet werden, da sie beispielsweise in einem "Multi-Tasking"-Environment z. B. Mail-Funktionen oder Prozeßüberwachungen, die ständig im Betrieb sind, durchführen werden.

Bei dem Schnittstellengerät gemäß der vorliegenden Erfindung besteht ein enormer Vorteil der Trennung der tatsächlichen Hardware, die zur Verbindung der Schnittstelleneinrichtung 10 mit der Sende/Empfangseinrichtung benötigt wird, wie es aus dem nachfolgend beschriebenen Ausführungsbeispiel offensichtlich ist, von der Kommunikations-Einheit, die durch den digitalen Signalprozessor 13, den Speicher 14 und die erste Verbindungseinrichtung 12 implementiert ist, darin, daß verschiedenste Gerätetypen parallel auf identische Weise bedient werden können. An ein Hostgerät können demnach viele Schnittstelleneinrichtungen 10 angeschlossen werden, dasselbe wird dann verschiedenste sozusagen "virtuelle" Festplatten sehen. Zum anderen ist auch eine eventuelle Änderung der speziellen Hardware, die durch die zweite Verbindungseinrichtung 15 symbolisiert ist, im wesentlichen ohne Veränderung der Bedienung der Schnittstellengeräts gemäß der vorliegenden Erfindung realisierbar. Ferner kann ein erfahrener Anwender jederzeit beliebig tief in die vorhandene zweite Verbindungseinrichtung eingreifen, indem er die oben erwähnte Option des Erstellens einer Konfigurationsdatei oder des Hinzufügens oder Abspeicherns neuer Programmteile für die zweite Verbindungseinrichtung verwendet.

Ein wesentlicher Vorteil der Schnittstelleneinrichtung 10 der vorliegenden Erfindung besteht ferner darin, daß sie

extrem hohe Datenübertragungsraten ermöglicht, und zwar bereits dadurch, daß die Hostgerät-eigenen BIOS-Routinen, die vom Hersteller des Hostgeräts bzw. BIOS-Systems für jedes Hostgerät optimiert sind, zum Datenaustausch verwendet werden. Außerdem werden die Daten aufgrund der Simulation eines virtuellen Massenspeichers so verwaltet und zur Verfügung gestellt, daß sie direkt gewissermaßen ohne Prozessorintervention des Hostgeräts auf andere Speichermedien, z. B. eine tatsächliche Festplatte des Hostgeräts, übertragen werden können. Die einzige Begrenzung für eine Langzeit-Datenübertragung mit hoher Geschwindigkeit ist daher allein durch die Geschwindigkeit und Speichergröße des Massespeichers des Hostsystems gegeben. Dies ist der Fall, da der digitale Signalprozessor 13 die über die zweite Verbindungseinrichtung 15 von der Sende/Empfangseinrichtung eingelesenen Daten bereits in für eine Festplatte des Hostgeräts geeignete Blockgrößen formatiert, wodurch die Datenübertragungsgeschwindigkeit lediglich durch die mechanische Trägheit des Festplattensystems des Hostgeräts begrenzt ist. An dieser Stelle sei angemerkt, daß üblicherweise ein Datenfluß vom einem Hostgerät in Blöcke formatiert werden muß, um auf einer Festplatte geschrieben werden zu können und anschließend wiedergewonnen werden zu können, wie es für Fachleute bekannt ist.

Durch Einrichtung eines direkten Speicherzugriffs (DMA; DMA = Direct Memory Access) oder RAM-Laufwerks im Hostsystem kann die genannte Datenübertragungsrate nochmals erhöht werden. Wie es für Fachleute bekannt ist, benötigt die Einrichtung eines RAM-Laufwerks jedoch Prozessorresourcen des Hostgeräts, weshalb der Vorteil, bei dem die Daten auf ein Festplattenlaufwerk des Hostgeräts geschrieben werden, und im wesentlichen keine Prozessorresourcen benötigt werden, verlorengeht.

Wie es bereits erwähnt wurde, kann in dem Speicher 14 ein Datenpuffer implementiert sein, der die zeitliche Unabhängigkeit der Sende/Empfangseinrichtung, die mit der zwei-

ten Verbindungseinrichtung gekoppelt ist, von dem Hostgerät, das mit der ersten Verbindungseinrichtung gekoppelt ist, ermöglicht. Auf diese Weise ist selbst bei zeitkritischen Anwendungen der einwandfreie Betrieb der Schnittstelleneinrichtung 10 sogar in Multi-Tasking-Hostsystemen gewährleistet.

Fig. 2 zeigt ein detailliertes Blockschaltbild einer Schnittstelleneinrichtung 10 gemäß der vorliegenden Erfindung.

Ein digitaler Signalprozessor (DSP) 1300 bildet gewissermaßen das Herzstück der Schnittstelleneinrichtung 10. Der DSP kann ein beliebiger DSP sein, wobei es jedoch bevorzugt wird, daß er einen Auf-Chip-Direkt-Zugriffsspeicher (RAM) von 20 KB aufweist. In dem Direktzugriffsspeicher, der bereits auf dem DSP integriert ist, können beispielsweise bestimmte Befehlssätze gespeichert sein. Mit dem DSP 1300 verbunden ist ein 80-MHz-Taktbauglied 1320, um den DSP zu takten. Der DSP implementiert eine schnelle Fouriertransformation (FFT) in Echtzeit sowie eine optionale Datenkompression für von der Sende/Empfangseinrichtung zu dem Hostgerät zu übertragenden Daten, um eine höhere Effizienz zu erreichen, und um mit Hostgeräten, die kleinere Speichereinrichtungen besitzen, zusammenarbeiten zu können.

Die erste Verbindungseinrichtung 12 von Fig. 1 enthält bei dem in Fig. 2 gezeigten bevorzugten Ausführungsbeispiel der Schnittstelleneinrichtung 10 folgende Bausteine: eine SCSI-Schnittstelle 1220 sowie einen 50-Pin-SCSI-Verbinder 1240 zur Verbindung mit einer bei den meisten Hostgeräten oder Laptops vorhandenen SCSI-Schnittstelle. Die SCSI-Schnittstelle (SCSI = Small Computer System Interface = Kleincomputersystemschnittstelle) 1220 wandelt die über den SCSI-Verbinder 1240 empfangenen Daten in für den DSP 1300 verständliche Daten um, wie es für Fachleute bekannt ist. Die erste Verbindungseinrichtung 12 umfaßt ferner einen EPP mit einer Datenrate von ungefähr 1 MB/s (EPP = Enhanced Parallel Port)

für eine im Vergleich zur Datenrate von 10 MB/s der SCSI-Schnittstelle moderateren Datenübertragungsrate von 1 MB/s. Der EPP 1260 ist mit einem 25-Pin-sub-D-Verbinder 1280 verbunden, um beispielsweise an eine Druckerschnittstelle eines Hostgeräts angeschlossen zu werden. Optional umfaßt die erste Verbindungseinrichtung 12 ferner einen 25-Pin-Verbinder 1282, der den Anschluß von 8 Digitalausgängen und 8 Digitaleingängen 1284 an einem Hostgerät ermöglicht.

Die zweite Verbindungseinrichtung umfaßt vorzugsweise 8 BNC-Eingänge mit Kalibrationsrelais 1505, einen Block 1510 mit 8 Geräteverstärkern mit einem Überspannungsschutz von ± 75 V, wobei dieser Block wiederum mit 8 Abtast/Halte-Gliedern 1515 verbunden ist (Abtasten/Halten = Sample/Hold = S&H). Die Kalibrationsrelais sind Relais, die ein gesteuertes Umschalten zwischen einer Meßspannung und einer Kalibrationsreferenzspannung erlauben. Jede Abtast/Halten-Einrichtung ist mit einem entsprechenden Eingang eines 8-Kanal-Multiplexers 1520 verbunden, welcher seine Ausgangssignale über einen programmierbaren Verstärker 1525 in einen Analog/Digital-Wandler (ADW) mit 12 Bit und 1,25 MHz 1530 dem DSP 1300 zuführt. Der ADW 1530 wird mittels eines 20-Bit-Zeitgebers 1535 gesteuert, wie es für Fachleute bekannt ist. Der programmierbare Verstärker 1525 sowie der 8-Kanal-Multiplexer 1520 werden über ein Verstärkungs-Kanal-Auswahlbauglied 1540 gesteuert, das wiederum von dem DSP 1300 gesteuert wird.

Die gesamte Schnittstelleneinrichtung 10 wird von einem externen AC/DC-Wandler 1800 versorgt, der eine digitale Leistungsversorgung von +5 V liefert und mit einem DC/DC-Wandler 1810 verbunden ist, der analoge Leistungsversorgungsspannungen von ± 5 V und ± 15 V liefern kann, wie sie für die Schnittstelleneinrichtung 10 benötigt werden. Der DC/DC-Wandler steuert ferner eine Präzisions-Spannungs-Referenz 1820, die sowohl die 8-BNC-Eingänge 1505 als auch den ADW 1530 sowie einen Digital/Analog-Wandler (DAW) 1830 steuert, welcher über einen Ausgangsverstärkerblock mit 4 Aus-

gangsverstärkern 1840 und einen 9-Pin-Verbinder 1850 die analoge Ausgabe direkt von dem DSP 1300 zu einer mit dem 9-Pin-Verbinder 1850 verbindbaren Ausgabeeinrichtung, wie z. B. eine Druckereinrichtung oder eine Bildschirmeinrichtung, ermöglicht, wodurch optional eine Datenüberwachung der zu dem Hostgerät übertragenen Daten oder beispielsweise auch, ohne Prozessorzeit von dem Hostgerät zu verwenden, eine FFT betrachtet werden kann, um eine schnelle und umfassende Datenanalyse zu erreichen.

Die Speichereinrichtung 14 von Fig. 1 ist in Fig. 2 durch ein EPROM 1400 implementiert, der bei einem bevorzugten Ausführungsbeispiel der vorliegenden Erfindung das Betriebssystem des digitalen Signalprozessors 1300 hält. Ein Direktzugriffsspeicher mit einer Zugriffszeit von 15 ns und einer Größe von 512 KB oder optional 1024 KB 1420 dient als Datenpuffer, um eine zeitliche Unabhängigkeit der Ausgangsleitung 16 von den Ausgangsleitungen 11a, 11b und 11c zur Sende/Empfangseinrichtung bzw. zum Hostgerät zu erreichen. Wie es bereits erwähnt wurde, enthält der digitale Signalprozessor 1300 bei einem bevorzugten Ausführungsbeispiel der vorliegenden Erfindung bereits einen 20-KB-Auf-Chip-RAM 1440, der bestimmte Befehlssätze, Funktionen oder auch kleinere Anwendungssoftwareeinheiten speichern kann.

Der durch die Leitung 16 symbolisierte Verbindungsanschluß der Schnittstelleneinrichtung 10 mit einer beliebigen Sende/Empfangseinrichtung implementiert mit den Blöcken 1505 - 1535 einen Analogeingang mit einer Abtastrate von 1,25 MHz und einer Quantisierung von 12 Bit. Es existieren 8 Kanäle mit einem Überspannungsschutz von ± 75 V. Mittels des programmierbaren Verstärkers 1525 kann jeder Kanal unabhängig voneinander in Spannungsbereichen von max. ± 10 V programmiert werden. Unbenutzte Kanäle können intern mit Masse verbunden werden, um Nebensprecheffekte zu verringern. Der Block 1515 ist als monolithischer hochgenauer Hochgeschwindigkeits-Abtasten/Halten-Verstärker für das gleichzeitige Abtasten aller Kanäle ausgeführt. Die Präzisionsspannungsre-

ferenz 1820 schafft eine hochgenaue Temperatur-kompensierte monolithische Bandabstandsspannungsreferenz für eine Autokalibration jedes Kanals und jeder Verstärkung. Es ist ferner eine Offset-Feinabstimmung für jeden Kanal durch dieselbe implementiert.

Die Blöcke 1830, 1840 und 1850 implementieren einen direkten Analogausgang für den digitalen Signalprozessor 1300, wobei der DAW 1830 eine Datenrate von 625 KHz und eine Quantisierung von 12 Bit schafft. Der Block 1840 umfaßt 4 Kanäle mit einem gemeinsamen Ausgangslatch.

Die Schnittstelleneinrichtung 10 umfaßt ferner eine digitale Eingabe/Ausgabe-Einrichtung, die durch die Blöcke 1284 und 1282 implementiert ist. Hier existieren 8 digitale Eingänge, 8 digitale Ausgänge mit einem gemeinsamen Latch, wobei der digitale Port vorzugsweise an einer Seitenwand der Schnittstelleneinrichtung 10 angebracht sein kann, damit auf denselben ohne weiteres zugegriffen werden kann.

Der digitale Signalprozessor 1300 liefert eine On-Board-Digitaldatenverarbeitung. Insbesondere ist er ein Hochleistungs-DSP mit einer Taktrate von 80 MHz und einem 20-Bit-Zeitgeber 1535.

Die erste Verbindungseinrichtung 12 umfaßt, wie es bereits erwähnt wurde, die SCSI-Schnittstelle 1220 mit einer Spitzenübertragungsrate von 10 MB/s. Ein optional einbaubarer PCMCIA-zu-SCSI-Adapter ermöglicht eine Hochgeschwindigkeitskommunikation mit Laptop-Computern, welche besonders bei mobilen Servicetechnikern verbreitet und erwünscht sind. Eine moderatere Datenübertragung ermöglicht der EPP 1260 mit seinem zugehörigen Verbinder 1280.

Wie es bereits erwähnt wurde, wird die Leistungsversorgung der Schnittstelleneinrichtung 10 mittels eines externen AC/DC-Adapters erreicht, der einen Universalleistungseingang (85 - 264 VAC, 47 - 63 Hz) aufweist. Die Interferenzunter-

drückung erreicht die Standards EN 55022, Kurve B und FCC, Klasse B). Ferner ist sie gemäß internationalen Sicherheitsbestimmungen (TÜV, UL, CSA) ausgeführt. Die Schnittstelleneinrichtung 10 ist nach außen abgeschirmt und erreicht einen Wert von 55 dB bei 30 - 60 MHz und einen Wert von etwa 40 dB bei 1 GHz, und entspricht somit dem Standard MILSTD 285-1.

Die Schnittstelleneinrichtung gemäß der vorliegeden Erfindung ermöglicht also unter Verwendung einer Standardschnittstelle eines Hostgeräts die Kommunikation mit beliebigen Hostgeräten. Durch die Simulation eines Eingabe/Ausgabe-Geräts für das Hostgerät und bei einem bevorzugten Ausführungsbeispiel durch Simulation eines virtuellen Massenspeichers wird die Schnittstelleneinrichtung 10 von allen bekannten Hostsystemen ohne jede zusätzliche aufwendige Treibersoftware automatisch unterstützt. Die Simulation einer beliebig definierbaren Dateistruktur auf der "virtuellen" Festplatte liefert einfache Bedienungs- und Erweiterungsmöglichkeiten sowie durch Implementation beliebiger Programme die Unabhängigkeit von spezieller auf dem Hostgerät implementierter Software. Auf der Schnittstelleneinrichtung 10 enthaltene Hilfedateien und die Unterstützung von "Plug-and Play" stellen den einfachen Einsatz selbst in tragbaren flexiblen Hostgeräten sicher. Dem erfahrenen Anwender steht trotz einfachster Bedienungsoberfläche jederzeit die Möglichkeit des systemnahen Eingriffs in Funktionen der Schnittstelleneinrichtung 10 offen. Eine universelle Lösung, die die gesamte Bandbreite möglicher Sende/Empfangseinrichtungen abdecken kann, ist demnach durch die Schnittstelleneinrichtung 10 geschaffen.

Patentansprüche

1. Schnittstellengerät (10) zur Kommunikation zwischen einem Hostgerät mit Eingabe/Ausgabe-Schnittstellen und einer Datensende/Empfangseinrichtung, mit folgenden Merkmalen:

   einer Prozessoreinrichtung (13; 1300; 1320);

   einer Speichereinrichtung (14; 1400, 1420, 1440);

   einer ersten Verbindungseinrichtung (12; 1220, 1240, 1260, 1280) zum schnittstellenmäßigen Verbinden des Hostgeräts mit dem Schnittstellengerät (10);

   einer zweiten Verbindungseinrichtung (15; 1505 - 1535) zum schnittstellenmäßigen Verbinden der Schnittstellengeräts (10) mit der Datensende/Empfangseinrichtung,

   wobei das Schnittstellengerät (10) durch die Prozessoreinrichtung und die Speichereinrichtung derart konfiguriert ist, daß das Schnittstellengerät bei einer Anfrage des Hostgeräts über die erste Verbindungseinrichtung, die die Art eines an das Hostgerät angeschlossenen Geräts betrifft, unabhängig von dem Typ der Datensende/Empfangseinrichtung ein Signal über die erste Verbindungseinrichtung zu dem Hostgerät sendet, das dem Hostgerät signalisiert, daß es mit einem Eingabe/Ausgabe-Gerät kommuniziert.

2. Schnittstellengerät (10) nach Anspruch 1,

   bei dem die Eingabe/Ausgabe-Schnittstellen des Hostgeräts eine Festplattenschnittstelle aufweisen, wobei das Signal dem Hostgerät signalisiert, daß dasselbe mit einer Festplatte kommuniziert.

3. Schnittstellengerät (10) nach Anspruch 1 oder 2,

bei dem die Speichereinrichtung einen Puffer (1420) aufweist, um zwischen der Datensende/Empfangseinrichtung und dem Hostgerät übertragbare Daten zwischenzuspeichern.

4. Schnittstellengerät (10) nach einem der vorhergehenden Ansprüche,

bei dem die erste Verbindungseinrichtung eine SCSI-Schnittstelle (1220) aufweist.

5. Schnittstellengerät (10) nach einem der vorhergehenden Ansprüche,

bei dem die zweite Verbindungseinrichtung einen Analogeingang (1505) mit nachfolgendem A/D-Wandler (1530) aufweist, um analoge Daten von einem mit dem Analogeingang (1505) verbindbaren Datensende/Empfangsgerät zu dem Hostgerät zu übertragen.

6. Schnittstellengerät (10) nach einem der vorhergehenden Ansprüche,

bei dem die Prozessoreinrichtung (13) ein digitaler Signalprozessor (1300) ist.

7. Schnittstellengerät (10) nach einem der Ansprüche 2 bis 6,

bei dem von der Datensende/Empfangseinrichtung zum Hostgerät zu übertragende Daten in dem Schnittstellengerät (10) in ein für eine in dem Hostgerät vorhandene Festplatte geeignetes Format formatiert werden.

8. Schnittstellengerät (10) nach einem der Ansprüche 2 bis 7,

das ferner ein Wurzelverzeichnis und virtuelle Dateien, die auf dem signalisierten Festplattenlaufwerk vorhanden sind, aufweist, auf die von dem Hostgerät zugegriffen werden kann.

9. Schnittstellengerät (10) nach Anspruch 8,

bei dem die virtuellen Dateien eine Konfigurationsdatei im Textformat aufweisen, die in der Speichereinrichtung (14) gespeichert sind, mittels der der Benutzer das Schnittstellengerät (10) für eine spezielle Datensende/Empfangseinrichtung konfigurieren kann.

10. Schnittstellengerät (10) nach Anspruch 8 oder 9,

bei dem die virtuellen Dateien Stapeldateien oder ausführbare Dateien für die Mikroprozessereinrichtung aufweisen, die in der Schnittstelleneinrichtung (10) gespeichert sind, um eine vom Hostgerät getrennte Datenverarbeitung von über die zweite Verbindungseinrichtung (15; 1505 - 1535) empfangenen Daten durchzuführen.

11. Schnittstellengerät (10) nach Anspruch 8 oder 9,

bei dem die virtuellen Dateien Stapeldateien oder ausführbare Dateien für das Hostgerät aufweisen, die in der Schnittstelleneinrichtung (10) gespeichert sind.

12. Verfahren zur Kommunikation zwischen einem Hostgerät mit Eingabe/Ausgabe-Schnittstellen und einer Datensende/Empfangseinrichtung mittels eines Schnittstellengeräts (10), mit folgenden Schritten:

schnittstellenmäßiges Verbinden des Hostgeräts mit dem Schnittstellengerät (10);

schnittstellenmäßiges Verbinden des Schnittstellengeräts

(10) mit der Datensende/Empfangseinrichtung;

Anfragen durch das Hostgerät bei dem Schnittstellengerät, welcher Typ eines Geräts mit dem Hostgerät verbunden ist;

Beantworten der Anfrage des Hostgeräts durch das Schnittstellengerät (10), derart, daß das Hostgerät mit einem Eingabe/Ausgabe-Gerät kommuniziert, unabhängig davon, welcher Typ einer Datensende/Empfangseinrichtung mit dem Schnittstellengerät (10) verbunden ist.

13. Verfahren nach Anspruch 12,

bei dem das Eingabe/Ausgabe-Gerät ein Speichergerät und insbesondere ein Festplattenlaufwerk ist.

Flexible Schnittstelle

Zusammenfassung

Ein Schnittstellengerät liefert eine schnelle Datenkommunikation zwischen einem Hostgerät mit Eingabe/Ausgabe-Schnittstellen und einer Datensende/Empfangseinrichtung, wobei das Schnittstellengerät eine Prozessoreinrichtung, eine Speichereinrichtung, eine erste Verbindungseinrichtung zum schnittstellenmäßigen Verbinden des Hostgeräts mit dem Schnittstellengerät und eine zweite Verbindungseinrichtung zum schnittstellenmäßigen Verbinden des Schnittstellengeräts mit der Datensende/Empfangseinrichtung aufweist. Das Schnittstellengerät ist durch die Prozessoreinrichtung und die Speichereinrichtung derart konfiguriert, daß das Schnittstellengerät bei einer Anfrage des Hostgeräts über die erste Verbindungseinrichtung, die die Art eines an demselben angeschlossenen Geräts betrifft, unabhängig von dem Typ der Datensende/Empfangseinrichtung ein Signal über die erste Verbindungseinrichtung zum Hostgerät sendet, das dem Hostgerät signalisiert, daß es mit einem Eingabe/Ausgabe-Gerät kommuniziert.

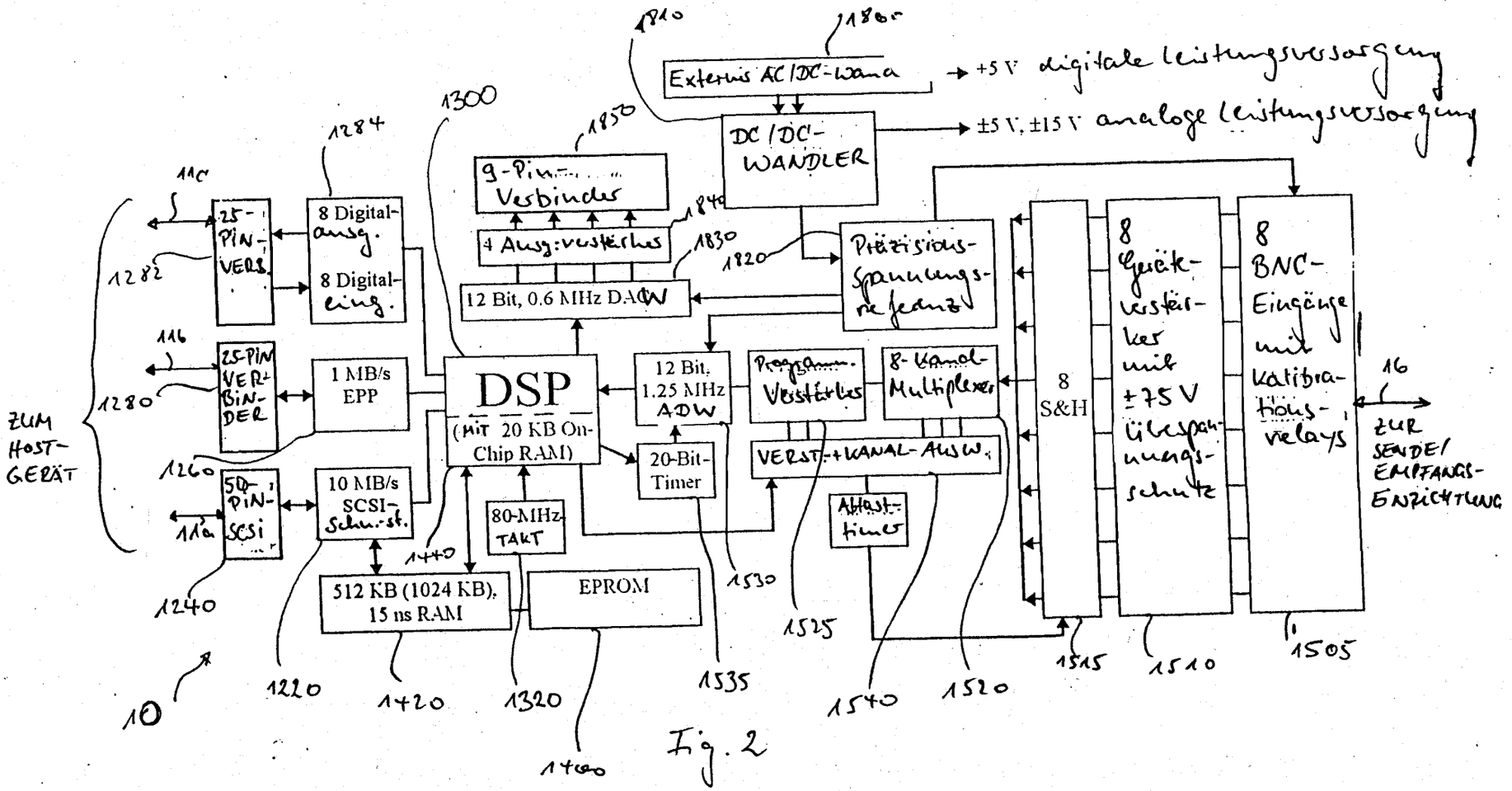
Externes AC/DC-Wandler
+5 V digitale Leistungsversorgung
±5 V, ±15 V analoge Leistungsversorgung
DC/DC-WANDLER
9-Pin-... Verbinder
4 Ausg.-verstärker
12 Bit, 0.6 MHz DAC/W
Präzisions-Spannungs-referenz
25-PIN-VERB.
8 Digital-ausg.
8 Digital-eing.
25-PIN VERBINDER
1 MB/s EPP
50-PIN-SCSI
10 MB/s SCSI-Schn.-st.
ZUM HOST-GERÄT
DSP
(mit 20 KB On-Chip RAM)
80-MHz-TAKT
512 KB (1024 KB), 15 ns RAM
EPROM
12 Bit, 1.25 MHz ADW
20-Bit-Timer
Programm.-Verstärkus
8-Kanal-Multiplexer
VERST.+KANAL-AUSW.
Abtast-timer
8 S&H
8 Gleich-verstär-ker mit ±75 V Überspan-nungs-schutz
8 BNC-Eingänge mit Kalibra-tions-relays
ZUR SENDE/EMPFANGS-EINRICHTUNG
1810
1800
1850
1840
1830
1820
1300
1284
1282
1280
1260
1240
1220
1420
1320
1400
1440
1530
1535
1525
1540
1520
1515
1510
1505
10
11c
11b
11a
16

Fig. 2

National Phase of PCT/EP98/01187 in U.S.A.
Title: Flexible Interface
Applicant: TASLER, Michael

Translation of PCT Application PCT/EP98/01187
as originally filed

Flexible Interface

Abstract of the Invention

An interface device provides fast data communication between a host device with input/output interfaces and a data transmit/receive device, wherein the interface device comprises a processor, a memory, a first connecting device for interfacing the host device with the interface device, and a second connecting device for interfacing the interface device with the data transmit/receive device. The interface device is configured by the processor and the memory in such a way that, when receiving an inquiry from the host device via the first connecting device as to the type of a device attached to the host device, regardless of the type of the data transmit/receive device, the interface device sends a signal to the host device via the first connecting device which signals to the host device that it is communicating with an input/output device.

09/331002

National Phase of PCT/EP98/01187 in U.S.A.
Title: Flexible Interface
Applicant: TASLER, Michael

Final version of PCT/EP98/01187 for the prosecution at the USPTO to be filed as first preliminary amendment

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Flexible Interface

Field of the Invention

The present invention relates to the transfer of data and in particular to interface devices for communication between a computer or host device and a data transmit/receive device from which data is to be acquired or with which two-way communication is to take place.

Background of the Invention

Existing data acquisition systems for computers are very limited in their areas of application. Generally such systems can be classified into two groups.

In the first group host devices or computer systems are attached by means of an interface to a device whose data is to be acquired. The interfaces of this group are normally standard interfaces which, with specific driver software, can be used with a variety of host systems. An advantage of such interfaces is that they are largely independent of the host device. However, a disadvantage is that they generally require very sophisticated drivers which are prone to malfunction and which limit data transfer rates between the device connected to the interface and the host device and vice versa. Further, it is often very difficult to implement such interfaces for portable systems and they offer few possibilities for adaptation with the result that such systems offer little flexibility.

The devices from which data is to be acquired cover the entire electrical engineering spectrum. In a typical case, it is assumed that a customer who operates, for example, a diagnostic radiology system in a medical engineering environment reports a fault. A field service technician of the system manufacturer visits the customer and reads system log files generated by the diagnostic radiology system by means a portable computer or laptop for example. If the fault cannot be localized or if the fault is intermittent, it will be necessary for the service technician to read not only an error

log file but also data from current operation. It is apparent that in this case fast data transfer and rapid data analysis are necessary.

Another case requiring the use of an interface could be, for example, when an electronic measuring device, e.g. a multimeter, is attached to a computer system to transfer the data measured by the multimeter to the computer. Particularly when long-term measurements or large volumes of data are involved is it necessary for the interface to support a high data transfer rate.

From these randomly chosen examples it can be seen that an interface may be put to totally different uses. It is therefore desirable that an interface be sufficiently flexible to permit attachment of very different electrical or electronic systems to a host device by means of the interface. To prevent operator error, it is also desirable that a service technician is not required to operate different interfaces in different ways for different applications but that, if possible, a universal method of operating the interface be provided for a large number of applications.

To increase the data transfer rates across an interface, the route chosen in the second group of data acquisition systems for the interface devices was to specifically match the interface very closely to individual host systems or computer systems. The advantage of this solution is that high data transfer rates are possible. However, a disadvantage is that the drivers for the interfaces of the second group are very closely matched to a single host system with the result that they generally cannot be used with other host systems or their use is very ineffective. Further, such types of interface have the disadvantage that they must be installed inside the computer casing to achieve maximum data transfer rates as they access the internal host bus system. They are therefore generally not suitable for portable host systems in the form of laptops whose minimum possible size leaves little internal space to plug in an interface card.

Description of Prior Art

A solution to this problem is offered by the interface devices of IOtech (business address: 25971 Cannon Road, Cleveland, Ohio 44146, USA) which are suitable for

laptops such as the WaveBook/512 (registered trademark). The interface devices are connected by means of a plug-in card, approximately the size of a credit card, to the PCMCIA interface which is now a standard feature in laptops. The plug-in card converts the PCMCIA interface into an interface known in the art as IEEE 1284. The said plug-in card provides a special printer interface which is enhanced as regards the data transfer rate and delivers a data transfer rate of approximately 2 MBps as compared with a rate of approx. 1 MBps for known printer interfaces. The known interface device generally consists of a driver component, a digital signal processor, a buffer and a hardware module which terminates in a connector to which the device whose data is to be acquired is attached. The driver component is attached directly to the enhanced printer interface thus permitting the known interface device to establish a connection between a computer and the device whose data is to be acquired.

In order to work with the said interface, an interface-specific driver must be installed on the host device so that the host device can communicate with the digital signal processor of the interface card. As described above, the driver must be installed on the host device. If the driver is a driver developed specifically for the host device, a high data transfer rate is achieved but the driver cannot be easily installed on a different host system. However, if the driver is a general driver which is as flexible as possible and which can be used on many host devices, compromises must be accepted with regard to the data transfer rate.

Particularly in an application for multi-tasking systems in which several different tasks such as data acquisition, data display and editing are to be performed quasi-simultaneously, each task is normally assigned a certain priority by the host system. A driver supporting a special task requests the central processing system of the host device for processor resources in order to perform its task. Depending on the particular priority assignment method and on the driver implementation, a particular share of processor resources is assigned to a special task in particular time slots. Conflicts arise if one or more drivers are implemented in such a way that they have the highest priority by default, i.e. they are incompatible, as happens in practice in many applications. It may occur that both drivers are set to highest priority which, in the worst case, can result in a system crash.

EP 0685799 A1 discloses an interface by means of which several peripheral devices can be attached to a bus. An interface is connected between the bus of a host device and various peripheral devices. The interface comprises a finite state machine and several branches each of which is assigned to a peripheral device. Each branch comprises a data manager, cycle control, user logic and a buffer. This known interface device provides optimal matching between a host device and a specific peripheral device.

The specialist publication IBM Technical Disclosure Bulletin, Vol. 38, No. 05, page 245; "Communication Method between Devices through FDD Interface" discloses an interface which connects a host device to a peripheral device via a floppy disk drive interface. The interface consists in particular of an address generator, an MFM encoder/decoder, a serial/parallel adapter and a format signal generator. The interface makes it possible to attach not only a floppy disk drive but also a further peripheral device to the FDD host controller of a host device. The host device assumes that a floppy disk drive is always attached to its floppy disk drive controller and communication is initiated if the address is correct. However, this document contains no information as to how communication should be possible if the interface is connected to a multi-purpose interface instead of to a floppy disk drive controller.

Summary of the Invention

It is an object of the present invention to provide an interface device for communication between a host device and a data transmit/receive device whose use is host device-independent and which delivers a high data transfer rate.

In accordance with a first aspect of the present invention, this object is met by an interface device for communication between a host device, which comprises drivers for input/output devices customary in a host device and a multi-purpose interface, and a data transmit/receive device comprising: a processor; a memory; a first connecting device for interfacing the host device with the interface device via the multi-purpose interface of the host device; and a second connecting device for interfacing the interface device with the data transmit/receive device, wherein the interface device is

configured by the processor and the memory in such a way that the interface device, when receiving an inquiry from the host device as to the type of a device attached to the multi-purpose interface of the host device, sends a signal, regardless of the type of the data transmit/receive device attached to the second connecting device of the interface device, to the host device which signals to the host device that it is an input/output device customary in a host device, whereupon the host device communicates with the interface device by means of the driver for the input/output device customary in a host device.

In accordance with a second aspect of the present invention, this object is met by an interface device for communication between a host device, which comprises a multi-purpose interface and a specific driver for this interface, and a data transmit/receive device comprising: a processor; a memory; a first connecting device for interfacing the host device with the interface device via the multi-purpose interface of the host device; and a second connecting device for interfacing the interface device with the data transmit/receive device, wherein the interface device is configured using the processor and the memory in such a way that the interface device, when receiving an inquiry from the host device as to the type of a device attached at the multi-purpose interface of the host device, sends a signal, regardless of the type of the data transmit/receive device attached to the second connecting device of the interface device, to the host device which signals to the host device that it is an input/output device customary in a host device, whereupon the host device communicates with the interface device by means of the specific driver for the multi-purpose interface.

In accordance with a third aspect of the present invention, this object is met by a method of communication between a host device, which comprises drivers for input/output devices customary in a host device and a multi-purpose interface, and a data transmit/receive device via an interface device comprising the steps of interfacing of the host device with a first connecting device of the interface device via the multi-purpose interface of the host device; interfacing of the data transmit/receive device with a second connecting device of the interface device; inquiring by the host device at the interface device as to the type of device to which the multi-purpose interface of the host device is attached; regardless of the type of the data transmit/receive device attached to the second connecting device of the interface

device, responding to the inquiry from the host device by the interface device in such a way that it is an input/output device customary in a host device, whereupon the host device communicates with the interface device by means of the usual driver for the input/output device.

The present invention is based on the finding that both a high data transfer rate and host device-independent use can be achieved if a driver for an input/output device customary in a host device, normally present in most commercially available host devices, is utilized. Drivers for input/output devices customary in a host device which are found in practically all host devices are, for example, drivers for hard disks, for graphics devices or for printer devices. As however the hard disk interfaces in common host devices which can be, for example, IBM PCs, IBM-compatible PCs, Commodore PCs, Apple computers or even workstations, are the interfaces with the highest data transfer rate, the hard disk driver is utilized in the preferred embodiment of the interface device of the present invention. Drivers for other storage devices such as floppy disk drives, CD-ROM drives or tape drives could also be utilized in order to implement the interface device according to the present invention.

As described in the following, the interface device according to the present invention is to be attached to a host device by means of a multi-purpose interface of the host device which can be implemented, for example, as an SCSI interface or as an enhanced printer interface. Multi-purpose interfaces comprise both an interface card and specific driver software for the interface card. The driver software can be designed so that it can replace the BIOS driver routines. Communication between the host device and the devices attached to the multi-purpose interface then essentially takes place by means of the specific driver software for the multi-purpose interface and no longer primarily by means of BIOS routines of the host device. Recently however drivers for multi-purpose interfaces can also already be integrated in the BIOS system of the host device as, alongside classical input/output interfaces, multi-purpose interfaces are becoming increasingly common in host devices. It is of course also possible to use BIOS routines in parallel with the specific driver software for the multi-purpose interface, if this is desired.

The interface device according to the present invention comprises a processor means, a memory means, a first connecting device for interfacing the host device with the interface device, and a second connecting device for interfacing the interface device with the data transmit/receive device. The interface device is configured by the processor means and the memory means in such a way that the interface device, when receiving an inquiry from the host device via the first connecting device as to the type of a device attached to the host device, sends a signal, regardless of the type of the data transmit/receive device, to the host device via the first connecting device which signals to the host device that it is communicating with an input/output device. The interface device according to the present invention therefore simulates, both in terms of hardware and software, the way in which a conventional input/output device functions, preferably that of a hard disk drive. As support for hard disks is implemented as standard in all commercially available host systems, the simulation of a hard disk, for example, can provide host device-independent use. The interface device according to the present invention therefore no longer communicates with the host device or computer by means of a specially designed driver but by means of a program which is present in the BIOS system (Basic Input/Output System) and is normally precisely matched to the specific computer system on which it is installed, or by means of a specific program for the multi-purpose interface. Consequently, the interface device according to the present invention combines the advantages of both groups. On the one hand, communication between the computer and the interface takes place by means of a host device-specific BIOS program or by means of a driver program which is matched to the multi-purpose interface and which could be regarded as a "device-specific driver". On the other hand, the BIOS program or a corresponding multi-purpose interface program which operates one of the common input/output interfaces in host systems is therefore present in all host systems so that the interface device according to the present invention is host device-independent.

Brief Description of the Drawings

In the following, preferred embodiments of the present invention will be explained in more detail with reference to the drawings enclosed, in which:

Fig. 1 shows a general block diagram of the interface device according to the present invention; and

Fig. 2 shows a detailed block diagram of an interface device according to a preferred embodiment of the present invention.

Detailed Description of Preferred Embodiments

Fig. 1 shows a general block diagram of an interface device 10 according to the present invention. A first connecting device 12 of the interface device 10 can be attached to a host device (not shown) via a host line 11. The first connecting device is attached both to a digital signal processor 13 and to a memory means 14. The digital signal processor 13 and the memory means 14 are also attached to a second connecting device 15 by means of bi-directional communication lines (shown for all lines by means of two directional arrows). The second connecting device can be attached by means of an output line 16 to a data transmit/receive device which is to receive data from the host device or from which data is to be read, i.e. acquired, and transferred to the host device. The data transmit/receive device itself can also communicate actively with the host device via the first and second connecting device, as described in more detail in the following.

Communication between the host system or host device and the interface device is based on known standard access commands as supported by all known operating systems (e.g. DOS, Windows, Unix). Preferably, the interface device according to the present invention simulates a hard disk with a root directory whose entries are "virtual" files which can be created for the most varied functions. When the host device system with which the interface device according to the present invention is connected is booted and a data transmit/receive device is also attached to the interface device 10, usual BIOS routines or multi-purpose interface programs issue an instruction, known by those skilled in the art as the INQUIRY instruction, to the input/output interfaces in the host device. The digital signal processor 13 receives this inquiry instruction via the first connecting device and generates a signal which is sent to the host device (not shown) again via the first connecting device 12 and the host

line 11. This signal indicates to the host device that, for example, a hard disk drive is attached at the interface to which the INQUIRY instruction was sent. Optionally, the host device can send an instruction, known by those skilled in the art as "Test Unit Ready", to the interface device to request more precise details regarding the queried device.

Regardless of which data transmit/receive device at the output line 16 is attached to the second connecting device, the digital signal processor 13 informs the host device that it is communicating with a hard disk drive. If the host device receives the response that a drive is present, it then sends a request to the interface device 10 to read the boot sequence which, on actual hard disks, normally resides on the first sectors of the disk. The digital signal processor 13, whose operating system in stored in the memory means 14, responds to this instruction by sending to the host device a virtual boot sequence which, in the case of actual drives, includes the drive type, the starting position and the length of the file allocation table (FAT), the number of sectors, etc., known to those skilled in the art. Once the host device has received this data, it assumes that the interface device 10 according to a preferred embodiment of the present invention is a hard disk drive. In reply to an instruction from the host device to display the directory of the "virtual" hard disk drive simulated by the interface device 10 with respect to the host device, the digital signal processor can respond to the host device in exactly the same way as a conventional hard disk would, namely by reading on request the file allocation table or FAT on a sector specified in the boot sequence, normally the first writable sector, and transferring it to the host device, and subsequently by transferring the directory structure of the virtual hard disk. Further, it is possible that the FAT is not read until immediately prior to reading or storing the data of the "virtual" hard disk and not already at initialization.

In a preferred embodiment of the present invention, the digital signal processor 13, which need not necessarily be implemented as a digital signal processor but may be any other kind of microprocessor, comprises a first and a second command interpreter. The first command interpreter carries out the steps described above whilst the second command interpreter carries out the read/write assignment to specific functions. If the user now wishes to read data from the data transmit/receive device via the line 16, the host device sends a command, for example "read file xy", to the

interface device. As described above, the interface device appears to the host device as a hard disk. The second command interpreter of the digital signal processor now interprets the read command of the host processor as a data transfer command, by decoding whether "xy" denotes, for example, a "real-time input" file, a "configuration" file or an executable file, whereby the same begins to transfer data from the data transmit/receive device via the second connecting device to the first connecting device and via the line 11 to the host device.

Preferably, the volume of data to be acquired by a data transmit/receive device is specified in a configuration file described in the following by the user specifying in the said configuration file that a measurement is to last, for example, five minutes. To the host device the "real-time input" file then appears as a file whose length corresponds to the anticipated volume of data in those five minutes. Those skilled in the art know that communication between a processor and a hard disk consists of the processor transferring to the hard disk the numbers of the blocks or clusters or sectors whose contents it wishes to read. By reference to the FAT the processor knows which information is contained in which block. In this case, communication between the host device and the interface device according to the present invention therefore consists of the very fast transfer of block numbers and preferably of block number ranges because a virtual "real-time input" file will not be fragmented. If the host device now wants to read the "real-time input" file, it transfers a range of block numbers to the interface device, whereupon data commences to be received via the second connecting device and data commences to be sent to the host device via the first connecting device.

In addition to the digital signal processor instruction memory, which comprises the operating system of the digital signal processor and can be implemented as an EPROM or EEPROM, the memory means 14 can have an additional buffer for purposes of synchronizing data transfer from the data transmit/receive device to the interface device 10 and data transfer from the interface device 10 to the host device.

Preferably, the buffer is implemented as a fast random access memory or RAM buffer.

Further, from the host device the user can also create a configuration file, whose entries automatically set and control various functions of the interface device 10, on the interface device 10 which appears to the host device as a hard disk. These settings can be, for example, gain, multiplex or sampling rate settings. By creating and editing a configuration file, normally a text file which is simple to understand with little prior knowledge, users of the interface device 10 are able to perform essentially identical operator actions for almost any data transmit/receive devices which can be attached to the second connecting device via the line 16, thus eliminating a source of error arising from users having to know many different command codes for different applications. In the case of the interface device 10 according to the present invention it is necessary for users to note the conventions of the configuration file once only in order to be able to use the interface device 10 as an interface between a host device and almost any data transmit/receive device.

As a result of the option of storing any files in agreed formats in the memory means 14 of the interface device 10, taking into account the maximum capacity of the memory means, any enhancements or even completely new functions of the interface device 10 can be quickly implemented. Even files executable by the host device, such as batch files or executable files (BAT or EXE files), and also help files can be implemented in the interface device, thus achieving independence of the interface device 10 from any additional software (with the exception of the BIOS routines) of the host device. On the one hand, this avoids licensing and/or registration problems and, on the other hand, installation of certain routines which can be frequently used, for example an FFT routine to examine acquired time-domain data in the frequency domain, is rendered unnecessary as the EXE files are already installed on the interface device 10 and appear in the virtual root directory, by means of which the host device can access all programs stored on the interface device 10.

In a preferred embodiment of the present invention in which the interface device 10 simulates a hard disk to the host device, the interface device is automatically detected and readied for operation when the host system is powered up or booted. This corresponds to the plug-and-play standard which is currently finding increasingly widespread use. The user is no longer responsible for installing the interface device 10 on the host device by means of specific drivers which must also be loaded; instead the

interface device 10 is automatically readied for operation when the host system is booted.

For persons skilled in the art it is however obvious that the interface device 10 is not necessarily signed on when the computer system is powered up but that a special BIOS routine or a driver for a multi-purpose interface can also be started on the host device during current operation of the computer system in order to sign on or mount the interface device 10 as an additional hard disk. This embodiment is suitable for larger workstation systems which are essentially never powered down as they perform, e.g. mail functions or monitor processes which run continuously, for example, in multi-tasking environments.

In the interface device according to the present invention an enormous advantage is to be gained, as apparent in the embodiment described in the following, in separating the actual hardware required to attach the interface device 10 to the data transmit/receive device from the communication unit, which is implemented by the digital signal processor 13, the memory means 14 and the first connecting device 12, as this allows a plurality of dissimilar device types to be operated in parallel in identical manner. Accordingly, many interface devices 10 can be connected to a host device which then sees many different "virtual" hard disks. In addition, any modification of the specific hardware symbolized by the second connecting device 15 can be implemented essentially without changing the operation of the interface device according to the present invention. Further, an experienced user can intervene at any time on any level of the existing second connecting device by making use of the above mentioned option of creating a configuration file or adding or storing new program sections for the second connecting device.

An important advantage of the interface device 10 of the present invention is that it also permits extremely high data transfer rates by using, for data interchange, the host device-own BIOS routines which are optimized for each host device by the host device manufacturer or BIOS system manufacturer, or by using driver programs which are normally optimized and included by the manufacturers of multi-purpose interfaces. Furthermore, due to the simulation of a virtual mass storage device, the data is managed and made available in such a way that it can be transferred directly to

other storage media, e.g. to an actual hard disk of the host device without, as it were, intervention of the host device processor. The only limitation to long-term data transfer at high speed is therefore imposed exclusively by the speed and the size of the mass storage device of the host device. This is the case as the digital signal processor 13 already formats the data read by the data transmit/receive device via the second connecting device 15 into block sizes suitable for a hard disk of the host device, whereby the data transfer speed is limited only by the mechanical latency of the hard disk system of the host device. At this point, it should be noted that normally data flow from a host device must be formatted in blocks to permit writing to a hard disk and subsequent reading from a hard disk, as known by those skilled in the art.

The said data transfer rate can be increased further by setting up a direct memory access (DMA) or RAM drive in the host system. As those skilled in the art know, the setting up of a RAM drive requires processor resources of the host device, with the result that the advantage of writing the data to a hard disk drive of the host device essentially without the need for processor resources is lost.

As described above, a data buffer can be implemented in the memory means 14 to permit independence in terms of time of the data transmit/receive device attached to the second connecting device from the host device attached to the first connecting device. This guarantees error-free operation of the interface device 10 even for time-critical applications in multi-tasking host systems.

Fig. 2 shows a detailed block diagram of an interface device 10 according to the present invention.

A digital signal processor (DSP) 1300 is, in a manner of speaking, the heart of the interface device 10. The DSP can be any DSP but preferably has a 20-MB on-chip random access memory (RAM). Certain instruction sets, for example, can be stored in the RAM already integrated in the DSP. An 80-MHz clock generator is attached to the DSP 1300 in order to synchronize the DSP. The DSP implements a fast Fourier transformation (FFT) in real time and also optional data compression of the data to be transferred from the data transmit/receive device to the host device in order to achieve

greater efficiency and to permit interoperation with host devices which have a smaller memory.

In the preferred embodiment of the interface device 10 shown in Fig. 2, the first connecting device 12 of Fig. 1 contains the following components: an SCSI interface 1220 and a 50-pin SCSI connector 1240 for attachment to an SCSI interface present on most host devices or laptops. The SCSI (small computer system interface) interface 1220 translates the data received via the SCSI connector 1240 into data understood by the DSP 1300, as known by those skilled in the art. Further, the first connecting device 12 comprises an EPP (enhanced parallel port) with a data transfer rate of approx. 1 MBps which delivers a more moderate data transfer rate of 1 MBps by comparison to the data transfer rate of 10 MBps of the SCSI interface. The EPP 1260 is connected to a 25-pin D-shell connector 1280 to permit attachment to a printer interface of a host device for example. Optionally, the first connecting device 12 also comprises a 25-pin connector 1282 which permits the attachment of 8 digital outputs and 8 digital inputs 1284 at a host device.

Preferably, the second connecting device comprises 8 BNC inputs with the calibration relay 1505, a block 1510 with 8 device amplifiers with an overvoltage protection of ±75 V, this block being connected in turn to 8 sample/hold (S&H) circuits 1515. The calibration relays are relays which permit controlled changeover between a test voltage and a calibration reference voltage. Each sample/hold circuit is connected to a corresponding input of an 8-channel multiplexer 1520 which feeds its output signals via a programmable amplifier 1525 into an analog/digital converter (ADC) with 12 bit and 1.25 MHz 1530 and to the DSP 1300. The ADC 1530 is controlled by means of a 20-bit timer 1535, as known by persons skilled in the art. The programmable amplifier 1525 and the 8-channel multiplexer 1520 are controlled via an amplifier channel selection circuit 1540 which is in turn controlled by the DSP 1300.

The complete interface device 10 is supplied with power by an external AC/DC converter 1800 which delivers a digital supply voltage of ±5 V and is attached to a DC/DC converter 1810 which can deliver analog supply voltages of ±5 V and ±15 V as required for the interface device 10. Further, the DC/DC converter controls a

precision voltage reference 1820 which controls the 8 BNC inputs 1505 and the ADC 1530 as well as a digital/analog converter (DAC) 1830 which permits, via an output amplifier block with 4 output amplifiers 1840 and a 9-pin connector 1850, analog output direct from the DSP 1300 to an output device, e.g. printer device or monitor device, which can be attached via the 9-pin connector 1850, thus providing the option of monitoring the data transferred to the host device or also, for example, of viewing an FFT to obtain rapid and comprehensive data analysis without using processor time of the host device.

In Fig. 2 the memory means 14 of Fig. 1 is implemented by an EPROM 1400 which, in a preferred embodiment of the present invention, contains the operating system of the digital signal processor 1300. A random access memory with an access time of 15 ns and a size of 512 KB or optionally 1024 KB 1420 serves as a data buffer to achieve independence in terms of time of the output line 16 from the output lines 11a, 11b and 11c to the data transmit/receive device and to the host device respectively. As described above, in a preferred embodiment of the present invention the digital signal processor 1300 already contains a 20-KB on-chip RAM 1440 which can store certain instruction sets, functions and also smaller application software units.

The connection, symbolized by the line 16, of the interface device 10 to any data transmit/receive device implements, by means of the blocks 1505 – 1535, an analog input with a sampling rate of 1.25 MHz and quantization of 12 bits. There are 8 channels with an overvoltage protection of ± 75 V. By means of the programmable amplifier 1525 the channels can be programmed independently of each other in voltage ranges up to a maximum of ± 10 V. Unused channels can be grounded internally to reduce channel intermodulation. The block 1515 is implemented as a monolithic high-precision, high-speed sample/hold amplifier for simultaneous sampling of all channels. The precision voltage reference 1820 provides a high-precision, temperature-compensated monolithic energy gap voltage reference for auto-calibration of each channel and each gain. Further, offset fine adjustment for each channel is implemented by the same.

The blocks 1830, 1840 and 1850 implement a direct analog output for the digital signal processor 1300, and the DAC 1830 provides a data transfer rate of 625 kHz and a quantization of 12 bits. The block 1840 comprises 4 channels with a common output latch.

Further, the interface device 10 comprises a digital input/output device implemented by the blocks 1284 and 1282. Here there are 8 digital inputs, 8 digital outputs with a common latch, and the digital port can be attached preferably to a side panel of the interface device 10 so that the port itself can easily be accessed.

The digital signal processor 1300 provides on-board digital data processing. In particular, it is a high-performance DSP with a clock speed of 80 MHz and a 20-bit timer 1535.

As described above, the first connecting device 12 comprises the SCSI interface 1220 with a peak transfer rate of 10 MBps. An optional PCMCIA-to-SCSI adapter permits high-speed communication with laptop computers which are desirable and in widespread use, particularly by mobile service technicians. The EPP 1260 with its associated connector 1280 permits data transfer at a more moderate rate.

As described above, the interface device 10 is supplied with power by means of an external AC/DC adapter which has a universal power input (85 – 264 VAC, 47 – 63 Hz). Interference suppression complies with the standards EN 55022, curve B and FFC, Class B). Further, it is also in accordance with international safety regulations (TÜV, UL, CSA). The interface device 10 is externally shielded and achieves a value of 55 dB at 30 – 60 MHz and a value of approximately 40 dB at 1 GHz, and therefore complies with the MILSTD 285-1 standard.

As described above, communication between the host device and the multi-purpose interface can take place not only via drivers for input/output device customary in a host device which reside in the BIOS system of the host device but also via specific interface drivers which, in the case of SCSI interfaces, are known as multi-purpose interface ASPI (advanced SCSI programming interface) drivers. This ASPI driver, which can also be referred to as an ASPI manager, is specific to a special SCSI host

adapter, i.e. to a special multi-purpose interface, and is normally included by the manufacturer of the multi-purpose interface. Generally speaking, this multi-purpose interface driver has the task of moving precisely specified SCSI commands from the host system program to the host system SCSI adapter. For this reason, the command set is almost identical to that of the SCSI interface itself. Essentially, only status and reset commands for the host adapter have been added.

The ASPI driver can be used if the hard disk was not already addressable at boot time or if the SCSI-related BIOS routines of the host computer were still disabled. Here too, the steps needed to initialize the interface device, preferably as a virtual hard disk, are similar to the steps taken when initializing at boot time.

In general terms, the ASPI manager comprises two sides. One side is the proprietary, hardware-oriented side. It is responsible for converting all commands into a form required by the corresponding multi-purpose interface. The hardware-oriented side of the ASPI driver is therefore matched to a very specific type of multi-purpose interface or SCSI interface. The other side is known as the user software side. This side is totally independent of the proprietary operating characteristics of the SCSI adapter and is therefore identical for all SCSI interfaces. This permits SCSI programming which is however independent of the individual SCSI adapter types.

In contrast to communication between the host device and the interface device according to the present invention on the basis of a BIOS driver, the use of such an ASPI driver for communication between the host device and the interface device according to the present invention allows various further possibilities of the SCSI multi-purpose interface to be exploited. In the case described above, the interface device which preferably signs on and behaves as a virtual hard disk is detected by the BIOS driver of the host computer at boot time and is configured as a hard disk. This step does not however support active requests sent by the interface device to the host computer. If however the virtual hard disk wishes to write data actively to, for example, a hard disk of the host computer or wishes to initiate communication with the processor of the host computer, the host computer must recognize the request of the virtual hard disk and tolerate a further issuer of instructions on its bus. If the interface device behaves solely like a virtual hard disk, it would always receive and

never issue commands. The BIOS has no objections to an additional issuer of commands that actively wishes to place data on the bus of the host device but the BIOS does not support the host device in recognizing corresponding requests of the interface device or in granting the interface device permission to access the bus.

Using the ASPI manager the interface device according to the present invention can now obtain active access to an SCSI hard disk of the host device connected to the same SCSI bus which, in contrast to the interface device, cannot be a virtual but a real SCSI mass storage device or also a further interface device according to the present invention. Thereupon, the interface device according to the present invention can write the desired data to the SCSI hard disk of the host computer totally independently of the host computer or can communicate with the same in some other manner. The interface device according to the present invention therefore initially behaves passively as a virtual hard disk and then, as required and using the driver software for the multi-purpose interface, actively on the same SCSI bus. This means however that the interface device according to the present invention, using a driver software for the multi-purpose interface which comprises the BIOS routines customary in host devices and simultaneously provides the option of active participation, can, regardless of the type of the data transmit/receive device attached to the second connecting device, behave initially as a virtual and at the same time passive hard disk but can, as required, participate actively on the bus so as to be able to initiate communication directly with other SCSI hard disks of the host device by bypassing the processor of the host device.

Using a standard interface of a host device, the interface device according to the present invention permits communication with any host device. By simulating an input/output device to the host device and, in a preferred embodiment, by simulating a virtual mass storage device, the interface device 10 is automatically supported by all known host systems without any additional sophisticated driver software. The simulation of a freely definable file structure on the "virtual" hard disk provides simple operation and expansion options and, through the implementation of any programs, independence from special software implemented on the host device. Help files included on the interface device 10 and plug-and-play support ensure ease of use even in portable, flexible host devices. Despite the very simple user interface,

experienced users are free at any time to intervene in the functions of the interface device 10 on system level. The interface device 10 thus provides a universal solution which can cover the entire spectrum of possible data transmit/receive devices.

Claims

Sub B1

1. An interface device for communication between a host device, which comprises drivers for input/output devices customary in a host device and a multi-purpose interface, and a data transmit/receive device comprising the following features:

   a processor;

   a memory;

   a first connecting device for interfacing the host device with the interface device via the multi-purpose interface of the host device; and

   a second connecting device for interfacing the interface device with the data transmit/receive device,

   wherein the interface device is configured by the processor and the memory in such a way that the interface device, when receiving an inquiry from the host device as to the type of a device attached to the multi-purpose interface of the host device, sends a signal, regardless of the type of the data transmit/receive device attached to the second connecting device of the interface device, to the host device which signals to the host device that it is an input/output device customary in a host device, whereupon the host device communicates with the interface device by means of the driver for the input/output device customary in a host device.

2. An interface device according to claim 1,

   wherein the drivers for input/output drivers customary in a host device comprise a hard disk driver, and the signal indicates to the host device that the host device is communicating with a hard disk.

3. An interface device according to claim 1,

wherein the memory means comprises a buffer to buffer data to be transferred between the data transmit/receive device and the host device.

4. An interface device according to claim1,

wherein the multi-purpose interface of the host device is an SCSI interface and the first connecting device also comprises an SCSI interface.

5. An interface device according to claim 1,

wherein the second connecting device comprises an analog input with a subsequent A/D converter in order to transfer analog data to the host device from a data transmit/receive device connectable to the analog device.

6. An interface device according to claim 1,

wherein the processor is a digital signal processor.

7. An interface device according to claim 2,

wherein the data to be transferred from the data transmit/receive device to the host device in the interface device is formatted in a suitable format for a hard disk present in the host device.

8. An interface device according to claim 2,

which further comprises a root directory and virtual files which are present on the signaled hard disk drive and which can be accessed from the host device.

9. An interface device according to claim 8,

wherein the virtual files comprise a configuration file in text format which are stored in the memory means and using which the user can configure the interface

device for a specific data transmit/receive device.

9 7
10. An interface device according to claim 8,

wherein the virtual files comprise batch files or executable files for the microprocessor means which are stored in the interface device in order to perform data processing, independently of the host device, of data received via the second connecting device.

10 7
11. An interface device according to claim 8,

wherein the virtual files comprise batch files or executable files for the host device which are stored in the interface device.

Sub B2 > 12. An interface device for communication between a host device, which comprises a multi-purpose interface and a specific driver for this interface, and a data transmit/receive device comprising the following features:

a processor;

a memory;

a first connecting device for interfacing the host device with the interface device via the multi-purpose interface of the host device; and

a second connecting device for interfacing the interface device with the data transmit/receive device,

where the interface device is configured using the processor and the memory in such a way that the interface device, when receiving an inquiry from the host device as to the type of a device attached at the multi-purpose interface of the host device, sends a signal, regardless of the type of the data transmit/receive device attached to the second connecting device of the interface device, to the host device which signals to the host device that it is an input/output device customary in a

host device, whereupon the host device communicates with the interface device by means of the specific driver for the multi-purpose interface.

B2 13. An interface device according to claim 12,

wherein, in addition to the first connecting device of the interface device, there is a further input/output device at the multi-purpose interface of the host device, and wherein the interface device can communicate directly with the hard disk via the specific driver for the multi-purpose interface.

13 14. An interface device according to claim ~~12~~ 11,

wherein the multi-purpose interface is an SCSI interface, and wherein the specific driver for the multi-purpose interface is an ASPI manager.

Sub B3 15. A method of communication between a host device, which comprises drivers for input/output devices customary in a host device and a multi-purpose interface, and a data transmit/receive device via an interface device comprising the following steps:

interfacing of the host device with a first connecting device of the interface device via the multi-purpose interface of the host device;

interfacing of the data transmit/receive device with a second connecting device of the interface device;

inquiring by the host device at the interface device as to the type of device to which the multi-purpose interface of the host device is attached;

regardless of the type of the data transmit/receive device attached to the second connecting device of the interface device, responding to the inquiry from the host device by the interface device in such a way that it is an input/output device customary in a host device, whereupon the host device communicates with the

interface device by means of the usual driver for the input/output device.

16. A method according to claim 15,

wherein the drivers for input/output devices customary in a host device comprise a driver for a storage device and in particular for a hard disk drive.

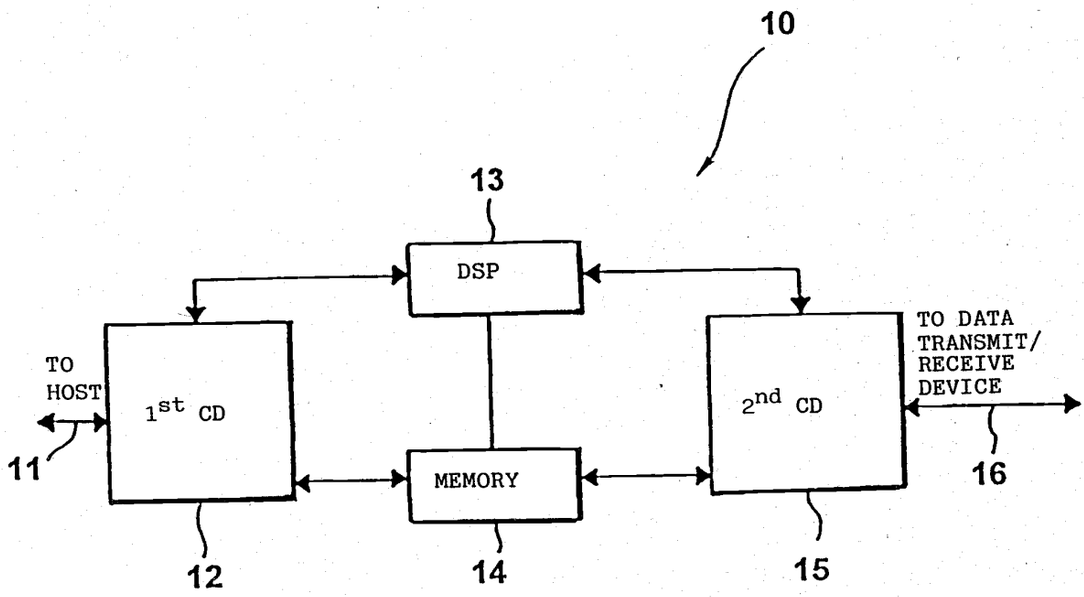

FIG.1

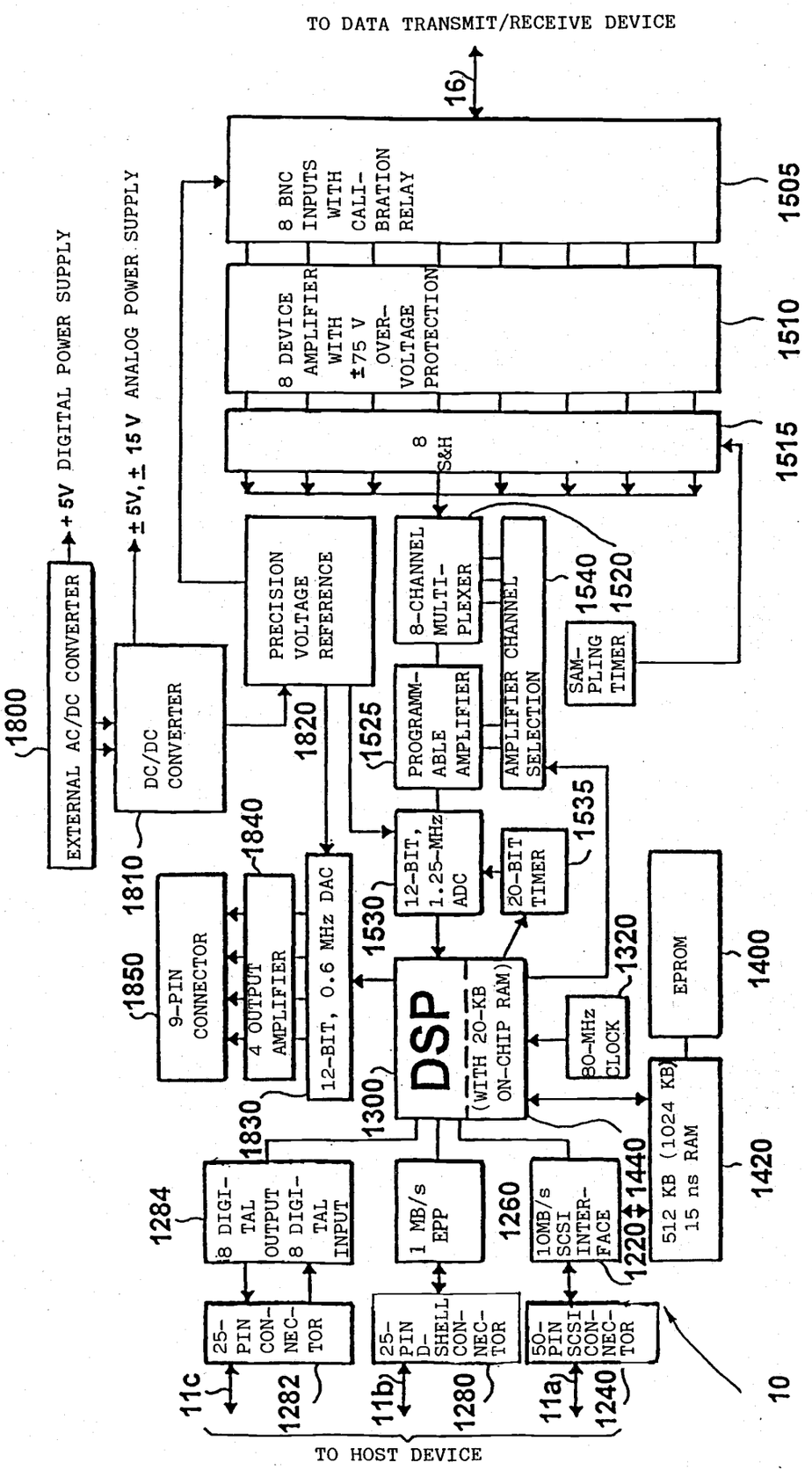
TO DATA TRANSMIT/RECEIVE DEVICE
16
8 BNC INPUTS WITH CALI-BRATION RELAY
1505
8 DEVICE AMPLIFIER WITH ±75 V OVER-VOLTAGE PROTECTION
1510
8 S&H
1515
8-CHANNEL MULTI-PLEXER
1520
AMPLIFIER CHANNEL SELECTION
1540
SAM-PLING TIMER
PROGRAMM-ABLE AMPLIFIER
1525
PRECISION VOLTAGE REFERENCE
1820
1800
EXTERNAL AC/DC CONVERTER
+ 5V DIGITAL POWER SUPPLY
DC/DC CONVERTER
± 5V, ± 15 V ANALOG POWER SUPPLY
1810
1840
1850
9-PIN CONNECTOR
4 OUTPUT AMPLIFIER
12-BIT, 0.6 MHz DAC
1530
12-BIT, 1.25-MHz ADC
20-BIT TIMER
1535
DSP
(WITH 20-KB ON-CHIP RAM)
1300
1320
80-MHz CLOCK
EPROM
1400
1830
1284
8 DIGI-TAL OUTPUT 8 DIGI-TAL INPUT
1 MB/s EPP
1260
10MB/s SCSI INTER-FACE
1220
1440
512 KB (1024 KB) 15 ns RAM
1420
25-PIN CON-NEC-TOR
1282
25-PIN D-SHELL CON-NEC-TOR
1280
50-PIN SCSI CON-NEC-TOR
1240
11c
11b
11a
10
TO HOST DEVICE

FIG.2

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Flexible Schnittstelle

Flexible Schnittstelle

Beschreibung

Die vorliegende Erfindung bezieht sich auf die Übertragung von Daten und insbesondere auf Schnittstellengeräte zur Kommunikation zwischen einem Computer oder Hostgerät und einer Datensende/Empfangseinrichtung, von der Daten erfaßt werden sollen, bzw. mit der zweiseitig kommuniziert werden soll.

Bisherige Datenerfassungssysteme für Computer sind sehr stark in ihrem Einsatzbereich limitiert. Allgemein können dieselben in zwei Gruppen eingeteilt werden.

Bei der ersten Gruppe werden Hostgeräte oder Computersysteme mittels einer Schnittstelle mit einem Gerät verbunden, dessen Daten erfaßt werden sollen. Die Schnittstellen dieser Gruppe sind üblicherweise Standardschnittstellen, die mit spezieller Treibersoftware für verschiedene Hostsysteme einsetzbar sind. Ein Vorteil dieser Schnittstellengeräte besteht darin, daß sie vom Hostgerät weitgehend unabhängig sind. Nachteilig ist jedoch, daß sie im allgemeinen sehr aufwendige Treiber benötigen, die störungsanfällig sind und die Datenübertragungsraten zwischen dem mit der Schnittstelle verbundenen Gerät und dem Hostgerät und umgekehrt limitieren. Ferner sind Implementationen dieser Schnittstellen für tragbare Systeme teilweise nur schwer möglich und die Anpassungsmöglichkeiten sind gering, weshalb diese Systeme eine geringe Flexibilität besitzen.

Die Geräte, von denen Daten zu erfassen sind, besetzen die ganze Bandbreite der Elektrotechnik. So ist bei einem typischen Szenario davon auszugehen, daß ein Kunde, der beispielsweise im medizintechnischen Bereich eine Röntgendiagnoseanlage betreibt, über einen Fehler berichtet. Ein Servicemitarbeiter des Geräteherstellers wird dann zu dem Kunden gehen und von dem Röntgendiagnosegerät erstellte

Systemprotokolldateien beispielsweise mittels eines tragbaren Computer oder Laptops auslesen. Wenn der Fehler dann nicht zu lokalisieren ist, oder wenn ein Fehler nur sporadisch auftritt, wird es erforderlich sein, daß der Servicemitarbeiter nicht nur eine Fehlerprotokolldatei sondern auch Daten aus dem laufenden Betrieb auslesen muß. Es ist offensichtlich, daß hier eine schnelle Datenübertragung sowie eine schnelle Datenanalyse notwendig ist.

Ein anderer Fall zum Einsatz einer Schnittstelle kann beispielsweise das Verbinden eines elektronischen Meßgeräts, z. B. eines Multimeters, mit einem Computersystem sein, um von dem Multimeter gemessene Daten auf den Computer zu übertragen. Insbesondere bei Langzeitmessungen oder beim Auftreten großer Datenmengen ist es erforderlich, daß die Schnittstelle eine hohe Datenübertragungsrate ermöglicht.

Aus diesen zufällig gewählten Beispielen ist zu sehen, daß die Einsatzmöglichkeiten einer Schnittstelle völlig voneinander unterschiedlich sein können. Es ist daher wünschenswert, daß eine Schnittstelle derart flexibel ist, daß mittels einer Schnittstelle sehr unterschiedliche elektrische oder elektronische Systeme mit einem Hostgerät verbunden werden können. Um Fehlbedienungen zu vermeiden, ist es ferner wünschenswert, daß ein Servicemitarbeiter nicht für jede unterschiedliche Anwendung unterschiedliche Schnittstellen auf unterschiedliche Art und Weise bedienen muß, sondern daß möglichst eine universelle Schnittstellenbedienung für eine große Anzahl von Einsatzmöglichkeiten geschaffen wird.

Um die Datenübertragungsraten über eine Schnittstelle zu erhöhen, wurde bei der zweiten Gruppe von Schnittstellengeräten der Weg beschritten, die Schnittstelle sehr stark an individuelle Hostsysteme oder Computersysteme einzeln anzupassen. Der Vorteil dieser Lösung besteht darin, daß hohe Transferraten möglich sind. Ein Nachteil ist jedoch, daß die Treiber für die Schnittstellen der zweiten Gruppe sehr stark

an ein einziges Hostsystem angepaßt sind, weshalb sie im allgemeinen nicht oder nur sehr uneffektiv für andere Hostsysteme einsetzbar sind. Ferner weisen diese Typen von Schnittstellen den Nachteil auf, daß sie im Computergehäuse montiert werden müssen, da sie auf das interne Hostbussystem zugreifen, um maximale Datenübertragungsraten zu erreichen. Sie sind daher im allgemeinen nicht für tragbare Hostsysteme in Form von Laptops geeignet, die aufgrund ihrer möglichst geringen Größe kein freies Innenvolumen zum Einstecken einer Schnittstellenkarte besitzen.

Eine Lösung für dieses Problem bieten Schnittstellengeräte der Firma IOtech (Geschäftsadresse: 25971 Cannon Road, Cleveland, Ohio 44146, USA), die für Laptops geeignet sind, wie z. B. das Modell WaveBook/512 (eingetragenens Warenzeichen). Die Schnittstellengeräte werden mittels einer steckbaren, etwa scheckkartengroßen Einsteckkarte mit der PCMCIA-Schnittstelle, die mittlerweile an Laptops standardmäßig vorgesehen sind, verbunden. Die Einsteckkarte bewirkt eine Transformation der PCMCIA-Schnittstelle zu einer in der Technik bekannten Schnittstelle IEEE 1284. Die genannte Steckkarte schafft eine bezüglich der Datenrate erweiterte Spezial-Druckerschnittstelle, die eine Datenübertragungsrate von etwa 2 MB/s im Gegensatz zu einer Rate von etwa 1MB/s bei bekannten Druckerschnittstellen liefert. Das bekannte Schnittstellengerät besteht im allgemeinen aus einem Treiberbaustein, einem digitalen Signalprozessor, einem Puffer und einer Hardwarebaugruppe, die in einem Verbinder mündet, an dem das Gerät angeschlossen wird, dessen Daten zu erfassen sind. Der Treiberbaustein ist direkt mit der erweiterten Druckerschnittstelle verbunden, wodurch die bekannte Schnittstelleneinrichtung eine Verbindung zwischen einem Computer und dem Gerät herstellt, dessen Daten erfaßt werden sollen.

Um mit der genannten Schnittstelle zu arbeiten, muß ein schnittstellenspezifischer Treiber in dem Hostgerät installiert werden, damit das Hostgerät mit dem digitalen

Signalprozessor der Schnittstellenkarte kommunizieren kann. Wie es bereits erwähnt wurde, muß der Treiber auf dem Hostgerät installiert werden. Ist der Treiber ein speziell für das Hostgerät entworfener Treiber, so wird zwar eine schnelle Datenübertragung ermöglicht, der Treiber kann jedoch nicht ohne weiteres auf einem anderen Hostsystem installiert werden. Ist der Treiber jedoch ein möglichst flexibler allgemeiner Treiber, der für viele Hostgeräte einsetzbar ist, dann müssen Kompromisse bezüglich der Datenübertragungsrate in Kauf genommen werden.

Speziell bei einer Anwendung für Multi-Tasking-Systeme, bei denen mehrere verschiedene Aufgaben, wie z. B. eine Datenerfassung, eine Datendarstellung oder ein Editieren im wesentlichen gleichzeitig zu bearbeiten sind, wird üblicherweise jeder Aufgabe vom Hostsystem eine gewisse Priorität zugeordnet. Ein Treiber, der eine spezielle Aufgabe unterstützt, fragt im zentralen Verarbeitungssystem des Hostgeräts an, ob er Prozessorresourcen haben kann, um seine Aufgabe zu erledigen. Abhängig vom jeweiligen Prioritätszuweisungsverfahren und abhängig von der Implementation des Treibers wird eine spezielle Aufgabe einen bestimmten Anteil der Prozessorresourcen in bestimmten Zeitschlitzen erhalten. Konflikte ergeben sich dann, wenn einer oder mehrere Treiber derart implementiert sind, daß sie standardmäßig die höchste Priorität haben, d. h. daß sie inkompatibel sind, wie es bei vielen Anwendungen in der Praxis der Fall ist. So kann es vorkommen, daß beide Treiber eingestellt sind, um die höchste Priorität zu haben, was im schlimmsten Fall sogar zu einem Systemabsturz führen kann.

Die EP 0685799 A1 offenbart eine Schnittstelle mittels derer mehrere Peripheriegeräte an einen Bus angeschlossen werden können. Eine Schnittstelle ist zwischen den Bus eines Hostgeräts und verschiedene Peripheriegeräte geschaltet. Die Schnittstelle umfaßt eine Zustandsmaschine sowie mehrere jeweils einem Peripheriegerät zugeordnete Zweige. Jeder Zweig umfaßt einen Daten-Manager, eine Zyklussteuerung, eine

Benutzerlogik sowie einen Puffer. Dieses bekannte Schnittstellengerät schafft eine optimale Anpassung zwischen einem Hostgerät und einem speziellen Peripheriegerät.

Die Fachveröffentlichung IBM Technical Disclosure Bulletin, Bd. 38, Nr. 05, S. 245; "Communication Method between Devices through FDD Interface" offenbart eine Schnittstelle, die ein Hostgerät über eine Diskettenlaufwerksschnittstelle mit einem Peripheriegerät verbindet. Die Schnittstelle besteht insbesondere aus einem Adressengenerator, einem MFM-Decodierer/Codierer, einem Seriell/Parallel-Wandler und einem Formatsignalgenerator. Durch die Schnittstelle ist es möglich, an den FDD-Host-Controller eines Hostgeräts nicht nur ein Diskettenlaufwerk sondern auch ein anderes Peripheriegerät anzuschließen. Das Hostgerät nimmt dabei an, daß an seiner Diskettenlaufwerksteuerung immer ein Diskettenlaufwerk angeschlossen ist, wobei bei einer Adressenübereinstimmung eine Kommunikation startet. Die Schrift enthält jedoch keinen Hinweis darauf, wie eine Kommunikation möglich werden soll, wenn die Schnitttstelle statt an eine Diskettenlaufwerkssteuerung an eine Vielzweckschnittstelle angeschlossen wird.

Die Aufgabe der vorliegenden Erfindung besteht darin, ein Schnittstellengerät zur Kommunikation zwischen einem Hostgerät und einer Datensende/Empfangseinrichtung zu schaffen, das unabhängig vom Hostgerät einsetzbar ist und eine hohe Datenübertragungsrate ermöglicht.

Diese Aufgabe wird durch ein Schnittstellengerät gemäß Anspruch 1 oder 12 sowie durch ein Verfahren gemäß Anspruch 15 gelöst.

Der vorliegenden Erfindung liegt die Erkenntnis zugrunde, daß sowohl eine hohe Datenübertragungsrate als auch eine vom Hostgerät unabhängige Einsetzbarkeit erreicht werden können, wenn auf einen Treiber für ein Hostgerät-übliches Eingabe/Ausgabe-Gerät zurückgegriffen wird, der üblicherweise in

den allermeisten auf dem Markt verfügbaren Hostgeräten vorhanden ist. Treiber für Hostgerät-übliche Eingabe/Ausgabe-Geräte, die praktisch in jedem Hostgerät vorhanden sind, sind beispielsweise Treiber für Festplatten, Graphikgeräte oder Druckergeräte. Da jedoch die Festplattenschnittstellen bei den üblichen Hostgeräten, die beispielsweise IBM-PCs, IBM-kompatible-PCs, Commodore-PCs, Apple-Computer oder auch Workstations sein können, die Schnittstellen mit der schnellsten Datenübertragungsrate sind, wird bei dem bevorzugten Ausführungsbeispiel des Schnittstellengeräts der vorliegenden Erfindung auf den Treiber für die Festplatte zurückgegriffen. Auf Treiber für andere Speichergeräte, wie z. B. Diskettenlaufwerke, CD-ROM-Laufwerke oder Bandlaufwerke, könnte jedoch ebenfalls zurückgegriffen werden, um das Schnittstellengerät gemäß der vorliegenden Erfindung zu implementieren.

Wie es weiter hinten noch ausgeführt wird, soll das erfindungsgemäße Schnittstellengerät mit einer Vielzweckschnittstelle des Hostgeräts, die z. B. als SCSI-Schnittstelle oder erweiterte Druckerschnittstelle implementiert sein kann, mit demselben verbunden werden. Vielzweckschnittstellen umfassen zum einen eine Schnittstellenkarte und zum anderen eine dafür spezifische Treibersoftware. Die Treibersoftware kann so ausgestaltet sein, daß sie BIOS-Treiberroutinen ersetzen kann. Die Kommunikation zwischen dem Hostgerät und den an der Vielzweckschnittstelle angeschlossenen Geräten findet dann im wesentlichen mittels der für die Vielzweckschnittstelle spezifischen Treibersoftware statt und nicht mehr überwiegend durch BIOS-Routinen des Hostgeräts. Neuerdings können jedoch auch Treiber für Vielzweckschnittstellen bereits im BIOS-System des Hostgeräts integriert sein, da Vielzweckschnittstellen neben den klassischen Eingabe/Ausgabe-Schnittstellen für Hostgeräte immer üblicher werden. Selbstverständlich ist es ebenfalls möglich, BIOS-Routinen parallel zu der spezifischen Treibersoftware für die Vielzweckschnittstelle zu verwenden, wenn es erwünscht ist.

Das Schnittstellengerät gemäß der vorliegenden Erfindung umfaßt eine Prozessoreinrichtung, eine Speichereinrichtung, eine erste Verbindungseinrichtung zum schnittstellenmäßigen Verbinden des Hostgeräts mit dem Schnittstellengerät und eine zweite Verbindungseinrichtung zum schnittstellenmäßigen Verbinden des Schnittstellengeräts mit der Datensende/Empfangseinrichtung. Das Schnittstellengerät wird durch die Prozessoreinrichtung und die Speichereinrichtung derart konfiguriert, daß das Schnittstellengerät bei einer Anfrage des Hostgeräts über die erste Verbindungseinrichtung, die die Art eines Geräts betrifft, das mit dem Hostgerät verbunden ist, unabhängig von dem Typ der Datensende/Empfangseinrichtung ein Signal über die erste Verbindungseinrichtung zum Hostgerät sendet, das dem Hostgerät signalisiert, daß es mit einem Eingabe/Ausgabe-Gerät kommuniziert. Das Schnittstellensystem gemäß der vorliegenden Erfindung simuliert somit sowohl hardware- als aus auch softwaretechnisch die Funktionsweise eines üblichen Eingabe/Ausgabe-Geräts und vorzugsweise eines Festplattenlaufwerks. Da die Unterstützung von Festplatten in allen verfügbaren Hostsystemen standardmäßig implementiert ist, kann beispielsweise die Simulation einer Festplatte die Unabhängigkeit vom verwendeten Hostsystem erreichen. Das erfindungsgemäße Schnittstellengerät kommuniziert somit mit dem Hostgerät oder Computer nicht mehr über einen speziell entworfenen Treiber sondern über ein in dem BIOS-System (BIOS = Basic Input/Output System = Grund Eingabe/Ausgabe System) vorhandenes Programm, das üblicherweise genau auf das spezielle Computersystem abgestimmt ist, auf dem es installiert ist, bzw. über ein für die Vielzweckschnittstelle spezifisches Programm. Somit vereinigt das Schnittstellengerät gemäß der vorliegenden Erfindung die Vorteile beider Gruppen. Zum einen findet die Datenkommunikation zwischen dem Computer und der Schnittstelle über ein Hostgerät-spezifisches BIOS-Programm bzw. über ein auf die Vielzweckschnittstelle zugeschnittenes Treiberprogramm statt, das als "gerätespezifischer Treiber" angesehen werden könnte. Zum anderen ist das BIOS-Programm bzw. ein entsprechendes Vielzweckschnittstellenprogramm, das

eine der üblichen Eingabe/Ausgabe-Schnittstellen in Hostsystemen bedient, in eben jedem Hostsystem vorhanden, weshalb das Schnittstellengerät gemäß der vorliegenden Erfindung Hostgerät-unabhängig ist.

Bevorzugte Ausführungsbeispiele der vorliegenden Erfindung werden nachfolgend bezugnehmend auf die beiliegenden Zeichnungen detaillierter erläutert. Es zeigen:

Fig. 1 ein prinzipielles Blockschaltbild des Schnittstellengeräts gemäß der vorliegenden Erfindung; und

Fig. 2 ein detailliertes Blockschaltbild eines Schnittstellengeräts gemäß einem bevorzugten Ausführungsbeispiel der vorliegenden Erfindung.

Fig. 1 zeigt ein prinzipielles Blockschaltbild eines Schnittstellengeräts 10 gemäß der vorliegenden Erfindung. Über eine Hostleitung 11 ist eine erste Verbindungseinrichtung 12 des Schnittstellengeräts 10 mit einem Hostgerät (nicht gezeigt) verbindbar. Die erste Verbindungseinrichtung ist sowohl an einen digitalen Signalprozessor 13 als auch an einen Speicher 14 angeschlossen. Der digitale Signalprozessor 13 sowie der Speicher 14 sind ferner mittels bidirektionaler Kommunikationsleitungen (bei allen Leitungen durch zwei Richtungspfeile angezeigt) mit einer zweiten Verbindungseinrichtung 15 gekoppelt. Mittels einer Ausgangsleitung 16 kann die zweite Verbindungseinrichtung mit einer Sende/Empfangseinrichtung gekoppelt werden, die Daten von dem Hostgerät empfangen soll oder von der Daten ausgelesen, d. h. erfaßt, und zu dem Hostgerät übertragen werden sollen. Über die erste und die zweite Verbindungseinrichtung kann die Sende/Empfangseinrichtung selbst ebenfalls aktiv mit dem Hostgerät kommunizieren, wie es weiter hinten noch detaillierter dargestellt wird.

Die Kommunikation zwischen dem Hostsystem oder Hostgerät und dem SWchnittstellengerät basiert auf bekannten Standard-Zu-

griffsbefehlen, wie sie von allen bekannten Betriebssystemen (z. B. DOS, Windows, Unix) unterstützt werden. Vorzugsweise simuliert das Schnittstellengerät gemäß der vorliegenden Erfindung eine Festplatte mit einem Wurzelverzeichnis oder "Root-Directory", dessen Einträge "virtuelle" Dateien sind, die für verschiedenste Funktionen angelegt werden können. Wenn das Hostgerätsystem, mit dem das Schnittstellengerät gemäß der vorliegenden Erfindung verbunden ist, wobei mit dem Schnittstellengerät 10 ferner eine Sende/Empfangseinrichtung verbunden ist, hochgefahren wird, geben übliche BIOS-Routinen oder Vielzweckschnittstellenprogramme an in dem Hostgerät vorhandene Eingabe/Ausgabe-Schnittstellen einen Befehl aus, der in der Fachwelt als Befehl "INQUIRY" ("Erkundigung") bekannt ist. Über die erste Verbindungseinrichtung wird der digitale Signalprozessor 13 diese Anfrage empfangen und ein Signal erzeugen, das wiederum über die erste Verbindungseinrichtung 12 und die Hostleitung 11 zum Hostgerät (nicht gezeigt) gesendet wird. Dieses Signal wird dem Hostgerät signalisieren, daß an der betreffenden Schnittstelle, zu der der Befehl INQUIRY gesendet wurde, z. B. ein Festplattenlaufwerk angeschlossen ist. Optional kann das Hostgerät einen für Fachleute bekannten Befehl "Test Unit Ready" zum Schnittstellengerät senden, der genauere Details bezüglich des angefragten Geräts wünscht.

Unabhängig davon, welche Sende/Empfangseinrichtung an der Ausgangsleitung 16 mit der zweiten Verbindungseinrichtung verbunden ist, teilt der digitale Signalprozessor 13 dem Hostgerät mit, daß das Hostgerät mit einem Festplattenlaufwerk kommuniziert. Empfängt das Hostgerät die Antwort, daß ein Laufwerk vorhanden ist, wird es nun die Aufforderung zum Schnittstellengerät 10 schicken, die Boot-Sequenz, die sich üblicherweise bei tatsächlichen Festplatten auf den ersten Sektoren derselben befindet, zu lesen. Der digitale Signalprozessor 13, dessen Betriebssystem in der Speichereinrichtung 14 gespeichert ist, wird diesen Befehl beantworten, indem er eine virtuelle Boot-Sequenz zum Hostgerät sendet, die bei tatsächlichen Laufwerken den Typ, die Startposition

und die Länge der FAT (FAT = File Allocation Table = Dateipositionstabelle), die Anzahl der Sektoren, usw. enthält, wie es für Fachleute bekannt ist. Wenn das Hostgerät diese Daten empfangen hat, geht es davon aus, daß das Schnittstellengerät 10 gemäß einem bevorzugten Ausführungsbeispiel der vorliegenden Erfindung ein Festplattenlaufwerk ist. Auf einen Befehl vom Hostgerät, das Verzeichnis des "virtuellen" Festplattenlaufwerks, das von der Schnittstelleneinrichtung 10 dem Hostgerät gegenüber simuliert wird, anzuzeigen, kann der digitale Signalprozessor dem Hostgerät genauso antworten, wie es eine herkömmliche Festplatte tun würde, nämlich indem auf Anfrage die Dateipositionstabelle oder FAT auf einem in der Bootsequenz bestimmten Sektor, der im allgemeinen der erste beschreibbare Sektor ist, gelesen wird und zum Hostgerät übertragen wird, und indem im Anschluß die Datenverzeichnisstruktur der virtuellen Festplatte übertragen wird. Es ist ferner möglich, daß die FAT erst direkt vor dem Lesen oder Speichern von Daten der "virtuellen" Festplatte gelesen wird und nicht bereits beim Initialisieren.

Bei einem bevorzugten Ausführungsbeispiel der vorliegenden Erfindung umfaßt der digitale Signalprozessor 13, der nicht unbedingt als digitaler Signalprozessor sondern auch als beliebiger anderer Mikroprozessor ausgeführt sein kann, einen ersten und einen zweiten Befehlsinterpretierer. Der erste Befehlsinterpretierer führt die gerade genannten Schritte durch, während der zweite Befehlsinterpretierer die Lese/Schreib-Zuordnung zu bestimmten Funktionen durchführt. Besteht nun der Wunsch des Benutzers, von der Sende/Empfangseinrichtung über die Leitung 16 Daten zu lesen, so schickt das Hostgerät einen Befehl zur Schnittstelleneinrichtung, der beispielsweise "Lese Datei xy" lauten könnte. Wie es bereits erwähnt wurde, erscheint die Schnittstelleneinrichtung dem Hostgerät gegenüber wie eine Festplatte. Die zweite Interpretiereinrichtung des digitalen Signalprozessors interpretiert nun den Lesen-Befehl des Hostprozessors durch Entschlüsseln, ob "xy" beispielsweise eine Datei "Echtzeiteingabe", "Konfiguration" oder eine ausführbare

Datei bezeichnet, als Datenübertragungsbefehl, wodurch derselbe beginnt, von der Sende/Empfangseinrichtung über die zweite Verbindungseinrichtung Daten zur ersten Verbindungseinrichtung und über die Leitung 11 zum Hostgerät zu übertragen.

Vorzugsweise wird in einer nachfolgend beschriebenen Konfigurationsdatei die Menge von einer Datensende/Empfangseinrichtung zu erfassenden Daten angegeben, indem der Benutzer in der Konfigurationsdatei angibt, daß sich eine Messung z. B. über fünf Minuten erstrecken soll. Für das Hostgerät wird dann die Datei "Echtzeiteingabe" wie eine Datei erscheinen, deren Länge der in den fünf Minuten erwarteten Datenmenge entspricht. Für Fachleute ist es bekannt, daß die Kommunikation zwischen einem Prozessor und einer Festplatte darin besteht, daß der Prozessor der Festplatte Nummern von Blöcken oder Clustern oder Sektoren übermittelt, deren Inhalt er lesen möchte. Aus der FAT weiß der Prozessor, welche Informationen in welchem Block stehen. Die Kommunikation von dem Hostgerät zu dem Schnittstellengerät der vorliegenden Erfindung besteht also bei diesem Szenario in der sehr schnellen Übertragung von Blocknummern und vorzugsweise von Blocknummernbereichen, da eine "virtuelle" Datei "Echtzeiteingabe" nicht fragmentiert sein wird. Will nun das Hostgerät die Datei "Echtzeiteingabe" lesen, so übermittel es einen Bereich von Blocknummern zur Schnittstelleneinrichtung, woraufhin damit begonnen wird, daß über die zweite Verbindungseinrichtung Daten empfangen und über die erste Verbindungseinrichtung zu dem Hostgerät gesendet werden.

Die Speichereinrichtung 14 kann neben dem Befehlsspeicher für den digitalen Signalprozessor, der das Betriebssystem desselben umfaßt und als EPROM oder EEPROM ausgeführt sein kann, einen zusätzlichen Puffer aufweisen, der zu Synchronisationszwecken zwischen der Datenübertragung von der Sende/Empfangseinrichtung zur Schnittstelleneinrichtung 10 und der Datenübertragung von der Schnittstelleneinrichtung 10 zum Hostgerät dient.

Vorzugsweise ist der Puffer als schneller Direktzugriffsspeicher oder RAM-Puffer ausgeführt.

Der Benutzer kann ferner vom Hostgerät aus auf der Schnittstelleneinrichtung 10, die dem Hostgerät gegenüber wie eine Festplatte erscheint, eine Konfigurationsdatei erstellen, deren Einträge automatisch verschiedene Funktionen des Schnittstellengeräts 10 einstellen und steuern. Dies können beispielsweise Verstärkungs-, Multiplex- oder Abtastrateneinstellungen sein. Durch das Erstellen und Editieren einer Konfigurationsdatei, welche üblicherweise eine Textdatei ist, die ohne große Vorkenntnis einfach verständlich ist, kann der Benutzer der Schnittstelleneinrichtung 10 für nahezu beliebiege Sende/Empfangseinrichtungen, die über die Leitung 16 mit der zweiten Verbindungseinrichtung koppelbar sind, die im wesentlichen gleichen Bedienhandlungen durchführen, wodurch eine Fehlerquelle beseitigt wird, die daraus entsteht, daß ein Benutzer für verschiedene Anwendungen viele verschiedene Befehlcodes kennen muß. Bei der Schnittstelleneinrichtung 10 gemäß der vorliegenden Erfindung ist es lediglich notwendig, daß der Benutzer einmal die Konventionen der Konfigurationsdatei notiert, wonach er die Schnittstelleneinrichtung 10 als Schnittstelle zwischen einem Hostgerät und einem nahezu beliebigen Sende/Empfangsgerät verwenden kann.

Durch die Möglichkeit, beliebige Dateien in vereinbarten Formaten unter Berücksichtigung der maximalen Speicherkapazität der Speichereinrichtung auf der Schnittstelleneinrichtung 10 in der Speichereinrichtung 14 abzuspeichern, sind beliebige Erweiterungen oder sogar gänzlich neue Funktionen der Schnittstelleneinrichtung 10 ohne Zeitverlust zu realisieren. Selbst vom Hostgerät ausführbare Dateien, wie z. B. Stapeldateien oder ausführbare Dateien (BAT-Dateien oder EXE-Dateien) oder auch Hilfedateien können in der Schnittstelleneinrichtung implementiert werden und somit die Unabhängikeit der Schnittstelleneinrichtung 10 von jeglicher

zusätzlicher Software (abgesehen von den BIOS-Routinen) des Hostgeräts erreichen. Dies vermeidet zum einen Lizenz- bzw. Anmeldungsprobleme. Zum anderen werden Installationen von bestimmten Routinen, die oft verwendet werden können, wie z. B. eine FFT-Routine, um beispielsweise erfaßte Zeitbereichsdaten im Frequenzbereich betrachten zu können, hinfällig, da diese EXE-Dateien bereits auf der Schnittstelleneinrichtung 10 installiert sind und in dem virtuellen Wurzel-Verzeichnis erscheinen, durch das das Hostgerät auf alle beliebigen auf der Schnittstelleneinrichtung 10 gespeicherten Programme zugreifen kann.

Bei einem bevorzugten Ausführungsbeispiel der vorliegenden Erfindung, bei dem die Schnittstelleneinrichtung 10 dem Hostgerät gegenüber ein Festplattenlaufwerk simuliert, wird dieselbe bereits beim Einschalten oder Hochfahren des Hostsystems automatisch erkannt und zum Betrieb bereitgestellt. Dies entspricht dem derzeit immer weiter verbreiteten "Plug-and-Play"-Standard. Der Benutzer muß sich nicht mehr um die Installation der Schnittstelleneinrichtung 10 auf dem Hostgerät durch spezielle zu ladende Treiber kümmern, sondern die Schnittstelleneinrichtung 10 wird beim Hochfahren des Hostsystems automatisch zum Betrieb bereitgestellt.

Für Fachleute ist es jedoch offensichtlich, daß die Schnittstelleneinrichtung 10 nicht notwendigerweise beim Einschalten des Rechners angemeldet wird, sondern daß auf dem Hostgerät auch eine spezielle BIOS-Routine bzw. einen Treiber für eine Vielzweckschnittstelle während des Laufs des Rechners gestartet werden kann, um die Schnittstelleneinrichtung 10 als zusätzliche Festplatte anzubinden oder zu "mounten". Dieses Ausführungsbeispiel ist für größere Workstation-Systeme geeignet, welche im wesentlichen nie ausgeschaltet werden, da sie beispielsweise in einem "Multi-Tasking"-Environment z. B. Mail-Funktionen oder Prozeßüberwachungen, die ständig im Betrieb sind, durchführen werden.

Bei dem Schnittstellengerät gemäß der vorliegenden Erfindung besteht ein enormer Vorteil der Trennung der tatsächlichen Hardware, die zur Verbindung der Schnittstelleneinrichtung 10 mit der Sende/Empfangseinrichtung benötigt wird, wie es aus dem nachfolgend beschriebenen Ausführungsbeispiel offensichtlich ist, von der Kommunikations-Einheit, die durch den digitalen Signalprozessor 13, den Speicher 14 und die erste Verbindungseinrichtung 12 implementiert ist, darin, daß verschiedenste Gerätetypen parallel auf identische Weise bedient werden können. An ein Hostgerät können demnach viele Schnittstelleneinrichtungen 10 angeschlossen werden, dasselbe wird dann verschiedenste sozusagen "virtuelle" Festplatten sehen. Zum anderen ist auch eine eventuelle Änderung der speziellen Hardware, die durch die zweite Verbindungseinrichtung 15 symbolisiert ist, im wesentlichen ohne Veränderung der Bedienung der Schnittstellengeräts gemäß der vorliegenden Erfindung realisierbar. Ferner kann ein erfahrener Anwender jederzeit beliebig tief in die vorhandene zweite Verbindungseinrichtung eingreifen, indem er die oben erwähnte Option des Erstellens einer Konfigurationsdatei oder des Hinzufügens oder Abspeicherns neuer Programmteile für die zweite Verbindungseinrichtung verwendet.

Ein wesentlicher Vorteil der Schnittstelleneinrichtung 10 der vorliegenden Erfindung besteht ferner darin, daß sie extrem hohe Datenübertragungsraten ermöglicht, und zwar bereits dadurch, daß die Hostgerät-eigenen BIOS-Routinen, die vom Hersteller des Hostgeräts bzw. BIOS-Systems für jedes Hostgerät optimiert sind, zum Datenaustausch verwendet werden, bzw. daß üblicherweise vom Hersteller von Vielzweckschnittstellen optimierte und mitgelieferte Treiberprogramme verwendet werden. Außerdem werden die Daten aufgrund der Simulation eines virtuellen Massenspeichers so verwaltet und zur Verfügung gestellt, daß sie direkt gewissermaßen ohne Prozessorintervention des Hostgeräts auf andere Speichermedien, z. B. eine tatsächliche Festplatte des Hostgeräts, übertragen werden können. Die einzige Begrenzung für eine Langzeit-Datenübertragung mit hoher Geschwindigkeit ist

daher allein durch die Geschwindigkeit und Speichergröße des Massespeichers des Hostsystems gegeben. Dies ist der Fall, da der digitale Signalprozessor 13 die über die zweite Verbindungseinrichtung 15 von der Sende/Empfangseinrichtung eingelesenen Daten bereits in für eine Festplatte des Hostgeräts geeignete Blockgrößen formatiert, wodurch die Datenübertragungsgeschwindigkeit lediglich durch die mechanische Trägheit des Festplattensystems des Hostgeräts begrenzt ist. An dieser Stelle sei angemerkt, daß üblicherweise ein Datenfluß vom einem Hostgerät in Blöcke formatiert werden muß, um auf einer Festplatte geschrieben werden zu können und anschließend wiedergewonnen werden zu können, wie es für Fachleute bekannt ist.

Durch Einrichtung eines direkten Speicherzugriffs (DMA; DMA = Direct Memory Access) oder RAM-Laufwerks im Hostsystem kann die genannte Datenübertragungsrate nochmals erhöht werden. Wie es für Fachleute bekannt ist, benötigt die Einrichtung eines RAM-Laufwerks jedoch Prozessorresourcen des Hostgeräts, weshalb der Vorteil, bei dem die Daten auf ein Festplattenlaufwerk des Hostgeräts geschrieben werden, und im wesentlichen keine Prozessorresourcen benötigt werden, verlorengeht.

Wie es bereits erwähnt wurde, kann in dem Speicher 14 ein Datenpuffer implementiert sein, der die zeitliche Unabhängigkeit der Sende/Empfangseinrichtung, die mit der zweiten Verbindungseinrichtung gekoppelt ist, von dem Hostgerät, das mit der ersten Verbindungseinrichtung gekoppelt ist, ermöglicht. Auf diese Weise ist selbst bei zeitkritischen Anwendungen der einwandfreie Betrieb der Schnittstelleneinrichtung 10 sogar in Multi-Tasking-Hostsystemen gewährleistet.

Fig. 2 zeigt ein detailliertes Blockschaltbild einer Schnittstelleneinrichtung 10 gemäß der vorliegenden Erfindung.

Ein digitaler Signalprozessor (DSP) 1300 bildet gewissermaßen das Herzstück der Schnittstelleneinrichtung 10. Der DSP kann ein beliebiger DSP sein, wobei es jedoch bevorzugt wird, daß er einen Auf-Chip-Direkt-Zugriffsspeicher (RAM) von 20 KB aufweist. In dem Direktzugriffsspeicher, der bereits auf dem DSP integriert ist, können beispielsweise bestimmte Befehlssätze gespeichert sein. Mit dem DSP 1300 verbunden ist ein 80-MHz-Taktbauglied 1320, um den DSP zu takten. Der DSP implementiert eine schnelle Fouriertransformation (FFT) in Echtzeit sowie eine optionale Datenkompression für von der Sende/Empfangseinrichtung zu dem Hostgerät zu übertragenden Daten, um eine höhere Effizienz zu erreichen, und um mit Hostgeräten, die kleinere Speichereinrichtungen besitzen, zusammenarbeiten zu können.

Die erste Verbindungseinrichtung 12 von Fig. 1 enthält bei dem in Fig. 2 gezeigten bevorzugten Ausführungsbeispiel der Schnittstelleneinrichtung 10 folgende Bausteine: eine SCSI-Schnittstelle 1220 sowie einen 50-Pin-SCSI-Verbinder 1240 zur Verbindung mit einer bei den meisten Hostgeräten oder Laptops vorhandenen SCSI-Schnittstelle. Die SCSI-Schnittstelle (SCSI = Small Computer System Interface = Kleincomputersystemschnittstelle) 1220 wandelt die über den SCSI-Verbinder 1240 empfangenen Daten in für den DSP 1300 verständliche Daten um, wie es für Fachleute bekannt ist. Die erste Verbindungseinrichtung 12 umfaßt ferner einen EPP mit einer Datenrate von ungefähr 1 MB/s (EPP = Enhanced Parallel Port) für eine im Vergleich zur Datenrate von 10 MB/s der SCSI-Schnittstelle moderateren Datenübertragungsrate von 1 MB/s. Der EPP 1260 ist mit einem 25-Pin-sub-D-Verbinder 1280 verbunden, um beispielsweise an eine Druckerschnittstelle eines Hostgeräts angeschlossen zu werden. Optional umfaßt die erste Verbindungseinrichtung 12 ferner einen 25-Pin-Verbinder 1282, der den Anschluß von 8 Digitalausgängen und 8 Digitaleingängen 1284 an einem Hostgerät ermöglicht.

Die zweite Verbindungseinrichtung umfaßt vorzugsweise 8 BNC-Eingänge mit Kalibrationsrelais 1505, einen Block 1510

mit 8 Geräteverstärkern mit einem Überspannungsschutz von ± 75 V, wobei dieser Block wiederum mit 8 Abtast/Halte-Gliedern 1515 verbunden ist (Abtasten/Halten = Sample/Hold = S&H). Die Kalibrationsrelais sind Relais, die ein gesteuertes Umschalten zwischen einer Meßspannung und einer Kalibrationsreferenzspannung erlauben. Jede Abtast/Halten-Einrichtung ist mit einem entsprechenden Eingang eines 8-Kanal-Multiplexers 1520 verbunden, welcher seine Ausgangssignale über einen programmierbaren Verstärker 1525 in einen Analog/Digital-Wandler (ADW) mit 12 Bit und 1,25 MHz 1530 dem DSP 1300 zuführt. Der ADW 1530 wird mittels eines 20-Bit-Zeitgebers 1535 gesteuert, wie es für Fachleute bekannt ist. Der programmierbare Verstärker 1525 sowie der 8-Kanal-Multiplexer 1520 werden über ein Verstärkungs-Kanal-Auswahlbauglied 1540 gesteuert, das wiederum von dem DSP 1300 gesteuert wird.

Die gesamte Schnittstelleneinrichtung 10 wird von einem externen AC/DC-Wandler 1800 versorgt, der eine digitale Leistungsversorgung von +5 V liefert und mit einem DC/DC-Wandler 1810 verbunden ist, der analoge Leistungsversorgungsspannungen von ± 5 V und ± 15 V liefern kann, wie sie für die Schnittstelleneinrichtung 10 benötigt werden. Der DC/DC-Wandler steuert ferner eine Präzisions-Spannungs-Referenz 1820, die sowohl die 8-BNC-Eingänge 1505 als auch den ADW 1530 sowie einen Digital/Analog-Wandler (DAW) 1830 steuert, welcher über einen Ausgangsverstärkerblock mit 4 Ausgangsverstärkern 1840 und einen 9-Pin-Verbinder 1850 die analoge Ausgabe direkt von dem DSP 1300 zu einer mit dem 9-Pin-Verbinder 1850 verbindbaren Ausgabeeinrichtung, wie z. B. eine Druckereinrichtung oder eine Bildschirmeinrichtung, ermöglicht, wodurch optional eine Datenüberwachung der zu dem Hostgerät übertragenen Daten oder beispielsweise auch, ohne Prozessorzeit von dem Hostgerät zu verwenden, eine FFT betrachtet werden kann, um eine schnelle und umfassende Datenanalyse zu erreichen.

Die Speichereinrichtung 14 von Fig. 1 ist in Fig. 2 durch

ein EPROM 1400 implementiert, der bei einem bevorzugten Ausführungsbeispiel der vorliegenden Erfindung das Betriebssystem des digitalen Signalprozessors 1300 hält. Ein Direktzugriffsspeicher mit einer Zugriffszeit von 15 ns und einer Größe von 512 KB oder optional 1024 KB 1420 dient als Datenpuffer, um eine zeitliche Unabhängigkeit der Ausgangsleitung 16 von den Ausgangsleitungen 11a, 11b und 11c zur Sende/Empfangseinrichtung bzw. zum Hostgerät zu erreichen. Wie es bereits erwähnt wurde, enthält der digitale Signalprozessor 1300 bei einem bevorzugten Ausführungsbeispiel der vorliegenden Erfindung bereits einen 20-KB-Auf-Chip-RAM 1440, der bestimmte Befehlssätze, Funktionen oder auch kleinere Anwendungssoftwareeinheiten speichern kann.

Der durch die Leitung 16 symbolisierte Verbindungsanschluß der Schnittstelleneinrichtung 10 mit einer beliebigen Sende/Empfangseinrichtung implementiert mit den Blöcken 1505 - 1535 einen Analogeingang mit einer Abtastrate von 1,25 MHz und einer Quantisierung von 12 Bit. Es existieren 8 Kanäle mit einem Überspannungsschutz von ± 75 V. Mittels des programmierbaren Verstärkers 1525 kann jeder Kanal unabhängig voneinander in Spannungsbereichen von max. ± 10 V programmiert werden. Unbenutzte Kanäle können intern mit Masse verbunden werden, um Nebensprecheffekte zu verringern. Der Block 1515 ist als monolithischer hochgenauer Hochgeschwindigkeits-Abtasten/Halten-Verstärker für das gleichzeitige Abtasten aller Kanäle ausgeführt. Die Präzisionsspannungsreferenz 1820 schafft eine hochgenaue Temperatur-kompensierte monolithische Bandabstandsspannungsreferenz für eine Autokalibration jedes Kanals und jeder Verstärkung. Es ist ferner eine Offset-Feinabstimmung für jeden Kanal durch dieselbe implementiert.

Die Blöcke 1830, 1840 und 1850 implementieren einen direkten Analogausgang für den digitalen Signalprozessor 1300, wobei der DAW 1830 eine Datenrate von 625 KHz und eine Quantisierung von 12 Bit schafft. Der Block 1840 umfaßt 4 Kanäle mit einem gemeinsamen Ausgangslatch.

Die Schnittstelleneinrichtung 10 umfaßt ferner eine digitale Eingabe/Ausgabe-Einrichtung, die durch die Blöcke 1284 und 1282 implementiert ist. Hier existieren 8 digitale Eingänge, 8 digitale Ausgänge mit einem gemeinsamen Latch, wobei der digitale Port vorzugsweise an einer Seitenwand der Schnittstelleneinrichtung 10 angebracht sein kann, damit auf denselben ohne weiteres zugegriffen werden kann.

Der digitale Signalprozessor 1300 liefert eine On-Board-Digitaldatenverarbeitung. Insbesondere ist er ein Hochleistungs-DSP mit einer Taktrate von 80 MHz und einem 20-Bit-Zeitgeber 1535.

Die erste Verbindungseinrichtung 12 umfaßt, wie es bereits erwähnt wurde, die SCSI-Schnittstelle 1220 mit einer Spitzenübertragungsrate von 10 MB/s. Ein optional einsetzbarer PCMCIA-zu-SCSI-Adapter ermöglicht eine Hochgeschwindigkeitskommunikation mit Laptop-Computern, welche besonders bei mobilen Servicetechnikern verbreitet und erwünscht sind. Eine moderatere Datenübertragung ermöglicht der EPP 1260 mit seinem zugehörigen Verbinder 1280.

Wie es bereits erwähnt wurde, wird die Leistungsversorgung der Schnittstelleneinrichtung 10 mittels eines externen AC/DC-Adapters erreicht, der einen Universalleistungseingang (85 - 264 VAC, 47 - 63 Hz) aufweist. Die Interferenzunterdrückung erreicht die Standards EN 55022, Kurve B und FCC, Klasse B). Ferner ist sie gemäß internationalen Sicherheitsbestimmungen (TÜV, UL, CSA) ausgeführt. Die Schnittstelleneinrichtung 10 ist nach außen abgeschirmt und erreicht einen Wert von 55 dB bei 30 - 60 MHz und einen Wert von etwa 40 dB bei 1 GHz, und entspricht somit dem Standard MILSTD 285-1.

Wie es bereits erwähnt wurde, kann die Kommunikation zwischen dem Hostgerät und der Vielzweckschnittstelle nicht nur über in dem BIOS-System des Hostgeräts vorhandene Treiber

für Hostgerät-übliche Eingabe/Ausgabe-Geräte stattfinden, sondern auch über spezifische Schnittstellentreiber, welche im Falle einer SCSI-Schnittstelle als Vielzweckschnittstelle ASPI-Treiber genannt werden (ASPI = Advanced SCSI Programming Interface). Dieser ASPI-Treiber, der auch als ASPI-Manager bezeichnet werden kann, ist für einen speziellen SCSI-Hostadapter, d. h. für eine spezielle Vielzweckschnittstelle spezifisch und wird üblicherweise vom Hersteller dieser Vielzweckschnittstelle mitgeliefert. Allgemein gesagt hat dieser Vielzweckschnittstellentreiber die Aufgabe, die genau spezifizierten SCSI-Befehle vom Hostsystem-Programm zum Hostsystem-SCSI-Adapter zu bringen. Daher ist der Befehlssatz beinahe identisch zu dem der SCSI-Schnittstelle selber. Er wird im wesentlichen lediglich um Status- und Reset-Befehle für den Hostadapter erweitert.

Der ASPI-Treiber kann dann eingesetzt werden, wenn zum Zeitpunkt des Bootens die Festplatte noch nicht ansprechbar war, oder wenn die SCSI-bezogenen BIOS-Routinen des Hostrechners noch deaktiviert waren. Auch hier sind die dann einzuleitenden Schritte zum Initialisieren des Schnittstellengeräts vorzugsweise als virtuelle Festplatte den Schritten beim Initialisieren während des Bootens ähnlich.

Der ASPI-Manager umfaßt grob gesprochen zwei Seiten. Die eine Seite ist die herstellerspezifische Hardware-orientierte Seite. Sie übernimmt die Umsetzung aller Befehle in eine Form, die die entsprechende Vielzweckschnittstelle benötigt. Die Hardware-orientierte Seite des ASPI-Treibers ist also auf einen ganz speziellen Typ einer Vielzweckschnittstelle bzw. einer SCSI-Schnittstelle zugeschnitten. Die andere Seite wird als Benutzersoftwareseite bezeichnet. Diese Seite ist absolut unabhängig von den herstellerspezifischen Bedienungseigenschaften des SCSI-Adapters und ist daher für alle SCSI-Schnittstellen gleich. Dies ermöglicht eine SCSI-Programmierung, die jedoch von den einzelnen SCSI-Adaptertypen unabhängig ist.

Der Einsatz eines solchen ASPI-Treibers zur Kommunikation zwischen dem Hostgerät und dem erfindungsgemäßen Schnittstellengerät erlaubt jedoch im Gegensatz zu einer Kommunikation des Hostgeräts mit dem erfindungsgemäßen Schnittstellengerät auf der Basis eines BIOS-Treibers die Ausschöpfung verschiedener weiterer Möglichkeiten der SCSI-Vielzweckschnittstelle. Im vorher beschriebenen Fall wird das Schnittstellengerät, das sich vorzugsweise als virtuelle Festplatte meldet und verhält, beim Booten durch den BIOS-Treiber des Hostrechners erkannt und als Festplatte konfiguriert. Dieser Schritt unterstützt jedoch keine aktiven Anfragen des Schnittstellengeräts an den Hostrechner. Will jedoch die virtuelle Festplatte Daten aktiv auf z. B. eine Festplatte des Hostrechners schreiben bzw. mit dem Prozessor des Hostrechners von sich aus in Verbindung treten, so muß der Hostrechner die Anfrage der virtuellen Festplatte erkennen und einen weiteren Befehlsgeber an seinem Bus dulden. Verhält sich das Schnittstellengerät ausschließlich wie eine virtuelle Festplatte, so würde es immer ein Befehlsempfänger und kein Befehlsgeber sein. Das BIOS wehrt sich zwar nicht gegen einen solchen weiteren Befehlsgeber, welcher aktiv Daten auf den Bus des Hostgeräts geben will, dasselbe unterstützt jedoch das Hostgerät nicht dabei, entsprechende Anfragen des Schnittstellengeräts zu erkennen oder dem Schnittstellengerät für Zugriffe auf den Bus die Erlaubnis zu erteilen.

Das erfindungsgemäße Schnittstellengerät kann jedoch nun unter Verwendung des ASPI-Managers einen aktiven Zugriff auf eine am selben SCSI-Bus angeschlossene SCSI-Festplatte des Hostgeräts erhalten, welche im Gegensatz zum Schnittstellengerät kein virtueller sondern ein realer SCSI-Massenspeicher sein kann oder aber auch ein weiteres erfindungsgemäßes Schnittstellengerät. Daraufhin kann das Schnittstellengerät gemäß der vorliegenden Erfindung völlig unabhängig vom Hostrechner die SCSI-Festplatte des Hostrechners mit erwünschten Daten beschreiben bzw. auf sonstige Art und Weise mit derselben kommunizieren. Das Schnittstellengerät gemäß der vor-

liegenden Erfindung tritt somit zunächst passiv als virtuelle Festplatte auf und dann bei Bedarf unter Verwendung der Treibersoftware für die Vielzweckschnittstelle aktiv am selben SCSI-Bus auf. Dies bedeutet jedoch, daß das Schnittstellengerät gemäß der vorliegenden Erfindung unter Verwendung einer Treibersoftware für die Vielzweckschnittstelle, die zum einen die Hostgerät-üblichen BIOS-Routinen umfaßt und gleichzeitig die Möglichkeit der aktiven Teilnahme bietet, unabhängig von dem Typ der an die zweite Verbindungseinrichtung angeschlossenen Sende/Empfangseinrichtung zunächst als virtuelle und zugleich passive Festplatte erscheinen kann, jedoch aber bei Bedarf aktiv am Bus teilnehmen kann, um unter Umgehung des Prozessors des Hostgeräts direkt mit anderen SCSI-Festplatten des Hostgeräts in Kontakt treten zu können.

Die Schnittstelleneinrichtung gemäß der vorliegeden Erfindung ermöglicht also unter Verwendung einer Standardschnittstelle eines Hostgeräts die Kommunikation mit beliebigen Hostgeräten. Durch die Simulation eines Eingabe/Ausgabe-Geräts für das Hostgerät und bei einem bevorzugten Ausführungsbeispiel durch Simulation eines virtuellen Massenspeichers wird die Schnittstelleneinrichtung 10 von allen bekannten Hostsystemen ohne jede zusätzliche aufwendige Treibersoftware automatisch unterstützt. Die Simulation einer beliebig definierbaren Dateistruktur auf der "virtuellen" Festplatte liefert einfache Bedienungs- und Erweiterungsmöglichkeiten sowie durch Implementation beliebiger Programme die Unabhängigkeit von spezieller auf dem Hostgerät implementierter Software. Auf der Schnittstelleneinrichtung 10 enthaltene Hilfedateien und die Unterstützung von "Plug-and Play" stellen den einfachen Einsatz selbst in tragbaren flexiblen Hostgeräten sicher. Dem erfahrenen Anwender steht trotz einfachster Bedienungsoberfläche jederzeit die Möglichkeit des systemnahen Eingriffs in Funktionen der Schnittstelleneinrichtung 10 offen. Eine universelle Lösung, die die gesamte Bandbreite möglicher Sende/Empfangseinrichtungen abdecken kann, ist demnach durch die Schnitt-

stelleneinrichtung 10 geschaffen.

Patentansprüche

1. Schnittstellengerät (10) zur Kommunikation zwischen einem Hostgerät, das Treiber für Hostgerät-übliche Eingabe/Ausgabe-Geräte sowie eine Vielzweck-Schnittstelle aufweist, und einer Datensende/Empfangseinrichtung, mit folgenden Merkmalen:

einer Prozessoreinrichtung (13; 1300, 1320);

einer Speichereinrichtung (14; 1400, 1420, 1440);

einer ersten Verbindungseinrichtung (12; 1220, 1240, 1260, 1280) zum schnittstellenmäßigen Verbinden des Hostgeräts mit dem Schnittstellengerät (10) über die Vielzweck-Schnittstelle des Hostgeräts; und

einer zweiten Verbindungseinrichtung (15; 1505 - 1535) zum schnittstellenmäßigen Verbinden der Schnittstellengeräts (10) mit der Datensende/Empfangseinrichtung,

wobei das Schnittstellengerät (10) durch die Prozessoreinrichtung (13; 1300, 1320) und die Speichereinrichtung (14; 1400, 1420, 1440) derart konfiguriert ist, daß das Schnittstellengerät bei einer Anfrage des Hostgeräts, die die Art eines an der Vielzweckschnittstelle des Hostgeräts angeschlossenen Geräts betrifft, unabhängig von dem Typ der mit der zweiten Verbindungseinrichtung (15; 1505 - 1535) des Schnittstellengeräts (10) verbundenen Datensende/Empfangseinrichtung ein Signal dem Hostgerät sendet, das dem Hostgerät signalisiert, daß es ein Hostgerät-übliches Eingabe/Ausgabe-Gerät ist, woraufhin das Hostgerät mittels des Treibers für das Hostgerät-übliche Eingabe/Ausgabe-Gerät mit dem Schnittstellengerät (10) kommuniziert.

2. Schnittstellengerät (10) nach Anspruch 1,

bei dem die Treiber für Hostgerät-übliche Eingabe/Ausgabe-Geräte einen Festplattentreiber aufweisen, wobei das Signal dem Hostgerät signalisiert, daß dasselbe mit einer Festplatte kommuniziert.

3. Schnittstellengerät (10) nach Anspruch 1 oder 2,

bei dem die Speichereinrichtung einen Puffer (1420) aufweist, um zwischen der Datensende/Empfangseinrichtung und dem Hostgerät übertragbare Daten zwischenzuspeichern.

4. Schnittstellengerät (10) nach einem der vorhergehenden Ansprüche,

bei dem die Vielzweckschnittstelle des Hostgeräts eine SCSI-Schnittstelle ist und die erste Verbindungseinrichtung ebenfalls eine SCSI-Schnittstelle (1220) aufweist.

5. Schnittstellengerät (10) nach einem der vorhergehenden Ansprüche,

bei dem die zweite Verbindungseinrichtung einen Analogeingang (1505) mit nachfolgendem A/D-Wandler (1530) aufweist, um analoge Daten von einem mit dem Analogeingang (1505) verbindbaren Datensende/Empfangsgerät zu dem Hostgerät zu übertragen.

6. Schnittstellengerät (10) nach einem der vorhergehenden Ansprüche,

bei dem die Prozessoreinrichtung (13) ein digitaler Signalprozessor (1300) ist.

7. Schnittstellengerät (10) nach einem der Ansprüche 2 bis 6,

bei dem von der Datensende/Empfangseinrichtung zum Host-

gerät zu übertragende Daten in dem Schnittstellengerät (10) in ein für eine in dem Hostgerät vorhandene Festplatte geeignetes Format formatiert werden.

8. Schnittstellengerät (10) nach einem der Ansprüche 2 bis 7,

das ferner ein Wurzelverzeichnis und virtuelle Dateien, die auf dem signalisierten Festplattenlaufwerk vorhanden sind, aufweist, auf die von dem Hostgerät zugegriffen werden kann.

9. Schnittstellengerät (10) nach Anspruch 8,

bei dem die virtuellen Dateien eine Konfigurationsdatei im Textformat aufweisen, die in der Speichereinrichtung (14) gespeichert sind, mittels der der Benutzer das Schnittstellengerät (10) für eine spezielle Datensende/Empfangseinrichtung konfigurieren kann.

10. Schnittstellengerät (10) nach Anspruch 8 oder 9,

bei dem die virtuellen Dateien Stapeldateien oder ausführbare Dateien für die Mikroprozessereinrichtung aufweisen, die in der Schnittstelleneinrichtung (10) gespeichert sind, um eine vom Hostgerät getrennte Datenverarbeitung von über die zweite Verbindungseinrichtung (15; 1505 - 1535) empfangenen Daten durchzuführen.

11. Schnittstellengerät (10) nach Anspruch 8 oder 9,

bei dem die virtuellen Dateien Stapeldateien oder ausführbare Dateien für das Hostgerät aufweisen, die in dem Schnittstellengerät (10) gespeichert sind.

12. Schnittstellengerät (10) zur Kommunikation zwischen einem Hostgerät, das eine Vielzweck-Schnittstelle sowie

einen dafür spezifischen Treiber aufweist, und einer Datensende/Empfangseinrichtung, mit folgenden Merkmalen:

einer Prozessoreinrichtung (13; 1300, 1320);

einer Speichereinrichtung (14; 1400, 1420, 1440);

einer ersten Verbindungseinrichtung (12; 1220, 1240, 1260, 1280) zum schnittstellenmäßigen Verbinden des Hostgeräts mit dem Schnittstellengerät (10) über die Vielzweck-Schnittstelle des Hostgeräts; und

einer zweiten Verbindungseinrichtung (15; 1505 - 1535) zum schnittstellenmäßigen Verbinden der Schnittstellengeräts (10) mit der Datensende/Empfangseinrichtung,

wobei das Schnittstellengerät (10) durch die Prozessoreinrichtung (13; 1300, 1320) und die Speichereinrichtung (14; 1400, 1420, 1440) derart konfiguriert ist, daß das Schnittstellengerät bei einer Anfrage des Hostgeräts, die die Art eines an der Vielzweckschnittstelle des Hostgeräts angeschlossenen Geräts betrifft, unabhängig von dem Typ der mit der zweiten Verbindungseinrichtung (15; 1505 - 1535) des Schnittstellengeräts (10) verbundenen Datensende/Empfangseinrichtung ein Signal dem Hostgerät sendet, das dem Hostgerät signalisiert, daß es ein Hostgerät-übliches Eingabe/Ausgabe-Gerät ist, woraufhin das Hostgerät mittels des für die Vielzweckschnittstelle spezifischen Treibers mit dem Schnittstellengerät (10) kommuniziert.

13. Schnittstellengerät nach Anspruch 12,

bei dem sich neben der ersten Verbindungseinrichtung des Schnittstellengeräts ein weiteres Eingabe/Ausgabe-Gerät an der Vielzweck-Schnittstelle des Hostgeräts befindet, und bei dem das Schnittstellengerät eine direkte Kommunikation mit der Festplatte über den spezifischen Trei-

ber für die Vielzweck-Schnittstelle durchführen kann.

14. Schnittstellengerät nach Anspruch 12 oder 13,

bei dem die Vielzweck-Schnittstelle eine SCSI-Schnittstelle ist, und bei dem der spezifische Treiber für die Vielzweck-Schnittstelle ein ASPI-Manager ist.

15. Verfahren zur Kommunikation zwischen einem Hostgerät, das Treiber für Hostgerät-übliche Eingabe/Ausgabe-Geräte sowie eine Vielzweck-Schnittstelle aufweist, und einer Datensende/Empfangseinrichtung über ein Schnittstellengerät (10), mit folgenden Schritten:

schnittstellenmäßiges Verbinden des Hostgeräts mit einer ersten Verbindungseinrichtung (12; 1220, 1240, 1260, 1280) des Schnittstellengeräts (10) über die Vielzweckschnittstelle des Hostgeräts;

schnittstellenmäßiges Verbinden der Datensende/Empfangseinrichtung mit einer zweiten Verbindungseinrichtung (15; 1505 - 1535) des Schnittstellengeräts (10);

Anfragen bei dem Schnittstellengerät (10) durch das Hostgerät, welcher Typ eines Geräts mit der Vielzweckschnittstelle des Hostgeräts verbunden ist;

unabhängig davon, welcher Typ einer Datensende/Empfangseinrichtung mit der zweiten Verbindungseinrichtung des Schnittstellengeräts (10) verbunden ist, Beantworten der Anfrage des Hostgeräts durch das Schnittstellengerät (10), derart, daß es ein Hostgerät-übliches Eingabe/Ausgabe-Gerät ist, woraufhin das Hostgerät mittels des für das Eingabe/Ausgabe-Gerät üblichen Treibers mit dem Schnittstellengerät (10) kommuniziert.

16. Verfahren nach Anspruch 15,

bei dem die Treiber für Hostgerät-übliche Eingabe/Ausgabe-Geräte einen Treiber für ein Speichergerät und insbesondere für ein Festplattenlaufwerk aufweist.

Flexible Schnittstelle

Zusammenfassung

Ein Schnittstellengerät (10) liefert eine schnelle Datenkommunikation zwischen einem Hostgerät mit Eingabe/Ausgabe-Schnittstellen und einer Datensende/Empfangseinrichtung, wobei das Schnittstellengerät (10) eine Prozessoreinrichtung (13), eine Speichereinrichtung (14), eine erste Verbindungseinrichtung (12) zum schnittstellenmäßigen Verbinden des Hostgeräts mit dem Schnittstellengerät und eine zweite Verbindungseinrichtung (15) zum schnittstellenmäßigen Verbinden des Schnittstellengeräts (10) mit der Datensende/Empfangseinrichtung aufweist. Das Schnittstellengerät (10) ist durch die Prozessoreinrichtung (13) und die Speichereinrichtung (14) derart konfiguriert, daß das Schnittstellengerät bei einer Anfrage des Hostgeräts über die erste Verbindungseinrichtung (12), die die Art eines an demselben angeschlossenen Geräts betrifft, unabhängig von dem Typ der Datensende/Empfangseinrichtung ein Signal über die erste Verbindungseinrichtung (12) zum Hostgerät sendet, das dem Hostgerät signalisiert, daß es mit einem Eingabe/Ausgabe-Gerät kommuniziert.

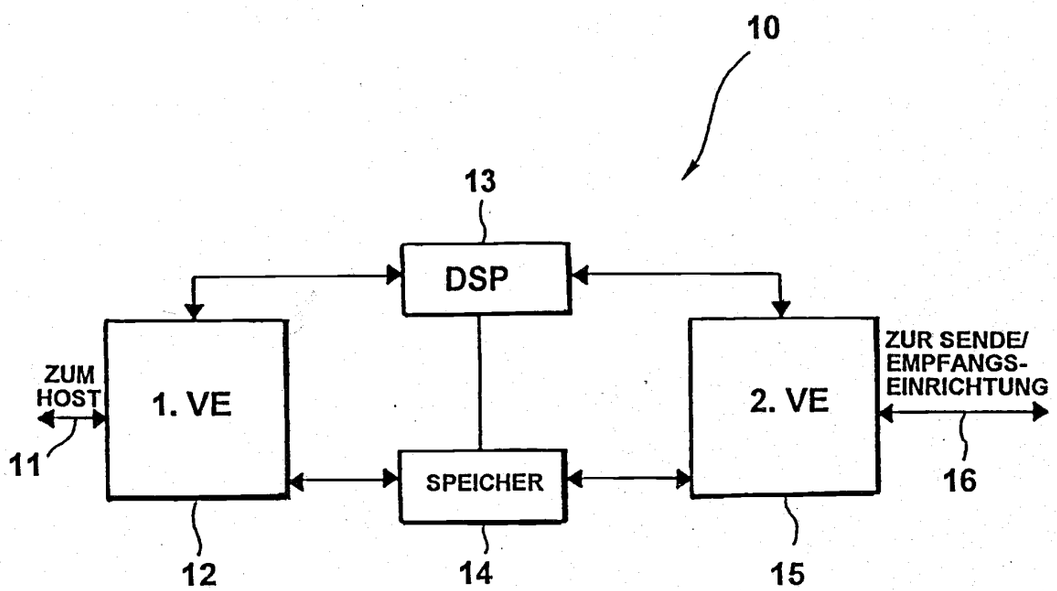
10
13
DSP
ZUM HOST
1. VE
11
12
SPEICHER
14
2. VE
15
ZUR SENDE/ EMPFANGS- EINRICHTUNG
16

FIG.1

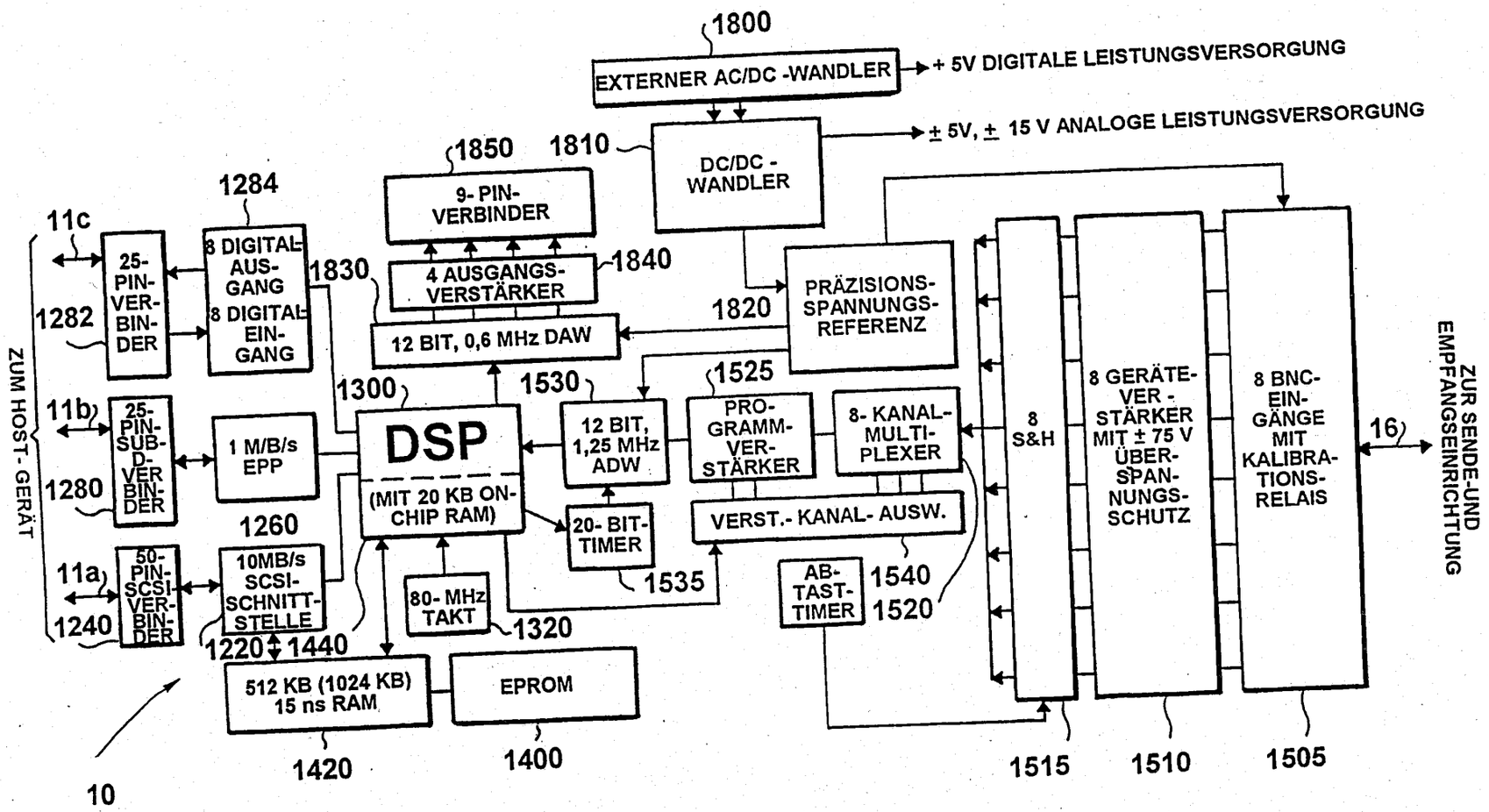
1800
EXTERNER AC/DC -WANDLER
+ 5V DIGITALE LEISTUNGSVERSORGUNG
± 5V, ± 15 V ANALOGE LEISTUNGSVERSORGUNG
1850
1810
DC/DC - WANDLER
9- PIN- VERBINDER
1284
11c
25- PIN- VER- BIN- DER
8 DIGITAL- AUS- GANG
8 DIGITAL- EIN- GANG
1830
4 AUSGANGS- VERSTÄRKER
1840
1282
12 BIT, 0,6 MHz DAW
1820
PRÄZISIONS- SPANNUNGS- REFERENZ
1300
1530
1525
11b
25- PIN- SUB- D- VER BIN- DER
1 M/B/s EPP
DSP
(MIT 20 KB ON- CHIP RAM)
12 BIT, 1,25 MHz ADW
PRO- GRAMM- VER- STÄRKER
8- KANAL- MULTI- PLEXER
1280
1260
20- BIT- TIMER
VERST.- KANAL- AUSW.
1535
11a
50- PIN- SCSI- VER- BIN- DER
10MB/s SCSI- SCHNITT- STELLE
80- MHz TAKT
1320
AB- TAST- TIMER
1540
1520
1240
1220
1440
512 KB (1024 KB) 15 ns RAM
EPROM
1420
1400
10
8 S&H
8 GERÄTE- VER - STÄRKER MIT ± 75 V ÜBER- SPAN- NUNGS- SCHUTZ
8 BNC- EIN- GÄNGE MIT KALIBRA- TIONS- RELAIS
16
ZUR SENDE-UND EMPFANGSEINRICHTUNG
ZUM HOST- GERÄT
1515
1510
1505

FIG.2

UNITED STATES DEPARTMENT OF COMMERCE
Patent and Trademark Office
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#2

U.S. APPLICATION NO.	FIRST NAMED APPLICANT	ATTY. DOCKET NO.
09/331002	TASLER M	2055/101

INTERNATIONAL APPLICATION NO.
PCT/EP98/01187

I.A. FILING DATE	PRIORITY DATE
03 MAR 98	04 MAR 97

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DATE MAILED: 26 JUL 1999

NOTIFICATION OF ACCEPTANCE OF APPLICATION UNDER 35 U.S.C. 371 AND 37 CFR 1.494 OR 1.495

1. The applicant is hereby advised that the United States Patent and Trademark Office in its capacity as ☐ a Designated Office (37 CFR 1.494), ☒ an Elected Office (37 CFR 1.495), has determined that the above identified international application has met the requirements of 35 U.S.C. 371, and is **ACCEPTED** for national patentability examination in the United States Patent and Trademark Office.

2. The United States Application Number assigned to the application is shown above and the relevant dates are:

14 JUN 99	14 JUN 99
35 U.S.C. 102(e) DATE	DATE OF RECEIPT OF 35 U.S.C. 371 REQUIREMENTS

A Filing Receipt (PTO-103X) will be issued for the present application in due course. **THE DATE APPEARING ON THE FILING RECEIPT AS THE "FILING DATE" IS THE DATE ON WHICH THE LAST OF THE 35 U.S.C. 371(C) REQUIREMENTS HAS BEEN RECEIVED IN THE OFFICE. THIS DATE IS SHOWN ABOVE.** *The filing date of the above identified application is the international filing date of the international application (Article 11(3) and 35 U.S.C. 363).* Once the Filing Receipt has been received, send all correspondence to the Group Art Unit designated thereon.

3. ☒ A request for immediate examination under 35 U.S.C. 371(f) was received on 14 JUN 99 and the application will be examined in turn.

4. The following items have been received:
- ☒ U.S. Basic National Fee.
- ☒ Copy of the international application in:
  - ☒ a non-English language.
  - ☐ English.
- ☒ Translation of the international application into English.
- ☒ Oath or Declaration of inventors(s) for DO/EO/US.
- ☐ Copy of Article 19 amendments. ☐ Translation of Article 19 amendments into English.
  The Article 19 amendments ☐ have ☐ have not been entered.
- ☒ The International Preliminary Examination Report in English and its Annexes, if any.
- ☐ Copy of the Annexes to the International Preliminary Examination Report (IPER).
  - ☐ Translation of Annexes to the IPER into English.
  - The Annexes ☐ have ☐ have not been entered.
- ☒ Preliminary amendment(s) filed 14 JUN 99 and _____.
- ☒ Information Disclosure Statement(s) filed 14 JUN 99 and _____.
- ☐ Assignment document.
- ☐ Power of Attorney and/or Change of Address.
- ☐ Substitute specification filed _____.
- ☒ Verified Statement Claiming Small Entity Status.
- ☒ Priority Document.
- ☒ Copy of the International Search Report ☒ and copies of the references cited therein.
- ☐ Other:

Applicant is reminded that any communication to the United States Patent and Trademark Office must be mailed to the address given in the heading and include the U.S. application no. shown above. (37 CFR 1.5)

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FORM PCT/DO/EO/903 (December 1997)

DO/EO BIBLIOGRAPHIC DATA ENTRY

SERIAL NUMBER: 09 / 331002 RECEIPT DATE: 06 / 14 / 9
IA NUMBER: PCT/ EP90 / 01187 IA FILING DATE: 03 / 03 / 9
FAMILY NAME: TASLER DELAY WAIVED (Y/N):
GIVEN NAME: MICHAEL DEMAND RECEIVED (Y/N):
PRIORITY CLAIMED (Y/N): Y PRIORITY DATE: 03 / 04 / 9
NO BASIC FEE (Y/N): N US DESIGNATED ONLY (Y/N):
ATTORNEY DOCKET NUMBER: 2055/101 COUNTRY: EPX
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APPLICATION TITLE:
FLEXIBLE INTERFACE

TAB TO LAST POSITION, PUSH SEND

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
AS DESIGNATED/ELECTED OFFICE DO/EO/US

#3/A

U.S. Patent Application No.: Applied For)
) Group Art Unit: Unknown
International Application No.: PCT/EP98/01187)
) Examiner: Unknown
International Filing Date: 03 March 1998)
) Docket No: 2055/101
Priority Date: 04 March 1997)
)
For: FLEXIBLE INTERFACE)
)
Applicant (Inventor): Michael Tasler)

ATTENTION: EO/US
BOX PCT
ASSISTANT COMMISSIONER FOR PATENTS
WASHINGTON, DC 20231

June 12, 1999

Dear Sir:

FIRST PRELIMINARY AMENDMENT

In the Specification:

Please substitute the attached specification for the original PCT specification.

In the Claims:

Please substitute the enclosed claims 1 - 16, on pages 20 through 24, inclusive, attached to the substitute specification, for original claims 1 - 16.

In the Abstract:

Please substitute the enclosed abstract, attached to the substitute specification on page 25, for the original abstract.

Drawings

Please substitute the enclosed FIGS. 1 - 2 for the original FIGS. 1 - 2.

REMARKS

Applicant respectfully requests that the Examiner base the examination upon the attached substitute specification, claims, abstract, and drawings.

The PCT specification, claims, abstract and drawings have been revised to conform to U.S. requirements. It is believed that no new matter was introduced in revising the specification, claims, and abstract.

In view of the foregoing amendments, it is believed that the application, including claims 1 - 16, is in condition for allowance, and favorable action is respectfully requested. The Examiner is invited to contact the undersigned by collect telephone call to advance the prosecution in any respect.

No additional fee for this Preliminary Amendment is seen to be required. If any additional fee is required, please charge it to Deposit Account No. 04-1697.

Respectfully submitted,
DUFT, GRAZIANO & FOREST, P.C.

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National Phase of PCT/EP98/01187 in U.S.A.
Title: Flexible Interface
Applicant: TASLER, Michael

Translation of PCT Application PCT/EP98/01187
as originally filed

Flexible Interface

Description

The present invention relates to the transfer of data and in particular to interface devices for communication between a computer or host device and a data transmit/receive device from which data is to be acquired or with which two-way communication is to take place.

Existing data acquisition systems for computers are very limited in their areas of application. Generally such systems can be classified into two groups.

In the first group host devices or computer systems are attached by means of an interface to a device whose data is to be acquired. The interfaces of this group are normally standard interfaces which, with specific driver software, can be used with a variety of host systems. An advantage of such interfaces is that they are largely independent of the host device. However, a disadvantage is that they generally require very sophisticated drivers which are prone to malfunction and which limit data transfer rates between the device connected to the interface and the host device and vice versa. Further, it is often very difficult to implement such interfaces for portable systems and they offer few possibilities for adaptation with the result that such systems offer little flexibility.

The devices from which data is to be acquired cover the entire electrical engineering spectrum. In a typical case, it is assumed that a customer who operates, for example, a diagnostic radiology system in a medical engineering environment reports a fault. A field service technician of the system manufacturer visits the customer and reads system log files generated by the diagnostic radiology system by means a portable computer or laptop for example. If the fault cannot be localized or if the fault is intermittent, it will be necessary for the service technician to read not only an error log file but also data from current operation. It is apparent that in this case fast data transfer and rapid data analysis are necessary.

Another case requiring the use of an interface could be, for example, when an electronic measuring device, e.g. a multimeter, is attached to a computer system to transfer the data measured by the multimeter to the computer. Particularly when long-term measurements or large volumes of data are involved is it necessary for the interface to support a high data transfer rate.

From these randomly chosen examples it can be seen that an interface may be put to totally different uses. It is therefore desirable that an interface be sufficiently flexible to permit attachment of very different electrical or electronic systems to a host device by means of the interface. To prevent operator error, it is also desirable that a service technician is not required to operate different interfaces in different ways for different applications but that, if possible, a universal method of operating the interface be provided for a large number of applications.

To increase the data transfer rates across an interface, the route chosen in the second group of data acquisition systems for the interface devices was to specifically match the interface very closely to individual host systems or computer systems. The advantage of this solution is that high data transfer rates are possible. However, a disadvantage is that the drivers for the interfaces of the second group are very closely matched to a single host system with the result that they generally cannot be used with other host systems or their use is very ineffective. Further, such types of interface have the disadvantage that they must be installed inside the computer casing to achieve maximum data transfer rates as they access the internal host bus system. They are therefore generally not suitable for portable host systems in the form of laptops whose minimum possible size leaves little internal space to plug in an interface card.

A solution to this problem is offered by the interface devices of IOtech (business address: 25971 Cannon Road, Cleveland, Ohio 44146, USA) which are suitable for laptops such as the WaveBook/512 (registered trademark). The interface devices are connected by means of a plug-in card, approximately the size of a credit card, to the PCMCIA interface which is now a standard feature in laptops. The plug-in card converts the PCMCIA interface into an interface known in the art as IEEE 1284. The said plug-in card provides a special printer interface which is enhanced as regards the data transfer rate and delivers a data transfer rate of approximately 2 MBps as

compared with a rate of approx. 1 MBps for known printer interfaces. The known interface device generally consists of a driver component, a digital signal processor, a buffer and a hardware module which terminates in a connector to which the device whose data is to be acquired is attached. The driver component is attached directly to the enhanced printer interface thus permitting the known interface device to establish a connection between a computer and the device whose data is to be acquired.

In order to work with the said interface, an interface-specific driver must be installed on the host device so that the host device can communicate with the digital signal processor of the interface card. As described above, the driver must be installed on the host device. If the driver is a driver developed specifically for the host device, a high data transfer rate is achieved but the driver cannot be easily installed on a different host system. However, if the driver is a general driver which is as flexible as possible and which can be used on many host devices, compromises must be accepted with regard to the data transfer rate.

Particularly in an application for multi-tasking systems in which several different tasks such as data acquisition, data display and editing are to be performed quasi-simultaneously, each task is normally assigned a certain priority by the host system. A driver supporting a special task requests the central processing system of the host device for processor resources in order to perform its task. Depending on the particular priority assignment method and on the driver implementation, a particular share of processor resources is assigned to a special task in particular time slots. Conflicts arise if one or more drivers are implemented in such a way that they have the highest priority by default, i.e. they are incompatible, as happens in practice in many applications. It may occur that both drivers are set to highest priority which, in the worst case, can result in a system crash.

EP 0685799 A1 discloses an interface by means of which several peripheral devices can be attached to a bus. An interface is connected between the bus of a host device and various peripheral devices. The interface comprises a finite state machine and several branches each of which is assigned to a peripheral device. Each branch comprises a data manager, cycle control, user logic and a buffer. This known interface

device provides optimal matching between a host device and a specific peripheral device.

The specialist publication IBM Technical Disclosure Bulletin, Vol. 38, No. 05, page 245; "Communication Method between Devices through FDD Interface" discloses an interface which connects a host device to a peripheral device via a floppy disk drive interface. The interface consists in particular of an address generator, an MFM encoder/decoder, a serial/parallel adapter and a format signal generator. The interface makes it possible to attach not only a floppy disk drive but also a further peripheral device to the FDD host controller of a host device. The host device assumes that a floppy disk drive is always attached to its floppy disk drive controller and communication is initiated if the address is correct. However, this document contains no information as to how communication should be possible if the interface is connected to a multi-purpose interface instead of to a floppy disk drive controller.

It is the object of the present invention to provide an interface device for communication between a host device and a data transmit/receive device whose use is host device-independent and which delivers a high data transfer rate.

This object is achieved by an interface device according to claim 1 or 12 and by a method according to claim 15.

The present invention is based on the finding that both a high data transfer rate and host device-independent use can be achieved if a driver for an input/output device customary in a host device, normally present in most commercially available host devices, is utilized. Drivers for input/output devices customary in a host device which are found in practically all host devices are, for example, drivers for hard disks, for graphics devices or for printer devices. As however the hard disk interfaces in common host devices which can be, for example, IBM PCs, IBM-compatible PCs, Commodore PCs, Apple computers or even workstations, are the interfaces with the highest data transfer rate, the hard disk driver is utilized in the preferred embodiment of the interface device of the present invention. Drivers for other storage devices such as floppy disk drives, CD-ROM drives or tape drives could also be utilized in order to implement the interface device according to the present invention.

As described in the following, the interface device according to the present invention is to be attached to a host device by means of a multi-purpose interface of the host device which can be implemented, for example, as an SCSI interface or as an enhanced printer interface. Multi-purpose interfaces comprise both an interface card and specific driver software for the interface card. The driver software can be designed so that it can replace the BIOS driver routines. Communication between the host device and the devices attached to the multi-purpose interface then essentially takes place by means of the specific driver software for the multi-purpose interface and no longer primarily by means of BIOS routines of the host device. Recently however drivers for multi-purpose interfaces can also already be integrated in the BIOS system of the host device as, alongside classical input/output interfaces, multi-purpose interfaces are becoming increasingly common in host devices. It is of course also possible to use BIOS routines in parallel with the specific driver software for the multi-purpose interface, if this is desired.

The interface device according to the present invention comprises a processor means, a memory means, a first connecting device for interfacing the host device with the interface device, and a second connecting device for interfacing the interface device with the data transmit/receive device. The interface device is configured by the processor means and the memory means in such a way that the interface device, when receiving an inquiry from the host device via the first connecting device as to the type of a device attached to the host device, sends a signal, regardless of the type of the data transmit/receive device, to the host device via the first connecting device which signals to the host device that it is communicating with an input/output device. The interface device according to the present invention therefore simulates, both in terms of hardware and software, the way in which a conventional input/output device functions, preferably that of a hard disk drive. As support for hard disks is implemented as standard in all commercially available host systems, the simulation of a hard disk, for example, can provide host device-independent use. The interface device according to the present invention therefore no longer communicates with the host device or computer by means of a specially designed driver but by means of a program which is present in the BIOS system (Basic Input/Output System) and is normally precisely matched to the specific computer system on which it is installed,

or by means of a specific program for the multi-purpose interface. Consequently, the interface device according to the present invention combines the advantages of both groups. On the one hand, communication between the computer and the interface takes place by means of a host device-specific BIOS program or by means of a driver program which is matched to the multi-purpose interface and which could be regarded as a "device-specific driver". On the other hand, the BIOS program or a corresponding multi-purpose interface program which operates one of the common input/output interfaces in host systems is therefore present in all host systems so that the interface device according to the present invention is host device-independent.

In the following, preferred embodiments of the present invention will be explained in more detail with reference to the drawings enclosed, in which:

Fig. 1 shows a general block diagram of the interface device according to the present invention; and

Fig. 2 shows a detailed block diagram of an interface device according to a preferred embodiment of the present invention.

Fig. 1 shows a general block diagram of an interface device 10 according to the present invention. A first connecting device 12 of the interface device 10 can be attached to a host device (not shown) via a host line 11. The first connecting device is attached both to a digital signal processor 13 and to a memory means 14. The digital signal processor 13 and the memory means 14 are also attached to a second connecting device 15 by means of bi-directional communication lines (shown for all lines by means of two directional arrows). The second connecting device can be attached by means of an output line 16 to a data transmit/receive device which is to receive data from the host device or from which data is to be read, i.e. acquired, and transferred to the host device. The data transmit/receive device itself can also communicate actively with the host device via the first and second connecting device, as described in more detail in the following.

Communication between the host system or host device and the interface device is based on known standard access commands as supported by all known operating

systems (e.g. DOS, Windows, Unix). Preferably, the interface device according to the present invention simulates a hard disk with a root directory whose entries are "virtual" files which can be created for the most varied functions. When the host device system with which the interface device according to the present invention is connected is booted and a data transmit/receive device is also attached to the interface device 10, usual BIOS routines or multi-purpose interface programs issue an instruction, known by those skilled in the art as the INQUIRY instruction, to the input/output interfaces in the host device. The digital signal processor 13 receives this inquiry instruction via the first connecting device and generates a signal which is sent to the host device (not shown) again via the first connecting device 12 and the host line 11. This signal indicates to the host device that, for example, a hard disk drive is attached at the interface to which the INQUIRY instruction was sent. Optionally, the host device can send an instruction, known by those skilled in the art as "Test Unit Ready", to the interface device to request more precise details regarding the queried device.

Regardless of which data transmit/receive device at the output line 16 is attached to the second connecting device, the digital signal processor 13 informs the host device that it is communicating with a hard disk drive. If the host device receives the response that a drive is present, it then sends a request to the interface device 10 to read the boot sequence which, on actual hard disks, normally resides on the first sectors of the disk. The digital signal processor 13, whose operating system in stored in the memory means 14, responds to this instruction by sending to the host device a virtual boot sequence which, in the case of actual drives, includes the drive type, the starting position and the length of the file allocation table (FAT), the number of sectors, etc., known to those skilled in the art. Once the host device has received this data, it assumes that the interface device 10 according to a preferred embodiment of the present invention is a hard disk drive. In reply to an instruction from the host device to display the directory of the "virtual" hard disk drive simulated by the interface device 10 with respect to the host device, the digital signal processor can respond to the host device in exactly the same way as a conventional hard disk would, namely by reading on request the file allocation table or FAT on a sector specified in the boot sequence, normally the first writable sector, and transferring it to the host device, and subsequently by transferring the directory structure of the virtual hard

disk. Further, it is possible that the FAT is not read until immediately prior to reading or storing the data of the "virtual" hard disk and not already at initialization.

In a preferred embodiment of the present invention, the digital signal processor 13, which need not necessarily be implemented as a digital signal processor but may be any other kind of microprocessor, comprises a first and a second command interpreter. The first command interpreter carries out the steps described above whilst the second command interpreter carries out the read/write assignment to specific functions. If the user now wishes to read data from the data transmit/receive device via the line 16, the host device sends a command, for example "read file xy", to the interface device. As described above, the interface device appears to the host device as a hard disk. The second command interpreter of the digital signal processor now interprets the read command of the host processor as a data transfer command, by decoding whether "xy" denotes, for example, a "real-time input" file, a "configuration" file or an executable file, whereby the same begins to transfer data from the data transmit/receive device via the second connecting device to the first connecting device and via the line 11 to the host device.

Preferably, the volume of data to be acquired by a data transmit/receive device is specified in a configuration file described in the following by the user specifying in the said configuration file that a measurement is to last, for example, five minutes. To the host device the "real-time input" file then appears as a file whose length corresponds to the anticipated volume of data in those five minutes. Those skilled in the art know that communication between a processor and a hard disk consists of the processor transferring to the hard disk the numbers of the blocks or clusters or sectors whose contents it wishes to read. By reference to the FAT the processor knows which information is contained in which block. In this case, communication between the host device and the interface device according to the present invention therefore consists of the very fast transfer of block numbers and preferably of block number ranges because a virtual "real-time input" file will not be fragmented. If the host device now wants to read the "real-time input" file, it transfers a range of block numbers to the interface device, whereupon data commences to be received via the second connecting device and data commences to be sent to the host device via the first connecting device.

In addition to the digital signal processor instruction memory, which comprises the operating system of the digital signal processor and can be implemented as an EPROM or EEPROM, the memory means 14 can have an additional buffer for purposes of synchronizing data transfer from the data transmit/receive device to the interface device 10 and data transfer from the interface device 10 to the host device.

Preferably, the buffer is implemented as a fast random access memory or RAM buffer.

Further, from the host device the user can also create a configuration file, whose entries automatically set and control various functions of the interface device 10, on the interface device 10 which appears to the host device as a hard disk. These settings can be, for example, gain, multiplex or sampling rate settings. By creating and editing a configuration file, normally a text file which is simple to understand with little prior knowledge, users of the interface device 10 are able to perform essentially identical operator actions for almost any data transmit/receive devices which can be attached to the second connecting device via the line 16, thus eliminating a source of error arising from users having to know many different command codes for different applications. In the case of the interface device 10 according to the present invention it is necessary for users to note the conventions of the configuration file once only in order to be able to use the interface device 10 as an interface between a host device and almost any data transmit/receive device.

As a result of the option of storing any files in agreed formats in the memory means 14 of the interface device 10, taking into account the maximum capacity of the memory means, any enhancements or even completely new functions of the interface device 10 can be quickly implemented. Even files executable by the host device, such as batch files or executable files (BAT or EXE files), and also help files can be implemented in the interface device, thus achieving independence of the interface device 10 from any additional software (with the exception of the BIOS routines) of the host device. On the one hand, this avoids licensing and/or registration problems and, on the other hand, installation of certain routines which can be frequently used, for example an FFT routine to examine acquired time-domain data in the frequency

domain, is rendered unnecessary as the EXE files are already installed on the interface device 10 and appear in the virtual root directory, by means of which the host device can access all programs stored on the interface device 10.

In a preferred embodiment of the present invention in which the interface device 10 simulates a hard disk to the host device, the interface device is automatically detected and readied for operation when the host system is powered up or booted. This corresponds to the plug-and-play standard which is currently finding increasingly widespread use. The user is no longer responsible for installing the interface device 10 on the host device by means of specific drivers which must also be loaded; instead the interface device 10 is automatically readied for operation when the host system is booted.

For persons skilled in the art it is however obvious that the interface device 10 is not necessarily signed on when the computer system is powered up but that a special BIOS routine or a driver for a multi-purpose interface can also be started on the host device during current operation of the computer system in order to sign on or mount the interface device 10 as an additional hard disk. This embodiment is suitable for larger workstation systems which are essentially never powered down as they perform, e.g. mail functions or monitor processes which run continuously, for example, in multi-tasking environments.

In the interface device according to the present invention an enormous advantage is to be gained, as apparent in the embodiment described in the following, in separating the actual hardware required to attach the interface device 10 to the data transmit/receive device from the communication unit, which is implemented by the digital signal processor 13, the memory means 14 and the first connecting device 12, as this allows a plurality of dissimilar device types to be operated in parallel in identical manner. Accordingly, many interface devices 10 can be connected to a host device which then sees many different "virtual" hard disks. In addition, any modification of the specific hardware symbolized by the second connecting device 15 can be implemented essentially without changing the operation of the interface device according to the present invention. Further, an experienced user can intervene at any time on any level of the existing second connecting device by making use of the above mentioned

option of creating a configuration file or adding or storing new program sections for the second connecting device.

An important advantage of the interface device 10 of the present invention is that it also permits extremely high data transfer rates by using, for data interchange, the host device-own BIOS routines which are optimized for each host device by the host device manufacturer or BIOS system manufacturer, or by using driver programs which are normally optimized and included by the manufacturers of multi-purpose interfaces. Furthermore, due to the simulation of a virtual mass storage device, the data is managed and made available in such a way that it can be transferred directly to other storage media, e.g. to an actual hard disk of the host device without, as it were, intervention of the host device processor. The only limitation to long-term data transfer at high speed is therefore imposed exclusively by the speed and the size of the mass storage device of the host device. This is the case as the digital signal processor 13 already formats the data read by the data transmit/receive device via the second connecting device 15 into block sizes suitable for a hard disk of the host device, whereby the data transfer speed is limited only by the mechanical latency of the hard disk system of the host device. At this point, it should be noted that normally data flow from a host device must be formatted in blocks to permit writing to a hard disk and subsequent reading from a hard disk, as known by those skilled in the art.

The said data transfer rate can be increased further by setting up a direct memory access (DMA) or RAM drive in the host system. As those skilled in the art know, the setting up of a RAM drive requires processor resources of the host device, with the result that the advantage of writing the data to a hard disk drive of the host device essentially without the need for processor resources is lost.

As described above, a data buffer can be implemented in the memory means 14 to permit independence in terms of time of the data transmit/receive device attached to the second connecting device from the host device attached to the first connecting device. This guarantees error-free operation of the interface device 10 even for time-critical applications in multi-tasking host systems.

Fig. 2 shows a detailed block diagram of an interface device 10 according to the present invention.

A digital signal processor (DSP) 1300 is, in a manner of speaking, the heart of the interface device 10. The DSP can be any DSP but preferably has a 20-MB on-chip random access memory (RAM). Certain instruction sets, for example, can be stored in the RAM already integrated in the DSP. An 80-MHz clock generator is attached to the DSP 1300 in order to synchronize the DSP. The DSP implements a fast Fourier transformation (FFT) in real time and also optional data compression of the data to be transferred from the data transmit/receive device to the host device in order to achieve greater efficiency and to permit interoperation with host devices which have a smaller memory.

In the preferred embodiment of the interface device 10 shown in Fig. 2, the first connecting device 12 of Fig. 1 contains the following components: an SCSI interface 1220 and a 50-pin SCSI connector 1240 for attachment to an SCSI interface present on most host devices or laptops. The SCSI (small computer system interface) interface 1220 translates the data received via the SCSI connector 1240 into data understood by the DSP 1300, as known by those skilled in the art. Further, the first connecting device 12 comprises an EPP (enhanced parallel port) with a data transfer rate of approx. 1 MBps which delivers a more moderate data transfer rate of 1 MBps by comparison to the data transfer rate of 10 MBps of the SCSI interface. The EPP 1260 is connected to a 25-pin D-shell connector 1280 to permit attachment to a printer interface of a host device for example. Optionally, the first connecting device 12 also comprises a 25-pin connector 1282 which permits the attachment of 8 digital outputs and 8 digital inputs 1284 at a host device.

Preferably, the second connecting device comprises 8 BNC inputs with the calibration relay 1505, a block 1510 with 8 device amplifiers with an overvoltage protection of ±75 V, this block being connected in turn to 8 sample/hold (S&H) circuits 1515. The calibration relays are relays which permit controlled changeover between a test voltage and a calibration reference voltage. Each sample/hold circuit is connected to a corresponding input of an 8-channel multiplexer 1520 which feeds its output signals

via a programmable amplifier 1525 into an analog/digital converter (ADC) with 12 bit and 1.25 MHz 1530 and to the DSP 1300. The ADC 1530 is controlled by means of a 20-bit timer 1535, as known by persons skilled in the art. The programmable amplifier 1525 and the 8-channel multiplexer 1520 are controlled via an amplifier channel selection circuit 1540 which is in turn controlled by the DSP 1300.

The complete interface device 10 is supplied with power by an external AC/DC converter 1800 which delivers a digital supply voltage of ±5 V and is attached to a DC/DC converter 1810 which can deliver analog supply voltages of ±5 V and ±15 V as required for the interface device 10. Further, the DC/DC converter controls a precision voltage reference 1820 which controls the 8 BNC inputs 1505 and the ADC 1530 as well as a digital/analog converter (DAC) 1830 which permits, via an output amplifier block with 4 output amplifiers 1840 and a 9-pin connector 1850, analog output direct from the DSP 1300 to an output device, e.g. printer device or monitor device, which can be attached via the 9-pin connector 1850, thus providing the option of monitoring the data transferred to the host device or also, for example, of viewing an FFT to obtain rapid and comprehensive data analysis without using processor time of the host device.

In Fig. 2 the memory means 14 of Fig. 1 is implemented by an EPROM 1400 which, in a preferred embodiment of the present invention, contains the operating system of the digital signal processor 1300. A random access memory with an access time of 15 ns and a size of 512 KB or optionally 1024 KB 1420 serves as a data buffer to achieve independence in terms of time of the output line 16 from the output lines 11a, 11b and 11c to the data transmit/receive device and to the host device respectively. As described above, in a preferred embodiment of the present invention the digital signal processor 1300 already contains a 20-KB on-chip RAM 1440 which can store certain instruction sets, functions and also smaller application software units.

The connection, symbolized by the line 16, of the interface device 10 to any data transmit/receive device implements, by means of the blocks 1505 – 1535, an analog input with a sampling rate of 1.25 MHz and quantization of 12 bits. There are 8 channels with an overvoltage protection of ± 75 V. By means of the programmable

amplifier 1525 the channels can be programmed independently of each other in voltage ranges up to a maximum of ± 10 V. Unused channels can be grounded internally to reduce channel intermodulation. The block 1515 is implemented as a monolithic high-precision, high-speed sample/hold amplifier for simultaneous sampling of all channels. The precision voltage reference 1820 provides a high-precision, temperature-compensated monolithic energy gap voltage reference for auto-calibration of each channel and each gain. Further, offset fine adjustment for each channel is implemented by the same.

The blocks 1830, 1840 and 1850 implement a direct analog output for the digital signal processor 1300, and the DAC 1830 provides a data transfer rate of 625 kHz and a quantization of 12 bits. The block 1840 comprises 4 channels with a common output latch.

Further, the interface device 10 comprises a digital input/output device implemented by the blocks 1284 and 1282. Here there are 8 digital inputs, 8 digital outputs with a common latch, and the digital port can be attached preferably to a side panel of the interface device 10 so that the port itself can easily be accessed.

The digital signal processor 1300 provides on-board digital data processing. In particular, it is a high-performance DSP with a clock speed of 80 MHz and a 20-bit timer 1535.

As described above, the first connecting device 12 comprises the SCSI interface 1220 with a peak transfer rate of 10 MBps. An optional PCMCIA-to-SCSI adapter permits high-speed communication with laptop computers which are desirable and in widespread use, particularly by mobile service technicians. The EPP 1260 with its associated connector 1280 permits data transfer at a more moderate rate.

As described above, the interface device 10 is supplied with power by means of an external AC/DC adapter which has a universal power input (85 – 264 VAC, 47 – 63 Hz). Interference suppression complies with the standards EN 55022, curve B and FFC, Class B). Further, it is also in accordance with international safety regulations

(TÜV, UL, CSA). The interface device 10 is externally shielded and achieves a value of 55 dB at 30 – 60 MHz and a value of approximately 40 dB at 1 GHz, and therefore complies with the MILSTD 285-1 standard.

As described above, communication between the host device and the multi-purpose interface can take place not only via drivers for input/output device customary in a host device which reside in the BIOS system of the host device but also via specific interface drivers which, in the case of SCSI interfaces, are known as multi-purpose interface ASPI (advanced SCSI programming interface) drivers. This ASPI driver, which can also be referred to as an ASPI manager, is specific to a special SCSI host adapter, i.e. to a special multi-purpose interface, and is normally included by the manufacturer of the multi-purpose interface. Generally speaking, this multi-purpose interface driver has the task of moving precisely specified SCSI commands from the host system program to the host system SCSI adapter. For this reason, the command set is almost identical to that of the SCSI interface itself. Essentially, only status and reset commands for the host adapter have been added.

The ASPI driver can be used if the hard disk was not already addressable at boot time or if the SCSI-related BIOS routines of the host computer were still disabled. Here too, the steps needed to initialize the interface device, preferably as a virtual hard disk, are similar to the steps taken when initializing at boot time.

In general terms, the ASPI manager comprises two sides. One side is the proprietary, hardware-oriented side. It is responsible for converting all commands into a form required by the corresponding multi-purpose interface. The hardware-oriented side of the ASPI driver is therefore matched to a very specific type of multi-purpose interface or SCSI interface. The other side is known as the user software side. This side is totally independent of the proprietary operating characteristics of the SCSI adapter and is therefore identical for all SCSI interfaces. This permits SCSI programming which is however independent of the individual SCSI adapter types.

In contrast to communication between the host device and the interface device according to the present invention on the basis of a BIOS driver, the use of such an ASPI driver for communication between the host device and the interface device

according to the present invention allows various further possibilities of the SCSI multi-purpose interface to be exploited. In the case described above, the interface device which preferably signs on and behaves as a virtual hard disk is detected by the BIOS driver of the host computer at boot time and is configured as a hard disk. This step does not however support active requests sent by the interface device to the host computer. If however the virtual hard disk wishes to write data actively to, for example, a hard disk of the host computer or wishes to initiate communication with the processor of the host computer, the host computer must recognize the request of the virtual hard disk and tolerate a further issuer of instructions on its bus. If the interface device behaves solely like a virtual hard disk, it would always receive and never issue commands. The BIOS has no objections to an additional issuer of commands that actively wishes to place data on the bus of the host device but the BIOS does not support the host device in recognizing corresponding requests of the interface device or in granting the interface device permission to access the bus.

Using the ASPI manager the interface device according to the present invention can now obtain active access to an SCSI hard disk of the host device connected to the same SCSI bus which, in contrast to the interface device, cannot be a virtual but a real SCSI mass storage device or also a further interface device according to the present invention. Thereupon, the interface device according to the present invention can write the desired data to the SCSI hard disk of the host computer totally independently of the host computer or can communicate with the same in some other manner. The interface device according to the present invention therefore initially behaves passively as a virtual hard disk and then, as required and using the driver software for the multi-purpose interface, actively on the same SCSI bus. This means however that the interface device according to the present invention, using a driver software for the multi-purpose interface which comprises the BIOS routines customary in host devices and simultaneously provides the option of active participation, can, regardless of the type of the data transmit/receive device attached to the second connecting device, behave initially as a virtual and at the same time passive hard disk but can, as required, participate actively on the bus so as to be able to initiate communication directly with other SCSI hard disks of the host device by bypassing the processor of the host device.

Using a standard interface of a host device, the interface device according to the present invention permits communication with any host device. By simulating an input/output device to the host device and, in a preferred embodiment, by simulating a virtual mass storage device, the interface device 10 is automatically supported by all known host systems without any additional sophisticated driver software. The simulation of a freely definable file structure on the "virtual" hard disk provides simple operation and expansion options and, through the implementation of any programs, independence from special software implemented on the host device. Help files included on the interface device 10 and plug-and-play support ensure ease of use even in portable, flexible host devices. Despite the very simple user interface, experienced users are free at any time to intervene in the functions of the interface device 10 on system level. The interface device 10 thus provides a universal solution which can cover the entire spectrum of possible data transmit/receive devices.

hard disk driver, and the signal indicates to the host device that the host device is communicating with a hard disk.

3. An interface device (10) according to claim 1 or 2,

   wherein the memory means comprises a buffer (1420) to buffer data to be transferred between the data transmit/receive device and the host device.

4. An interface device (10) according to one of the preceding claims,

   wherein the multi-purpose interface of the host device is an SCSI interface and the first connecting device also comprises an SCSI interface (1220).

5. An interface device (10) according to one of the preceding claims,

   wherein the second connecting device comprises an analog input (1505) with a subsequent A/D converter (1530) in order to transfer analog data to the host device from a data transmit/receive device connectable to the analog device (1505).

6. An interface device (10) according to one of the preceding claims,

   wherein the processor means (13) is a digital signal processor (1300).

7. An interface device (10) according to one of the claims 2 to 6,

   wherein the data to be transferred from the data transmit/receive device to the host device in the interface device (10) is formatted in a suitable format for a hard disk present in the host device.

8. An interface device (10) according to one of the claims 2 to 7,

   which further comprises a root directory and virtual files which are present on the

Claims

1. An interface device (10) for communication between a host device, which comprises drivers for input/output devices customary in a host device and a multi-purpose interface, and a data transmit/receive device comprising the following features:

   a processor means (13; 1300, 1320);

   a memory means (14; 1400, 1420, 1440);

   a first connecting device (12; 1220, 1240, 1260, 1280) for interfacing the host device with the interface device (10) via the multi-purpose interface of the host device; and

   a second connecting device (15; 1505 – 1535) for interfacing the interface device (10) with the data transmit/receive device,

   wherein the interface device (10) is configured by the processor means (13; 1300, 1320) and the memory means (14; 1400, 1420, 1440) in such a way that the interface device, when receiving an inquiry from the host device as to the type of a device attached to the multi-purpose interface of the host device, sends a signal, regardless of the type of the data transmit/receive device attached to the second connecting device (15; 1505 – 1535) of the interface device (10), to the host device which signals to the host device that it is an input/output device customary in a host device, whereupon the host device communicates with the interface device (10) by means of the driver for the input/output device customary in a host device.

2. An interface device (10) according to claim 1,

   wherein the drivers for input/output drivers customary in a host device comprise a

signaled hard disk drive and which can be accessed from the host device.

9. An interface device (10) according to claim 8,

wherein the virtual files comprise a configuration file in text format which are stored in the memory means (14) and using which the user can configure the interface device (10) for a specific data transmit/receive device.

10. An interface device (10) according to claim 8 or 9,

wherein the virtual files comprise batch files or executable files for the microprocessor means which are stored in the interface device (10) in order to perform data processing, independently of the host device, of data received via the second connecting device (15; 1505 – 1535).

11. An interface device (10) according to claim 8 or 9,

wherein the virtual files comprise batch files or executable files for the host device which are stored in the interface device (10).

12. An interface device (10) for communication between a host device, which comprises a multi-purpose interface and a specific driver for this interface, and a data transmit/receive device comprising the following features:

a processor means (13; 1300, 1320);

a memory means (14; 1400, 1420, 1440);

a first connecting device (12; 1220, 1240, 1260, 1280) for interfacing the host device with the interface device (10) via the multi-purpose interface of the host device; and

a second connecting device (15; 1505 – 1535) for interfacing the interface device (10) with the data transmit/receive device,

where the interface device (10) is configured using the processor means (13; 1300, 1320) and the memory means (14; 1400, 1420, 1440) in such a way that the interface device, when receiving an inquiry from the host device as to the type of a device attached at the multi-purpose interface of the host device, sends a signal, regardless of the type of the data transmit/receive device attached to the second connecting device (15; 1505 – 1535) of the interface device (10), to the host device which signals to the host device that it is an input/output device customary in a host device, whereupon the host device communicates with the interface device (10) by means of the specific driver for the multi-purpose interface.

13. An interface device according to claim 12,

wherein, in addition to the first connecting device of the interface device, there is a further input/output device at the multi-purpose interface of the host device, and wherein the interface device can communicate directly with the hard disk via the specific driver for the multi-purpose interface.

14. An interface device according to claim 12 or 13,

wherein the multi-purpose interface is an SCSI interface, and wherein the specific driver for the multi-purpose interface is an ASPI manager.

15. A method of communication between a host device, which comprises drivers for input/output devices customary in a host device and a multi-purpose interface, and a data transmit/receive device via an interface device (10) comprising the following steps:

interfacing of the host device with a first connecting device (12; 1220, 1240, 1260, 1280) of the interface device (10) via the multi-purpose interface of the host device;

interfacing of the data transmit/receive device with a second connecting device (15; 1505 – 1535) of the interface device (10);

inquiring by the host device at the interface device (10) as to the type of device to which the multi-purpose interface of the host device is attached;

regardless of the type of the data transmit/receive device attached to the second connecting device of the interface device (10), responding to the inquiry from the host device by the interface device (10) in such a way that it is an input/output device customary in a host device, whereupon the host device communicates with the interface device (10) by means of the usual driver for the input/output device.

16. A method according to claim 15,

wherein the drivers for input/output devices customary in a host device comprise a driver for a storage device and in particular for a hard disk drive.

Flexible Interface

ABSTRACT

An interface device (10) provides fast data communication between a host device with input/output interfaces and a data transmit/receive device, wherein the interface device (10) comprises a processor means (13), a memory means (14), a first connecting device (12) for interfacing the host device with the interface device, and a second connecting device (15) for interfacing the interface device (10) with the data transmit/receive device. The interface device (10) is configured by the processor means (13) and the memory means (14) in such a way that, when receiving an inquiry from the host device via the first connecting device (12) as to the type of a device attached to the host device, regardless of the type of the data transmit/receive device, the interface device sends a signal to the host device via the first connecting device (12) which signals to the host device that it is communicating with an input/output device.

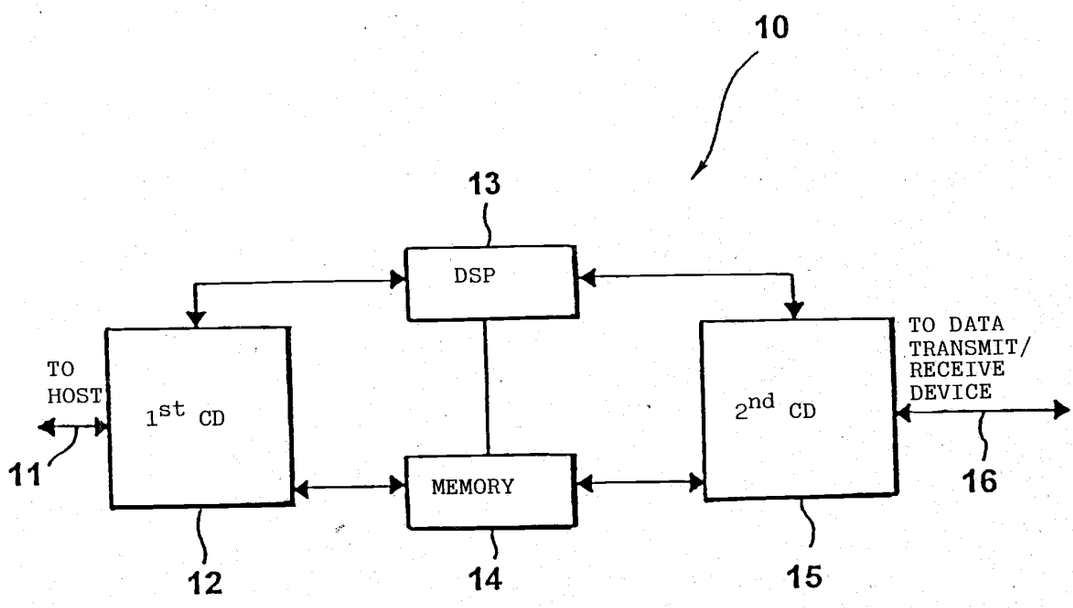
10
13
DSP
TO
HOST
1st CD
11
12
MEMORY
14
2nd CD
15
TO DATA
TRANSMIT/
RECEIVE
DEVICE
16

FIG.1

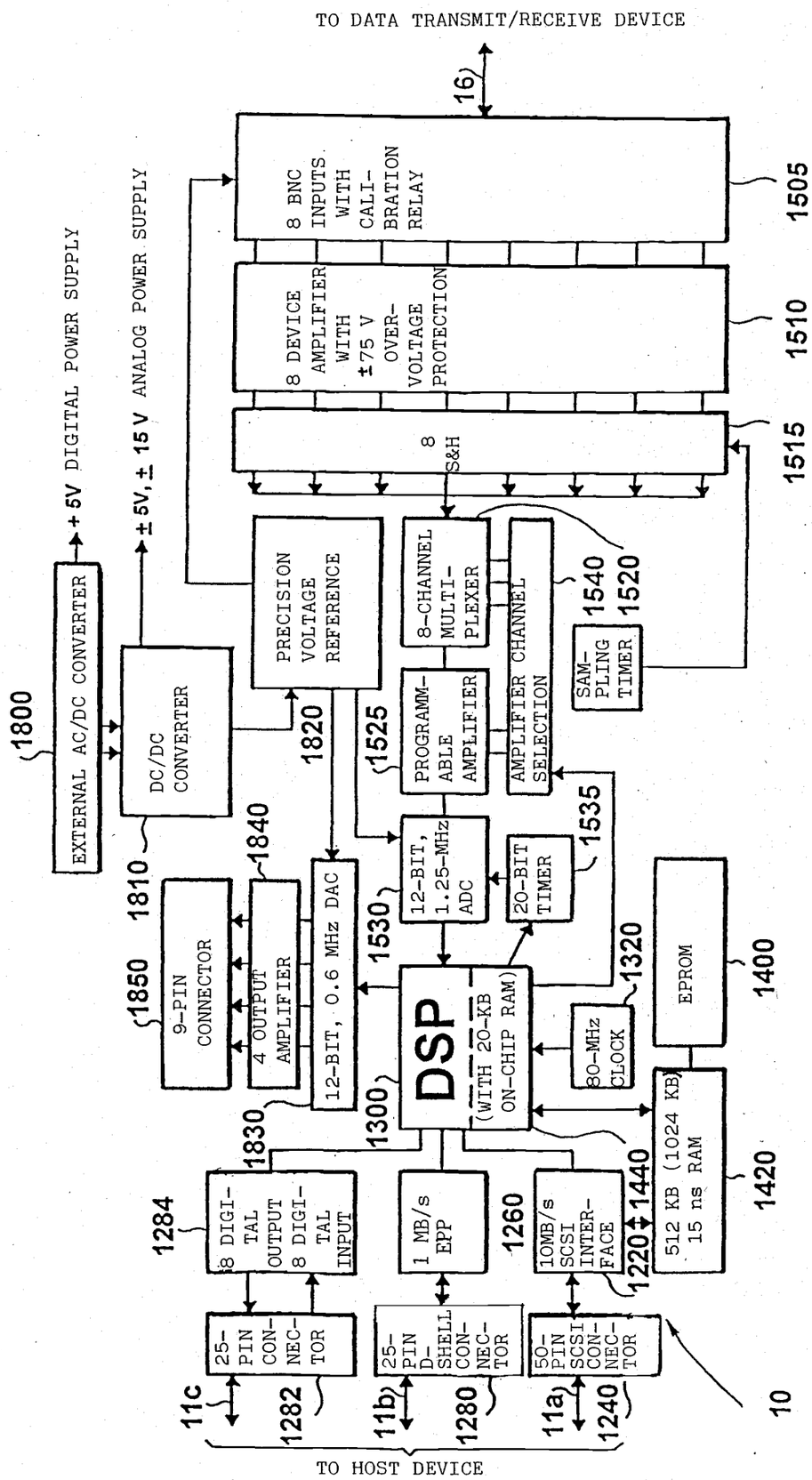
TO DATA TRANSMIT/RECEIVE DEVICE
16
8 BNC INPUTS WITH CALI-BRATION RELAY
1505
8 DEVICE AMPLIFIER WITH ±75 V OVER-VOLTAGE PROTECTION
1510
8 S&H
1515
8-CHANNEL MULTI-PLEXER
1540
PROGRAMM-ABLE AMPLIFIER
1525
AMPLIFIER CHANNEL SELECTION
SAM-PLING TIMER
1520
PRECISION VOLTAGE REFERENCE
1820
DC/DC CONVERTER
1810
EXTERNAL AC/DC CONVERTER
1800
+5V DIGITAL POWER SUPPLY
±5V, ±15V ANALOG POWER SUPPLY
12-BIT, 1.25-MHz ADC
1530
20-BIT TIMER
1535
9-PIN CONNECTOR
1850
4 OUTPUT AMPLIFIER
1840
12-BIT, 0.6 MHz DAC
DSP
(WITH 20-KB ON-CHIP RAM)
1300
80-MHz CLOCK
1320
EPROM
1400
8 DIGI-TAL OUTPUT 8 DIGI-TAL INPUT
1284
1830
1 MB/s EPP
1260
10MB/s SCSI INTER-FACE
1220
1440
512 KB (1024 KB) 15 ns RAM
1420
25-PIN CON-NEC-TOR
1282
25-PIN D-SHELL CON-NEC-TOR
1280
50-PIN SCSI CON-NEC-TOR
1240
11c
11b
11a
10
TO HOST DEVICE

FIG.2

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Application Number	09/331,002
Filing Date	14 Jun 1999
First Named Inventor	Michael Tasler
Group Art Unit	2782 ✓
Examiner Name	Unknown
Attorney Docket Number	2055/101

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Practitioner's Docket No. 13189.129 (Formerly 2055/101) *PATENT* 10-29-01

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:	Tasler, Michael		
Application No.:	09/331,002	Group No.:	2182
Filed:	June 14, 1999	Examiner:	Lee, Thomas C.
For:	FLEXIBLE INTERFACE		

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TRANSMITTAL OF SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT WITHIN THREE MONTHS OF FILING OR BEFORE MAILING OF FIRST OFFICE ACTION (37 C.F.R. Section 1.97(b))

IDENTIFICATION OF TIME OF FILING THE ACCOMPANYING SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

The Supplemental information Disclosure Statement submitted herewith is being filed within three months of the filing date of the application or date of entry into the national stage of an international application or before the mailing date of a first Office Action on the merits, whichever event occurs last. 37 C.F.R. Section 1.97(b). A concise explanation of the relevance, as it is present understood by the individual designated in Section 1.56(c) most knowledgeable about the content of the information, of each patent, publication, or other information listed that is not in the English language, is attached hereto.

STATEMENT ACCORDING TO 37 C.F.R. Section 1.97(3)(1)

Each item of information contained in this Supplemental Information Disclosure Statement was cited in a communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this Supplemental Information Disclosure Statement.

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Carl A. Forest
Customer No.: 24283

US Patent Application Serial No. 09/331,002 Group Art Unit No.: 2182
Filing Date: June 14, 1999 Examiner: Lee, Thomas C.
Inventor: Michael Tasler
Title: Flexible Interface

CONCISE EXPLANATION OF RELEVANCE OF REFERENCES

DE 195 28 889 A1 discloses a method and apparatus for video coding. The video source and an audio source are coupled to an MPEG encoder which is coupled with an intermediate memory. Connected to the intermediate memory are a hard drive controller which is associated with a hard drive and a network controller which is associated with an interface to a network. The hard drive itself is also connected to an interface to a network. Therefore, data output by the MPEG encoder are not transmitted to the hard drive immediately but via the intermediate memory. The intermediate memory which may be a dynamic RAM can, therefore, be regarded as a virtual drive.

This reference is silent about an interface device having drivers for customary input/ output devices. Additionally, this reference does not disclose an interface device which is configured by the processor and the memory in such a way as described in the last paragraph of claim 1 of the subject application.

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Application Number	09/331,002
Filing Date	06/14/1999
First Named Inventor	Michael Tasler
Group Art Unit	2182
Examiner Name	Lee, Thomas C.
Attorney Docket Number	13189.129 (Formerly 2055/101)

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U.S. PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	U.S. Patent Document Number	Kind Code[2] (if known)	Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
TC	1	5,506,692		Kazuyuki Murata	04/09/1996	

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FOREIGN PATENT DOCUMENTS

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TC	2	EP	0 436 458 A2		Bryan Striemer	07/10/1991		
TC	3	WO	94/19746		Clay et al.	09/01/1994		
TC	4	JP	06301607 A		Ugajin Atsushi	10/28/1994		X
TC	5	JP	08110883 A		Nakahara Toru	04/30/1996		X
TC	6	DE	195 28 889 A1		Jurmann et al.	02/06/1997		

Examiner Signature	Thomas Lee	Date Considered	12/06/01

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Filing Date	06/14/1999
First Named Inventor	Michael Tasler
Group Art Unit	2182
Examiner Name	Lee, Thomas C.
Attorney Docket Number	13189.129 (Formerly 2055/101)

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OTHER PRIOR ART -- NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
TL	7	STEVE MARTIN, "PC-based Data Acquisition in an Industrial Environment," p. 1-3 (1990).	
TL	8	PAYNE ET AL., "High Speed PC-based Data Acquisition Systems," IEEE, p. 2140-2145 (1995).	

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(19) JAPANESE PATENT OFFICE

PATENT ABSTRACTS OF JAPAN

(11) Publication number: 06301607 A

(43) Date of publication of application: 28 . 10 . 94

(51) Int. Cl G06F 13/00
G06F 13/12

(21) Application number: 05086000

(22) Date of filing: 13 . 04 . 93

(71) Applicant: HITACHI LTD

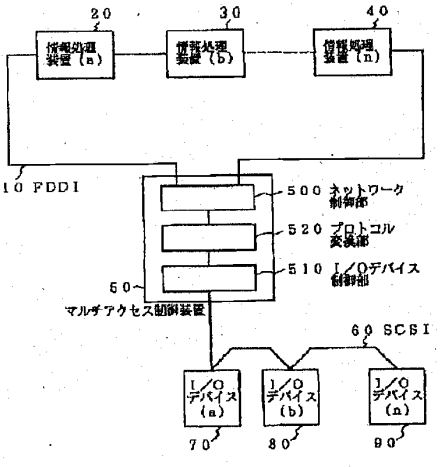
(72) Inventor: UGAJIN ATSUSHI

(54) MULTIACCESS I/O CONTROL SYSTEM

(57) Abstract:

PURPOSE: To make it possible to access plural I/O devices from plural information processors.

CONSTITUTION: Plural information processors 20, 30, 40 and a multi-access control device 50 are connected to an FDDI 10 and the device 50 is connected to I/O devices 70, 80, 90 through an SCSI 60. Each information processor accesses the device 50 in each FDDI frame. A network control part 500 transmits/receives data to/from the information processor by an FDDI interface, a protocol conversion part 520 converts the received information into an SCSI protocol and accesses respective I/O devices 70, 80, 90 through an I/O device control part 510.



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CLAIMS

[Claim(s)]
[Claim 1] It is the multi-access I/O control system which establishes the multi-access-control means which consists of a protocol conversion means perform interface conversion of a network-control means perform an interface control of this network, an I/O device control means control two or more I/O devices through an I/O interface, and this network-control means and an I/O device control means, in the system which connected two or more information processors through the network, and is characterized by for two or more aforementioned information processors to access two or more aforementioned I/O devices through this multi-access-control means.
[Claim 2] The multi-access I/O control system according to claim 1 characterized by building the aforementioned I/O device control means in the control section in the aforementioned I/O device.
[Claim 3] It is the multi-access I/O control system according to claim 1 which stores in the aforementioned predetermined I/O device the processed data which two or more aforementioned information processors performed through the aforementioned multi-access-control means, changes them to a spare information processor at the time of failure occurrence of this information processor, and is characterized by the information processor of this reserve continuing processing with reference to the I/O device in which the aforementioned processed data were stored.
[Claim 4] Each aforementioned information processor is a multi-access I/O control system according to claim 1 characterized by storing in the I/O device corresponding to the aforementioned information processor the information which has a local I/O device and is recorded on this local I/O device, and backing it up through the aforementioned multi-access-control means.
[Claim 5] The aforementioned I/O interface is a multi-access I/O control system according to claim 1 characterized by consisting of an interface only for sendings, and an interface of reception only.

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DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention] this invention relates to the control system of an accessible I/O device from two or more information processors about a multi-access I/O control system in the system which connected two or more information processors especially through the network.
[0002]
[Description of the Prior Art] There is a method indicated by JP,4-196737,A as technique which shares an I/O device with two or more processors. In this method, after sharing one set of the console for a maintenance between two or more sets of host computers and buffering the received data from a host computer, it notifies to a control unit, and this control unit sets up the switch for host selection, and outputs a host's selected data to the console for a maintenance.
[0003]
[Problem(s) to be Solved by the Invention] However, since the above-mentioned technique has formed the buffer independently for every host interface Since the amount of hardware increases, and the peculiar hardware like a host selecting switch is needed and a number equivalent to the number of hosts of host interface connectors are needed further When the hosts who connect increased in number, while the whole equipment large-sized-ized, there was a fault that only the configuration which connected one set of a console to two or more sets of hosts could be taken.
[0004] The purpose of this invention is to offer the multi-access I/O control system which enables the access to two or more I/O devices from two or more information processors.
[0005]
[Means for Solving the Problem] In order to attain the aforementioned purpose, in invention according to claim 1 In the system which connected two or more information processors through the network A network control means to perform an interface control of this network, An I/O device control means to control two or more I/O devices through an I/O interface, The multi-access-control means which consists of a protocol conversion means to perform interface conversion of this network control means and an I/O device control means is established. It is characterized by two or more aforementioned information processors accessing two or more aforementioned I/O devices through this multi-access-control means.
[0006] In invention according to claim 2, it is characterized by building the aforementioned I/O device control means in the control section in the aforementioned I/O device.
[0007] In invention according to claim 3, the processed data which two or more aforementioned information processors performed are stored in the aforementioned predetermined I/O device through the aforementioned multi-access-control means, and are changed to a spare information processor at the time of failure occurrence of this information processor, and it is characterized by the information processor of this reserve continuing processing with reference to the I/O device in which the aforementioned processed data were stored.
[0008] In invention according to claim 4, it is characterized by storing each aforementioned information processor in the I/O device corresponding to the aforementioned information processor, and backing up the information which has a local I/O device and is recorded on this local I/O device through the aforementioned multi-access-control means.
[0009] In invention according to claim 5, the aforementioned I/O interface is characterized by

consisting of an interface only for sendings, and an interface of reception only.
[0010]
[Function] Two or more information processors and multi-access-control equipments are connected to FDDI, and SCSI connection of the multi-access-control equipment is made at the I/O device. Multi-access-control equipment consists of the network control section, the protocol conversion section, and an I/O device control section. An information processor is accessed with FDDI frame to multi-access-control equipment. After the network control section transmits and receives the data from an information processor with FDDI interface, in the protocol conversion section, it is changed into SCSI protocol and accesses an I/O device through an I/O device control section. Thereby, two or more I/O devices can be controlled from two or more information processors [add / multi-access-control equipment], without adding change to the conventional I/O device in any way.
[0011]
[Example] Hereafter, one example of this invention is concretely explained using a drawing. Drawing 1 is a system configuration view concerning one example of this invention. Two or more information processors 20, 30, and 40 and multi-access-control equipments 50 are connected to FDDI (FiberDistributed Data Interface)10 (LAN), and the system of this invention is constituted.
[0012] The information processors 20, 30, and 40 connected to FDDI10 are accessed with FDDI frame to the multi-access-control equipment 50. The multi-access-control equipment 50 consists of the network control section 500 which performs FDDI interface control, an I/O device control section 510 which controls I/O devices 70, 80, and 90 (for example, means of communications, such as storages, such as a hard disk, and a circuit) connected to SCSI60, and the protocol conversion section 520 which performs interface conversion of FDDI protocol and SCSI protocol.

[0013] Drawing 2 is a block block diagram of the multi-access-control equipment 50. In the multi-access-control equipment 50, the network control section 500, the I/O device control section 510, RAM523, and the access-control section 524 are connected by I/O bus 525, and a processor 521, ROM522, and the access-control section 524 are connected by processor bus 526.
[0014] The program for performing protocol conversion is stored in ROM522, and operates on a processor 521. Although the processor bus 526 is formed in order to lower the activity ratio of I/O bus 525, when the access frequency from information processors 20, 30, and 40 is low, an I/O bus and a processor bus may carry out and consist of this example into the same bus.
[0015] The access-control section 524 is performing the access control to RAM523 from the access control to RAM523, the network control section 500, and the I/O device control section 510 and the network control section 500 from a processor 521, and the I/O device control section 510 while it performs the interrupt control to a processor 521 from the network control section 500 or the I/O device control section 510.
[0016] MAC (Media Access Control) address of FDDI other than a program is stored in ROM522. RAM523 is used as a descriptor field for using it as a buffer for a send data and a reception, and also performing the control to the network control section 500 and the I/O device control section 510. Moreover, it is used as a table for the status management in multi-access-control equipment, the management for every I/O device, etc.
[0017] Drawing 3 is drawing showing a format of the control frame to the multi-access-control equipment from an information processor. In drawing 3 , it controls by adding SNAP HDR 110, IP HDR 120, TCP HDR 130 (all being prescribed by Request For Comment), and the data 140 to FDDI HDR 100 (ANSI canonical).
[0018] TCP (Transmission Cotrol Protocol) performs the confirmation of receipt and sequence control between information processors 20, 30, and 40 and the multi-access-control equipment 50.

[0019] Data 140 consist of control block 1410 and 1450 and transmitting I/O data 1460, and control block consists of 1 or two or more blocks. Moreover, although the transmitting I/O data 1460 may be added or it is not necessary to add, the maximum frame length needs to be based on FDDI specification.

[0020] Control block 1410 and 1450 consists of 28 bytes. In control block 1410, the control-block length 1411 is 2 bytes of field, and shows the total byte chief of control block. It is shown whether the command chain bit 1412 consists of 1 bit, and control block of a different command is continuing. Command chain **** is shown at command chain nothing and the time of "1" at the time of "0."
[0021] It is 2 bytes of field and a device ID 1413 is SCSI_ID. 4 bits, LUN (Logical Unit Number) 4 bits, extended LUN It consists of 8 bits. The CDB format 1414 is a 5-bit field. Since CDB has 6 bytes, 10 bytes, and 12 bytes, it shows the class. 6 bytes and "1" show 10 bytes, and "2" shows ["0"] 12 bytes.
[0022] The inaccurate length suppression bit 1415 is a 1-bit field. It is a bit for not carrying out an error report, even if a lead demand differs from an actual readout data length. An error report is not carried out at the time of "1", but an error report is carried out at the time of "0."
[0023] The end report bit 1416 is a 1-bit field. An end report block (drawing 4) reports a processing end at the time of "1." It does not report at the time of "0."
[0024] A command 1421 is a 8-bit field. The designation to a data reception, a send data, and the multi-access-control equipment 50 etc. is shown. SCSI NO.1422 are a 8-bit field. When controlling two or more SCSI in the multi-access-control equipment 50, it is an information for discriminating which SCSI it is. Sequence NO.1420 are a 16-bit field. It is an information for making the end report from the demand and the multi-access-control equipment 50 from information processors 20, 30, and 40 correspond.
[0025] The data count 1418 is 4 bytes of field, and shows the data length which transmits or receives. In this example, CDB1419 is 10 bytes and stores CDB based on SCSI specification.
[0026] Drawing 4 is drawing showing a format of the end frame to an information processor from multi-access-control equipment. In drawing, FDDI HDR 100, SNAP HDR 110, IP HDR 120, and TCP HDR 130 are the same as that of what was mentioned above. Data 140 consist of end report block 1470 and receiving I/O data 1480.
[0027] The end report block 1470 consists of 16 bytes. The end report block length 1471 is 16-bit ********, and shows the total byte count of an end report block. The end report chain bit 1472 is a 1-bit field, and when there are two or more end reports, it sets up "1."
[0028] The status 1474 is a 16-bit field. This field consists of 4 bits of the ****** tee bits which show the gravity of an error, and 12 bits of error-status fields. SAVE The DMA count 1473 is 4 bytes of field, and shows the difference of the byte count which actually carried out the completion of processing with the data count 1418. For example, this field is set to 0 when the data which the data count 1418 actually processed by 1000 bytes are 1000 bytes.
[0029] Drawing 5 shows the access sequence to the multi-access-control equipment 50 from an information processor 20 and the information processor 30. Hereafter, an operation of the example in the case of writing data in an I/O device from an information processor is explained.
[0030] It transmits to the multi-access-control equipment 50 from an information processor 20 by the frame format which shows data write-in designation in drawing 3 . The network control section 500 receives a frame and stores data in the buffer on RAM523 beforehand passed from the protocol conversion section 520. The network control section 500 notifies interruption to a processor 521 through the access-control section 524 after data storage.
[0031] After directing [data write-in] from an information processor 20, it transmits to the multi-access-control equipment 50 from an information processor 30 by the frame format which shows data write-in designation in drawing 3 . The network control section 500 stores data in the buffer on RAM523 which receives a frame and was beforehand passed from the protocol conversion section 520. The network control section 500 notifies interruption to a processor 521 through the access-control section 524 after data storage. However, it becomes a processing hold until the processing is completed, since processing from an information processor 20 is the point.
[0032] The protocol conversion section 520 which received interruption analyzes the HDR of the received frame, and performs TCP and IP (Internet Protocol) processing. Then, control block 1410 is analyzed. It is SCSI if a format is normal. A command is published to SCSI which NO.1422 and the device ID 1413 show. Issue of a command is performed by applying activation

to the hardware register in the I/O device control section 510, after storing CDB in the descriptor on RAM523. The I/O device control section 510 which received the command performs data transfer to I/O device 70 specified by the information processor 20, after transiting an Arbitration, a selection, a message, and a command phase according to SCSI specification.
[0033] Data transfer at this time is performed by DMA (Direct Memory Access). Stator and command complete-after [a data transfer end] and from I/O device 70 **********. The I/O device control section 510 which received this notifies interruption of processor 521 ** through the access-control section 524.
[0034] The processor 521 which received interruption analyzes the status stored in RAM523. Then, the end report block shown in drawing 4 , IP HDR, TCP HDR, and SNAP HDR are created on RAM523, and transmitting designation is written in the hardware register in the network control section 500. The network control section 500 which received this transmits an end report to an information processor 20 according to FDDI protocol.
[0035] Processing of an information processor 30 is performed after completing processing of an information processor 20. Since the operation is the same as that of the case of the information processor 20 mentioned above, an explanation is omitted.
[0036] Drawing 6 is drawing showing the configuration of other examples at the time of making multi-access-control equipment and an I/O device unify. That is, mode of processing which becomes unnecessary to prepare the I/O device control section 510 which the control section in an I/O device (SCSI controller) takes over the I/O device control section 510, therefore is shown in drawing 2 , and passes control block to the I/O control section 700 in a direct I/O device by unification will be taken.
[0037] drawing 7 -- present -- business -- it is drawing showing the configuration of other examples in the case of performing the change to a reserve system information processor from a system information processor present -- business -- when performing processing, through the multi-access-control equipment 50, the system information processors 21 and 22 are succeeded in arbitrary I/O devices 70, and carry out store processing of the information 71 and -- present -- business -- when failure occurs in the system information processors 21 and 22, the reserve system information processor 23 reads the taking over information 71 in I/O device 70, and continues processing
[0038] Drawing 8 is drawing showing the configuration of other examples in the case of backing up an information processor by the I/O device, and each information processor has taken the configuration equipped with the local I/O device.
[0039] while each information processors 20, 30, and 40 write out data to local I/O devices 201, 301, and 401, respectively -- an information processor 20 -- for example, to I/O device 70, an information processor 40 writes out data to I/O device 90, respectively, and an information processor 30 backs up data at I/O device 80 The sequence of the drawing 5 mentioned above performs this beginning.
[0040] Drawing 9 shows the configuration of other examples by which multi-access-control equipment controls two SCSI. In this example, two SCSI is controlled from one multi-access-control equipment, one side is made only into for sendings, and another side is made into reception only.
[0041] In drawing, the SCSI controller 511 is only for sendings, and the SCSI controller 512 is reception only. And in the writing to I/O device 70, the readout from I/O device 70 uses the SCSI controller 512 using the SCSI controller 511. However, the SCSI controller 511 performs the command to an I/O device altogether irrespective of a transmitting reception.
[0042] The method of this example is effective especially when the number of I/O devices is one. That is, since a device can specify it as one set, an Arbitration and a selection are [an Arbitration and a selection] omissible at the time of a deed and a subsequent access once [of the beginning]. Therefore, since it can be again made a command phase, without acting as a bus free-lancer after command complete sending by phase transition of SCSI, a high-speed data access becomes possible.
[0043] In addition, although this example described above, otherwise it can be constituted so that

the same data may be distributed to two or more I/O devices by using a broadcasting function, and a network and an interface may not be limited to above-mentioned FDDI and above-mentioned SCSI, but may be other networks and an interface.

[0044]

[Effect of the Invention] As mentioned above, the access to two or more I/O devices is attained from two or more information processors, without changing an I/O device, since the multi-access-control means which consists of a network control means, an I/O device control means, and a protocol conversion means is established according to invention according to claim 1 as explained.

[0045] According to invention according to claim 2, since the I/O device control section and SCSI controller in an I/O device are sharing-ized, an equipment configuration can be simplified.

[0046] Since the processed data which two or more information processors performed are stored in an I/O device according to invention according to claim 3, a preliminary change can be performed at high speed at the time of failure occurrence.

[0047] When according to invention according to claim 4 the unitary management of the backup data can be carried out and especially the removable I/O device like DAT is used, a media management becomes easy by specifying the information processor which backs up for every I/O device.

[0048] According to invention according to claim 5, since SCSI is divided into the transmitting interface and the receiving interface, an I/O device access of a high throughput is realizable.

[Translation done.]

(19) JAPANESE PATENT OFFICE

PATENT ABSTRACTS OF JAPAN

(11) Publication number: **08110883 A**

(43) Date of publication of application: **30 . 04 . 96**

(51) Int. Cl **G06F 13/14**
G06F 13/10

(21) Application number: **06245963**

(22) Date of filing: **12 . 10 . 94**

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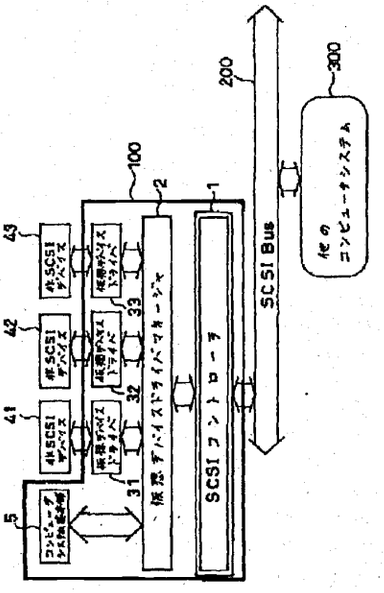
(54) **ACCESS METHOD FOR NON-SCSI DEVICE**

(57) Abstract:

PURPOSE: To enable even another computer system that is connected by an SCSI bus to directly use a non-SCSI device without performing the physical connection change of an existing SCSI bus, the addition of devices nor the set-up change of a terminal.

CONSTITUTION: An SCSI controller 1 picks up the command of another system 300 that is sent through an SCSI bus 200. The command picked up by the controller 1 is sent to a virtual device driver manager 2. The manager 2 distributes the commands to the virtual device drivers 31 to 33 which are designated by the LUN included in the command received from the controller 1. The devices 31 to 33 serve as the mediators to transfer the commands to the non-SCSI devices 41 to 43.



* NOTICES *

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

CLAIMS

[Claim(s)]
[Claim 1] The access technique of the non-SCSI device characterized by accessing the non-SCSI device connected to the virtual device driver according to the assigned command through the virtual device driver to which the command sent through SCSI bus is picked up, this picked-up command is sent to a virtual driver manager, the aforementioned command is assigned to a suitable virtual device driver by this virtual driver manager, and this command was assigned.
[Claim 2] The command sent through SCSI bus from other computer systems is picked up. This picked-up command is sent to a virtual driver manager. The aforementioned command is assigned the virtual device driver specified by the logical unit number contained in the command by this virtual driver manager. The access technique of the non-SCSI device characterized by accessing the non-SCSI device connected to the virtual device driver through the virtual device driver to which this command was assigned according to the assigned command.

[Translation done.]

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DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention] This invention relates to the access technique of the non-SCSI device which enables direct use (sharing) also from other computer systems that the device (non-SCSI (Small Computer System Interfase) device) connected with the interface peculiar to a computer system was connected to the computer system by SCSI bus.
[0002]
[Description of the Prior Art] A method which was shown in JP,4-297945,A ("the access technique of an electronic filing system") as a conventional example of the technique of sharing a non-SCSI device is held. In this method, a gateway unit is prepared in the connection place of SCSI bus, and use of the non-SCSI device connected outside is enabled by changing SCSI command within a gateway unit.
[0003]
[Problem(s) to be Solved by the Invention] However, in this method, a gateway unit must connect by SCSI bus. Moreover, since there was constraint that one ID must be assigned to a gateway unit, it had become the failure at the time of making extension and connection. Moreover, in this method, the non-SCSI device connected with the interface peculiar to a computer system cannot be directly used from other computer systems connected to the computer system by SCSI bus.
[0004] It is for offering the access technique of the non-SCSI device whose direct use of the non-SCSI device connected with the interface peculiar to a computer system also from other computer systems connected by SCSI bus is enabled, without having been made in order that this invention might solve such a technical probrem, and the place made into the purpose being able to make extension and connection easily, and performing change of the physical connection on the existing SCSI connection, addition of equipment, and setting change of a terminal.
[0005]
[Means for Solving the Problem] In order to attain such a purpose, the 1st invention (invention concerning a claim 1) picks up the command sent through SCSI bus, sends this picked-up command to a virtual driver manager, and is made to access the non-SCSI device connected to the virtual device driver by this virtual driver manager according to the assigned command through the virtual device driver to which the aforementioned command is assigned to a suitable virtual device driver, and this command was assigned.
[0006] The 2nd invention (invention concerning a claim 2) picks up the command sent through SCSI bus from other computer systems. This picked-up command is sent to a virtual driver manager. The aforementioned command is assigned the virtual device driver specified by the logical unit number contained in the command by this virtual driver manager. According to the assigned command, it is made to access the non-SCSI device connected to the virtual device driver through the virtual device driver to which this command was assigned.
[0007]
[Function] Therefore, according to this invention, by the 1st invention, the non-SCSI device connected to the virtual device driver to which the command sent through SCSI bus was assigned to the suitable virtual device driver by the virtual driver manager, and this command was assigned is accessed according to the assigned command.

[0008] In the 2nd invention, the non-SCSI device connected to the virtual device driver to which the virtual device driver the command sent through SCSI bus from other computer systems is specified to be by the logical unit number contained in the command was assigned by the virtual driver manager, and this command was assigned is accessed according to the assigned command.
[0009]
[Example] Hereafter, this invention is explained in detail based on an example. Drawing 1 is a structure-of-a-system view which comes to apply one example of this invention. In this drawing, 100 is the non-SCSI device connected with the computer system, the computer system of others [200 / 300 / SCSI bus and], and the interface with 41-43. / peculiar to a computer system 100
[0010] The SCSI controller 1 which picks up the command to the computer system 100 to which a computer system 100 is sent through the SCSI bus 200, A recognition [the logical unit number (LUN) contained in the command in the command which the SCSI controller 1 picked up] top, The virtual driver manager 2 assigned to the virtual device drivers 31-33 specified by the recognized LUN, The virtual device drivers 31-33 which perform a suitable operation or mediate a transfer of the command to non-SCSI devices 41-43 according to the command sent from a virtual driver manager 2, It has the computer-system basic section 5 which makes the basic section of a computer system 100.
[0011] In this example, a virtual driver manager 2 is installed on a computer system 100 at the time of system activation. A virtual driver manager 2 not only receives the command made into the object of the access to the SCSI device connected to SCSI interface not to illustrate, but performs assignment of starting of the virtual device drivers 31-33 at the time of activation, and LUN to virtual device drivers 31-33, and assignment of a command according to LUN contained in a command.
[0012] On the other hand, virtual device drivers 31-33 mediate the data transfer to the thing for which processing which doubled with the actual condition of each interface the command assigned from the virtual driver manager 2 is performed, and non-SCSI devices 41-43. By combining these, the access to non-SCSI 41-43 connected to the computer system 100 is attained from other computer systems 300.
[0013] Next, an example of SCSI command transfer explains a concrete operation of this system. In addition, the data flow from the computer-system basic section 5 and the data flow from the SCSI controller 1 are shown in drawing 2 as reference. The SCSI controller 1 will pick up the command, if own ID is held in a register and the command for self exists on the SCSI bus 200. And the picked-up command is sent to a virtual driver manager 2.
[0014] A virtual driver manager 2 assigns the command sent from the SCSI controller 1 to the virtual device drivers 31-33 specified by the recognized LUN after a recognition of LUN contained in the command. Virtual device drivers 31-33 perform an access by returning a virtual driver manager 2 to through and other computer systems 300 for the response according to the device type.
[0015] For example, this printer shall be accessed from other computer systems 300, using as a printer non-SCSI device 41 connected to the parallel port which exists on a computer system 100.
[0016] As the eye DIN ******** (Identify) message (it is hereafter called ID message) for making logical connection specified in the specification of SCSI was shown in drawing 3 , although, a virtual driver manager 2 recognizes LUN (number showing a target device) of ID message, and passes ID message to the virtual device driver 31 specified by this recognized LUN. In addition, in drawing 3 , if LUNTAR is "0", LUN expresses a target device.
[0017] If there is no problem in setting up logical connection, a command will be transmitted continuously and the art of the data sent after that will be specified. In the case of a printer, although logic connection may not be made with a paper jam etc., when other, the command which notifies print start is transmitted to a virtual device driver 31 after ID message sending.
[0018] After that, print data are transmitted to a printer 41 via a virtual driver manager 2 and the virtual device driver 31, and the access from other computer systems 300 is performed. And after a printing end, the command which cancels logic connection is sent from other computer systems 300, and printing is ended.

[0019] In addition, a release of the SCSI bus 200 is taken into consideration by sending during a printing, the disconnection message by which a virtual device driver 31 is defined during SCSI convention to other computer systems 300, when the receive buffer of print data becomes full by a certain cause and the reception beyond it cannot be performed.
[0020] Thus, by considering that non-SCSI devices 41-43 are SCSI equipments, and processing them Only by changing the software configuration only by the side of a computer system 100, without performing change of the physical connection on the existing SCSI connection, addition of equipment, and setting change of a terminal It is enabled to use directly non-SCSI devices 41-43 connected with the interface peculiar to a computer system 100 also from other computer systems 300 connected by SCSI bus 200, and extension and connection can also be easily made now.
[0021]
[Effect of the Invention] According to this invention, so that clearly from having explained above in the 1st invention The command sent through SCSI bus by the virtual driver manager is assigned to a suitable virtual device driver. The non-SCSI device connected to the virtual device driver to which this command was assigned By becoming what is accessed according to the assigned command, considering that a non-SCSI device is SCSI equipment, and processing it without performing change of the physical connection on the existing SCSI connection, addition of equipment, and setting change of a terminal It is enabled to use directly the non-SCSI device connected with the interface peculiar to a computer system also from other computer systems connected by SCSI bus, and extension and connection can also be easily made now.
[0022] In the 2nd invention, the command sent by the virtual driver manager through SCSI bus from other computer systems The virtual device driver specified by the logical unit number contained in the command is assigned. The non-SCSI device connected to the virtual device driver to which this command was assigned By becoming what is accessed according to the assigned command, considering that a non-SCSI device is SCSI equipment, and processing it without performing change of the physical connection on the existing SCSI connection, addition of equipment, and setting change of a terminal It is enabled to use directly the non-SCSI device connected with the interface peculiar to a computer system also from other computer systems connected by SCSI bus, and extension and connection can also be easily made now.

[Translation done.]

PC-based Data Acquisition in an Industrial Environment

Steve Martin (Application Engineer Burr-Brown)

Almost as soon as the IBM "PC" was introduced, data acquisition boards that could be plugged into it appeared on the market. These early boards were quite basic - they handled analog to digital conversion, digital to analog conversion, and digital I/O.

Nevertheless, these forerunners to modern data acquisition and control boards gave scientists and engineers away to apply the power of the personal computer to their real-world measurement and control problems. Most importantly, they did it an unprecedentedly low system cost.

As time went on, the boards became increasingly advanced. Faster analog to digital convertors were incorporated with programmable gain instrumentation amplifier front ends. Powerful features such as on-board memory and sophisticated DMA techniques began to appear.

A major limitation of the IBM "PC/XT/AT" family of computers in data acquisition and control applications is the fact that they were designed with office automation in mind. They were intended to be single user, single tasking, simple, low cost machines.

They excel at word processing and spreadsheet applications, but are often not up to the real-time requirements of high performance data acquisition and control. Indeed, many of the technical advances found in today's data acquisition and control boards have been directed at overcoming this sort of limitation.

One excellent solution to this problem is to put a high-performance processor right on the data acquisition board. This processor can assume control of the data acquisition functions, allowing the personal computer to act in a supervisory role. The PC can transfer programs to the data acquisition system and leave all the time critical operations where they are most effectively dealt with.

One data acquisition and control application was developed by a small company in West Germany. They used an intelligent data acquisition board designed to monitor and control 16 ultrasonic welders in real time.

At the beginning of the operation, the PC transfers the control program to the board from disc. It also transfers various standard parameters as explained below, and then starts the boards processor. After this point the PC has no further interaction with the system other than to act as a power supply.

Sixteen of the digital I/O channels are connected to relays used to turn the individual welders on or off. Additional channels are connected to an external machine controller which provides supervisory control.

For example, it determines when a part is available for welding and informs the board. It also monitors various system level alarm conditions, such as open welder doors, and

communicates these to the board as well.

Each of the 16 analog input channels are connected to one of the welders. These are used to monitor the power output of individual welders whenever a part is being welded. The bandwidth of interest is 50 Hz for each channel. To attain a clean 50 Hz bandwidth, the power is sampled at 1,000 samples/sec for each channel.

These samples are passed through a finite impulse response (FIR) digital filtering algorithm to remove a 50 Hz hum. A 20:1 downsampling algorithm then is used to develop 50 clean samples/sec/channel.

Note that since there are 16 channels, and each must be sampled at 1,000 samples/sec, the maximum aggregate system throughput is 16,000 samples/sec if all 16 welders are operating concurrently. Since all required processing must be performed in real time, each channels processing must be performed in between two successive samples 1/16,000 sec, or 62.5 usec. This would be an impossible task for a PC alone.

The power verses time curves developed above are compared with a stored optimum which was transferred from the PC at start-up. Additionally, alarm signals from the system supervisory controller are monitored, the on-time of each individual welder is monitored, and total power for each welder is summed to give energy.

Any anomalies in any of the monitored inputs are used to shut down the offending welder. This provides early detection of error conditions, prevents serious damage to the machine, and prevents the production of large amounts of scrap material.

Another data acquisition and control application for this type of system is in a high speed pneumatic actuator application. Such systems can be found in a variety of industries including aircraft simulators, automotive chassis testing, and high speed manipulators.

This application uses digital and serial I/O to monitor and control the position of a piston in a pneumatic tube. The position of the piston in the tube is determined by four solenoid valve connected to a high pressure compressed air system-two valves each for upward and downward movement.

The position of the piston is monitored by a sophisticated linear magnetic detection system. A small magnet is attached to the piston and hundreds of sensors on the tube detect the position of the piston.

With this system, an accuracy of better than 0.1 mm can be maintained over a length of one meter.

To achieve this, the detector system communicates with an intelligent board with a serial data stream of 1.5 Mbaud on the processor's serial input. The board has 32 channels of digital I/O to drive the four solenoid valves in response to set point commands from the host computer.

The PC's role is only supervisory, all of the complex feedback control algorithms are performed locally in the program running on the board. With the actuator attaining speeds of several meters per second, this is a demanding real-time data acquisition and control application which would be very difficult for the PC to accomplish on its own.

Another demanding application having appeal in a variety of industrial applications was demonstrated to a major aircraft manufacturer. Their specific interest was in airframe structural

testing, but the principles applied would apply quite well in virtually any high speed, multichannel control application.

The aircraft manufacturer was using hydraulic jacks which were controlled by analog proportional valves to produce stress on aircraft wings. Strain gages were used to monitor the stress, and the manufacturer wanted to construct a stress test control system.

Each hydraulic jack would have one or two strain gauges associated with it. On computer command, a given stress level would be called for by the system which would then drive the jacks and monitor the output from the strain gauges to achieve that level in a feedback control arrangement.

The company wanted to control as many as 32 jacks, with up to 64 strain gauges as feedback elements. They felt that an update rate of 200 point/sec for each hydraulic jack would be the optimum sample rate. Considering that there would be a possible maximum of 64 analog inputs to monitor, this would be an aggregate system throughput of 12,800 point/sec.

The intelligent board would acquire the analog inputs, perform all necessary calculations, and send the analog control outputs to a small block of the PC's memory under DMA control. Through a second DMA process, again synchronised by the boards pacer clock, these outputs are removed from the PC's memory and sent to the analog output devices.

All of the data transfers through the PC is done via DMA, so none of the PC's computing time is required after system start-up. The total data transfer rate to the PC is 32 outputs * 2 bytes/output * 200 updates/sec, or 12,800 bytes/sec.

The DMA transfer rate from the PC's memory to the analog output is the same, resulting in a total rate of 25,600 bytes/sec. Since a PC is capable of bursts of up to 400 kbytes/sec, clearly this system uses very little of the PC's capacity.

The control algorithm for each channel must be run in the time between analog sample's (within 78 usec), this leaves 73 usec available to process each channel.

With a typical TMS320C25 processor instruction requiring 286 nsec in a system, roughly 250 instructions are allowed for each of the 32 algorithms. The Texas Instruments TMS320 user's guide gives a simple example of a PID loop, roughly equivalent to the task at hand, which requires 11 instructions running in approximately 5,3 usec.

From these rough calculations it is clear there is plenty of time to execute a fairly complex control algorithm in real time for each channel.

Applications such as above are being satisfied today, but typically not with personal computers. These applications are being fulfilled with high powered VME and multibus systems, with very high cost and long development times.

With sophisticated data acquisition and control processors, many of these tasks now can be accomplished using low-cost personal computers. System integration and software development are greatly simplified, and the total system cost can be reduced to a fraction of its present level.

High Speed PC-based Data Acquisition Systems

Jeffrey R. Payne
Bradford A. Menz
et al.

Abstract -- **Currently a number of PC-based data acquisition development systems are commercially available to users. These systems read and write data in real-time from embedded control systems, and then store and display that data for use by the end user. However, many of these systems falter when pushed into the realm of high speed data acquisition, which in this paper is defined as less than 0.5 second sampling. They not only falter in this regard, but also fail to achieve many of the goals established herein for a robust, open system. This paper discusses goals and components for PC-based data acquisition systems which monitor high speed processes such as drive and tension control.**

I. Introduction

Until recently, within the last three years, high speed data acquisition systems which guaranteed data integrity could only be implemented on high end platforms such as VAX/VMS™ or UNIX™ systems. These provided sophisticated multitasking operating systems and enough horsepower to not only provide data collection of tens of thousands of I/O points, but also provide graphical interfaces to users. These systems were, and still are, expensive to buy and maintain.

Data collection on PCs has been, and continues to be, rather disappointing for users who demand high speed sampling, data integrity, and data storage. This has been due to a combination of the lack of CPU power, the lack of sophistication of PC operating systems, and the slow speed of peripheral devices such as disk drives. Therefore, many users are reluctant to leave their high end systems and look at what can be done on the PC platform.

However, the recent availability of powerful PC hardware and software has now made it possible for the PC platform to match the data acquisition performance of traditional high end systems. The following sections describe the design and implementation of such a system on the PC. The design of the system maximizes the use of the large PC application base which already exists, instead of reinventing existing functionality. The following sections are presented:

II. Goals: List of goals which a good PC-based high speed data acquisition and display system should achieve.

III. System description: Description of existing hardware and software products for the system which achieve the stated goals.

IV. Case study: Brief overview of an existing data acquisition system created using the stated system description.

V. Conclusion: Review of the issues discussed.

II. Goals

The first step in designing and implementing a flexible, high speed data acquisition system on the PC platform is to specify a set of goals which the system must achieve. This section list these goals, and also how most other PC systems fail to meet them. The failure of these existing systems to meet these goals is what separates them from the PC system being designed. The following goals are discussed:

A) Guaranteed high speed data acquisition
B) Minimized sample skew
C) High speed response
D) Data acquisition functionality
E) Low cost
F) Look and feel
G) Extensibility
H) Compatibility

A. Guaranteed High Speed Data Acquisition

High speed processes, such as variable speed drive control, and steel rolling, demand high speed data acquisition. Sample intervals of 20 milliseconds to 50 milliseconds are the goal of the system being discussed here. Also, to meet the data demands of modern production machinery, the system must be able to provide this sampling for up to 10,000 analog and digital values from the monitored system.

In addition, to provide reliable diagnostic and operator information, data collection at the stated interval must be guaranteed. Guaranteed sampling ensures that data samples are not missed because the system is busy doing some other task, such as updating an operator screen.

This is the most important goal to meet in the development of the data acquisition system. However, this is the one which most PC systems fail to meet. Without

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meeting this goal, most PC systems are useless in monitoring and diagnosing high speed processes. This is due to the following facts: inadequate "fast" sampling rates of 1 second or 0.5 second; data sampling cannot be guaranteed.

B. Minimized Sample Skew

Skew refers to drifting in time from the specified sampling interval. For example, reading a 20ms sample at 18ms since the last sample, or at 22ms since the last sample means that a 2ms skew has been introduced into the data collection. When skew approaches the sample interval, detecting cause and effect relationships using trended and exception data becomes impossible.

Not only must skew be minimized from sample to sample, but also within samples. For example, skew is introduced into a sample if the system interrupts its sampling to perform an operator task such as responding to a mouse click. Introducing skew within a sample makes the data collected in that sample questionable, and there is no way to tell that the skew was introduced.

Due to communication propagation delays and other latencies involved in data acquisition systems, it is impossible to eliminate skew. However, the components of the PC system should ensure that the data acquisition system does not further skew samples. The operating software of most PC systems often do further skew because of the environment under which it runs.

C. High Speed Response

In order to monitor high speed processes, the PC platform must be powerful enough to support the running software. This includes components such as the microprocessor, peripheral devices like the disk drive and video accelerator, and memory capacity. Powerful PC platforms have become available only within past several years. Also, the operating software must be sophisticated enough to take advantage of provided platform.

This goal must be met in order to provide a useful operator interface. Graphical elements on the screen should update fast enough to emulate analog display devices, such as bar graphs. If these graphical elements cannot update this quickly, problems in the monitored process can be masked.

All graphical elements on an operator screens must update a minimum of five times per second in order to provide accurate timely data about the monitored process. Trend screens must be able to scroll smoothly while displaying 20 to 30 samples per second. When leaving one operator screen, the next screen must be displayed with current data in two seconds or less.

Since most PC systems do not use robust operating software, operator interface performance can sometimes only be improved through additional hardware investments. This is also true in regard to inaccurate data acquisition.

D. Data Acquisition Functionality

The system must provide all expected data acquisition functionality, such as fault and alarm management, and trending. This functionality must be provided at the sampling rates being supported, and for suitable lengths of time, for example, storing trended data for several days.

Indeed, one of the goals of the system is to provide trending for up to 1,000 digital and analog values continuously and simultaneously. This allows operators and maintenance personnel to diagnose a problem without having to specify which values to trend beforehand.

In contrast, some PC systems only trend data when they are told to. This means that the person setting up the trend must know which values to trend before a problem occurs. If an important value is not setup beforehand, nothing can be done about it until the problem occurs again.

E. Low Cost

In order to provide a competitive product. the development costs must be low in order to keep the selling price as low as possible. Engineering costs for customizing the system for end users must also be kept low. In addition, hardware costs must be minimized while still providing enough computing power for the system.

Proprietary hardware and software must be minimized in order to meet these low cost goals. For example, development effort should not be put into a graphics editor if a superior off-the-shelf product is available, nor should a proprietary operating system be developed if a superior off-the-shelf product is available.

Most PC system providers, however, do develop a number of proprietary components in their systems. This not only increases the cost to the end user and the cost of engineering to the provider, but also makes the end user dependent on the provider for features and functionality. This locks the end user into the provider for the lifetime of the system, and requires specialized knowledge to work with the proprietary system.

Proprietary systems usually try to match functionality which already exists, and usually fail. For example, proprietary graphics editors, database managers, and even operating systems cannot match the features and installed base of commercially available, "off-the-shelf" products.

By using off-the-shelf, "open" products, add ons and improvements to the system can be made by end users at their discretion, independent of the provider. In addition, the end user is usually familiar with off-the-shelf products before the PC system is purchased. Thus, the end user is already familiar with the PC system, thereby reducing the learning curve and the costs associated with it.

F. Look and Feel

The PC system must provide a familiar "look and feel" to the end user's engineers and operators. For example, pushbuttons on the screen look like pushbuttons and behave like pushbuttons, i.e., they "depress" when clicked, and return to their original look when released.

Some PC systems, however, cannot provide this look and feel because, for example, they are designed to be "portable." A portable application can be developed on a Microsoft® Windows™ platform, and then moved to a UNIX platform without requiring any additional development (theoretically, of course). In order to provide this feature, however, look and feel is sacrificed since all platforms do this differently, and the system is thus designed to the lowest common denominator.

G. Extensibility

Extensibility means that the functionality of the PC system can be easily extended and enhanced. For example, if communication is required from the PC system to an external computer system in order to transfer data, then it must be possible to add that functionality to the basic PC system. Ideally, extensibility should be built into the system, and should allow the end user to make enhancements without assistance from the provider. The goals described in section IIE, Low Cost, must be met here as well.

Most PC systems are extensible. However, the PC system providers usually require that the end user purchase separately some kind of development toolkit. In addition, these toolkits usually require that a good deal of C language code be written to implement the desired functionality, which is difficult for the end user with a small engineering staff. Sometimes providers sell bundled functionality, such as a communication package, but this runs counter to the issues described in section IIE, Low Cost, in that it is a proprietary component.

H. Compatibility

The PC system must be compatible with other PC software products. This means that the development components and the data collection components of the system work with Microsoft Windows products. In addition, communication from the PC system to other systems support industry-standard protocols such as TCP/IP.

Meeting this goal also requires that the issues listed in section IIE, Low Cost, be addressed. Proprietary solutions to compatibility, especially in communications, must be avoided since these require a large engineering effort to develop and maintain.

III. System Description

This section describes the hardware and software components required to implement the PC data acquistion system. Each of these components is used in the PC system in order to address the issues listed in section II, Goals. The following PC system components are discussed:

A) Hardware
B) Operating systems
C) Graphical interface development package

A. Hardware

The hardware of the PC system is the foundation of high speed data acquisition and storage. The most sophisticated operating software cannot provide the required functionality if the hardware cannot run it fast enough. As mentioned previously, it is only in recent years that hardware powerful enough for this system has become available.

A very powerful PC platform can be put together today for less than $5,000. The base platform for the PC system being designed here is a desktop PC. All of the components listed below can be modified where desired; the following are the minimum requirements:

- Intel 80486/66MHz microprocessor
- 16Mb of RAM
- 540Mb IDE hard drive
- Video accelerator card with 1Mb of VRAM
- Industrial trackball
- 14" color VGA monitor

This PC platform addresses several of the goals presented in the previous section. These include:

- Section IIA, Guaranteed High Speed Data Acquisition
- Section IIC, High Speed Response
- Section IIE, Low Cost

B. Operating Systems

The operating system provides the environment in which all of the PC system software runs. It controls which competing software tasks can have access to the underlying hardware, including the CPU. It also controls when tasks can access the hardware. Different operating systems control access differently. In the PC environment, either "cooperative" multitasking or "preemptive" multitasking is provided.

1. Cooperative Multitasking

The most popular PC operating system, Microsoft Windows, control tasks' access to the hardware using cooperative multitasking. Windows cannot allow a task to run until the currently running task decides to give up its access to the hardware. For example, a data acquisition task

running in Windows cannot sample data when an operator is switching screens; screen switching is performed by a separate task. Since most PC systems are designed to run under Windows' cooperative multitasking, neither high speed sampling nor guaranteed data acquisition can be provided by these systems.

2. Preemptive Multitasking

Another PC operating system, Intel's® iRMX™, controls tasks' access to the hardware using preemptive multitasking. iRMX decides, based on a task's priority and whether or not it is ready to run, whether the currently running task should be preempted in order to run another task. For example, a data acquisition task with a high priority is run by iRMX whenever it is ready, based on sample interval; iRMX preempts any currently running, lower priority task in favor of the high priority one.

Preemptive multitasking ensures that a data acquisition task meets the specified sampling interval. In addition, it is run at exactly the sampling interval, thereby minimizing skew between samples. Once the data acquisition task is running, iRMX ensures that the task is not interrupted until it is finished. This minimizes skew within a sample.

In fact, because of the deterministic, preemptive operation provided by iRMX, it is the operating system used by the New York Stock Exchange. iRMX allows the Exchange to provide information to all traders simultaneously, thereby ensuring fairness and timeliness to all users. Also, iRMX is used in many banking ATM systems because of its features.

3. iRMX and DOS/Windows

iRMX allows Microsoft DOS™ to run as a task controlled by iRMX. This means that a PC running iRMX may also run DOS and Windows at the same time. DOS/Windows provides its cooperative multitasking for tasks it is running, while iRMX provides preemptive multitasking to all of the tasks it is running. This allows a user to run all DOS applications and Windows applications (in standard mode) without knowing that iRMX is really in control.

4. Conclusions for the PC System

The PC system being designed here should use the iRMX and DOS/Windows combination. The data acquisition, trending, fault and alarm management, and other critical tasks are written to run as iRMX tasks and take advantage of its preemptive multitasking. The graphical interface tasks are written under DOS/Windows to take advantage of the large application base, and the user's familiarity with its look and feel.

By using this combination of operating systems, a number of goals in the previous section have been addressed. These include:

- Section IIA, Guaranteed High Speed Data Acquisition
- Section IIB, Minimized Sample Skew
- Section IIC, High Speed Response
- Section IIE, Low Cost
- Section IIF, Look and Feel

C. Graphical Interface Development Package

After the data acquisition and data management issues have been addressed, the presentation of data to operators is the next issue. The graphical interface development package is the key to how this is done. Many PC system providers supply their own proprietary packages. However, with the recent introduction of Microsoft's Visual Basic™, these proprietary packages have become obsolete. The following sections highlight Visual Basic's usefulness as an operator interface development tool.

1. Visual Basic Introduction

Visual Basic is an inexpensive development tool which allows the user to easily create Windows-based graphical interface applications. Development is done using "drag-and-drop" graphical objects, and event-based programming. Event-based programming allows the developer to specify, for example, what the program should do when a user clicks a pushbutton, or selects an item from a list box.

The programming language is the powerful object-oriented Basic which Microsoft uses across all of its productivity tools, such as Access™, Excel™, and Word™. This is not a proprietary scripting language, which is typically provided on most PC platforms; it is a full featured, enhanced Basic. It is easy to learn without spending a great deal of money and time at a provider's training facility. In fact, Visual Basic is becoming a de facto standard for programming under Windows because of its ease of use.

Visual Basic provides industry standard extensibility already built in. Since it is a Microsoft product, it provides excellent compatibility with other Microsoft products and formats, such as Excel spreadsheets, Access and FoxPro™ databases, and OLE™ compliance. These items are discussed in the following sections.

2. Visual Basic Extensibility

A standard set of Windows graphical tools are provided with Visual Basic in order to create graphical screens. These include tools such as pushbuttons, radio buttons, list boxes, frames, and panels. If other kinds of tools are required, then they can be created by using Microsoft's VBX™ standard. This allows users to create tools which fit their application. For example, a user can buy or create a

VBX to provide a drag-and-drop graphical tool which shows current values read by the data acquisition portion of the PC system.

Visual Basic also allows a programmer to make calls to external Dynamic Link Libraries, or DLLs™. A DLL is a module which contains routines not defined in the Visual Basic application. For example, the programmer can call the Windows API DLLs to directly manipulate the Windows environment. The programmer can also write an application-specific DLL to implement functionality not possible through Visual Basic.

3. Visual Basic Compatibility

Visual Basic provides compatibility with all other Microsoft "suite" products right out of the box. For example, Visual Basic contains a data control tool which can read and write Access databases, FoxPro databases, Btrieve databases, and others. OLE compliance is not only built in, but is also complete. This allows data created through other OLE-compliant applications such as Excel and Word to be brought directly into a Visual Basic application without programming.

4. Conclusions for the PC System

By using Visual Basic, the PC system being designed provides an excellent graphical tool, which is also an inexpensive off-the-shelf package. Therefore, this eliminates the cost of development and maintenance of a proprietary package. Also, Visual Basic provides more functionality and ease of use than most of the proprietary packages supplied by other PC system providers.

By using Visual Basic, the following goals listed in the previous section have been addressed:

- Section IIE, Low Cost
- Section IIF, Look and Feel
- Section IIG, Extensibility
- Section IIH, Compatibility

IV. Case Study: SIGMA™

The authors of this paper have used the tools described in section III, System Description, to develop a PC-based high speed data acquisition system called SIGMA, which achieves many of the goals described in section section II, Goals. The SIGMA system is used to monitor and provide diagnostics for high speed drive applications. Refer to Fig. 1, SIGMA Trend Screen displaying 50ms data, which shows 50ms trend data being displayed on SIGMA's standard trend screen.

The SIGMA system has the following features:

- Guaranteed 30ms to 50ms sample intervals with minimal skew and guaranteed sampling for 10,000+ analog and digital values.
- Trending of 1,000+ analog and digital values from the monitored system continuously at the sample interval. Storage is limited only by disk space.
- Trending of one second samples, which are generated by averaging the high speed samples together. Storage is limited only by disk space.
- Standard alarm and fault management for 7,500+ digital values.
- Data are updated on screens between five and eight times per second based on screen complexity.
- Standard VGA screens running under Windows for displaying trended data and alarm fault data, which eliminates reengineering from system to system.
- Easy custom screen generation with a set of drag-and-drop graphical tools which interface directly with the data acquisition engine.

The SIGMA system consists of the following:

- PC hardware as described in section IIIA, Hardware.
- iRMX operating system running DOS/Windows and the data acquisition tasks preemptively.
- Visual Basic as the graphical interface development tool for standard and custom screens.

The amount of proprietary hardware and software used in the SIGMA system has been minimized as much as possible. The SIGMA system uses industry-standard operating systems, graphical development tools, and data representations, such as Excel spreadsheets and Access databases. However, proprietary software is used as follows:

- iRMX data acquisition tasks. It must be noted, however, that all data acquisition system providers implement proprietary data acquisition schemes.
- Visual Basic extensions through proprietary VBXs, which display collected data in a variety of text or graphical formats without requiring any user programming in Visual Basic. These VBXs were written solely for the convenience of the end user, but are not required to create data display screens.
- DLLs which provide fast access to all collected data; these move data from the iRMX environment to the DOS/Windows environment. DLL transfer is used instead of DDE™ transfers because it is at least an order of magnitude faster.

The design of the SIGMA system also involved specifying non-goals, i.e., those issues which would explicitly be left out of the design. The non-goals of the SIGMA system included:

- Portability: SIGMA was designed only as a PC system running under iRMX, and DOS/Windows.
- Universality: SIGMA was designed to communicate only with one major drive system manufacturer.

The SIGMA system succeeds in achieving many of the goals established herein. It has low development and engineering costs because of its use of off-the-shelf products, excellent data integrity because of the operating system and data acquisition tasks, high throughput between the monitored system and the PC, and the familiar look and feel of Windows.

V. Conclusion

The case study, the SIGMA system, shows that the PC system described in the preceding sections can be implemented, and can monitor and diagnose high speed processes. Furthermore, the system described in the preceding sections is unique in two aspects:

1. High speed, high integrity data acquisition, storage, and display on the PC platform formerly possible only on high end platforms, such as VAX/VMS or UNIX systems.
2. Reliance on low cost, off-the-shelf, industry-standard products to implement the system, rather than on high cost, proprietary products.

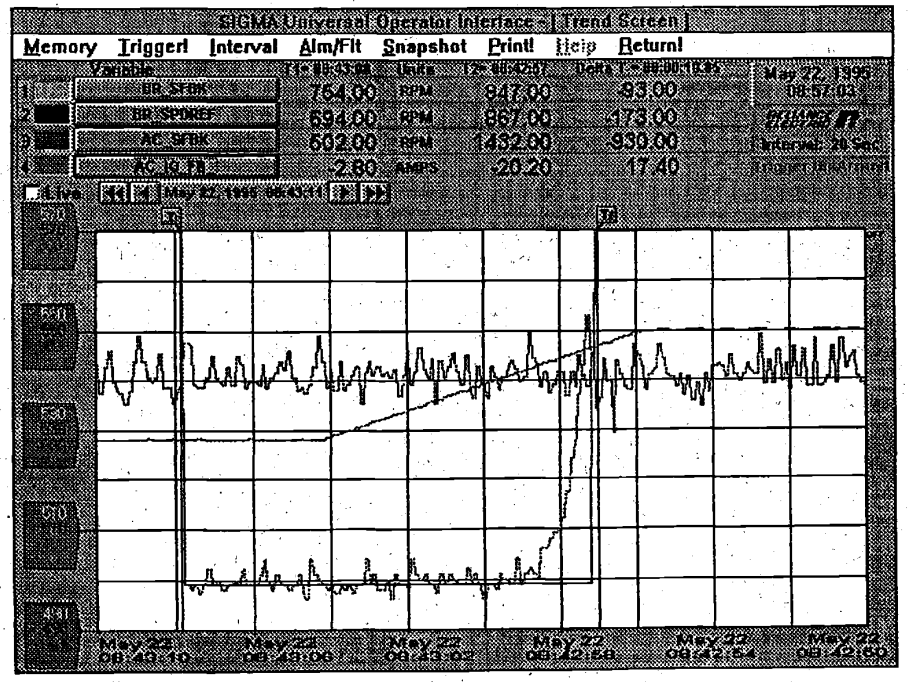

Fig. 1, SIGMA Trend Screen displaying 50ms data

09/331002

Practitioner's Docket No. . /101

PATENT

510 Rec'd PCT/PTO 14 JUN 1999

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

PCT/EP98/01187	03 March 1998 (3.03.98)	04 March 1997 (4.03.97)
International Application Number	**International Filing Date**	**International Earliest Priority Date**

TITLE OF INVENTION: FLEXIBLE INTERFACE
APPLICANT(S): Tasler, Michael

Attention: EO/US
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Assistant Commissioner for Patents
Washington, DC 20231

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Sheet 1 of 2

Complete if Known	
Application Number	Applied For
Filing Date	Herewith
First Named Inventor	Michael Tasler
Group Art Unit	Unknown
Examiner Name	Unknown
Attorney Docket Number	2055/101

510 Rec'd PCT/PTO 14 JUN 1999

U.S. PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	U.S. Patent Document Number	Kind Code[2] (if known)	Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
TT	1	5,291,611		Davis et al.	03/01/1994	
TT	2	5,444,644		August A. Divjak	08/22/1995	
TT	3	5,487,154		Keita Gunji	01/23/1996	
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Examiner Initials*	Cite No.[1]	Foreign Patent Document Office[3]	Number[4]	Kind Code[5] (if known)	Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T[6]
TT	5	EP	0 685 799 A1		Avery et al.	12/06/1995		

Examiner Signature	Thuan Du	Date Considered	12/06/01

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Sheet 2 of 2

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Application Number	Applied For
Filing Date	Herewtih
First Named Inventor	Michael Tasler
Group Art Unit	Unknown
Examiner Name	Unknown
Attorney Docket Number	2055/101

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TD	6	NATIONAL INSTRUMENTS CORPORATION, "Dynamic Signal Acquisition and DSP Board for the PC AT," IEEE 488 and VXIbus Control, Data Acquuisition, and Analysis, p. 3-118 - 3-123, (1994).	
TD	7	IBM CORPORATION, "Communication Method between Devices through FDD Interface," IBM Technical Disclosure Bulletin, Vol. 38 (No. 05), p. 245 (May, 1995).	

Examiner Signature	Thuan Du	Date Considered	12/06/01

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A. Documents cited in the national German examination proceedings

EP 0685799 A1

This reference discloses an interface by means of which several peripheral devices can be attached to a bus. An interface is connected between the bus of a host device and various peripheral devices. The interface comprises a finite state machine and several branches, each of which is assigned to a peripheral device. Each branch comprises a data manager, cycle control, user logic and a buffer. This interface device provides optimal matching between a host device and the specific peripheral device.

This reference is not pertinent to the present invention, since it does not disclose that the interface device is configured by the processor and the memory in such a way that the interface device, when receiving an inquiry from the host device as to the type of device attached to the multi-purpose interface of the host device, sends a signal, regardless of the type of the data transmit/receive device attached to the second connecting device of the interface device, to the host device, which signals to the host device that it is an input/output device customary in the host device, whereupon the host device communicates with the interface device by means of the driver for the input/output device customary in the host device. In contrast thereto, this reference provides an optimal matching between the host device and the specific peripheral device. This reference teaches awway from the present invention. The present invention provides a general purpose interface device which simulates a certain input/output device to a computer, respective of the actual peripheral device connected to the inventive interface device, wherein this reference teaches to provide an optimal adaption of the host processor to the specific interface actually connected to it.

"Communication method between devices through FDD interface"

The specialist publication IBM Technical Disclosure Bulletin, Volume 38, No. 5, page 245, "Communication method between devices through FDD interface" discloses an interface which connects a host device with peripheral devices via a floppy disk drive interface. The interface consists in particular of an address generator and MFM encoder/decoder, a serial/parallel adaptor and a format signal generator. The interface makes it possible to attach not only a floppy disk drive but also a further peripheral device to the FDT host controller of a host device. The host device assumes that a floppy disk drive is always attached to its floppy disk drive controller and communication is initiated if a corresponding address is correct.

This reference is not pertinent to the present invention, since it does not contain information as to how communication should be possible if the interface is connected to a multi-purpose interface instead of to a floppy disk drive controller. Additionally, this reference does not disclose any inquiries similar to the inquiry of the last feature of claim 1.

"IEEE 488 and VXIbus control, data acquistion and analysis", National Instruments, pages 3-118 to 3-123

This reference discloses a DSP board having a DMA controller, a memory, analog inputs and analog outputs. This reference, however, does not include any hint to the inventive configuration which is the subject of the present application.

B. Documents cited in the International examination proceedings

U. S. Patent No. 5,487,154

This reference discloses a digital signal processing system having a CPU which is connected to a digital signal processor (DSP), a memory, a DMA controller and a decoder, via an address

bus. The DSP, the memory and the DMA controller are connected to an external input/output device, which is, for example, an analog/digital converter. An input/output peripheral device is connected to the data bus. This peripheral device can be addressed by the CPU via the address decoder. Thus, this reference shows an interface device which turns on its analog/digital converter or bypasses its analog/digital converter, in dependence upon the timing of a connected analog/digital converter.

This reference, however, is not pertinent to the present invention, since it does not disclose an interface device that connects the host device and the data transmitter-receiver, the host device comprising drivers customary in the host device. Additionally, this reference does not disclose the inventive configuration which comprises the inquiry in the last paragraph of claim 1. When the inventive interface device receives an inquiry from the main CPU, it replies to this inquiry by stating that a certain input/output device is connected to itself. This reply, however, is independent on the device actually connected to the inventive interface device. By using this configuration, the host computer will communicate with the interface device and such, with the peripheral device connected to the interface device by using a driver which is optimally adjusted to the host computer, i.e. the main CPU.

U. S. Patent No. 5,510,775

This reference discloses a method of personalizing an electronic module and electronic circuit and module for implementing the method. In a vehicle in which the electric cable tree is replaced by a serial data transmission bus connecting electronic modules for controlling actuators or for acquiring signals from sensors, this method is used for personalizing these modules. In other words, these modules are provided with unique identities such that they can be addressed individually.

This reference is not pertinent to the present invention, since

it does not disclose an interface device for communication between a host device which comprises drivers for input/output devices customary in a host device and a multi-purpose interface. Additionally, this reference does not disclose the inventive configuration of the interface device as outlined above.

U. S. Patent No. 5,444,644

This reference discloses an auto-configured instrumentation interface. This interface, which is controlled by a microprocessor of a data acquiring system, allows an identification of the type of different input/output devices by means of a systematic analysis of analog characteristics of the input/output devices.

This reference is not pertinent to the present invention, since it discloses that the host computer must have detailed knowledge about the actual type of the peripheral device connected to the host computer. In contrast thereto, the inventive interface device tells the host device that it is connected with a certain input/output device customary for such a host device, while the type of the input/output device connected to the inventive interface device may be totally different.

U. S. Patent No. 5,291,611

This reference discloses a modular signal processing unit in which single chip digital signal processors can be combined parallely or serially.

This reference is not pertinent to the present invention, since it does not disclose the inventive configuration of the interface device.

Contents

Introduction

Section 1 Instrumentation Software Products

Section 2 GPIB Interface Products

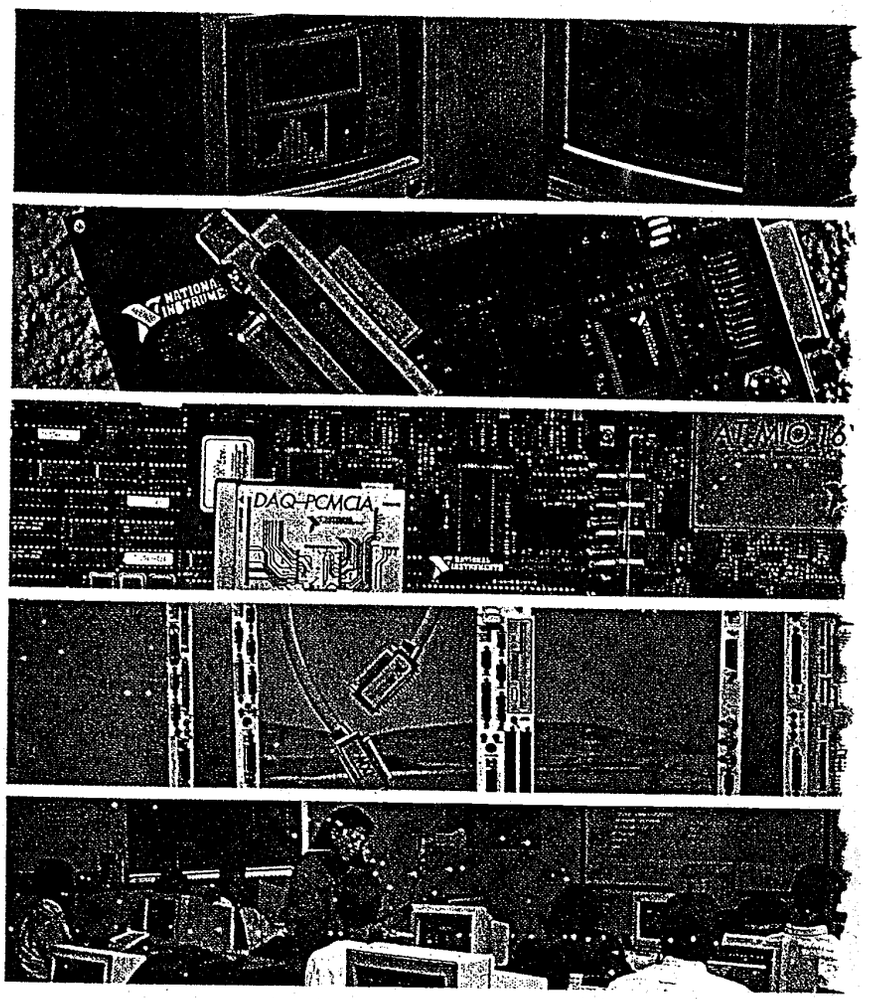
Section 3 Data Acquisition Products

Section 4 VXIbus and MXIbus Products

Section 5 Customer Education

Appendix

1994



IEEE 488 and VXIbus Control, Data Acquisition, and Analysis

NATIONAL INSTRUMENTS®
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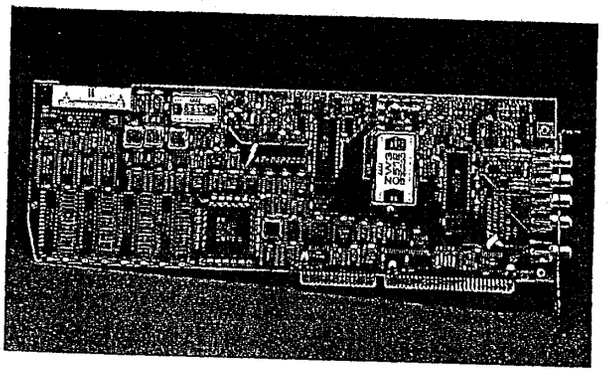
Dynamic Signal Acquisition and DSP Board for the PC AT

AT-DSP2200



AT-DSP2200

Features

- WE DSP32C single-chip digital signal processor
  - Operates at 50 MHz clock speed
  - 25 MFLOPS
  - 32-bit floating-point precision/24-bit integer precision
  - 12.5 MIPS
  - On-chip DMA for SIO and PIO to local memory
- Interrupt use
  - Interrupts from the AT-DSP2200 to the PC AT
  - Interrupts from the PC AT to the WE DSP32C
- Memory options for 64, 128, 256, or 384 kwords available
- High-accuracy analog inputs (2)
  - 2 analog 16-bit resolution delta-sigma ADCs with simultaneous sampling
  - Linear-phase antialiasing filters
  - 90 dB SNR for low-noise signal acquisition
  - 95 dB THD for high accuracy
  - ±2828 V input range (2 Vrms)
  - Software-programmable AC/DC coupling
- Precision analog outputs
  - 2 analog output channels with simultaneous conversions
  - 16-bit resolution, 8-times oversampling filters, 64-times oversampling delta-sigma modulating DACs
  - Linear-phase anti-imaging filters for precise signal generation
  - 90 dB THD for high accuracy

Software Included

- SpectrumWare
- NI-DAQ for DOS
- NI-DAQ for Windows
- NI-DSP for DOS/LabWindows/LabVIEW

RELATED PRODUCTS

Hardware 3-118

Software T-73, T-83, T-50, T-64, T-73

Overview

The AT-DSP2200 is a high-performance digital signal processing (DSP) board with high-accuracy audio bandwidth analog input/output for the PC AT. The AT-DSP2200 gives the PC a dedicated high-speed floating point computation engine that can perform scientific calculations faster than the general-purpose 80x86 microprocessor on the PC. At the heart of the AT-DSP2200 is the AT&T WE DSP32C chip.

Additionally, there are two channels of 16-bit analog input with 64-times oversampling delta-sigma modulating analog-to-digital converters (ADCs) and antialiasing filters. A 90 dB signal-to-noise ratio (SNR), -95 dB total harmonic distortion (THD), and ± 0.025 dB amplitude flatness make it possible to acquire signals with extremely high accuracy without introducing noise.

The board also has two channels of 16-bit analog output with 8-times oversampling filters and 64-times oversampling delta-sigma modulating DACs. Analog output filters smooth the waveform to remove unwanted higher frequency images.

On-chip DMA from the analog serial input to local memory and from local memory to the analog serial output, along with on-chip DMA from the PC interface to local memory make data management very efficient.

Applications

The AT-DSP2200 provides the computational power so that many test and measurement applications can operate in real time. You can use the AT-DSP2200 for analysis of audio bandwidth signals (DC to 22 kHz) or in numerically intensive applications. You can use high-speed data acquisition combined with the simultaneous digital signal analysis capabilities of the AT-DSP2200 in real-time applications such as Fourier analysis, spectral analysis, digital filtering, waveform analysis, and statistical analysis. The AT-DSP2200 computational power also makes it appropriate for process control applications requiring complex controller algorithms.

The ultra-fast numeric computational power of the AT-DSP2200 makes it ideal for vector multiply and add applications. The AT-DSP2200 has unique versatility and real-time performance capabilities, which you can use in the following applications:

- General-purpose DSP
- Vibration and machine test
- Instrumentation and spectral analysis
- Voice and speech analysis
- Acoustics
- Analog telephony
- Medical research
- Sonar
- Distortion measurements

In addition, the high-resolution audio frequency A/D and D/A is used for digitizing and synthesizing signals with

Dynamic Signal Acquisition and DSP Board for the PC AT

22 kHz bandwidth or less. The antialiasing filters on the input and the anti-imaging filters on the output ensure that signals are acquired and reproduced with extremely high fidelity. Applications include audio signal processing and analysis, audio workstations, audio and music synthesis, acoustics and speech research, and sonar and audio frequency test and measurement.

Hardware

Single Chip DSP Processor – The processor on the AT-DSP2200 is the AT&T WE DSP32C, which has the following features:

- Four-stage instruction pipeline with conflicts managed transparently to the user
- 80 ns single-cycle instruction and execution time for 12.5 MIPS
- Parallel multiplier and ALU instructions in a single cycle for 25 MFLOPS
- Up to 384 Kwords (1 word is 32 bits) of local, zero wait-state memory
- 1.5 Kwords of on-chip RAM
- Memory can be addressed as 8, 16, or 32 bits
- 32-bit instruction and data words, 24-bit addresses
- Four 40-bit floating point accumulators
- IEEE standard 32-bit floating-point operations
- 16 and 24-bit integer operations
- 25 Mbits/s serial I/O ports with DMA or interrupt options capable of servicing an AT-A2150 or AT-MIO-16X
- 16-bit parallel I/O port with DMA or interrupt options
- Two and three-operand instructions
- Zero-overhead looping
- Internal and external interrupts
- Low-power CMOS technology

The WE DSP32C is a floating-point digital signal processor. Floating-point applications are simpler to develop, and they also execute faster on floating-point digital signal processors than on fixed-point processors because numbers do not need to be continually scaled during multi-stage calculations.

DMA Controller – The on-chip DMA controller is capable of transferring data from the serial input to local or on-chip memory, from local or on-chip memory to the serial output, and to or from local or on-chip memory from or to the parallel I/O port.

Memory – The WE DSP32C has 1.5 Kwords of on-chip memory. In addition, the AT-DSP2200 has 64, 128, 256, or 384 Kwords of local, zero-wait-state memory. Only the 128 and 256 Kwords versions can be upgraded to larger memory configurations.

Board	Sampling Rates
AT-DSP2200	4, 5.5125, 6, 6.4, 8, 11.025, 12, 12.8, 16, 22.05, 24, 25.6, 32, 44.1, 48, and 51.2 kS/s

Analog Inputs – The AT-DSP2200 has two channels of 16-bit resolution analog input. The channels are simultaneously sampled at various software-programmable rates, including divisions of 32.0, 44.1, 48.0, and 51.2 kS/s (44.1 kS/s is the standard for compact disk (CD) players, 32.0 and

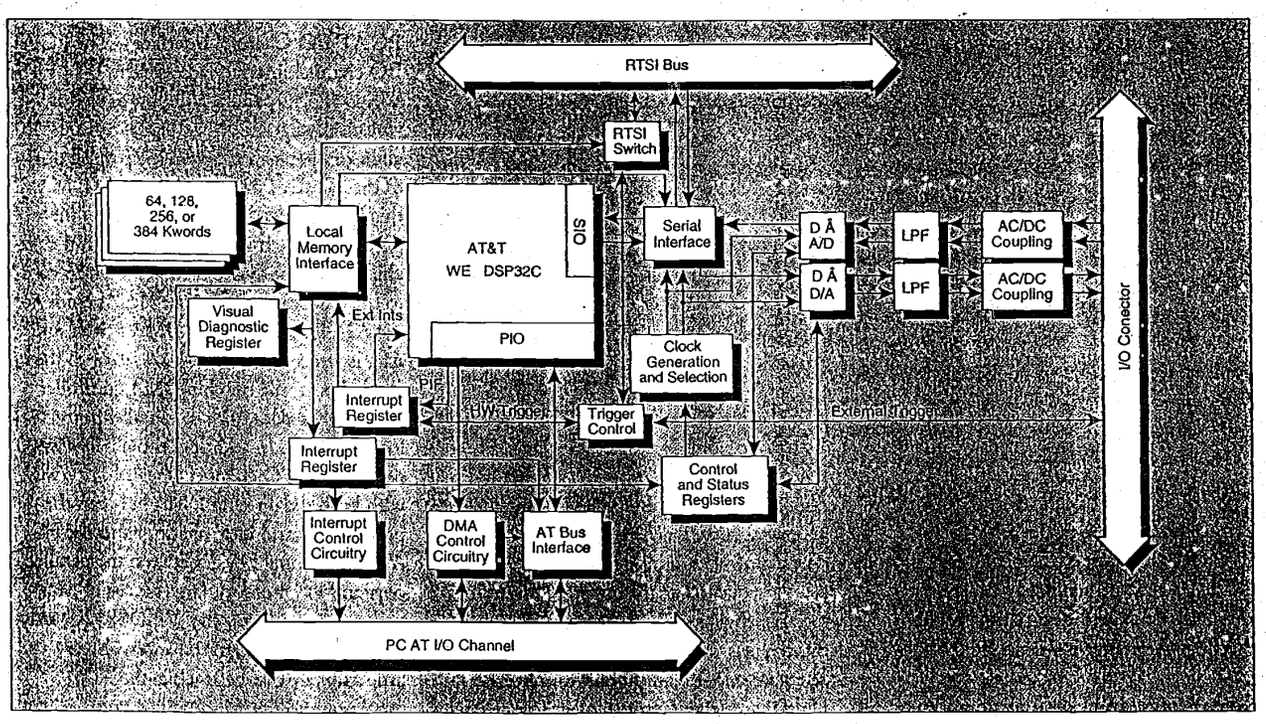


Figure 1. AT-DSP2200 Block Diagram

Dynamic Sign... Acquisition and DSP Board for the PC AT

Interrupts – The AT-DSP2200 and the PC can communicate with each other by sending interrupts. The AT-DSP2200 can interrupt the PC by asserting an interrupt request line on the PC AT I/O channel. Similarly, the PC can interrupt the WE DSP32C by writing to the interrupt register of the chip's parallel interface. The data sent during this write can be information for the WE DSP32C to use during its interrupt service routine.

RTSI Bus – The RTSI bus is a ribbon-cable bus that interconnects along the top of the AT Series boards. The bus uses a RTSI switch custom gate array to route timing signals, trigger signals, interrupt signals, and serial digital data to and from the RTSI bus. Several DAQ and DSP boards can then use RTSI to synchronize analog-to-digital (D/A) conversions, digital inputs, digital outputs, and counter/timer operations between multiple boards. In addition, the RTSIbus can send interrupts directly to the AT-DSP2200 from other AT-DSP2200 boards or AT Series DAQ boards.

Software

National Instruments has developed several software packages to control data acquisition functions on PC-based DAQ boards. The following software is included with the AT-DSP2200:

- SpectrumWare
- NI-DAQ for DOS
- NI-DAQ for Windows
- NI-DAQ for Windows NT
- NI-DSP for DOS/LabWindows

The following software is available separately:

- LabWindows for DOS
- LabWindows/CVI
- LabVIEW for Windows
- LabVIEW for Windows NT

Developer Toolkit – includes an AT&T C compiler, assembler, linker, debugger, and documentation. With these tools, a developer can program the AT-DSP2200 directly, using its flexibility to custom tailor a PC AT DSP system to his or her application.

Specifications

Typical at 25 °C unless otherwise noted. Refer to the Data Acquisition Overview, page 2-2, for typical frequency response plots.

Analog Input

Input Characteristics

Number of channels	2 single-ended, simultaneously sampled
Type of ADC	Delta-sigma
Resolution	16 bits, 1 in 65,536
Sampling rates	4.0, 5.5125, 6.0, 6.4, 8.0, 11.025, 12.0, 12.8, 16.0, 22.05, 24.0, 25.6, 32.0, 44.1, 48.0, and 51.2 kS/s
Input ranges	±2.828 V (2 Vrms)
Input coupling	AC or DC, software-selectable
Overvoltage protection	±20 V powered on or off
Input impedance	ACH0–ACH1
Data transfers	DMA, interrupts, programmed I/O

Transfer Characteristics

Offset error after calibration	±5 LSB typical, ±15 LSB max
Gain adjustment range	±5.5% (±0.3 dB)

Amplifier Characteristics

Input impedance	450 kΩ in parallel with 68 pF

Dynamic Characteristics

Bandwidth (–3 dB)	DC to 0.45 times sampling rate, DC coupled 8.8 Hz to 0.45 times sampling rate, AC coupled
System noise (including quantization error)	±0.5 LSB rms
Dynamic range	92 dB
Signal-to-THD plus noise	90 dB for 0 dB input, DC to 22 kHz
THD	–95 dB for 0 dB input, DC to 22 kHz
Amplitude flatness	±0.01 dB typical, ±0.025 dB max, DC to 20 kHz
Phase linearity	±0.5°, DC to 20 kHz
Interchannel phase	±1°, DC to 20 kHz
IMD	
SMPTE (60 Hz, 7 kHz)	–85 dB
DIN (250 Hz, 8 kHz)	–85 dB
CCIF (14 kHz, 15 kHz)	–95 dB
Crosstalk	–85 dB, DC to 20 kHz

Filters

Type	Analog and digital antialiasing
Passband ripple	±0.01 dB pk-pk, DC to 20 kHz
Stopband attenuation	86 dB
Attenuation rate	90 dB in 1/6 of an octave
Signal delay	35.6 sample periods

Analog Output

Output Characteristics

Number of channels	2 single-ended, simultaneously updated
Resolution	16 bits, 1 in 65,536
Update rates	4.0, 5.5125, 6.0, 6.4, 8.0, 11.025, 12.0, 12.8, 16.0, 22.05, 24.0, 25.6, 32.0, 44.1, 48.0, and 51.2 kS/s
Type of DAC	Delta-sigma
Data transfers	DMA, interrupts, programmed I/O

Transfer Characteristics

Offset error after calibration	13 mV max
Gain adjustment range	16% (±0.5 dB)

Voltage Output

Ranges	±2.828 V (2 Vrms)
Output coupling	AC or DC, jumper selectable
Output impedance	1 Ω
Recommended load impedance	10 kΩ or greater
Crosstalk	–85 dB
Dynamic range	92 dB, DC to 20 kHz (48 kS/s conversion rate)
Amplitude flatness	±0.05 dB, DC to 20 kHz (48 kS/s conversion rate)

Dynamic Signal Acquisition and DSP Board for the PC AT

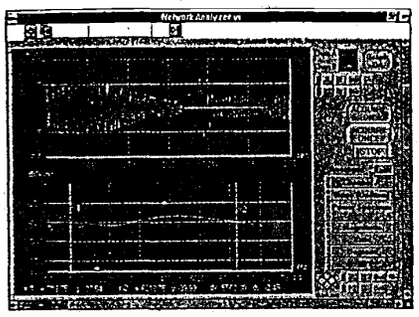


Figure 2. SpectrumWare delivered with the AT-DSP2200 acquires and analyzes dynamic signals.

48.0 kS/s are standard rates used in digital audio tape (DAT) recorders, and 51.2 kS/s is a standard frequency for use with Fourier analysis). The analog input has software-programmable AC/DC coupling and can digitize signals within a voltage range of ±2.828 V (2 Vrms). To prevent damage to the board, the input circuitry also has over-voltage protection for inputs up to ±20 V.

Antialiasing – the AT-DSP2200 has both analog and real-time digital filters implemented in hardware to prevent aliasing. Input signals are first filtered with analog filters to remove any signals with frequency components beyond the range of the AT-DSP2200. Then, digital antialiasing filters automatically adjust their cutoff frequency to remove any frequency components above one-half the programmed sampling rate. Because of this advanced analog input design, you do not have to add any filters to prevent aliasing.

The analog input stage acquires signals with extremely low noise and low distortion. The board has a 93 dB dynamic range that makes it possible to acquire waveforms without any significant noise error. Because the board has a THD of only -95 dB, the digitized signals are a true representation of the analog signal applied to the input of the board. Signals from DC to 22 kHz are acquired with accurate amplitude because the amplitude flatness in this frequency range is within ±0.025 dB.

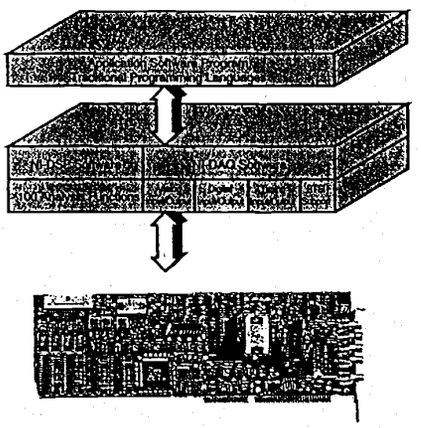
The low noise and low distortion of the AT-DSP2200 are achieved by using state-of-the-art 64-times oversampling, delta-sigma modulating ADCs. These ADCs sample at 64 times the specified sampling rate with 1-bit resolution. A noise-shaping technique then shifts quantization noise to higher frequencies. Extremely flat, linear-phase, lowpass digital filters then remove this noise, divide the sample rate by 64, and increase the resolution to 16 bits. Using the delta-sigma modulating ADCs, the AT-DSP2200 is immune to differential nonlinearity (DNL) distortion associated with conventional DAQ boards.

The offset voltage of the analog input is self-calibrated by software to within ±5 least significant bits (LSBs). The gain accuracy is calibrated to within ±0.01 dB by adjusting onboard trimpots. A precision voltage reference ensures that the input gain is stable and accurate.

Board	Update Rates
AT-DSP2200	4, 5.5125, 6, 6.4, 8, 11.025, 12, 12.8, 16, 22.05, 24, 25.6, 32, 44.1, 48, and 51.2 kS/s

Analog Outputs – The AT-DSP2200 has two channels of 16-bit resolution analog output. The channels are simultaneously updated at various software programmable rates including divisions of 32.0, 44.1, 48.0, and 51.2 kS/s. The analog output circuitry uses 8-times oversampling filters with 64-times oversampling delta-sigma modulators to generate high-quality signals. The board has jumper-selectable AC/DC coupling and can generate signals within a range of ±2.828 V (2 Vrms).

Antialiasing Filters – The AT-DSP2200 has both analog and digital anti-imaging filters. These filters remove unwanted glitches and high-frequency signals that are generated when an analog signal is generated from digital data. The digital filters limit the bandwidth of the output signal to half the original conversion rate, thereby rejecting images caused by the 8-times oversampling process. The analog filters are smooth, third-order, linear-phase filters that reject unwanted images created by the digital-to-analog converter.

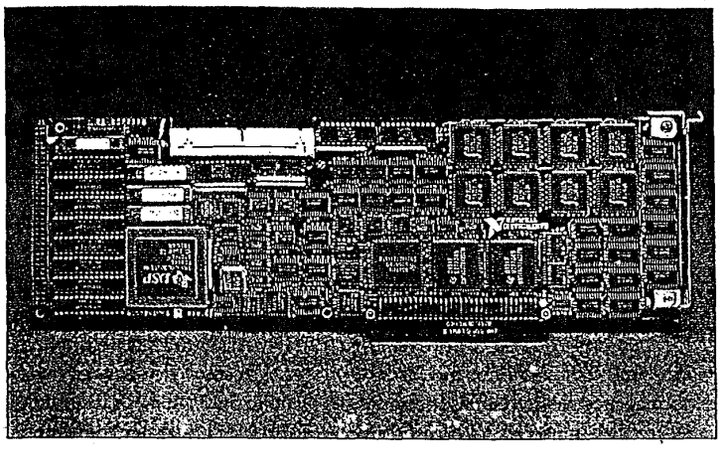


The signals generated by the analog output circuitry are low-distortion, low-noise, frequency-flat analog signals. The dynamic range is 92 dB and intermodulation distortion (IMD) is -90 dB. The analog output circuitry has a gain adjustment range of ±0.5 dB and offset accuracy within ±3 mV.

PC AT I/O Channel Interface – The PC AT I/O channel interface accesses the WE DSP32C parallel I/O port as well as various configuration and status registers. In addition, you can program the parallel port of the WE DSP32C to use on-chip DMA. If this DMA is used and data is read by the AT's processor from the parallel port, the on-chip DMA controller transfers the next data to the parallel port from the local memory of the AT-DSP2200. If this DMA is used and data is written by the AT's processor to the parallel port, the on-chip DMA controller transfers the data from the parallel port to local memory. In addition, the AT-DSP2200 uses PC AT I/O channel DMA. In this way, with both the on-chip DMA between the parallel port and local memory and the PC AT I/O channel DMA between the parallel port and PC memory, large blocks of data, such as programs for the WE DSP32C, may be sent in the background and with very little software overhead while the AT's processor and the WE DSP32C are performing other tasks.

DSP Boards for the Macintosh NuBus

NB-DSP2300 / NB-DSP2305



NB-DSP2305

Overview

The NB-DSP2300 and NB-DSP2305 are high-performance, digital signal processing (DSP) floating point accelerator boards for Macintosh NuBus computers; the NB-DSP2305 is the newer version. The boards are dedicated, high-speed, computation engines that perform scientific calculations much faster than the general-purpose 680X0 Macintosh microprocessor. The Texas Instruments (TI) TMS320C30 DSP chip gives the DSP boards their computational power. The NB-DSP2305 design is optimized so that the TMS320C30 chip operates at its maximum performance, delivering 40 MFLOPS. The NB-DSP2300 is also a lower cost board, using a slower version of the TMS320C30 to deliver 33.33 MFLOPS. A custom dual-DMA controller architecture on the DSP boards transfers data without requiring processor time. One DMA controller transfers data across the NuBus using block mode. Because the NB-DSP2305 is a full NuBus master, the DMA controller and the TMS320C30 chip can directly access NuBus address space, including the Macintosh main memory, or other NuBus boards. The NB-DSP2305 can therefore substantially accelerate system performance, because it can acquire and process data in parallel with the Macintosh processor at speeds far surpassing the Macintosh itself.

Applications

Because the DSP boards increase the floating point computational bandwidth of the Macintosh, many test and measurement applications can now run at the speeds required for real-time analysis. You can use the DSP boards for analysis with any of the NB Series data acquisition (DAQ) boards or any other NuBus hardware. High-speed data acquisition combined with the simultaneous digital signal analysis capabilities of the DSP boards are useful for such real-time applications as Fourier analysis, spectral analysis, digital filtering, waveform analysis, and statistical analysis. The computational power of the DSP board also makes it appropriate for process control applications requiring complex controller algorithms.

Hardware

Figure 1 illustrates the NB-DSP2300 and NB-DSP2305 hardware. The following paragraphs describe the major functions of the hardware.

Single-Chip DSP Processor – The DSP board processor is the TI TMS320C30, which has the following features.

– 1.0 micron CMOS technology
– Four-stage instruction pipeline with conflicts managed transparently to the programmer

Features

- TMS320C30 single-chip digital signal processor
  - NB-DSP2305 delivers 40 MFLOPS at 20 MIPS
  - NB-DSP2300 delivers 33.33 MFLOPS at 16.66 MIPS
  - 32-bit floating point precision/32-bit integer precision
  - TMS320C30 DMA controller transfers with sustained data rates up to 40 Mbytes/s with NB-DSP2305 and 33.33 Mbytes/s with NB-DSP2300
- Dual-ported memory
  - 4 Kwords (1 word = 32 bits) of zero-wait-state memory
- Dual-access memory
  - 64 Kwords of zero-wait-state memory
  - Expandable to 1088 Kwords of zero-wait-state memory
- RTSI bus for high-speed signal links
- Full NuBus master capability
- Hardware floating point circuitry translates between TMS320C30 format and Macintosh IEEE 754 format
- High-level analysis software for LabVIEW and C language
- Optional development software including TMS320C30 C compiler, assembler/linker, debugger, and code loader

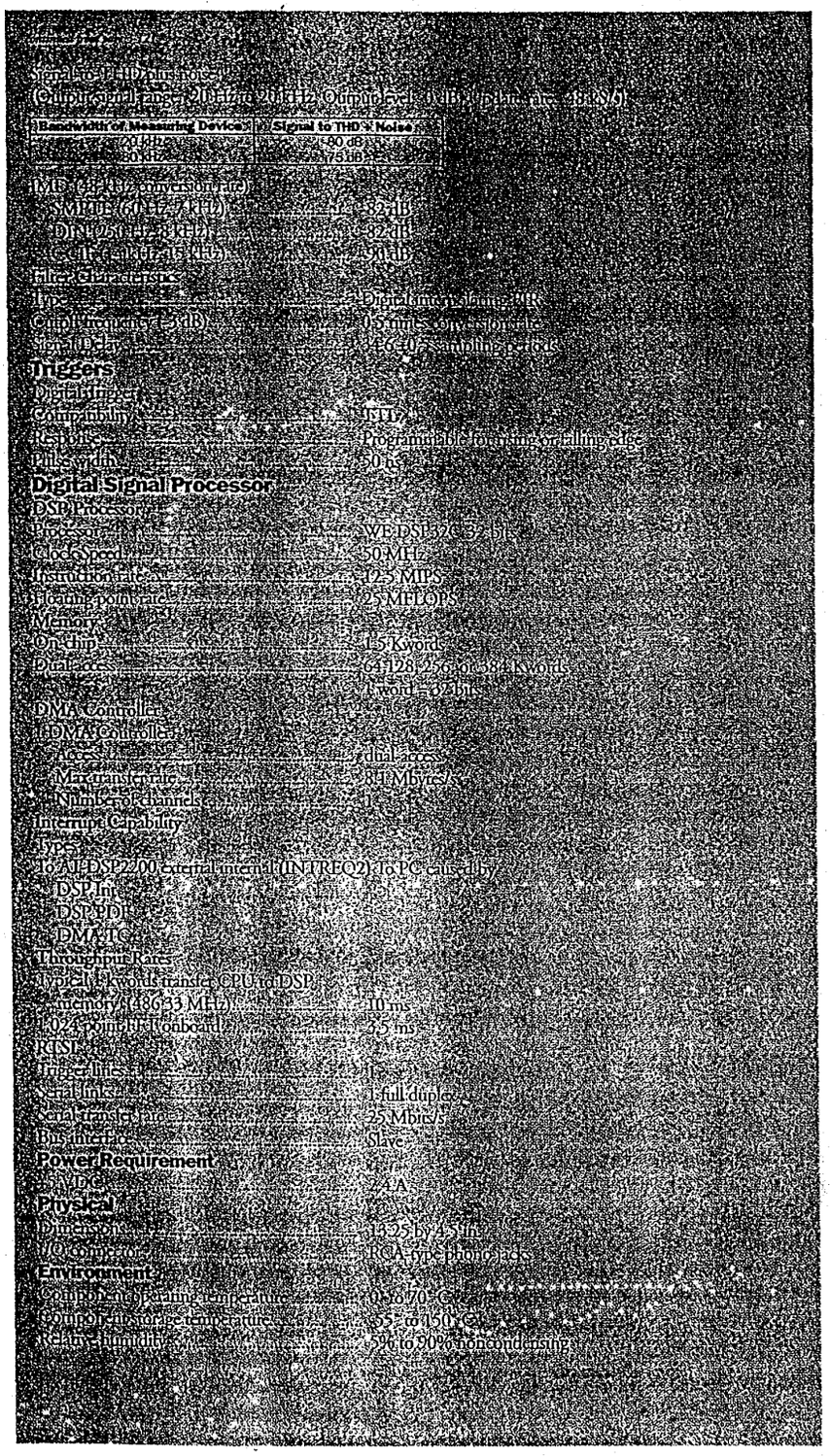
Software Included

- DSP Debug
- NI-DSP for Macintosh
- NI-DSP Interface Utilities

RELATED PRODUCTS

Hardware 3-65 THROUGH 3-101
Software 3-71 THROUGH 3-73
Accessories 3-85

Dynamic Sig[illegible]l Acquisition and DSP Board for the PC AT



The C compiler optimizes WE DSP32C code and generates assembly language c that can be assembled and linked into a time module. When a run-time module completed, use the download tools and debugger to load, debug, and execute th code, set parameters, and fetch results.

Part Numbers

AT-DSP2200 and software* with 64 Kw of memory.....776597-
AT-DSP2200 and software* with 128 Kwords of memory.....776597
AT-DSP2200 and software* with 256 Kwords of memory.....77659
AT-DSP2200 and software* with 384 Kwords of memory.....776597
AT Series RTSI bus cables for
2 boards.....77624
3 boards.....77624
4 boards.....776249-
5 boards.....776249-
Type RCA1 single cable
3 ft.....181341-
6 ft.....181341-
Type RCA2 dual cable
3 ft.....181342
6 ft.....181342-

** Includes plug-in board, SpectrumWare, NI-DSP for DOS, NI-DAQ for DOS a Windows software on both 5.25 in. DS/I and 3.5 in. 1.44 MB diskettes.*

Only the 128 and 256 Kwords versions c be upgraded to larger memory configurat

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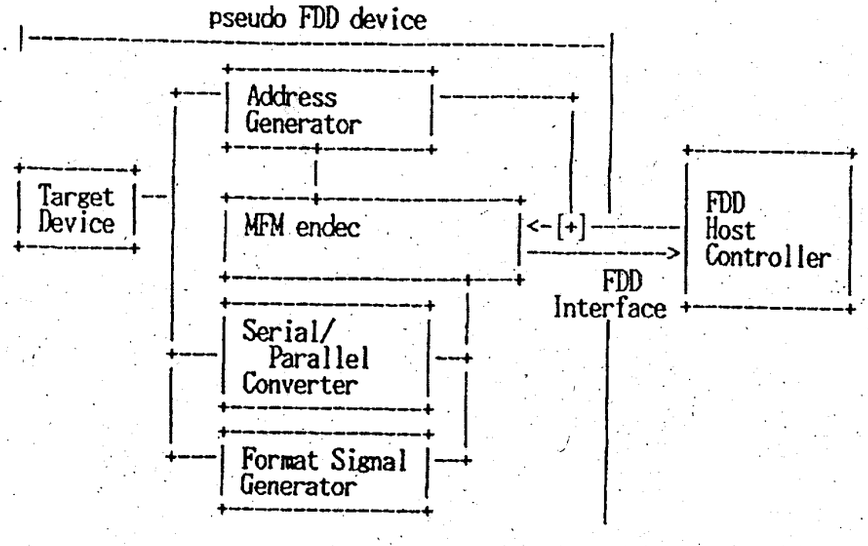
Communication Method between Devices through FDD Interface



Disclosed is a method for communicating between devices through Floppy Disk Drive (FDD) Interface which can be implemented via serial data lines, such as Write Data and Read Data. The FDD Host Controller compares a requested address and a address from the FDD in Read/Write operation. Only when the addresses are matched, the FDD Host Controller reads data on the data frame preceded by the address or writes data there. In the communication method through the FDD Interface, the sector data from the FDD, such as ID and DATA field information, are handled as packet data; ID field as packet header and data field as packet data. The packet header has the packet attributes to indicate data type in the packet data. The Figure shows the block diagram of the subject method.

- Address Generator generates the address information compatible with FDD ID information. It indicates packet attribute; Command Packet, Status Packet, Device Information Packet and Data Packet.
- MFM endec decodes and encodes MFM data on Read/Write data line.
- Format Signal Generator generates FDD compatible format pattern such as Synch-pattern.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
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Washington, D.C. 20231
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/331,002	06/14/1999	MICHAEL TASLER	2055/101	1117

24283 7590 12/18/2001

PATTON BOGGS
PO BOX 270930
LOUISVILLE, CO 80027

EXAMINER
DU, THUAN N

ART UNIT	PAPER NUMBER
2182	7

DATE MAILED: 12/18/2001

Please find below and/or attached an Office communication concerning this application or proceeding.

PTO-90C (Rev. 07-01)

Office Action Summary	Application No.	Applicant(s)	
	09/331,002	TASLER, MICHAEL	
	Examiner	Art Unit	
	Thuan N. Du	2182	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 June 1999* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☒ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *5,6* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

1. Claims 1-16 are presented for examination.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claim 13 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

4. Claim 13 recites the limitation "the hard disk" in line 4. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's admission of prior art [AAPA] and McNeill, Jr. et al. (U.S. Patent No. 5,499,378).

7. Regarding claims 1, 5, 6, 12 and 13, AAPA teaches an interface for communication between a host device and a transmit/receive device comprising:

a processor [Application's specification, p. 3, line 8];

a memory [Application's specification, p. 3, line 9];

a first connecting device for interfacing the host device with the interface device via a multi-purpose interface of the host device [Application's specification, p. 3, lines 1-3];

a second connecting device for interfacing the interface device with the data transmit/receive device [Application's specification, p. 3, lines 9-12].

AAPA teaches the host device communicates with the interface device by means of an interface-specific driver installed in the host device. AAPA does not teaches the interface device receiving an inquiry from the host device as to type of device is attached and responding to the host that it is an I/O device customary in a host device, whereupon the host device communicates with the interface device by means of the driver for the I/O device customary in a host device.

McNeill, Jr. et al. teaches an interface device responds to the host inquiry command as to the type of device attached to the multi-purpose interface (SCSI interface) of the host device [col. 2, lines 39-44; col. 5, lines 14-15 and 23-31], whereupon the host device communicates with the interface device by means of the driver for the I/O device customary in a host device [col. 3, lines 23-30; col. 5, lines 59-64].

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of AAPA and McNeill, Jr. et al. because it would enhance the system by allowing the host device communicates with a transmit/receive device, through an interface device, by means of the standard driver in the host device instead of installing a device-specific driver into the host device.

8. Regarding claims 2, 7-11, McNeill, Jr. et al. teaches the device drivers for I/O drivers customary in a host device comprise a hard disk driver, and the signal indicates to the host device that the host device is communicating with a hard disk [col. 5, lines 33-39].

9. Regarding claim 3, McNeill, Jr. et al. teaches the system including a buffer for buffering data to be transferred between two systems [col. 5, lines 52-54].

10. Regarding claims 4 and 14, McNeill, Jr. et al. teaches the communication is between a host and a SCSI device (SCSI target computer) [abstract]. Therefore, the host and the device must have SCSI interfaces.

11. Regarding claims 15 and 16, since they recite method of operating of the apparatus defined in the apparatus claims, they are rejected accordingly based on the rejection of the apparatus claims.

Conclusion

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thuan N. Du whose telephone number is (703) 308-6292 or via e-mail, **thuan.du@uspto.gov**. The examiner can normally be reached on Monday-Friday: 9:00 AM - 5:30 PM, EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thomas C. Lee can be reached on (703) 305-9717.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks
Washington, D.C. 20231.

The fax numbers for the organization where this application or proceeding is assigned are as follow:

- (703) 746-7238 [After Final Communication]
- (703) 746-7239 [Official Communication]
- (703) 746-7240 [Non-Official Communication]

and/or:

(703) 746-5668 (use this fax number, only after approval by Examiner, for "INFORMAL" or "DRAFT" communication).

Hand-delivered responses should be brought to:

Crystal Park II
2121 Crystal Drive
Arlington, VA 22202
Fourth Floor (Receptionist).

THOMAS LEE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100

Thuan N. Du
December 7, 2001

Attachment for PTO-948 (Rev. 03/01, or earlier)
6/18/01

The below text replaces the pre-printed text under the heading, "Information on How to Effect Drawing Changes," on the back of the PTO-948 (Rev. 03/01, or earlier) form.

INFORMATION ON HOW TO EFFECT DRAWING CHANGES

1. Correction of Informalities -- 37 CFR 1.85

New corrected drawings must be filed with the changes incorporated therein Identifying indicia, if provided, should include the title of the invention, inventor's name, and application number, or docket number (if any) if an application number has not been assigned to the application. If this information is provided, it must be placed on the front of each sheet and centered within the top margin. If corrected drawings are required in a Notice of Allowability (PTOL-37), the new drawings **MUST** be filed within the **THREE MONTH** shortened statutory period set for reply in the Notice of Allowability. Extensions of time may NOT be obtained under the provisions of 37 CFR 1.136(a) or (b) for filing the corrected drawings after the mailing of a Notice of Allowability. The drawings should be filed as a separate paper with a transmittal letter addressed to the Official Draftsperson.

2. Corrections other than Informalities Noted by Draftsperson on form PTO-948.

All changes to the drawings, other than informalities noted by the Draftsperson, **MUST** be made in the same manner as above except that, normally, a highlighted (preferably red ink) sketch of the changes to be incorporated into the new drawings **MUST** be approved by the examiner before the application will be allowed. No changes will be permitted to be made, other than correction of informalities, unless the examiner has approved the proposed changes.

Timing of Corrections

Applicant is required to submit the drawing corrections within the time period set in the attached Office communication. See 37 CFR 1.85(a).

Failure to take corrective action within the set period will result in ABANDONMENT of the application.

Form PTO 948 (Rev. 8-98) U.S. DEPARTMENT OF COMMERCE - Patent and Trademark Office Application No. 33/002

NOTICE OF DRAFTSPERSON'S PATENT DRAWING REVIEW

The drawing(s) filed (insert date) 9/4/99 are:

A. ☐ approved by the Draftsperson under 37 CFR 1.84 or 1.152.

B. ☒ objected to by the Draftsperson under 37 CFR 1.84 or 1.152 for the reasons indicated below. The Examiner will require submission of new, corrected drawings when necessary. Corrected drawing must be submitted according to the instructions on the back of this notice.

1. DRAWINGS. 37 CFR 1.84(a): Acceptable categories of drawings: Black ink. Color.
   - ____ Color drawings are not acceptable until petition is granted. Fig(s) ____
   - ____ Pencil and non black ink not permitted. Fig(s) ____
2. PHOTOGRAPHS. 37 CFR 1.84 (b)
   - ____ Four-tone set is required. Fig(s) ____
   - ____ Photographs not properly mounted (must be mounted on bristol board or photographic double-weight paper). Fig(s) ____
   - ____ Poor quality (half-tone). Fig(s) ____
3. TYPE OF PAPER. 37 CFR 1.84(e)
   - ____ Paper not flexible, strong, white, and durable. Fig(s) ____
   - ____ Erasures, alterations, overwritings, interlineations, folds, copy machine marks not accepted. Fig(s) ____
   - ____ Mylar, vellum paper is not acceptable (too thin). Fig(s) ____
4. SIZE OF PAPER. 37 CFR 1.84(f): Acceptable sizes:
   - ____ 21.0 cm by 29.7 cm (DIN size A4)
   - ____ 21.6 cm by 27.9 cm (8 1/2 x 11 inches)
   - ____ All drawing sheets not the same size. Sheet(s) ____
   - ____ Drawings sheets not an acceptable size. Fig(s) ____
5. MARGINS. 37 CFR 1.84(g): Acceptable margins:

   Top 2.5 cm Left 2.5cm Right 1.5 cm Bottom 1.0 cm
   SIZE: A4 Size

   Top 2.5 cm Left 2.5 cm Right 1.5 cm Bottom 1.0 cm
   SIZE: 8 1/2 x 11

   Margins not acceptable. Fig(s) ____
   - ____ Top (T) ☒ Left (L)
   - ____ Right (R) ____ Bottom (B)
6. VIEWS. 37 CFR 1.84(h)

   REMINDER: Specification may require revision to correspond to drawing changes.

   Partial views. 37 CFR 1.84(h)(2)
   - ____ Brackets needed to show figure as one entity. Fig(s) ____
   - ____ Views not labeled separately or properly. Fig(s) ____
   - ____ Enlarged view not labeled separately or properly. Fig(s) ____
7. SECTIONAL VIEWS. 37 CFR 1.84 (h)(3)
   - ____ Hatching not indicated for sectional portions of an object. Fig(s) ____
   - ____ Sectional designation should be noted with Arabic or Roman numbers. Fig(s) ____
8. ARRANGEMENT OF VIEWS. 37 CFR 1.84(i)
   - ____ Words do not appear on a horizontal, left-to-right fashion when page is either upright or turned so that the top becomes the right side, except for graphs. Fig(s) ____
9. SCALE. 37 CFR 1.84(k)
   - ____ Scale not large enough to show mechanism without crowding when drawing is reduced in size to two-thirds in reproduction. Fig(s) ____
10. CHARACTER OF LINES, NUMBERS, & LETTERS. 37 CFR 1.84(l)
    - ☒ Lines, numbers & letters not uniformly thick and well defined, clean, durable, and black (poor line quality). Fig(s) 1-2
11. SHADING. 37 CFR 1.84(m)
    - ____ Solid black areas pale. Fig(s) ____
    - ____ Solid black shading not permitted. Fig(s) ____
    - ____ Shade lines, pale, rough and blurred. Fig(s) ____
12. NUMBERS, LETTERS, & REFERENCE CHARACTERS. 37 CFR 1.84(p)
    - ____ Numbers and reference characters not plain and legible. Fig(s) ____
    - ____ Figure legends are poor. Fig(s) ____
    - ____ Numbers and reference characters not oriented in the same direction as the view. 37 CFR 1.84(p)(1) Fig(s) ____
    - ____ English alphabet not used. 37 CFR 1.84(p)(2) Fig(s) ____
    - ____ Numbers, letters and reference characters must be at least .32 cm (1/8 inch) in height. 37 CFR 1.84(p)(3) Fig(s) ____
13. LEAD LINES. 37 CFR 1.84(q)
    - ____ Lead lines cross each other. Fig(s) ____
    - ____ Lead lines missing. Fig(s) ____
14. NUMBERING OF SHEETS OF DRAWINGS. 37 CFR 1.84(t)
    - ____ Sheets not numbered consecutively, and in Arabic numerals beginning with number 1. Sheet(s) ____
15. NUMBERING OF VIEWS. 37 CFR 1.84(u)
    - ____ Views not numbered consecutively, and in Arabic numerals, beginning with number 1. Fig(s) ____
16. CORRECTIONS. 37 CFR 1.84(w)
    - ____ Corrections not made from prior PTO-948 dated ____
17. DESIGN DRAWINGS. 37 CFR 1.152
    - ____ Surface shading shown not appropriate. Fig(s) ____
    - ____ Solid black shading not used for color contrast. Fig(s) ____

COMMENTS

REVIEWER _____ DATE 9/12/99 TELEPHONE NO. 703 305 0891

ATTACHMENT TO PAPER NO. 7

Notice of References Cited	Application/Control No. 09/331,002	Applicant(s)/Patent Under Reexamination TASLER, MICHAEL	
	Examiner Thuan N. Du	Art Unit 2182	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
	A	US-5,297,124	03-1994	Plotkin et al.	703/25
	B	US-5,430,855	07-1995	Walsh et al.	703/23
	C	US-5,499,378	03-1996	McNeill et al.	703/24
	D	US-5,548,783	08-1996	Jones et al.	710/15
	E	US-6,012,113	01-2000	Tuckner, Steven A.	710/64
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

2182 pages 4-8-02

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

RECEIVED
APR 05 2002
Technology Center 2100

Patent Application Serial No. 09/331,002	)	Group Art Unit: 2182
Filing Date: June 14, 1999	)	Examiner: Du, Thuan N.
For: Flexible Interface	)	Docket No.: 13189.129 (Formerly 2055/101)
Inventor: Michael Tasler	)	Paper No.: 8

OIPE JC63 APR 03 2002 PATENT & TRADEMARK OFFICE

Certificate of Mailing Under 37 CFR 1.8

I hereby certify that this correspondence, along with all papers referred to as being enclosed or attached, are being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to Box Non-Fee Amendment, Assistant Commissioner for Patents, Washington, DC 20231.

March 18, 2002
Date

Elaine C. VonSpreckelsen

BOX NON-FEE AMEMDMENT
ASSISTANT COMMISSIONER FOR PATENTS
WASHINGTON, DC 20231

Sir:

This Amendment and Remarks is responsive to the Office Action mailed December 18, 2001.

AMENDMENT

In The Claims:

Please cancel claim 5.

Please amend claims 1, 12, 13 and 15 as follows:

1. (Amended) An interface device for communication between a host device, which comprises drivers for input/output devices customary in a host device and a multi-purpose interface, and a data transmit/receive device, the data transmit/receive device being arranged for providing analog data, comprising:

a processor;

a memory;

a first connecting device for interfacing the host device with the interface device via the multi-purpose interface of the host device; and

a second connecting device for interfacing the interface device with the data transmit/receive device, the second connecting device including a sampling circuit for sampling the analog data provided by the data transmit/receive device and an analog-to-digital converter for converting data sampled by the sampling circuit into digital data,

wherein the interface device is configured by the processor and the memory to include a first command interpreter and a second command interpreter,

wherein the first command interpreter is configured in such a way that the command interpreter, when receiving an inquiry from the host device as to a type of a device attached to the multi-purpose interface of the host device, sends a signal, regardless of the type of the data transmit/receive device attached to the second connecting device of the interface device, to the host device which signals to the host device that it is an input/output device customary in a host device, whereupon the host device communicates with the interface device by means of the driver for the input/output device customary in a host device, and

wherein the second command interpreter is configured to interpret a data request command from the host device to the type of input/output device signaled by the first command interpreter as a data transfer command for initiating a transfer of the digital data to the host device.

11. (Amended) An interface device for communication between a host device, which comprises a multi-purpose interface and a specific driver for this interface, and a data transmit/receive device, the data transmit/receive device being arranged for providing analog data, comprising:

a processor;

a memory;

a first connecting device for interfacing the host device with the interface device via the multi-purpose interface of the host device; and

a second connecting device for interfacing the interface device with the data transmit/receive device, the second connecting device including a sampling circuit for sampling the analog data provided by the data transmit/receive device and an analog-to-digital converter for converting data sampled by the sampling circuit into digital data,

where the interface device is configured using the processor and the memory to include a first command interpreter and a second command interpreter,

wherein the first command interpreter is configured in such a way that the interface device, when receiving an inquiry from the host device as to the type of a device attached at the multi-purpose interface of the host device, sends a signal, regardless of the type of the data transmit/receive device attached to the second connecting device of the interface device, to the host device which signals to the host device that it is an input/output device customary in a host device, whereupon the host device communicates with the interface device by means of the specific driver for the multi-purpose interface, and

wherein the second command interpreter is configured to interpret a data request command from the host device to the type of input/output device signaled by the first command interpreter as a data transfer command for initiating a transfer of the digital data to the host device.

12 ~~13~~. (Amended) An interface device according to claim 11 ~~12~~, wherein in addition to the first connecting device of the interface device, there is a further input/output device at the multi-purpose interface of the host device, and wherein the interface device can communicate directly with said further input/output device via the specific driver for the multi-purpose interface.

14 ~~15~~. (Amended) A method of communication between a host device, which comprises drivers for input/output devices customary in a host device and a multi-purpose interface, and a data transmit/receive device, the data transmit/receive device being

arranged for providing analog data, via an interface device, comprising:

interfacing of the host device with a first connecting device of the interface device via the multi-purpose interface of the host device;

interfacing of the data transmit/receive device with a second connecting device of the interface device, the second connecting device including a sampling circuit for sampling the analog data provided by the data/transmit/receive device and an analog-to-digital converter for converting data sampled by the sampling circuit into digital data;

inquiring by the host device at the interface device as to the type of device to which the multi-purpose interface of the host device is attached;

regardless of the type of the data transmit/receive data attached to the second connecting device of the interface device, responding to the inquiry from the host device by the interface device in such a way that it is an input/output device customary in a host device, whereupon the host device communicates with the interface device by means of the usual driver for the input/output device, and

interpreting a data request command from the host device to the type of input/output device customary in the host device as a data transfer command for initiating a transfer of the digital data to the host device.

REMARKS

The draftsperson has objected to the drawings. Clean formal drawings responsive to the objections are enclosed.

The Office Action rejected claim 13 under 35 U.S.C. 112, second paragraph, on the basis of insufficient antecedent basis for "the hard disk" in line 4. This has been corrected by amendment.

The Office Action rejected claims 1 – 16 under 35 U.S.C. 103(a) as being unpatentable over Applicant's admission of prior art in view of United States Patent No. 5,499,378 issued to McNeill, Jr. et al. Claims 1, 12, 13 and 15 gave been amended, and this rejection is respectfully traversed with respect to the claims as amended for the

reasons given below. In particular, the data transmit/receive device is arranged for providing analog data. Support for this amendment is in the penultimate paragraph of page 4. Since the second connecting device includes sample and hold circuits 1515 and an A/D converter 1503, it is clear that the data transmit/receive device to be connected to the second connecting device of the subject interface provides analog data. As to the amendment raised with respect to the second connecting device, please refer to FIG. 2 and to the just outlined elements. Regarding the amendment "first command interpreter and second command interpreter", please refer to the last paragraph of page 9. The first command interpreter performs the response to the inquiry from the host device as outlined in the penultimate paragraph of amended claim 1, while the second command interpreter interprets a data request command from the host device; for example, "read file xy" as a data transfer command for initiating a transfer of the digital data to the first device, i.e., of the digital data that have been derived from the analog data of the data transmit/receive device. Support is in the first paragraph of page 10 of the specification (final version to be filed as first preliminary amendment).

McNeill, Jr. et al. discloses a small computer system emulator for non-local SCSI devices. When FIG. 2 is considered, one may compare the initiator with the host device in claim 1, one may compare the magnetic disk 16 to the data transmit/receive device, and one may compare the target device to the interface device in claim 1.

The purpose of McNeill, Jr. et al. is to provide an access to a non-SCSI device via a SCSI bus. In particular, the initiator sends a request to the target, the request being in accordance with the SCSI protocol. The target translates this request into a request suitable for magnetic disk 16 such that the initiator can access to magnetic disk 16 via SCSI commands. This reference does not disclose that the data transmit/receive device is arranged for providing analog data. It is well known that digital data are stored on magnetic disks.

Additionally, the target does not include any sample and hold circuit or any analog-

to-digital converter for converting data from magnetic disk 16 into digital data.

In addition, this reference does not include a first command interpreter that, when asked by the host device as to the type of device connected to the interface, lies to the host computer as to the real nature of the data transmit/receive device. In McNeill, Jr. et al., the initiator asks for a hard disk and the target states that there is a hard disk. In other words, the target does not lie as to the true type of the data transmit/receive device. The conversion done in McNeill, Jr. et al. is to transfer SCSI protocol commands into commands understandable for the magnetic disk.

Finally, McNeill, Jr. et al. does not include a second command interpreter as defined in the last paragraph of amended claim 1.

For the above reasons, McNeill, Jr. et al. is not pertinent to the present invention as defined in amended claim 1.

We also note that the examiner did not reject claim 5 in detail. Claim 5 includes the A/D converter feature that has been included into amended claim 1. Thus, this also supports the fact that the amended claims are patentable.

For the above reasons, the claims as amended are believed to be patentable and their reconsideration and allowance are respectfully requested. It is believed no fee is due. If any fees are due, the Commissioner is authorized to charge them to Deposit Account No. 50-1848.

Respectfully submitted,
PATTON BOGGS LLP

By: _____

Leslie S. Garmaise, Reg. No. 47,587
Telephone: (303) 379-1131
Facsimile: (303) 379-1155
Customer No.: 24283

Version With Markings To Show Changes Made

In The Claims:

Please cancel claim 5.

Please amend claims 1, 12, 13 and 15 as follows:

1. (Amended) An interface device for communication between a host device, which comprises drivers for input/output devices customary in a host device and a multi-purpose interface, and a data transmit/receive device, the data transmit/receive device being arranged for providing analog data, comprising [the following features]:

a processor;

a memory;

a first connecting device for interfacing the host device with the interface device via the multi-purpose interface of the host device; and

a second connecting device for interfacing the interface device with the data transmit/receive device, the second connecting device including a sampling circuit for sampling the analog data provided by the data transmit/receive device and an analog-to-digital converter for converting data sampled by the sampling circuit into digital data,

wherein the interface device is configured by the processor and the memory to include a first command interpreter and a second command interpreter,

wherein the first command interpreter is configured in such a way that the command interpreter, when receiving an inquiry from the host device as to [the] a type of a device attached to the multi-purpose interface of the host device, sends a signal, regardless of the type of the data transmit/receive device attached to the second connecting device of the interface device, to the host device which signals to the host device that it is an input/output device customary in a host device, whereupon the host device communicates with the interface device by means of the driver for the input/output device customary in a host device, and

wherein the second command interpreter is configured to interpret a data request command from the host device to the type of input/output device signaled by the first

command interpreter as a data transfer command for initiating a transfer of the digital data to the host device.

12. (Amended) An interface device for communication between a host device, which comprises a multi-purpose interface and a specific driver for this interface, and a data transmit/receive device, the data transmit/receive device being arranged for providing analog data, comprising [the following features]:

a processor;

a memory;

a first connecting device for interfacing the host device with the interface device via the multi-purpose interface of the host device; and

a second connecting device for interfacing the interface device with the data transmit/receive device, the second connecting device including a sampling circuit for sampling the analog data provided by the data transmit/receive device and an analog-to-digital converter for converting data sampled by the sampling circuit into digital data,

where the interface device is configured using the processor and the memory to include a first command interpreter and a second command interpreter,

wherein the first command interpreter is configured in such a way that the interface device, when receiving an inquiry from the host device as to the type of a device attached at the multi-purpose interface of the host device, sends a signal, regardless of the type of the data transmit/receive device attached to the second connecting device of the interface device, to the host device which signals to the host device that it is an input/output device customary in a host device, whereupon the host device communicates with the interface device by means of the specific driver for the multi-purpose interface, and

wherein the second command interpreter is configured to interpret a data request command from the host device to the type of input/output device signaled by the first command interpreter as a data transfer command for initiating a transfer of the digital data to the host device.

13. (Amended) An interface device according to claim 12, wherein in addition

to the first connecting device of the interface device, there is a further input/output device at the multi-purpose interface of the host device, and wherein the interface device can communicate directly with [the hard disk] said further input/output device via the specific driver for the multi-purpose interface.

15. (Amended) A method of communication between a host device, which comprises drivers for input/output devices customary in a host device and a multi-purpose interface, and a data transmit/receive device, the data transmit/receive device being arranged for providing analog data, via an interface device, comprising [the following steps]:

interfacing of the host device with a first connecting device of the interface device via the multi-purpose interface of the host device;

interfacing of the data transmit/receive device with a second connecting device of the interface device, the second connecting device including a sampling circuit for sampling the analog data provided by the data/transmit/receive device and an analog-to-digital converter for converting data sampled by the sampling circuit into digital data;

inquiring by the host device at the interface device as to the type of device to which the multi-purpose interface of the host device is attached;

regardless of the type of the data transmit/receive data attached to the second connecting device of the interface device, responding to the inquiry from the host device by the interface device in such a way that it is an input/output device customary in a host device, whereupon the host device communicates with the interface device by means of the usual driver for the input/output device, and

interpreting a data request command from the host device to the type of input/output device customary in the host device as a data transfer command for initiating a transfer of the digital data to the host device.

10
TO DATA TRANSMIT/ RECEIVE DEVICE
16
2nd CD
15
13
DSP
MEMORY
14
1st CD
12
TO HOST
11

FIG.1

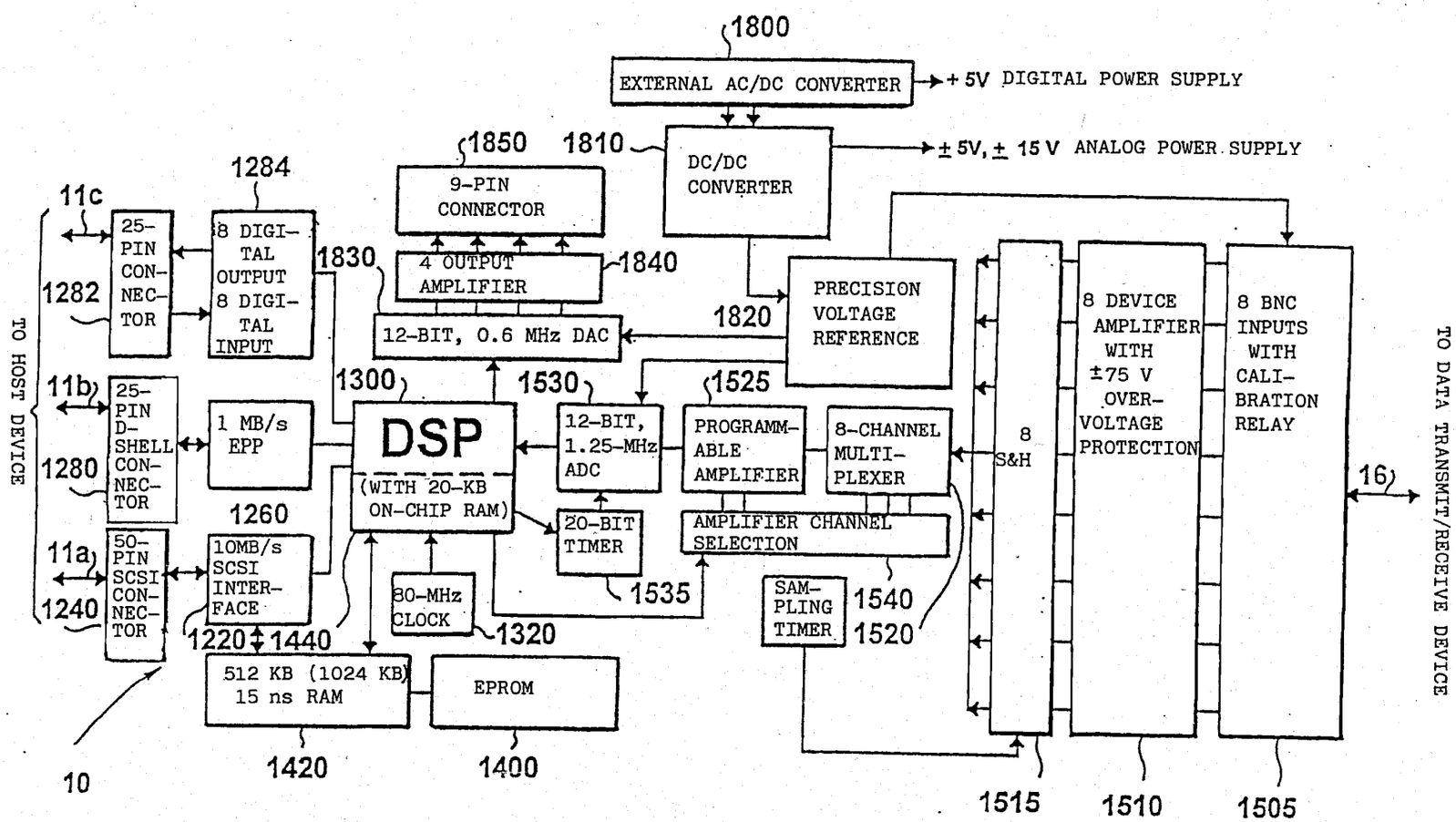

1800
EXTERNAL AC/DC CONVERTER
+5V DIGITAL POWER SUPPLY
1850
1810
DC/DC CONVERTER
±5V, ±15V ANALOG POWER SUPPLY
1284
11c
9-PIN CONNECTOR
25-PIN CON-NEC-TOR
8 DIGI-TAL OUTPUT 8 DIGI-TAL INPUT
1830
4 OUTPUT AMPLIFIER
1840
1282
12-BIT, 0.6 MHz DAC
1820
PRECISION VOLTAGE REFERENCE
TO HOST DEVICE
11b
1300
1530
1525
25-PIN D-SHELL CON-NEC-TOR
1 MB/s EPP
DSP
(WITH 20-KB ON-CHIP RAM)
12-BIT, 1.25-MHz ADC
PROGRAMM-ABLE AMPLIFIER
8-CHANNEL MULTI-PLEXER
8 S&H
8 DEVICE AMPLIFIER WITH ±75 V OVER-VOLTAGE PROTECTION
8 BNC INPUTS WITH CALI-BRATION RELAY
16
TO DATA TRANSMIT/RECEIVE DEVICE
1280
1260
11a
50-PIN SCSI CON-NEC-TOR
10MB/s SCSI INTER-FACE
20-BIT TIMER
AMPLIFIER CHANNEL SELECTION
1535
SAM-PLING TIMER
1540
1520
1240
1220
1440
80-MHz CLOCK
1320
512 KB (1024 KB) 15 ns RAM
EPROM
10
1420
1400
1515
1510
1505

FIG.2

8k #9/C

Notice of Allowability	Application No.	Applicant(s)	
	09/331,002	TASLER, MICHAEL	
	Examiner	Art Unit	
	Thuan N. Du	2185	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *amendment filed on March 18, 2002*.
2. ☒ The allowed claim(s) is/are *1-4 and 6-16 (renumbered as 1-15)*.
3. ☒ The drawings filed on *18 March 2002* are accepted by the Examiner.
4. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☒ All b) ☐ Some* c) ☐ None of the:
      1. ☒ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☒ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.
5. ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
   (a) ☐ The translation of the foreign language provisional application has been received.
6. ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application. **THIS THREE-MONTH PERIOD IS NOT EXTENDABLE**

7. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

8. ☐ CORRECTED DRAWINGS must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No. ____.
   (b) ☐ including changes required by the proposed drawing correction filed _____, which has been approved by the Examiner.
   (c) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No. _____.

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the top margin (not the back) of each sheet. The drawings should be filed as a separate paper with a transmittal letter addressed to the Official Draftsperson.

9. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1☐ Notice of References Cited (PTO-892)
3☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
5☐ Information Disclosure Statements (PTO-1449), Paper No. ____.
7☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
2☐ Notice of Informal Patent Application (PTO-152)
4☐ Interview Summary (PTO-413), Paper No.____ .
6☒ Examiner's Amendment/Comment
8☐ Examiner's Statement of Reasons for Allowance
9☐ Other

THOMAS LEE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100

EXAMINER'S AMENDMENT

1. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

2. The application has been amended as follows:

3. Pursuant to MPEP 606.01, the title has been changed to read:

-- FLEXIBLE INTERFACE FOR COMMUNICATION BETWEEN A HOST AND AN ANALOG I/O DEVICE CONNTECTED TO THE INTERFACE REGARDLESS THE TYPE OF THE I/O DEVICE --

Conclusion

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thuan N. Du whose telephone number is (703) 308-6292 or via e-mail, ***thuan.du@uspto.gov***. The examiner can normally be reached on Monday-Friday: 9:00 AM - 5:30 PM, EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thomas C. Lee can be reached on (703) 305-9717.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks
Washington, D.C. 20231.

The fax numbers for the organization where this application or proceeding is assigned are as follow:

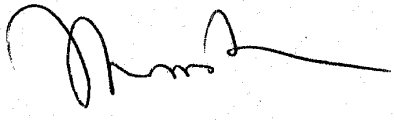
- (703) 746-7238 [After Final Communication]
- (703) 746-7239 [Official Communication]
- (703) 746-7240 [Non-Official Communication]

and/or:

(703) 746-5668 (use this fax number, only after approval by Examiner, for "INFORMAL" or "DRAFT" communication).

Hand-delivered responses should be brought to:

Crystal Park II
2121 Crystal Drive
Arlington, VA 22202
Fourth Floor (Receptionist).



THOMAS LEE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100

Thuan N. Du
May 15, 2002

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231
www.uspto.gov

NOTICE OF ALLOWANCE AND FEE(S) DUE

24283 7590 05/17/2002

PATTON BOGGS
PO BOX 270930
LOUISVILLE, CO 80027

EXAMINER	
DU, THUAN N	
ART UNIT	CLASS-SUBCLASS
2185	710-001000

DATE MAILED: 05/17/2002

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/331,002	06/14/1999	MICHAEL TASLER	2055/101	1117

TITLE OF INVENTION: FLEXIBLE INTERFACE FOR COMMUNICATION BETWEEN A HOST AND AN ANALOG I/O DEVICE CONNTECTED TO THE INTERFACE REGARDLESS THE TYPE OF THE I/O DEVICE

APPLN. TYPE	SMALL ENTITY	ISSUE FEE	PUBLICATION FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	YES	$640	$0	$640	08/19/2002

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE REFLECTS A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE APPLIED IN THIS APPLICATION. THE PTOL-85B (OR AN EQUIVALENT) MUST BE RETURNED WITHIN THIS PERIOD EVEN IF NO FEE IS DUE OR THE APPLICATION WILL BE REGARDED AS ABANDONED.

HOW TO REPLY TO THIS NOTICE:

I. Review the SMALL ENTITY status shown above. If the SMALL ENTITY is shown as YES, verify your current SMALL ENTITY status:

A. If the status is changed, pay the PUBLICATION FEE (if required) and twice the amount of the ISSUE FEE shown above and notify the United States Patent and Trademark Office of the change in status, or

B. If the status is the same, pay the TOTAL FEE(S) DUE shown above.

If the SMALL ENTITY is shown as NO:

A. Pay TOTAL FEE(S) DUE shown above, or

B. If applicant claimed SMALL ENTITY status before, or is now claiming SMALL ENTITY status, check the box below and enclose the PUBLICATION FEE and 1/2 the ISSUE FEE shown above.

☐ Applicant claims SMALL ENTITY status. See 37 CFR 1.27.

II. PART B - FEE(S) TRANSMITTAL should be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). Even if the fee(s) have already been paid, Part B - Fee(s) Transmittal should be completed and returned. If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Box ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

PTOL-85 (REV. 04-02) Approved for use through 01/31/2004.

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail Box ISSUE FEE
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Fax (703)746-4000

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24283 7590 05/17/2002

PATTON BOGGS
PO BOX 270930
LOUISVILLE, CO 80027

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I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Box Issue Fee address above, or being facsimile transmitted to the USPTO, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/331,002	06/14/1999	MICHAEL TASLER	2055/101	1117

TITLE OF INVENTION: FLEXIBLE INTERFACE FOR COMMUNICATION BETWEEN A HOST AND AN ANALOG I/O DEVICE CONNTECTED TO THE INTERFACE REGARDLESS THE TYPE OF THE I/O DEVICE

APPLN. TYPE	SMALL ENTITY	ISSUE FEE	PUBLICATION FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	YES	$640	$0	$640	08/19/2002

EXAMINER	ART UNIT	CLASS-SUBCLASS
DU, THUAN N	2185	710-001000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

❑ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.

❑ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list (1) the names of up to 3 registered patent attorneys or agents OR, alternatively, (2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1_____
2_____
3_____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. Inclusion of assignee data is only appropriate when an assignment has been previously submitted to the USPTO or is being submitted under separate cover. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE (B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) ❑ individual ❑ corporation or other private group entity ❑ government

4a. The following fee(s) are enclosed:

❑ Issue Fee
❑ Publication Fee
❑ Advance Order - # of Copies _____

4b. Payment of Fee(s):

❑ A check in the amount of the fee(s) is enclosed.
❑ Payment by credit card. Form PTO-2038 is attached.
❑ The Commissioner is hereby authorized by charge the required fee(s), or credit any overpayment, to Deposit Account Number _____(enclose an extra copy of this form).

Commissioner for Patents is requested to apply the Issue Fee and Publication Fee (if any) or to re-apply any previously paid issue fee to the application identified above.

(Authorized Signature) (Date)

NOTE; The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, Washington, D.C. 20231. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, Washington, DC 20231.

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PTOL-85 (REV. 04-02) Approved for use through 01/31/2004. OMB 0651-0033 U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/331,002	06/14/1999	MICHAEL TASLER	2055/101	1117

24283 7590 05/17/2002

PATTON BOGGS
PO BOX 270930
LOUISVILLE, CO 80027
UNITED STATES

EXAMINER	
DU, THUAN N	
ART UNIT	**PAPER NUMBER**
2185	

DATE MAILED: 05/17/2002

Determination of Patent Term Extension under 35 U.S.C. 154 (b)

(application filed after June 7, 1995 but prior to May 29, 2000)

The patent term extension is 0 days. Any patent to issue from the above identified application will include an indication of the 0 day extension on the front page.

If a continued prosecution application (CPA) was filed in the above-identified application, the filing date that determines patent term extension is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) system. (http://pair.uspto.gov)

PTOL-85 (REV. 04-02) Approved for use through 01/31/2004.

PATTON BOGGS LLP
ATTORNEYS AT LAW

867 Coal Creek Circle, Suite 200
Louisville, CO 80027-9750
303-379-1100

Facsimile 303-379-1155

To:	BOX ISSUE FEE
Company:	USPTO
Fax Number:	1-703-746-4000
Phone Number:	1-703-308-6803
Serial No.:	09/331,002
Total Pages Including Cover:	3
From:	Elaine C. VonSpreckelsen, Secretary to Carl A. Forest
Sender's Direct Line:	303-379-1111
Date:	August 16, 2002
Client Number:	13189.129 (Formerly 2055/101)

Comments:

Serial No.:	09/331,002	Art Unit:	2185
Filed:	14-Jun-1999	Examiner:	Du, Thuan N.

Attached please find two copies of the Fee(s) Transmittal to be entered in the above application. Please charge the total fee of $670.00 to Deposit Account No. 50-1848. Thank you for your assistance in this matter. If you need anything further, please do not hesitate to contact me.

ANCHORAGE
BOULDER
DALLAS
DENVER
NORTHERN VIRGINIA
WASHINGTON, D.C.

If you did not receive all of the pages or find that they are illegible, please call 303-379-1111.

3

OK to Enter

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Patent Application Serial No.: 09/331,002	Group Art Unit: 2[illegible]
Filing Date: June 14, 1999	Examiner: Du, Thuan N.
For: Flexible Interface For Communication Between A Host And An Analog I/O Device Conntected To The Interface Regardless The Type Of The I/O Device	Docket No.: 13189.129 (Formerly 2055/101)
	Paper No. 10
Inventor: Michael Tasler	

CERTIFICATE OF TRANSMISSION UNDER 37 CFR 1.8

I hereby certify that this correspondence, along with all papers referred to as being transmitted, are being facsimile transmitted to the Patent and Trademark Office Fax No. (703) 746-4000.

August 13, 2002
Date

Elaine C. VonSpreckelsen
Elaine C. VonSpreckelsen

BOX ISSUE FEE
ASSISTANT COMMISSIONER FOR PATENTS
WASHINGTON, DC 20231

Match and Return

Sir:

This Rule 312 Amendment and Remarks are filed in response to the Notice Of Allowability mailed May 17, 2002.

RULE 312 AMENDMENT

In the Specification:

Please amend the title to read as follows:

FLEXIBLE INTERFACE FOR COMMUNICATION BETWEEN A HOST AND AN ANALOG I/O DEVICE CONNECTED TO THE INTERFACE REGARDLESS THE TYPE OF THE I/O DEVICE

REMARKS

The title has been amended to correct a spelling error.

For the reasons given above, claims 1 – 4 and 6 – 16 are patentable and their reconsideration and allowance are respectfully requested. No additional fee is seen to be

OK to Enter

VERSION WITH MARKINGS SHOWING TO SHOW CHANGES MADE

In the Specification:

The title been amended to read as follows:

FLEXIBLE INTERFACE FOR COMMUNICATION BETWEEN A HOST AND AN ANALOG I/O DEVICE [CONNTECTED] CONNECTED TO THE INTERFACE REGARDLESS THE TYPE OF THE I/O DEVICE

due. However, if any additional fee is due, please charge it to Deposit Account No. 50-1848.

Respectfully submitted,
PATTON BOGGS LLP

By: _____

Carl A. Forest, Registration No. 28,494
Telephone: 303-379-1114
Facsimile: 303-379-1155
Customer No.: 24283

PART B - FEE(S) TRANSMITTAL

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Fax (703)746-4000

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24283 7590 05/17/2002

PATTON BOGGS
PO BOX 270930
LOUISVILLE, CO 80027

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Certificate of Mailing or Transmission
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CARL A. FORREST (Depositor's name)
(Signature)
8/16/02 (Date)

09/331,002

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/331,002	06/14/1999	MICHAEL TASLER	2055/101 *	1117

TITLE OF INVENTION: FLEXIBLE INTERFACE FOR COMMUNICATION BETWEEN A HOST AND AN ANALOG I/O DEVICE CONNTECTED TO THE INTERFACE REGARDLESS THE TYPE OF THE I/O DEVICE

*Now 13189.129

APPLN. TYPE	SMALL ENTITY	ISSUE FEE	PUBLICATION FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	YES	$640	$0	$640	08/19/2002

EXAMINER	ART UNIT	CLASS-SUBCLASS
DU, THUAN N	2185	710-001000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).
☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47) attached. Use of a Customer Number is required.

2. For printing on the patent front page, list (1) the names of up to 3 registered patent attorneys or agents OR, alternatively, (2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.
1 Patton Boggs LLP
2
3

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. Inclusion of assignee data is only appropriate when an assignment has been previously submitted to the USPTO or is being submitted under separate cover. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE: Labortechnik Tasler GmbH
(B) RESIDENCE: (CITY and STATE OR COUNTRY): Wuerzburg, Germany

Please check the appropriate assignee category or categories (will not be printed on the patent) ☒ individual ☐ corporation or other private group entity ☐ government

4a. The following fee(s) are enclosed:
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☐ Publication Fee
☒ Advance Order - # of Copies Ten (10) 30.00
$670.00

4b. Payment of Fee(s):
☐ A check in the amount of the fee(s) is enclosed.
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☒ The Commissioner is hereby authorized by charge the required fee(s), or credit any overpayment, to Deposit Account Number 50-1848 (enclose an extra copy of this form).

Commissioner for Patents is requested to apply the Issue Fee and Publication Fee (if any) or to re-apply any previously paid issue fee to the application identified above.

(Authorized Signature) (Date) 8/16/02

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

08/19/2002 BNGUYEN2 00000004 501848 09331002
01 FC:242 640.00 CH
02 FC:1561 30.00 CH

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, Washington, D.C. 20231. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, Washington, DC 20231.

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TRANSMIT THIS FORM WITH FEE(S)

3

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Patent Application Serial No.: 09/331,002

Filing Date: June 14, 1999

For: Flexible Interface For Communication Between A Host And An Analog I/O Device Conntected To The Interface Regardless The Type Of The I/O Device

Inventor: Michael Tasler

Group Art Unit: 2[illegible]

Examiner: Du, Thuan N.

Docket No.: 13189.129 (Formerly 2055/101)

Paper No. 10

CERTIFICATE OF TRANSMISSION UNDER 37 CFR 1.8

I hereby certify that this correspondence, along with all papers referred to as being transmitted, are being facsimile transmitted to the Patent and Trademark Office Fax No. (703) 746-4000.

August 13, 2002
Date

Elaine C. VonSpreckelsen
Elaine C. VonSpreckelsen

BOX ISSUE FEE
ASSISTANT COMMISSIONER FOR PATENTS
WASHINGTON, DC 20231

Match and Return

Sir:

This Rule 312 Amendment and Remarks are filed in response to the Notice Of Allowability mailed May 17, 2002.

RULE 312 AMENDMENT

In the Specification:

Please amend the title to read as follows:

FLEXIBLE INTERFACE FOR COMMUNICATION BETWEEN A HOST AND AN ANALOG I/O DEVICE CONNECTED TO THE INTERFACE REGARDLESS THE TYPE OF THE I/O DEVICE

REMARKS

The title has been amended to correct a spelling error.

For the reasons given above, claims 1 – 4 and 6 – 16 are patentable and their reconsideration and allowance are respectfully requested. No additional fee is seen to be

OK to Enter

VERSION WITH MARKINGS SHOWING TO SHOW CHANGES MADE

In the Specification:

The title been amended to read as follows:

FLEXIBLE INTERFACE FOR COMMUNICATION BETWEEN A HOST AND AN ANALOG I/O DEVICE [CONNTECTED] CONNECTED TO THE INTERFACE REGARDLESS THE TYPE OF THE I/O DEVICE

due. However, if any additional fee is due, please charge it to Deposit Account No. 50-1848.

Respectfully submitted,
PATTON BOGGS LLP

By: _____

Carl A. Forest, Registration No. 28,494
Telephone: 303-379-1114
Facsimile: 303-379-1155
Customer No.: 24283

09331002

COMPLETED

6470399

WELSH & KATZ, LTD.

120 South Riverside Plaza
22nd Floor
Chicago, Illinois 60606
Phone (312) 655-1500
Facsimile Number (312) 655-1501

FACSIMILE COVER SHEET

From: Jeffrey W. Salmon, Esq. Date: March 15, 2006

To: Group 2181
Commissioner for Patents
UNITED STATES PATENT & TRADEMARK OFFICE
Washington, D.C. 20231

Fax: (571) 273-8300

Number of pages including this cover letter: 4

COMMENTS:

File No. 9576/96908/09/10

Items being filed via this facsimile are listed below:

- Transmittal Letter (1 Page)
- Executed Revocation of Power of Attorney with New Power of Attorney, Change of Correspondence Address, and Statement Under 37 C.F.R. 3.73(b) (2 Pages)

IF YOU DO NOT RECEIVE ALL PAGES OR ARE HAVING TROUBLE, PLEASE CALL IMMEDIATELY (312) 655-1500 AND ASK FOR Maura Halvey

TRANSMITTAL LETTER (General - Patent Issued)	Docket No. 9576/96909

Patentee(s):
Michael Tasler

U.S. Patent No.	Issue Date
6,470,399	10/22/2002

Title: **FLEXIBLE INTERFACE FOR COMMUNICATION BETWEEN A HOST AND AN ANALOG I/O DEVICE CONNECTED TO THE INTERFACE REGARDLESS THE TYPE OF I/O DEVICE**

COMMISSIONER FOR PATENTS:

Transmitted herewith is:

Executed Revocation of Power Attorney With New Power of Attorney, Change of Correspondence Address, and Statement Under 37 C.F.R. 3.73(b)

- ☒ No additional fee is required.
- ☐ A check in the amount of is attached.
- ☒ The Director is hereby authorized to charge and credit Deposit Account **23-0920** as described below.
  - ☐ Charge the amount of
  - ☒ Credit any overpayment.
  - ☒ Charge any additional fee required.
- ☐ Payment by credit card. Form PTO-2038 is attached.

WARNING: Information on this form may become public. Credit card information should not be included on this form. Provide credit card information and authorization on PTO-2038.

Jeffrey W Glen
Signature

Dated: 15 Mar 2006

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to "Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450" [37 CFR 1.8(a)] on
3/15/06 via Facsimile
(Date) (571) 273-8300
Signature of Person Mailing Correspondence
Maura Halvey
Typed or Printed Name of Person Mailing Correspondence

Customer No.: **24628**

cc:

P17A/REV04

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

U.S. Patent Number:	6,470,399 B1
Issue Date:	Oct. 22, 2002
First Named Inventor:	Michael Tasler, Wurzburg (DE)
Title of Invention:	FLEXIBLE INTERFACE FOR COMMUNICATION BETWEEN A HOST AND AN ANALOG I/O DEVICE CONNECTED TO THE INTERFACE REGARDLESS THE TYPE OF I/O DEVICE
Attorney Docket Number:	9576/96909

REVOCATION OF POWER OF ATTORNEY WITH NEW POWER OF ATTORNEY, CHANGE OF CORRESPONDENCE ADDRESS, AND STATEMENT UNDER 37 C.F.R. 3.73(b)

1. Papst Licensing GmbH & Co. KG hearby revokes all previous powers of attorney given in the above-identified patent.

2. Papst Licensing GmbH & Co. KG hearby appoints the Practitioners named below as its attorneys or agents to prosecute the application identified above, and to transact all business in the United States Patent and Trademark Office connected therewith.

Name	Registration Number
Jeffrey W. Salmon	37,435
Richard L. Wood	22,839
Joseph R. Marcus	25,060
Gerald T. Shekleton	27,466
Edward P. Gamson, Ph.D.	29,381
Kathleen A. Rheintgen	34,044
Eric D. Cohen	38,110
John P. Christensen	34,137
Louise T. Walsh	45,195
Paul M. Vargo, Ph.D.	29,116
Richard J. Gurak	41,050
Daniel M. Gurfinkel	24,177

3. Please change the correspondence address for the above-identified patent to:

Jeffrey W. Salmon, Esq.
Welsh & Katz, Ltd.
120 S. Riverside Plaza, 22nd Floor
Chicago IL, 60606 USA
Telephone: (312) 655-1500
Facsimile: (312) 655-1501
Email: jwsalmon@welshkatz.com

4. Papst Licensing GmbH & Co. KG, a German Corporation, is the assignee of the entire right, title and interest the above-captioned patent by virtue of a chain of title from the inventor as set forth hereafter:

(a) From: Michael Tasler to Labortechnik Tasler GmbH. The assignment document was recorded in the Patent and Trademark Office on July 23, 2001 at reel/frame no. 012023/0515.

(b) From: Labortechnik Tasler GmbH to Papst Licensing GmbH & Co KG. A copy of this assignment is attached as Exhibit A hereto and, by separate filing, is being submitted to the U.S. Patent & Trademark Office for recordation.

5. I have reviewed all of the documents in the chain of title to this application and, to the best of my knowledge and belief, title is in Papst Licensing GmbH & Co. KG.

6. I aver that I am empowered to sign this document on behalf of Papst Licensing GmbH & Co. KG.

7. I hereby declare that all statements made herein of my own knowledge are true and that all statements made upon information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Papst Licensing GmbH & Co. KG

By: K. Papst

Title: PRESIDENT

Date: March 8, 2006

ASSIGNMENT

WHEREAS, LTT Labortechnik Tasler GmbH, is a corporation of Germany, has a P.O. address of Friedrich-Bergius-Ring 15, 97076 Würzburg, Germany, ("Assignor") and is the owner of the entire right, title, and interest in and to: United States Patent No. 6,470,399 B1, United States Patent No. 6,895,449 B2, and United States Patent Application No. 11/078,778 (hereinafter "Patent Rights").

WHEREAS, Papst Licensing GmbH & Co. KG, a German Corporation, having its principal place of business at Bahnhofstrasse 33, 78112 St. Georgen, Germany ("Assignee"), is desirous of acquiring the entire interest in and to the Patent Rights.

NOW, THEREFORE, for good and valuable consideration, the receipt of which is hereby acknowledged, and in consideration of the covenants and obligations hereinafter set forth to be well and truly performed, the parties hereby agree as follows.

1. Assignor hereby, sells, assigns, and transfers to Assignee, its lawful successors and assigns, Assignor's entire right, title and interest in and to the Patent Rights. Assignee hereby shall take, acquire and hold such right, title and interest in and to the Patent Rights.

2. Assignor hereby furthermore sells, assigns, and transfers to Assignee all claims for past, present, and future infringement of the inventions covered by Patent Rights, including without limitation all rights to recover damages and the right to grant releases for past infringement of the Patent Rights.

3. Assignor hereby further covenants and agrees, to render such assistance to Assignee as may be necessary to perfect the title to Patent Rights in said Assignee, its successors and assigns, to enable Assignee to prosecute all divisional, continuation, reexamination, and reissue applications, and to enable Assignee to obtain and enforce proper patent protection for the Patent Rights.

4. Assignor hereby covenants that no assignment, sale, agreement or encumbrance has been or will be made or entered into which would conflict with this assignment and sale.

5. Assignor further covenants that (i) Assignee will, upon its request, be provided promptly with all pertinent facts and documents relating to the Patent Rights as may be known and/or accessible to Assignor, (ii) Assignor shall testify as to the same in any interference or litigation related thereto, and (iii) Assignor shall promptly execute and deliver to Assignee or its legal representative any and all papers, instruments or affidavits required to apply for, obtain, maintain or enforce the Patent Rights and/or any U.S. patent rights evolving therefrom. Assignor shall use his best efforts to cooperate in good faith with Assignee.

LTT Labortechnik Tasler GmbH

By: Eckart Tasler

Title: General Manager

Date: March 8. 2006

Papst Licensing GmbH & Co. KG

By: [signature]

Title: PRESIDENT

Date: March. 8. 2006

Exhibit A

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371 (c) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
09/331,002	06/14/1999	MICHAEL TASLER	2055/101

22862
GLENN PATENT GROUP
3475 EDISON WAY, SUITE L
MENLO PARK, CA 94025

CONFIRMATION NO. 1117

OC000000020041771

Date Mailed: 08/16/2006

NOTICE REGARDING CHANGE OF POWER OF ATTORNEY

This is in response to the Power of Attorney filed 03/15/2006.

- The Power of Attorney to you in this application has been revoked by the assignee who has intervened as provided by 37 CFR 3.71. Future correspondence will be mailed to the new address of record(37 CFR 1.33).

DESHAWN D DURHAM
OIPE (703) 308-9010 EXT 173

OFFICE COPY

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371 (c) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
09/331,002	06/14/1999	MICHAEL TASLER	9576/96909

CONFIRMATION NO. 1117

OC0000000020041890

Jeffrey W Salmon Esq
Welsh & Katz Ltd
120 S Riverside Plaza 22nd Floor
Chicago, IL 60606

Date Mailed: 08/16/2006

NOTICE OF ACCEPTANCE OF POWER OF ATTORNEY

This is in response to the Power of Attorney filed 03/15/2006.

The Power of Attorney in this application is accepted. Correspondence in this application will be mailed to the above address as provided by 37 CFR 1.33.

DESHAWN D DURHAM
OIPE (703) 308-9010 EXT 173

OFFICE COPY

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

U.S. Patent Number:	6,470,399 B1
Issue Date:	Oct. 22, 2002
First Named Inventor:	Michael Tasler, Wurzburg (DE)
Title of Invention:	FLEXIBLE INTERFACE FOR COMMUNICATION BETWEEN A HOST AND AN ANALOG I/O DEVICE CONNECTED TO THE INTERFACE REGARDLESS THE TYPE OF I/O DEVICE
Attorney Docket Number:	9576/96909

DESIGNATION OF DOMESTIC REPRESENTATIVE PURSUANT TO 35 USC §293 AND 37 CFR §3.61

Papst Licensing GmbH & Co. KG, the assignee of the above-identified patent, hereby designates the following as Domestic Representative upon whom notice or process in proceedings affecting the above-identifed patent may be served at the following address:

Jerold B. Schnayer, Esq.
Welsh & Katz, Ltd.
120 South Riverside Plaza, 22nd Floor
Chicago, Illinois 60606
Telephone (312) 655-1500
Facsimile (312) 655-1501
E-mail jbschnayer@welshkatz.com

Papst Licensing GmbH & Co. KG

By: Papst

Title: Senior Manager Finance

Date: 06/27/07

Electronic Acknowledgement Receipt	
EFS ID:	1917870
Application Number:	09331002
International Application Number:	
Confirmation Number:	1117
Title of Invention:	FLEXIBLE INTERFACE FOR COMMUNICATION BETWEEN A HOST AND AN ANALOG I/O DEVICE CONNTECTED TO THE INTERFACE REGARDLESS THE TYPE OF THE I/O DEVICE
First Named Inventor/Applicant Name:	MICHAEL TASLER
Correspondence Address:	Jeffrey W Salmon Esq Welsh & Katz Ltd 120 S Riverside Plaza 22nd Floor - Chicago IL 60606 US 312-655-1500 jwsalmon@welshkatz.com
Filer:	Jeffrey W. Salmon/Maura Halvey
Filer Authorized By:	Jeffrey W. Salmon
Attorney Docket Number:	9576/96909
Receipt Date:	27-JUN-2007
Filing Date:	14-JUN-1999
Time Stamp:	18:03:18
Application Type:	U.S. National Stage under 35 USC 371

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)	Multi Part /.zip	Pages (if appl.)
1	Power of Attorney	6470399DesignationofDomesticRep.pdf	48540	no	1
Warnings:					
Information:					
		Total Files Size (in bytes):	48540		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

SOLICITOR

OCT 15 2007

AO 120 (Rev. 3/04)

U.S. PATENT & TRADEMARK OFFICE

TO:	REPORT ON THE FILING OR DETERMINATION OF AN ACTION REGARDING A PATENT OR TRADEMARK
Mail Stop 8 Director of the U.S. Patent and Trademark Office P.O. Box 1450 Alexandria, VA 22313-1450	

In Compliance with 35 U.S.C. § 290 and/or 15 U.S.C. § 1116 you are hereby advised that a court action has been filed in the U.S. District Court Central District on the following ☒ Patents or ☐ Trademarks:

DOCKET NO. 07-04249 PA(JCx)	DATE FILED 6/28/2007	U.S. DISTRICT COURT Central District
PLAINTIFF PAPST LICENSING GmbH & CO. KG		DEFENDANT SAMSUNG TECHWIN CO. and SAMSUNG OPTO-ELECTRONICS AMERICA, INC.

FILED
2007 JUN 28 PM 12:36
CLERK U.S. DISTRICT COURT
CENTRAL DIST. OF CALIF.
LOS ANGELES

	PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1	6,470,399 B1	10/22/2002	Papst Licensing GmbH & Co., KG
2	6,895,449 B2	5/17/2005	Papst Licensing GmbH & Co., KG
3			
4			
5			

In the above—entitled case, the following patent(s)/ trademark(s) have been included:

DATE INCLUDED	INCLUDED BY ☐ Amendment ☐ Answer ☐ Cross Bill ☐ Other Pleading	
PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1		
2		
3		
4		
5		

In the above—entitled case, the following decision has been rendered or judgement issued:

DECISION/JUDGEMENT
ORDER TRANSFERRING ACTION TO THE UNITED STATES DISTRICT COURT FOR THE DISTRICT OF NEW JERSEY FILED 10/3/07.

CLERK	(BY) DEPUTY CLERK	DATE
SHERRI R. CARTER		OCT 10 2007

Copy 1—Upon initiation of action, mail this copy to Director Copy 3—Upon termination of action, mail this copy to Director
Copy 2—Upon filing document adding patent(s), mail this copy to Director Copy 4—Case file copy

ENTER
SEND JS-6

FILED
CLERK, U.S. DISTRICT COURT
OCT - 3 2007
CENTRAL DISTRICT OF CALIFORNIA
BY CASL DEPUTY

ENTERED
CLERK, U.S. DISTRICT COURT
OCT 10 2007
CENTRAL DISTRICT OF CALIFORNIA
BY DEPUTY

UNITED STATES DISTRICT COURT

CENTRAL DISTRICT OF CALIFORNIA

PAPST LICENSING GmbH & CO. KG,

Plaintiff,

v.

SAMSUNG TECHWIN CO.; SAMSUNG OPTO-ELECTRONICS AMERICA, INC.,

Defendants.

No. CV 07-4249 PA (JCx)

ORDER TRANSFERRING ACTION TO THE UNITED STATES DISTRICT COURT FOR THE DISTRICT OF NEW JERSEY

THIS CONSTITUTES NOTICE OF ENTRY AS REQUIRED BY FRCP, RULE 77(d)

Before the Court is a Motion to Transfer ("Motion") filed by defendants Samsung Techwin Company and Samsung Opto-Electronics America, Inc. ("Defendants") (Docket No. 22).

Background

Plaintiff Papst Licensing GmbH & Co. KG ("Plaintiff" or "Papst") is in the business of licensing patents, and is a company organized and existing under the laws of Germany, with its principal place of business in Germany. Defendant Samsung Techwin Company ("Samsung Techwin") is a Korean company with no United States presence. Defendant Samsung Opto-Electronics America, Inc. ("Samsung America"), a subsidiary of Samsung Techwin, is a corporation organized under the laws of New Jersey, and is headquartered in Secaucus, New Jersey. Plaintiff alleges that Defendants have infringed on two of its licensed patents by selling infringing digital cameras. In addition to the case before the Court, Plaintiff has filed two other cases involving

(31)

infringement of the same patents, and Plaintiff is defending two additional actions involving the same patents. Pending before the United States District Court for the District of Columbia is Casio, Inc. v. Papst, Case No. 1:06cv1751 (D.D.C.) (Kessler, J.) ("Casio") and Fujifilm Corp., et al. v. Papst, Case No. 1:07cv01118 (D.D.C.) (Kessler, J.). Pending before the Northern District of Illinois is Papst v. Fujifilm Corp., et al., Case No. 07cv3401 (N.D. Ill.) (Holderman, C.J.). Finally, pending before the District of Delaware is Papst v. Olympus Corp., et al., Case No. 07cv0415 (D. Del.) (Vacant Judgeship). Plaintiff filed a motion before the Judicial Panel on Multidistrict Litigation ("MDL") to consolidate pretrial proceedings for all of these cases before a single district.[1/] Defendants then filed a motion for stay of the case before this Court pending the outcome of the motion before the MDL. On August 20, 2007, this Court granted Defendants' motion for stay. However, the Court required Defendants to respond to Papst's Complaint. Defendants filed the Motion to Transfer on September 4, 2007, and filed an answer on September 17, 2007.

Analysis

Defendants' Motion seeks transfer to the United States District Court for the District of Columbia. A court may transfer an action "to any other district where it might have been brought" "[f]or the convenience of parties and witnesses, [and] in the interest of justice." 28 U.S.C. § 1404(a). A court may transfer venue in response to a motion by either party in the case, or upon its own motion. See Muldoon v. Tropitone Furniture Co., 1 F.3d 964, 966 (9th Cir. 1993). Because a court may transfer on its own motion, this Court considers transfer to the District of New Jersey.

Transfer under Section 1404(a) is only available to districts in which the case "might have been brought" initially. Thus, the "transferee court" must have subject matter jurisdiction, venue must be proper, and the defendant must be subject to personal jurisdiction. Hoffman v. Blaski, 363 U.S. 335, 345, 80 S. Ct. 1084, 1090, 4 L. Ed. 2d 1254 (1960). The Section 1404(a) transfer analysis therefore has two steps. The Court must decide: (1) whether the district to which the moving party seeks to transfer meets the requirement of being one where the case "might have been brought"; and

---

[1/] After the motion before the MDL was filed, a sixth related case, Matsushita Elec. Indus. Co. Ltd. v. Papst, Case No. 07cv01222 (D.D.C.) (Kessler, J.), was also filed.

(2) if it does, whether transfer would serve the interests of convenience of parties and witnesses, and the "interest of justice."

A. The District of New Jersey is a Proper Forum for this Action

Any federal court has subject matter jurisdiction over this action because this case arises under federal patent law. See 28 U.S.C. §§ 1331, 1338. For the purposes of Chapter 28, "a corporation is deemed to reside in any judicial district in which it is subject to personal jurisdiction at the time the action is commenced." 28 U.S.C. § 1391(c); see also VE Holding Corp. v. Johnson Gas Appliance Co., 917 F.2d 1574, 1583 (Fed. Cir. 1990) (applying 28 U.S.C. § 1391(c) to a patent infringement case).

In the present litigation, Defendants acknowledge that they sell their cameras nationwide. (Defs.' Mot. 3.) They are therefore subject to general personal jurisdiction in every state in the United States, including New Jersey. See Asahi Metal Indus. Co. v. Sup. Crt., 480 U.S. 102, 112, 107 S. Ct. 1026, 1032, 94 L. Ed. 2d 92 (1987) (holding that a defendant's purposeful placement of its product in the stream of commerce bound for the forum state, plus additional contact such as "advertising in the forum State," or "establishing channels for providing regular advice to customers in the forum state," is sufficient "purposeful availment" to satisfy the "minimum contacts" requirement for personal jurisdiction); see also Bancroft & Masters, Inc. v. Augusta Nat'l, Inc., 223 F.3d 1082, 1086 (9th Cir. 2000) (factors the Court should consider in determining whether a party's contacts are sufficient to confer general jurisdiction include: "whether the defendant makes sales, solicits or engages in business in the state, serves the state's markets, designates an agent for service of process, holds a license, or is incorporated there") (citation omitted). Furthermore, Defendant Samsung America's principal place of business is in New Jersey. Because Defendants are subject to personal jurisdiction in New Jersey, this case could have originally been brought in the District of New Jersey.

B. The Interests of Convenience and Justice Are Served By Transfer

In analyzing the second prong of a transfer under Section 1404(a), the Court may consider several factors to determine whether the convenience and interest of justice elements are met by the proposed transfer: (1) convenience to the parties and witnesses; (2) relative ease of access to

evidence; (3) availability of compulsory process for attendance of unwilling witnesses; (4) plaintiff's choice of forum; and (5) administrative considerations. See Decker Coal Co.v Commonwealth Edison Co., 805 F.2d 834, 843 (9th Cir. 1986); see also E. & J. Gallo Winery v. F. & P. S.p.A., 899 F. Supp. 465, 466 (E.D. Cal. 1994). Additionally, "the presence of a related case in the transferee forum is a powerful reason to grant a change of venue." Blanning v. Tisch, 378 F. Supp. 1058, 1061 (E.D. Pa. 1974); see also Superior Savings Ass'n v. Bank of Dallas, 705 F. Supp. 326, 328–29 (N.D. Tex. 1989) (setting forth the "first to file" doctrine of federal comity) (citing Kerotest Mfg. Co. v. C-O-Two Fire Equip. Co., 342 U.S. 180, 183, 72 S. Ct. 219, 221, 96 L. Ed. 200 (1952)).

1. Plaintiff's Choice of Forum

Plaintiff has made clear, not only by its initial filing of its Complaint, but by its opposition to the Motion to Transfer, that it prefers to try this matter here in the Central District of California. Ordinarily, the plaintiff's choice of forum is entitled to "substantial weight." N. Acceptance Trust 1065 v. Gray, 423 F.2d 653, 654 (9th Cir. 1970). However,

> [P]laintiff's choice of forum . . . is not the final word. In judging the weight to be given such a choice, . . . consideration must be given to the extent both of the defendant's business contacts with the chosen forum and of the plaintiff's contacts, including those relating to his cause of action. If the operative facts have not occurred within the forum of original selection . . . the plaintiff's choice is entitled only to minimal consideration.

Pac. Car & Foundry Co. v. Pence, 403 F.2d 949, 954 (9th Cir. 1968) (footnotes omitted).

None of the parties in this case are California corporations, and none have their principal place of business in California. Cf. Piper Aircraft Co. v. Reyno, 454 U.S. 235, 255–56, 102 S. Ct. 252, 266, 70 L. Ed. 2d 419 (1981) (stating that a foreign plaintiff's choice of forum deserves less deference than that of a domestic plaintiff). Other than Defendants having a distribution warehouse in Rancho Dominguez, California, in which no development, design, or manufacturing takes place, Plaintiff has alleged no specific, unique contacts between the litigation and California. Therefore, although Plaintiff chose this forum, the limited nature of both parties' contact with California leads the Court to attach little weight to Plaintiff's preference. Rather, the acts of alleged infringement were precipitated by business decisions made by Defendants, at least partially, at Samsung

America's offices in New Jersey, and the allegedly infringing products are distributed nationwide. Thus, the "locus of operative facts" surrounding the patent infringement claims is centered on the East Coast, in New Jersey, and the Court finds that, if anything, this factor weighs in favor of transferring the case to New Jersey. Cf. Lencco Racing Co. v. Arctco, Inc., 953 F. Supp. 69, 71 (W.D.N.Y. 1997) (defining "operative facts surrounding the alleged infringement" to include "all the development, testing, research, production, marketing, and sales decisions").

Additionally, Defendants argue that Plaintiff's filing its action in this forum is simply an act of forum shopping. Specifically, the first filed of the suits related to this action was the Casio case filed before the District of Columbia in October of 2006. According to the docket in the Casio case, on May 31, 2007, Papst suffered an adverse ruling in a discovery dispute and was sanctioned by the Magistrate Judge. On June 15, 2007, Papst filed the case against Fujifilm Corporation, et al., in the Northern District of Illinois. On June 28, 2007, Plaintiff Papst filed the present action before this Court, and also the action against Olympus Corporation, et al., before the District of Delaware. On July 9, 2007, before answers were even filed in the latter of these two cases, Papst filed a motion before the MDL to transfer and consolidate all of these actions, plus an action filed by Fujifilm Corporation, et al., against Papst in the District of Columbia. The effect of Papst filing these suits, Defendants argue, was "to try to evade the harsh discovery sanctions handed down by the District of D.C." and "to broaden the geographic diversity of the case and make [Plaintiff's preferred forum of] the Northern District of Illinois appear to be the most convenient and central forum for the MDL panel." (Defs.' Mot. 2.) The Court finds Plaintiff's alleged reason for filing in this District — that Defendants have a distribution warehouse here — unavailing, and finds that Plaintiff's attempt at forum shopping is a reason to attach little weight to Plaintiff's choice of forum.[2/]

[2/] The Court also notes, however, that Defendants' attempt to transfer this case to the District of Columbia, where neither party is headquartered nor has a principal place of business, but where Plaintiff has already suffered an adverse discovery ruling, also appears to be an act of forum shopping.

2. **Convenience of the Parties**

Based on the location of Defendant Samsung America's principal place of business in Secaucus, New Jersey, where administrative and sales functions for the company are carried out by twenty-eight employees, the Court finds that the relevant sources of proof are more accessible from New Jersey. Those employees of Samsung America that might be deposed are in New Jersey. Defendant Samsung Techwin has its principal place of business in Seoul, Korea, and has no United States presence. While travel from Korea to this District might be marginally shorter than travel from Korea to New Jersey, extensive travel is required for either of these venues. Plaintiff, with its principal place of business in St. Georgen, Germany, also will have to travel extensively. However, New Jersey is marginally closer to Plaintiff than is Los Angeles. Based on these considerations, the Court finds that the "convenience of the parties" weighs in favor of transfer.

3. **Convenience of the Witnesses**

The third factor, "the convenience of the witnesses," is often considered the most important factor. In evaluating this factor, a court is required to look at who the likely witnesses are, what their potential testimony will be, and why such testimony is relevant or necessary. See A.J. Indus., Inc. v. U.S. Dist. Ct., 503 F.2d 384, 389 (9th Cir. 1974); Brandon Apparel Group, Inc. v. Quitman Mfg. Co. Inc., 42 F. Supp. 2d 821, 834 (N.D. Ill. 1999) ("The determination of whether a particular venue is more convenient for the witnesses should not turn on which party produces a longer witness list . . . . Rather, the court must look to the nature and quality of the witnesses' testimony with respect to the issues of the case.") (internal citation omitted) (citing Vandeveld v. Christoph, 877 F. Supp. 1160, 1168 (N.D. Ill. 1995)).

Neither party has yet demonstrated that non-party witnesses are required for this action. Therefore, this factor is less relevant in this case than it is in others. Cf. Anderson v. Thompson, 634 F. Supp. 1201, 1207 (D. Mont. 1986) ("The court must necessarily be concerned more with the inconvenience which a transfer will visit upon non-party witnesses than with the inconvenience that may result to parties."). However, to the extent that at least some of Defendants' witnesses are located in New Jersey and some of Plaintiff's witnesses are in Germany, and these witnesses will

provide material substantive testimony regarding the allegedly infringing products, this factor may weigh slightly in favor of transfer.

4. Interest of Justice

Under the final factor, the "interest of justice," courts often consider such things as the relative interests of the forum states in the litigation. Here, the Court returns again to its conclusion that efficiency and fairness militate in favor of trying this case in New Jersey. Since there is no unique contact between the Central District of California and the litigation other than the existence of Samsung America's distribution warehouse, and because neither of the Defendants nor Plaintiff are California corporations, the Central District's interest in the dispute is "considerably diminished." Asahi, 480 U.S. at 114, 107 S. Ct. at 1033.

On the other hand, Defendant Samsung America is headquartered in New Jersey, and actions associated with the alleged patent infringement occurred in New Jersey. Clearly, New Jersey has a significant interest in this dispute. See Lencco Racing, 953 F. Supp. at 71 (finding that the "preferred forum" for infringement claims is the district where defendant committed the allegedly infringing acts and where its business records are located); see also Saint-Gobain Calmar, Inc. v. Nat'l Prods. Corp., 230 F. Supp. 2d 655, 660 (E.D. Pa. 2002) ("The 'center of gravity' for [a patent infringement claim] is in the district where the alleged infringement occurred. In finding that 'center of gravity,' the district court 'ought to be as close as possible to the milieu of the infringing device and the hub of activity centered around its production.'") (quoting S.C. Johnson & Son, Inc. v. Gillette Co., 571 F. Supp. 1185, 1187–88 (N.D. Ill. 1983)).

Defendants have argued that the interests of judicial efficiency require transfer to the District of Columbia. Pending in the District of Columbia are two cases involving the very same patents. One of these cases, Casio, has been progressing for over a year, and discovery is well underway. However, both parties agree that all of the actions pending before the MDL, including the cases before the District of Columbia, involve the same patents. Assuming the MDL grants the motion to consolidate the pretrial proceedings, one court will hear all of the pretrial issues that these cases have in common. Because the majority of the issues in common will already be heard by one court during

the pretrial stage, judicial efficiency will be served even if the case before this Court is transferred to the District of New Jersey rather than the District of Columbia.

In view of the substantial weight of evidence indicating that New Jersey provides a more convenient and efficient forum than this District, the Court finds that the "interest of justice" is best served by a transfer.

Conclusion

For the foregoing reasons, transfer of venue to the District of New Jersey is appropriate in this case. The Court therefore orders the Clerk to transfer case number CV 07–4249 PA (JCx) to the United States District Court for the District of New Jersey.

IT IS SO ORDERED.

Dated: October 3, 2007

Percy Anderson
UNITED STATES DISTRICT JUDGE

AO 120 (Rev. 3/04)

SOLICITOR

TO:	REPORT ON THE
Mail Stop 8 **Director of the U.S. Patent and Trademark Office** **P.O. Box 1450** **Alexandria, VA 22313-1450**	**FILING OR DETERMINATION OF AN ACTION REGARDING A PATENT OR TRADEMARK**

JUN 29 2007

U.S. PATENT & TRADEMARK OFFICE

In Compliance with 35 U.S.C. § 290 and/or 15 U.S.C. § 1116 you are hereby advised that a court action has been filed in the U.S. District Court Delaware on the following X Patents or Trademarks:

DOCKET NO.	DATE FILED	U.S. DISTRICT COURT
07cv415	06/28/07	DISTRICT OF DELAWARE

PLAINTIFF	DEFENDANT
Papst Licensing GmbH & Co. KG	Olympus Corporation, Olympus Imaging America, Inc.

	PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1	6,470,399 B1	10/22/02	Labortechnik Tasler GmbH
2	6,895,449 B2	5/17/05	Labortechnik Tasler GmbH
3			
4			
5			

In the above—entitled case, the following patent(s)/ trademark(s) have been included:

DATE INCLUDED	INCLUDED BY ☐ Amendment ☐ Answer ☐ Cross Bill ☐ Other Pleading	
PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1		
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In the above—entitled case, the following decision has been rendered or judgement issued:

DECISION/JUDGEMENT

CLERK	(BY) DEPUTY CLERK	DATE
PETER T. DALLEO, CLERK OF COURT		6/29/07

Copy 1—Upon initiation of action, mail this copy to Director **Copy 3—Upon termination of action, mail this copy to Director**
Copy 2—Upon filing document adding patent(s), mail this copy to Director **Copy 4—Case file copy**

AO 120 (Rev. 2/99)

TO: Mail Stop 8 Director of the U.S. Patent & Trademark Office P.O. Box 1450 Alexandria, VA 22313-1450	E-filing	REPORT ON THE FILING OR DETERMINATION OF AN ACTION REGARDING A PATENT OR TRADEMARK

In Compliance with 35 § 290 and/or 15 U.S.C. § 1116 you are hereby advised that a court action has been filed in the U.S. District Court Northern District of California on the following X Patents or ☐ Trademarks:

DOCKET NO.	DATE FILED	U.S. DISTRICT COURT
CV 08-01732 JL	3/31/08	Northern District of California, San Francisco Division

PLAINTIFF	DEFENDANT
HEWLETT-PACKARD CO	PAPST LICENSING GMBH

	PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1	6,470,399		
2	6,895,449		
3			
4			
5			

In the above—entitled case, the following patent(s) have been included:

DATE INCLUDED	INCLUDED BY ☐ Amendment ☐ Answer ☐ Cross Bill ☐ Other Pleading	
PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1		
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In the above—entitled case, the following decision has been rendered or judgement issued:

DECISION/JUDGEMENT

CLERK	(BY) DEPUTY CLERK	DATE
Richard W. Wieking	Gloria Acevedo	April 2, 2008

Copy 1—Upon initiation of action, mail this copy to Commissioner Copy 3—Upon termination of action, mail this copy to Commissioner
Copy 2—Upon filing document adding patent(s), mail this copy to Commissioner Copy 4—Case file copy

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Attorneys for Plaintiff
Hewlett-Packard Company

UNITED STATES DISTRICT COURT

NORTHERN DISTRICT OF CALIFORNIA

HEWLETT-PACKARD COMPANY, a Delaware corporation, Plaintiff, v. PAPST LICENSING GMBH & CO. KG, a German company, Defendant.	Case No. **COMPLAINT FOR DECLARATORY JUDGMENT** **DEMAND FOR JURY TRIAL**

Plaintiff Hewlett-Packard Company ("HP"), for its Complaint for Declaratory Judgment against defendant Papst Licensing GmbH & Co. KG ("Papst" or "Defendant"), avers the following:

NATURE OF THE ACTION

1. This action is based on the patent laws of the United States, Title 35 of the United States Code. Defendant has asserted rights under U.S. Patent Nos. 6,470,399 ("the '399 patent)

and 6,895,449 ("the '449 patent") (collectively, "the patents-in-suit") based on certain ongoing activity by HP, and HP contends that it has the right to engage in this activity without license. True and correct copies of the patents-in-suit are attached hereto as Exhibits A and B. HP thus seeks a declaration that it does not infringe the patents-in-suit and/or that the patents-in-suit are invalid.

THE PARTIES

2. Plaintiff HP is a corporation organized under the laws of Delaware, with its headquarters at 3000 Hanover Street, Palo Alto, California.

3. On information and belief, Papst is a company existing under the laws of The Federal Republic of Germany with a place of business at Bahnofstrasse 33, 78112 St. Georgen, Germany.

JURISDICTION AND VENUE

4. This is a civil action regarding allegations of patent infringement arising under the patent laws of the United States, Title 35 of the United States Code, in which HP seeks declaratory relief under the Declaratory Judgment Act. Thus, the court has subject matter jurisdiction over this action pursuant to 28 U.S.C. §§ 1331, 1338, 2201, and 2202.

5. An actual controversy exists between HP and Defendant by virtue of Defendant's assertion of rights under the patents-in-suit based on certain ongoing activity by HP.

6. HP contends that it has a right to engage in making, using, offering to sell, and selling its products, including its digital camera products, without license from Defendant.

7. The Court has personal jurisdiction over Defendant because Defendant has established certain minimum contacts with California such that the exercise of personal jurisdiction over Defendant would not offend traditional notions of fair play and substantial justice.

8. Venue is proper in this court pursuant to 28 U.S.C. § 1391 because Defendant is an alien entity and therefore subject to suit in any district.

///

///

INTRADISTRICT ASSIGNMENT

9. This is an Intellectual Property Action subject to district-wide assignment under Local Rule 3-2(c).

FACTUAL BACKGROUND

10. HP is a leading provider of imaging and printing-related products and services, including, among other things, digital cameras.

11. On information and belief, Defendant is a patent licensing company that neither makes nor sells any products or services.

12. The '399 patent is entitled "Flexible interface for communication between a host and an analog I/O device connected to the interface regardless the type of the I/O device." The '399 patent on its face states that it issued on October 22, 2002. On its face, the '399 patent appears to have been originally assigned to Labortechnik Tasler GmbH. Defendant has asserted all right, title, and interest in the '399 patent.

13. The '449 patent is entitled "Flexible interface for communication between a host and an analog I/O device connected to the interface regardless the type of the I/O device." The '449 patent on its face states that it issued on May 17, 2005. On its face, the '449 patent appears to have been originally assigned to Labortechnik Tasler GmbH. Defendant has asserted all right, title, and interest in the '449 patent.

14. HP believes that its products, including its digital camera products, do not infringe the patents-in-suit and that the claims of the patents-in-suit are invalid. Accordingly, an actual controversy exists between HP and Defendant as to whether HP's manufacture, use or sale of its products infringes any valid and enforceable claim of the patents-in-suit. Absent a declaration of non-infringement and/or invalidity, Defendant will continue to wrongly assert the patents-in-suit against HP, and thereby cause HP irreparable harm.

FIRST CAUSE OF ACTION

(Declaratory Judgment of Non-Infringement of the '399 Patent)

15. HP hereby incorporates by reference its allegations contained in paragraphs 1 through 14 of this Complaint as though fully set forth herein.

16. Defendant contends that products imported, made, used, sold or offered for sale by HP infringe the '399 patent.

17. HP denies Defendant's contentions and alleges that HP's products do not directly or indirectly infringe the '399 patent.

18. An actual controversy thus exists between HP and Defendant as to whether the accused products infringe the '399 patent.

19. Accordingly, HP seeks and is entitled to a judgment against Defendant that it does not infringe and has not infringed, directly or indirectly, contributorily or by inducement, the '399 patent.

SECOND CAUSE OF ACTION

(Declaratory Judgment of Invalidity of the '399 Patent)

20. HP hereby incorporates by reference its allegations contained in paragraphs 1 through 14 of this Complaint as though fully set forth herein.

21. Defendant contends that the '399 patent is valid.

22. HP denies Defendant's contention and alleges that the '399 patent is invalid. The '399 patent is invalid for failure to meet at least one of the conditions of patentability specified in Title 35 of the United States Code. No claim of the '399 patent can be validly construed to cover any products imported, made, used, sold or offered for sale by HP and the alleged invention of the '399 patent is taught by, suggested by, and/or obvious in view of, the prior art.

23. An actual controversy thus exists between HP and Defendant as to whether the '399 patent is valid.

24. Accordingly, HP seeks and is entitled to a judgment against Defendant that the '399 patent is invalid.

THIRD CAUSE OF ACTION

(Declaratory Judgment of Non-Infringement of the '449 Patent)

25. HP hereby incorporates by reference its allegations contained in paragraphs 1 through 14 of this Complaint as though fully set forth herein.

///

26. Defendant contends that products imported, made, used, sold or offered for sale by HP infringe the '449 patent.

27. HP denies Defendant's contentions and alleges that HP's products do not directly or indirectly infringe the '449 patent.

28. An actual controversy thus exists between HP and Defendant as to whether the accused products infringe the '449 patent.

29. Accordingly, HP seeks and is entitled to a judgment against Defendant that it does not infringe and has not infringed, directly or indirectly, contributorily or by inducement, the '449 patent.

FOURTH CAUSE OF ACTION

(Declaratory Judgment of Invalidity of the '449 Patent)

30. HP hereby incorporates by reference its allegations contained in paragraphs 1 through 14 of this Complaint as though fully set forth herein.

31. Defendant contends that the '449 patent is valid.

32. HP denies Defendant's contention and alleges that the '449 patent is invalid. The '449 patent is invalid for failure to meet at least one of the conditions of patentability specified in Title 35 of the United States Code. No claim of the '449 patent can be validly construed to cover any products imported, made, used, sold or offered for sale by HP and the alleged invention of the '449 patent is taught by, suggested by, and/or obvious in view of, the prior art.

33. An actual controversy thus exists between HP and Defendant as to whether the '449 patent is valid.

34. Accordingly, HP seeks and is entitled to a judgment against Defendant that the '449 patent is invalid.

PRAYER FOR RELIEF

WHEREFORE, HP prays for a declaratory judgment against Defendant as follows:

A. Judgment against Defendant declaring that the '399 patent is not infringed by HP;

B. Judgment against Defendant declaring that the '399 patent is invalid;

A. Judgment against Defendant declaring that the '449 patent is not infringed by HP;

B. Judgment against Defendant declaring that the '449 patent is invalid;

C. A declaration that HP's case against Defendant is an exceptional case within the meaning of 35 U.S.C. § 285;

D. An award of costs and attorneys' fees to HP; and

E. Such other and further relief as the Court deems just and reasonable.

Dated: March 31, 2008

FENWICK & WEST LLP

By: _____
Charlene M. Morrow

Attorneys for Plaintiff
Hewlett-Packard Company

DEMAND FOR JURY TRIAL

Plaintiff HP hereby demands a trial by jury of all issues so triable.

Dated: March 31, 2008

FENWICK & WEST LLP

By: _____
Charlene M. Morrow

Attorneys for Plaintiff
Hewlett-Packard Company

07 AO 121 (6/90)

TO:	
COMMISSIONER OF PATENTS AND TRADEMARKS (USPTO) P.O. Box 1450 Alexandria, VA 22313-1450	REPORT ON THE FILING OF DETERMINATION OF AN ACTION OR APPEALREGARDING A COPYRIGHT

In compliance with the Act of July 19, 1952 (66 Stat. 814; 35 U.S.C. 290) you are hereby advised that a court action has been filed on the following patent(s) in the U.S. District Court:

DOCKET: 07-CV-3401	DATE FILED 06/15/07	UNITED STATES DISTRICT COURT, NORTHERN DISTRICT OF ILLINOIS, EASTERN DIVISION
PLAINTIFF: Papst Licensing GmbH & Co. KG		DEFENDANT: Fujifilm Corp., et al,

PATENT NO.	DATE OF PATENT	PATENTEE
#6,470,399 B1	10/22/02	Papst Licensing GmbH & Co. KG
#6,895,449 B2	05/17/05	Papst Licensing GmbH & Co. Kg

In the above-entitled case, the following patent(s) have been included:

DATE INCLUDED	INCLUDED BY [ ] Amendment [ ] Answer [ ] Cross Bill [ ] Other Pleading	
PATENT NO.	DATE OF PATENT	PATENT

In the above-entitled case, the following decision has been rendered or judgment issued:

DECISION/JUDGMENT		
CLERK MICHAEL W. DOBBINS	DEPUTY CLERK - Angela Revis	DATE: 06/20/07

IN THE UNITED STATES DISTRICT COURT
FOR THE NORTHERN DISTRICT OF ILLINOIS
EASTERN DIVISION

Papst Licensing GmbH & Co. KG
Plaintiff,

v.

FUJIFILM Corporation, FUJIFILM U.S.A., Inc.
Defendants

07cv3401
JUDGE HOLDERMAN
MAG. JUDGE ASHMAN

LOCAL RULE 3.4
NOTICE OF CLAIMS INVOLVING PATENTS

Plaintiff, Papst Licensing GmbH & Co. KG ("Papst Licensing"), by its undersigned counsel, hereby submits the following Notice of Claims Involving Patents.

Pursuant to Rule 35 U.S.C. 209:

Plaintiff, Papst Licensing is headquartered at Bahnofstrasse 33, 78112 St. Georgen, Germany.

Defendant, FUJIFILM Corporation is headquartered at 7-3, Akasaka 9-chome, Minato-Ku, Tokyo 107-0052, Japan.

Defendant, FUJIFILM U.S.A., Inc. is located at 850 Central Avenue, Hanover Park, IL 60133.

United States Patent No. 6,470,399 B1 duly and legally issued on October 22, 2002.

United States Patent No. 6,895,449 B2 duly and legally issued on May 17, 2005.

United States Patent No. 6,470,399 B1 and United States Patent No. 6,895,449 B2 identify Michael Tasler as the inventor.

Dated: June 15, 2007

Respectfully submitted,

Papst Licensing GmbH & Co. KG

Jerold B. Schnayer (ARDC No. 2495538)
John L. Ambrogi (ARDC No. 06203626)
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Email: jbschnayer@welshkatz.com
jambrogi@welshkatz.com

Attorneys for Papst Licensing GmbH & Co. KG

AO 121 (6/90)

TO:	
COMMISSIONER OF PATENTS AND TRADEMARKS (USPTO) P.O. Box 1450 Alexandria, VA 22313-1450	REPORT ON THE FILING OF DETERMINATION OF AN ACTION REGARDING A PATENT OR TRADEMARK

In compliance with 35 U.S.C. 290 and/or 15 U.S.C. 1116 you are hereby advised that a court action has been filed on the following patent(s)/trademark(s) in the U.S. District Court:

DOCKET NO.	DATE FILED	UNITED STATES DISTRICT COURT, NORTHERN DISTRICT OF ILLINOIS, EASTERN DIVISION
08cv1218	2/28/2008	

PLAINTIFFS	DEFENDANTS
Papst Licening GmbH & Co. KG	Ricoh Company, Ltd. et al

TRADEMARK NUMBER	DATE OF TRADEMARK	HOLDER OF PATENT OR TRADEMARK
6,470,399 B1	10/22/2002	**Papst Licensing GmbH & Co. KG**
6,895,449 B2	5/17/2005	**Papst Licensing GmbH & Co. KG**

In the above-entitled case, the following trademarks(s) have been included:

DATE INCLUDED	INCLUDED BY [ ] Amendment [ ] Answer [ ] Cross Bill [ ] Other Pleading	
TRADEMARK NUMBER	DATE OF TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1.		
2.		
3.		

In the above-entitled case, the following decision has been rendered or judgment issued:

DECISION/JUDGMENT		
CLERK MICHAEL W. DOBBINS	(BY) DEPUTY CLERK:	DATE: 3/3/08

AO 121 (6/90)

TO:	
COMMISSIONER OF PATENTS AND TRADEMARKS (USPTO) P.O. Box 1450 Alexandria, VA 22313-1450	REPORT ON THE FILING OF DETERMINATION OF AN ACTION OR APPEAL REGARDING A COPYRIGHT

In compliance with the Act of July 19, 1952 (66 Stat. 814; 35 U.S.C. 290) you are hereby advised that a court action has been filed on the following patent(s) in the U.S. District Court:

DOCKET 08-2510	DATE FILED 05/02/2008	UNITED STATES DISTRICT COURT, NORTHERN DISTRICT OF ILLINOIS, EASTERN DIVISION
PLAINTIFF Papst Licensing GmbH & Co. KG		DEFENDANT Nikon Corporation, Nikon Americas, Inc., Nikon, Inc.

PATENT NO.	DATE OF PATENT	PATENTEE
6,470,399 B1	10/22/2002	Papst Licensing
6,895,449 B2	5/17/2005	Papst Licensing

In the above-entitled case, the following patent(s) have been included:

DATE INCLUDED	INCLUDED BY [ ] Amendment [ ] Answer [ ] Cross Bill [ ] Other Pleading	
PATENT NO.	DATE OF PATENT	PATENT

In the above-entitled case, the following decision has been rendered or judgment issued:

DECISION/JUDGMENT		
CLERK Michael W. Dobbins	(BY) DEPUTY CLERK Kinielle Johnson	DATE 5/5/08

AO 121 (6/90)

TO:	
COMMISSIONER OF PATENTS AND TRADEMARKS (USPTO) P.O. Box 1450 Alexandria, VA 22313-1450	REPORT ON THE FILING OF DETERMINATION OF AN ACTION REGARDING A PATENT OR TRADEMARK

In compliance with 35 U.S.C. 290 and/or 15 U.S.C. 1116 you are hereby advised that a court action has been filed on the following patent(s)/trademark(s) in the U.S. District Court:

DOCKET NO.	DATE FILED	UNITED STATES DISTRICT COURT, NORTHERN DISTRICT OF ILLINOIS, EASTERN DIVISION
08cv1218	2/28/2008	
PLAINTIFFS Papst Licening GmbH & Co. KG	DEFENDANTS Ricoh Company, Ltd. et al	

TRADEMARK NUMBER	DATE OF TRADEMARK	HOLDER OF PATENT OR TRADEMARK
6,470,399 B1	10/22/2002	Papst Licensing GmbH & Co. KG
6,895,449 B2	5/17/2005	Papst Licensing GmbH & Co. KG

In the above-entitled case, the following trademarks(s) have been included:

DATE INCLUDED	INCLUDED BY [ ] Amendment [ ] Answer [ ] Cross Bill [ ] Other Pleading	
TRADEMARK NUMBER	DATE OF TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1.		
2.		
3.		

In the above-entitled case, the following decision has been rendered or judgment issued:

DECISION/JUDGMENT		
CLERK MICHAEL W. DOBBINS	(BY) ~~DEPUTY~~ CLERK:	DATE: 3/3/08

1

AO 121 (6/90)

TO:	
COMMISSIONER OF PATENTS AND TRADEMARKS (USPTO) P.O. Box 1450 Alexandria, VA 22313-1450	REPORT ON THE FILING OF DETERMINATION OF AN ACTION OR APPEAL REGARDING A COPYRIGHT

In compliance with the Act of July 19, 1952 (66 Stat. 814; 35 U.S.C. 290) you are hereby advised that a court action has been filed on the following patent(s) in the U.S. District Court:

DOCKET 08-3608	DATE FILED 06/24/2008	UNITED STATES DISTRICT COURT, NORTHERN DISTRICT OF ILLINOIS, EASTERN DIVISION
PLAINTIFF Papst Licensing GmbH & Co. KG		DEFENDANT **Sanyo Electric Co., Ltd., Sanyo North America Corporation.**

PATENT NO.	DATE OF PATENT	PATENTEE
6,470,399 B1	10/22/2002	Papst Licensing
6,895,449 B2	5/17/2005	Papst Licensing

In the above-entitled case, the following patent(s) have been included:

DATE INCLUDED	INCLUDED BY [ ] Amendment [ ] Answer [ ] Cross Bill [ ] Other Pleading	
PATENT NO.	DATE OF PATENT	PATENT

In the above-entitled case, the following decision has been rendered or judgment issued:

DECISION/JUDGMENT		
CLERK Michael W. Dobbins	(BY) DEPUTY CLERK Kinielle Johnson	DATE 6/26/08

AO 121 (6/90)

TO:	
COMMISSIONER OF PATENTS AND TRADEMARKS (USPTO) P.O. Box 1450 Alexandria, VA 22313-1450	REPORT ON THE FILING OF DETERMINATION OF AN ACTION OR APPEAL REGARDING A COPYRIGHT

In compliance with the Act of July 19, 1952 (66 Stat. 814; 35 U.S.C. 290) you are hereby advised that a court action has been filed on the following patent(s) in the U.S. District Court:

DOCKET	DATE FILED	UNITED STATES DISTRICT COURT, NORTHERN DISTRICT OF ILLINOIS, EASTERN DIVISION
08cv3627	6/25/2008	

PLAINTIFF	DEFENDANT
Papst Licensing GmbH & Co. KG	Eastman Kodak Company

PATENT NO.	DATE OF PATENT	PATENTEE
6,470,399 B1	10/22/2002	**Labortechnik Tasler GmbH**
6,895,449 B2	5/17/2005	**Labortechnik Tasler GmbH**

In the above-entitled case, the following patent(s) have been included:

DATE INCLUDED	INCLUDED BY [ ] Amendment [ ] Answer [ ] Cross Bill [ ] Other Pleading	
PATENT NO.	DATE OF PATENT	PATENT

In the above-entitled case, the following decision has been rendered or judgment issued:

DECISION/JUDGMENT

CLERK	(BY) DEPUTY CLERK	DATE
Michael W. Dobbins	TIANA DAVIS Tiana Davis	6/26/2008

AO 120 (Rev. 3/04)

TO:	REPORT ON THE FILING OR DETERMINATION OF AN ACTION REGARDING A PATENT OR TRADEMARK
Mail Stop 8 Director of the U.S. Patent and Trademark Office P.O. Box 1450 Alexandria, VA 22313-1450	

In Compliance with 35 U.S.C. § 290 and/or 15 U.S.C. § 1116 you are hereby advised that a court action has been filed in the U.S. District Court ____for the District of Columbia____ on the following X Patents or ☐ Trademarks:

DOCKET NO.	DATE FILED	U.S. DISTRICT COURT
08-612	5/16/08	FOR THE DISTRICT OF COLUMBIA

PLAINTIFF	DEFENDANT
PAPST LICENSING GmbH & Co. KG Bahnofstrasse 33, 78112 St. Georgen, Germany. Transferred from USDC -ILLINOIS NORTHERN MDL CASE **Attorney** Jerold B. Schnayer (2495538) James P. White (3001032) WELSH & KATZ, LTD. 120 South Riverside Plaza, 22nd Floor Chicago, Illinois 60606 (312) 655-1500	RICOH COMPANY, LTD., RICOH AMERICAS CORPORATION and RICOH CORPORATION, Ricoh Building, 8-13-1 Ginza Chuo-ku, Tokyo 104-8222, Japan.

	PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1	6,470,399 B1	10/22/02	Papst Licensing
2	6,895,449 B2	5/17/05	Papst Licensing
3			
4			
5			

In the above—entitled case, the following patent(s)/ trademark(s) have been included:

DATE INCLUDED	INCLUDED BY ☐ Amendment ☐ Answer ☐ Cross Bill ☐ Other Pleading	
PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1		
2		
3		
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5		

In the above—entitled case, the following decision has been rendered or judgement issued:

DECISION/JUDGEMENT

AO 120 (Rev. 3/04)

CLERK	(BY) DEPUTY CLERK	DATE
NANCY MAYER-WHITTINGTON by Joe Burgess		8/8/08

Copy 1—Upon initiation of action, mail this copy to Director Copy 3—Upon termination of action, mail this copy to Director
Copy 2—Upon filing document adding patent(s), mail this copy to Director Copy 4—Case file copy

AO 120 (Rev. 3/04)

TO:	REPORT ON THE FILING OR DETERMINATION OF AN ACTION REGARDING A PATENT OR TRADEMARK
Mail Stop 8 **Director of the U.S. Patent and Trademark Office** **P.O. Box 1450** **Alexandria, VA 22313-1450**	

In Compliance with 35 U.S.C. § 290 and/or 15 U.S.C. § 1116 you are hereby advised that a court action has been filed in the U.S. District Court for the District of Columbia on the following X Patents or ☐ Trademarks:

DOCKET NO.	DATE FILED	U.S. DISTRICT COURT
08-865	5/20/08	FOR THE DISTRICT OF COLUMBIA

PLAINTIFF	DEFENDANT
HEWLETT PACKARD COMPANY 3000 Hanover Street Palo Alto, CA Transferred from USDC -CALIFORNIA NORTHERN MDL CASE represented by **Charlene Marie Morrow** FENWICK & WEST, LLP Silicon Valley Center 801 California Street Mountain View, CA 94041-2008 (650) 988-8500 Fax: (650) 938-5200	**PAPST LICENSING GmbH & Co. KG** **Bahnofstrasse 33, 78112 St.** **Georgen, Germany.**

	PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1	6,470,399	10/22/02	Papst Licensing
2	6,895,449	5/17/05	Papst Licensing
3			
4			
5			

In the above—entitled case, the following patent(s)/ trademark(s) have been included:

DATE INCLUDED INCLUDED BY ☐ Amendment ☐ Answer ☐ Cross Bill ☐ Other Pleading

	PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1			
2			
3			
4			
5			

In the above—entitled case, the following decision has been rendered or judgement issued:

DECISION/JUDGEMENT

AO 120 (Rev. 3/04)

CLERK NANCY MAYER-WHITTINGTON by Joe Burgess	(BY) DEPUTY CLERK	DATE 8/8/08

Copy 1—Upon initiation of action, mail this copy to Director **Copy 3—Upon termination of action, mail this copy to Director**
Copy 2—Upon filing document adding patent(s), mail this copy to Director **Copy 4—Case file copy**

PTO/SB/82 (01-06)
Approved for use through 12/31/2008. OMB 0651-0035
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

REVOCATION OF POWER OF ATTORNEY WITH NEW POWER OF ATTORNEY AND CHANGE OF CORRESPONDENCE ADDRESS		
	Patent Number	6,470,399
	Application Number	09/331,002
	Filing Date	June 14, 1999
	First Named Inventor	Michael Tasler
	Art Unit	2185
	Examiner Name	Thuan N. Du
	Attorney Docket Number	

I hereby revoke all previous powers of attorney given in the above-identified application.

☐ A Power of Attorney is submitted herewith.

OR

☒ I hereby appoint the practitioners associated with the Customer Number: 04743

☐ Please change the correspondence address for the above-identified application to:

☐ The address associated with Customer Number: ____

OR

☒ Firm or Individual Name	Jeffrey W. Salmon, Esq.				
Address	Marshall, Gerstein & Borun LLP 233, South Wacker Drive, Suite 6300				
City	Chicago				
Country	United States	State	Illinois	Zip	60606
Telephone	312-474-6300	Email	jsalmon@marshallip.com		

I am the:

☐ Applicant/Inventor.

☒ Assignee of record of the entire interest. See 37 CFR 3.71.
Statement under 37 CFR 3.73(b) is enclosed. (Form PTO/SB/96)

SIGNATURE of Applicant or Assignee of Record

Signature	D. Papst		
Name	Daniel Papst, Patent Counsel		
Date	08/14/2008	Telephone	312-423-3450

NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required. Submit multiple forms if more than one signature is required, see below*.

☐ *Total of ____ forms are submitted.

PTO/SB/82 (01-06)
Approved for use through 12/31/2008. OMB 0651-0035
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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REVOCATION OF POWER OF ATTORNEY WITH NEW POWER OF ATTORNEY AND CHANGE OF CORRESPONDENCE ADDRESS

Patent Number	6,470,399
Application Number	09/331,002
Filing Date	June 14, 1999
First Named Inventor	Michael Tasler
Art Unit	2185
Examiner Name	Thuan N. Du
Attorney Docket Number	

I hereby revoke all previous powers of attorney given in the above-identified application.

☐ A Power of Attorney is submitted herewith.

OR

☒ I hereby appoint the practitioners associated with the Customer Number: 04743

☐ Please change the correspondence address for the above-identified application to:

☐ The address associated with Customer Number:

OR

☒ Firm *or* Individual Name	Jeffrey W. Salmon, Esq.				
Address	Marshall, Gerstein & Borun LLP 233, South Wacker Drive, Suite 6300				
City	Chicago				
Country	United States	State	Illinois	Zip	60606
Telephone	312-474-6300	Email	jsalmon@marshallip.com		

I am the:

☐ Applicant/Inventor.

☒ Assignee of record of the entire interest. See 37 CFR 3.71.
Statement under 37 CFR 3.73(b) is enclosed. (Form PTO/SB/96)

SIGNATURE of Applicant or Assignee of Record

Signature	D. Papst		
Name	Daniel Papst, Patent Counsel		
Date	08/14/2008	Telephone	312-423-3450

NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required. Submit multiple forms if more than one signature is required, see below*.

☐ *Total of _____ forms are submitted.

PTO/SB/82 (01-06)
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REVOCATION OF POWER OF ATTORNEY WITH NEW POWER OF ATTORNEY AND CHANGE OF CORRESPONDENCE ADDRESS		
	Patent Number	6,470,399
	Application Number	09/331,002
	Filing Date	June 14, 1999
	First Named Inventor	Michael Tasler
	Art Unit	2185
	Examiner Name	Thuan N. Du
	Attorney Docket Number	

I hereby revoke all previous powers of attorney given in the above-identified application.

☐ A Power of Attorney is submitted herewith.

OR

☒ I hereby appoint the practitioners associated with the Customer Number: 04743

☐ Please change the correspondence address for the above-identified application to:

☐ The address associated with Customer Number:

OR

☒ Firm or Individual Name	Jeffrey W. Salmon, Esq.				
Address	Marshall, Gerstein & Borun LLP 233, South Wacker Drive, Suite 6300				
City	Chicago				
Country	United States	State	Illinois	Zip	60606
Telephone	312-474-6300	Email	jsalmon@marshallip.com		

I am the:

☐ Applicant/Inventor.

☒ Assignee of record of the entire interest. See 37 CFR 3.71.
Statement under 37 CFR 3.73(b) is enclosed. (Form PTO/SB/96)

SIGNATURE of Applicant or Assignee of Record

Signature	D. Papst		
Name	Daniel Papst, Patent Counsel		
Date	08/14/2008	Telephone	312-423-3450

NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required. Submit multiple forms if more than one signature is required, see below*.

☐ *Total of _____ forms are submitted.

Electronic Acknowledgement Receipt	
EFS ID:	4349281
Application Number:	09331002
International Application Number:	
Confirmation Number:	1117
Title of Invention:	FLEXIBLE INTERFACE FOR COMMUNICATION BETWEEN A HOST AND AN ANALOG I/O DEVICE CONNTECTED TO THE INTERFACE REGARDLESS THE TYPE OF THE I/O DEVICE
First Named Inventor/Applicant Name:	MICHAEL TASLER
Correspondence Address:	Jeffrey W Salmon Esq Welsh & Katz Ltd 120 S Riverside Plaza 22nd Floor - Chicago IL 60606 US 312-655-1500 jwsalmon@welshkatz.com
Filer:	Jeffrey W. Salmon
Filer Authorized By:	
Attorney Docket Number:	9576/96909
Receipt Date:	25-NOV-2008
Filing Date:	14-JUN-1999
Time Stamp:	10:27:56
Application Type:	U.S. National Stage under 35 USC 371

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Power of Attorney	RevocationofPOA.PDF	93186 79ee48a67c1a42c517f3b68983d9cc8461580b74	no	1
Warnings:					
Information:					
2	Assignee showing of ownership per 37 CFR 3.73(b).	Statement373b.PDF	92640 1eb8828981825786b66fdb3a90547277e417ea7fc	no	1
Warnings:					
Information:					
		Total Files Size (in bytes):	185826		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PTO/SB/96 (01-08)
Approved for use through 06/30/2008. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

STATEMENT UNDER 37 CFR 3.73(b)

Patent Owner: Papst Licensing GmbH & Co. KG

Application No.: 09/331,002 Filed: June 14, 1999

Entitled: Flexible Interface For Communication Between A Host And An Analog I/O Device Connected To The Interface Regardless The Type Of The I/O Device

Papst Licensing GmbH & Co. KG (Name of Assignee) , a German Corporation (Type of Assignee, e.g., corporation, partnership, university, government agency, etc.)

states that it is:

1. [x] the assignee of the entire right, title, and interest; or

2. [ ] an assignee of less than the entire right, title and interest.
(The extent (by percentage) of its ownership interest is _____ %)

in the patent application/patent identified above by virtue of either:

A. [ ] An assignment from the inventor(s) of the patent application/patent identified above. The assignment was recorded in the United States Patent and Trademark Office at Reel _____, Frame _____, or for which a copy thereof is attached.

OR

B. [X] A chain of title from the inventor(s), of the patent application/patent identified above, to the current assignee as follows:

1. From: Michael Tasler To: Labortechnik Tasler GmbH
The document was recorded in the United States Patent and Trademark Office at
Reel 012023, Frame 0515, or for which a copy thereof is attached.

2. From: Labortechnik Tasler GmbH To: Papst Licensing GmbH & Co. KG
The document was recorded in the United States Patent and Trademark Office at
Reel 07314, Frame 0114, or for which a copy thereof is attached.

[ ] Additional documents in the chain of title are listed on a supplemental sheet.

[x] As required by 37 CFR 3.73(b)(1)(i), the documentary evidence of the chain of title from the original owner to the assignee was, or concurrently is being, submitted for recordation pursuant to 37 CFR 3.11.

[NOTE: A separate copy (*i.e.*, a true copy of the original assignment document(s)) must be submitted to Assignment Division in accordance with 37 CFR Part 3, to record the assignment in the records of the USPTO. See MPEP 302.08]

The undersigned (whose title is supplied below) is authorized to act on behalf of the assignee.

D. Papst — Signature

08/19/2008 — Date

Daniel Papst — Printed or Typed Name

312-425-3450 — Telephone Number

Patent Counsel — Title

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
09/331,002	06/14/1999	MICHAEL TASLER	9576/96909

CONFIRMATION NO. 1117

POWER OF ATTORNEY NOTICE

Jeffrey W Salmon Esq
Welsh & Katz Ltd
120 S Riverside Plaza 22nd Floor
Chicago, IL 60606

OC000000033447172

Date Mailed: 12/04/2008

NOTICE REGARDING CHANGE OF POWER OF ATTORNEY

This is in response to the Power of Attorney filed 11/25/2008.

- The Power of Attorney to you in this application has been revoked by the assignee who has intervened as provided by 37 CFR 3.71. Future correspondence will be mailed to the new address of record(37 CFR 1.33).

/dtvernon/

Office of Data Management, Application Assistance Unit (571) 272-4000, or (571) 272-4200, or 1-888-786-0101

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
09/331,002	06/14/1999	MICHAEL TASLER	9576/96909

CONFIRMATION NO. 1117

POA ACCEPTANCE LETTER

4743
MARSHALL, GERSTEIN & BORUN LLP
233 S. WACKER DRIVE, SUITE 6300
SEARS TOWER
CHICAGO, IL 60606

OC000000033447244

Date Mailed: 12/04/2008

NOTICE OF ACCEPTANCE OF POWER OF ATTORNEY

This is in response to the Power of Attorney filed 11/25/2008.

The Power of Attorney in this application is accepted. Correspondence in this application will be mailed to the above address as provided by 37 CFR 1.33.

/dtvernon/

Office of Data Management, Application Assistance Unit (571) 272-4000, or (571) 272-4200, or 1-888-786-0101

I hereby certify that this paper (along with any paper referred to as being attached or enclosed) is being transmitted via the Office electronic filing system in accordance with § 1.6(a)(4).

Dated: March 23, 2009 Signature: _____ (Jeffrey W. Salmon)

Docket No.: 31436/43543
(PATENT)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:
Michael Tasler

Application No.: 09/331,002

Confirmation No.: 1117

Filed: June 14, 1999

Art Unit: 2185

For: Flexible Interface For Communication Between A Host And An Analog I/O Device Connected To The Interface Regardless The Type Of The I/O Device

Examiner: Thuan N. Du

NOTICE OF LOSS OF RIGHT TO CLAIM SMALL ENTITY STATUS

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

When the instant application was filed on June 14, 1999, small entity status was claimed. By means of an assignment document that was executed on June 15, 2001, at reel/frame 07314/0114, Papst Licensing GmbH & Co. KG received full title to the above-noted application.

Since Papst Licensing is not entitled to claim small entity status in connection with its patent prosecution endeavors, all of the fees paid during the prosecution of the instant application by the undersigned attorney on or after March 8, 2006, were "large entity" fees.

However, no paper was filed in the USPTO to formally notify the USPTO that the previous claim of small entity status should be revoked.

The purpose of this paper is to request that the USPTO update its records to reflect the fact that, small entity status is no longer claimed in the instant application.

Dated: March 23, 2009

Respectfully submitted,

By _____
Jeffrey W. Salmon
Registration No.: 37,435
MARSHALL, GERSTEIN & BORUN LLP
233 S. Wacker Drive, Suite 6300
Sears Tower
Chicago, Illinois 60606-6357
(312) 474-6300
Attorney for Applicant

Electronic Acknowledgement Receipt	
EFS ID:	5012800
Application Number:	09331002
International Application Number:	
Confirmation Number:	1117
Title of Invention:	FLEXIBLE INTERFACE FOR COMMUNICATION BETWEEN A HOST AND AN ANALOG I/O DEVICE CONNTECTED TO THE INTERFACE REGARDLESS THE TYPE OF THE I/O DEVICE
First Named Inventor/Applicant Name:	MICHAEL TASLER
Customer Number:	23368
Filer:	Jeffrey W. Salmon/zyneene williams
Filer Authorized By:	Jeffrey W. Salmon
Attorney Docket Number:	9576/96909
Receipt Date:	23-MAR-2009
Filing Date:	14-JUN-1999
Time Stamp:	12:53:41
Application Type:	U.S. National Stage under 35 USC 371

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Miscellaneous Incoming Letter	3143643543NoticeofLossSmall Entity.PDF	76568 8b0cb6245ede541c78f5e006a2d570626832cdd6	no	2
Warnings:					
Information:					

Total Files Size (in bytes):	76568

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
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UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
09/331,002	06/14/1999	MICHAEL TASLER	9576/96909

CONFIRMATION NO. 1117

POA ACCEPTANCE LETTER

23368
DINSMORE & SHOHL LLP
ONE DAYTON CENTRE, ONE SOUTH MAIN STREET
SUITE 1300
DAYTON, OH 45402-2023

OC000000033456612

Date Mailed: 04/08/2009

NOTICE OF ACCEPTANCE OF POWER OF ATTORNEY

This is in response to the Power of Attorney filed 12/02/2008.

The Power of Attorney in this application is accepted. Correspondence in this application will be mailed to the above address as provided by 37 CFR 1.33.

/dtvernon/

Office of Data Management, Application Assistance Unit (571) 272-4000, or (571) 272-4200, or 1-888-786-0101

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
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www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
09/331,002	06/14/1999	MICHAEL TASLER	9576/96909

CONFIRMATION NO. 1117

POWER OF ATTORNEY NOTICE

4743
MARSHALL, GERSTEIN & BORUN LLP
233 S. WACKER DRIVE, SUITE 6300
SEARS TOWER
CHICAGO, IL 60606

OC000000033456580

Date Mailed: 04/08/2009

NOTICE REGARDING CHANGE OF POWER OF ATTORNEY

This is in response to the Power of Attorney filed 12/02/2008.

- The Power of Attorney to you in this application has been revoked by the assignee who has intervened as provided by 37 CFR 3.71. Future correspondence will be mailed to the new address of record(37 CFR 1.33).

/dtvernon/

Office of Data Management, Application Assistance Unit (571) 272-4000, or (571) 272-4200, or 1-888-786-0101

AO 120 (Rev. 3/04)

TO:	REPORT ON THE FILING OR DETERMINATION OF AN ACTION REGARDING A PATENT OR TRADEMARK
Mail Stop 8 Director of the U.S. Patent and Trademark Office P.O. Box 1450 Alexandria, VA 22313-1450	

In Compliance with 35 U.S.C. § 290 and/or 15 U.S.C. § 1116 you are hereby advised that a court action has been filed in the U.S. District Court OF COLUMBIA on the following X Patents or ☐ Trademarks:

DOCKET NO.	DATE FILED	U.S. DISTRICT COURT
08cv1404	8/13/08	for the District of Columbia

PLAINTIFF	DEFENDANT
Papst Licensing GmbH & Co. KG Bahnofstrasse 33, 78112 St. Georgen, Germany.	Konica-Minolta, Marunouchi Center Building, 1-6-1 Marunouchi, Chiyoda-ku, Tokyo, Japan.

	PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1	6,470,399 B1	10/22/02	PAPST LICENSING
2	6,895,449 B2	5/17/05	PAPST LICENSING
3			
4			
5			

In the above—entitled case, the following patent(s)/ trademark(s) have been included:

DATE INCLUDED	INCLUDED BY ☐ Amendment ☐ Answer ☐ Cross Bill ☐ Other Pleading	
PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1		
2		
3		
4		
5		

In the above—entitled case, the following decision has been rendered or judgement issued:

DECISION/JUDGEMENT
On 3/26/09 -ORDER granting the motion for judgment on the pleadings filed by Konica Minolta Business Solutions USA Inc. as docket no. 256 in Misc. No. 07-493. This case is dismissed and closed. Signed by Judge Rosemary M. Collyer on 3/26/09. (KD) (Entered: 03/26/2009)

2.

CLERK	(BY) DEPUTY CLERK	DATE
Nancy Mayer-Whittington, Clerk by Joe Burgess		5/11/09

Copy 1—Upon initiation of action, mail this copy to Director Copy 3—Upon termination of action, mail this copy to Director
Copy 2—Upon filing document adding patent(s), mail this copy to Director Copy 4—Case file copy

AO 120 (Rev. 3/04)

TO:	REPORT ON THE FILING OR DETERMINATION OF AN ACTION REGARDING A PATENT OR TRADEMARK
Mail Stop 8 Director of the U.S. Patent and Trademark Office P.O. Box 1450 Alexandria, VA 22313-1450	

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DOCKET NO.	DATE FILED	U.S. DISTRICT COURT
08cv1405	8/13/08	for the District of Columbia

PLAINTIFF	DEFENDANT
PAPST LICENSING GmbH & Co. KG Bahnofstrasse 33, 78112 St. Georgen, Germany.	Sanyo Electric Co., Ltd., Sanyo North America Corporation,5-5, Keihan-Hondori 2-Chome, Moriguchi City, Osaka 570-8677, Japan.

	PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1	6,470,399 B1	10/22/02	PAPST LICENSING
2	6,895,449 B2	5/17/05	PAPST LICENSING
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4			
5			

In the above—entitled case, the following patent(s)/ trademark(s) have been included:

DATE INCLUDED	INCLUDED BY ☐ Amendment ☐ Answer ☐ Cross Bill ☐ Other Pleading	
	PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
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In the above—entitled case, the following decision has been rendered or judgement issued:

DECISION/JUDGEMENT
On 11/2/08 Order granting the Motion to Dismiss, docket 223 in miscellaneous case 07-493, filed by Sanyo Electric Co., Ltd. and Sanyo North America Corp. This case is dismissed and closed. Signed by Judge Rosemary M. Collyer on 11/12/08. (KD) (Entered: 11/12/2008)

2.

CLERK	(BY) DEPUTY CLERK	DATE
Nancy Mayer-Whittington, Clerk by Joe Burgess		5/11/09

Copy 1—Upon initiation of action, mail this copy to Director Copy 3—Upon termination of action, mail this copy to Director
Copy 2—Upon filing document adding patent(s), mail this copy to Director Copy 4—Case file copy

AO 120 (Rev. 3/04)

TO:	REPORT ON THE FILING OR DETERMINATION OF AN ACTION REGARDING A PATENT OR TRADEMARK
Mail Stop 8 Director of the U.S. Patent and Trademark Office P.O. Box 1450 Alexandria, VA 22313-1450	

In Compliance with 35 U.S.C. § 290 and/or 15 U.S.C. § 1116 you are hereby advised that a court action has been filed in the U.S. District Court for the District of Columbia on the following ☑ Patents or ☐ Trademarks:

DOCKET NO.	DATE FILED	U.S. DISTRICT COURT
06cv1751	10/16/2006	for the District of Columbia

PLAINTIFF	DEFENDANT
CASIO AMERICA, INC. 570 Mount Pleasant Ave. Dover, NJ 07801	PAPST LICENSING GMBH & CO. KG Bahnhofstr, 33 78112 St. Georgen, Germany

	PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1	6,895,449		PAPST LICENSING GMBH & CO. KG
2	6,470,399		PAPST LICENSING GMBH & CO. KG
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In the above—entitled case, the following patent(s)/ trademark(s) have been included:

DATE INCLUDED	INCLUDED BY ☐ Amendment ☐ Answer ☐ Cross Bill ☐ Other Pleading	
PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
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In the above—entitled case, the following decision has been rendered or judgement issued:

DECISION/JUDGEMENT
09/11/2008 MINUTE ORDER approving 86 the parties' joint stipulation of dismissal with prejudice. This case is dismissed and closed. Signed by Judge Rosemary M. Collyer on 9/11/08. (KD) (Entered: 09/11/2008)

CLERK	(BY) DEPUTY CLERK	DATE
Greg Hughes, Interim Clerk	/s/ Nicole Wilkens	1/11/2010

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Copy 2—Upon filing document adding patent(s), mail this copy to Director **Copy 4—Case file copy**

AO 120 (Rev. 3/04)

TO:	REPORT ON THE FILING OR DETERMINATION OF AN ACTION REGARDING A PATENT OR TRADEMARK
Mail Stop 8 Director of the U.S. Patent and Trademark Office P.O. Box 1450 Alexandria, VA 22313-1450	

In Compliance with 35 U.S.C. § 290 and/or 15 U.S.C. § 1116 you are hereby advised that a court action has been filed in the U.S. District Court for the District of Columbia on the following ☑ Patents or ☐ Trademarks:

DOCKET NO.	DATE FILED	U.S. DISTRICT COURT
06cv1751	10/16/2006	for the District of Columbia

PLAINTIFF	DEFENDANT
CASIO AMERICA, INC. 570 Mount Pleasant Ave. Dover, NJ 07801	PAPST LICENSING GMBH & CO. KG Bahnhofstr, 33 78112 St. Georgen, Germany

	PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1	6,895,449		PAPST LICENSING GMBH & CO. KG
2	6,470,399		PAPST LICENSING GMBH & CO. KG
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In the above—entitled case, the following patent(s)/ trademark(s) have been included:

DATE INCLUDED	INCLUDED BY ☐ Amendment ☐ Answer ☐ Cross Bill ☐ Other Pleading	
PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
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In the above—entitled case, the following decision has been rendered or judgement issued:

DECISION/JUDGEMENT
09/11/2008 MINUTE ORDER approving 86 the parties' joint stipulation of dismissal with prejudice. This case is dismissed and closed. Signed by Judge Rosemary M. Collyer on 9/11/08. (KD) (Entered: 09/11/2008)

CLERK	(BY) DEPUTY CLERK	DATE
Greg Hughes, Interim Clerk	/s/ Nicole Wilkens	1/11/2010

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AO 120 (Rev. 3/04)

TO:	REPORT ON THE FILING OR DETERMINATION OF AN ACTION REGARDING A PATENT OR TRADEMARK
Mail Stop 8 Director of the U.S. Patent and Trademark Office P.O. Box 1450 Alexandria, VA 22313-1450	

In Compliance with 35 U.S.C. § 290 and/or 15 U.S.C. § 1116 you are hereby advised that a court action has been filed in the U.S. District Court for the District of Columbia on the following ☑ Patents or ☐ Trademarks:

DOCKET NO.	DATE FILED	U.S. DISTRICT COURT
08cv1433	8/18/2008	for the District of Columbia

PLAINTIFF	DEFENDANT
KONICA-MINOLTA PHOTO IMAGING, INC. 1 Sakura-machi, Hino-shi Tokyo 191-8511, Japan	PAPST LICENSING GMBH & CO. KG Bahnhofstrasse 33 78112 St. Georgen, Germany

	PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1	6,470,399 B1	10/22/2002	PAPST LICENSING GMBH & CO. KG
2	6,895,499 B2	5/17/2005	PAPST LICENSING GMBH & CO. KG
3			
4			
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In the above—entitled case, the following patent(s)/ trademark(s) have been included:

DATE INCLUDED	INCLUDED BY ☐ Amendment ☐ Answer ☐ Cross Bill ☐ Other Pleading	
PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
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In the above—entitled case, the following decision has been rendered or judgement issued:

DECISION/JUDGEMENT
06/26/2009 MINUTE ORDER approving the stipulation of dismissal filed in the MDL Master Docket 07-MC-493 by Papst Licensing GmbH & Co., joined by Konica Minolta Photo Imaging, Inc. (KMPI) and Konica Minolta Photo Imaging USA, Inc. (KMPUS). All of KMPI's claims against Papst are dismissed without prejudice, and Papst's counterclaims against KMPI and KMPUS are dismissed with prejudice. This case, 08-cv-1433, is dismissed and closed. Signed by Judge Rosemary M. Collyer on 6/26/09. (KD) (Entered: 06/26/2009)

CLERK	(BY) DEPUTY CLERK	DATE
Greg Hughes, Interim Clerk	/s/ Nicole Wilkens	2/12/2010

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AO 120 (Rev. 08/10)

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Mail Stop 8 Director of the U.S. Patent and Trademark Office P.O. Box 1450 Alexandria, VA 22313-1450	

In Compliance with 35 U.S.C. § 290 and/or 15 U.S.C. § 1116 you are hereby advised that a court action has been filed in the U.S. District Court for the Distict of Columbia on the following

☐ Trademarks or ☑ Patents. (☐ the patent action involves 35 U.S.C. § 292.):

DOCKET NO.	DATE FILED	U.S. DISTRICT COURT
08cv1407	8/13/2008	for the Distict of Columbia

PLAINTIFF	DEFENDANT
PAPST LICENSING GMBH & CO. KG Bahnofstrasse 33, 78112 St. Georgen, Germnay	EASTMAN KODAK COMPANY 343 State Street Rochester, NY 14650

	PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1	6,470,399 B1	10/22/2002	PAPST LICENSING
2	6,895,449 B2	5/17/2005	PAPST LICENSING
3			
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In the above—entitled case, the following patent(s)/ trademark(s) have been included:

DATE INCLUDED	INCLUDED BY ☐ Amendment ☐ Answer ☐ Cross Bill ☐ Other Pleading	
PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1		
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In the above—entitled case, the following decision has been rendered or judgement issued:

DECISION/JUDGEMENT

09/18/2013 view MINUTE ORDER approving 544 filed in MDL Master Docket 07-mc-743, notice of voluntary dismissal with prejudice. All claims and counterclaims in Civil Case No. 08-cv-1407 are hereby dismissed with prejudice, with each party to bear its own costs and attorney fees, and this case is closed. Signed by Judge Rosemary M. Collyer on 9/18/2013. (KD) (Entered: 09/18/2013)

CLERK	(BY) DEPUTY CLERK	DATE
Angela D. Caesar	/s/ Nicole M. Wilkens	9/19/2013

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PATENT APPLICATION FEE DETERMINATION RECORD

Effective November 10, 1998

Application or Docket Number: 09/331,002

CLAIMS AS FILED - PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA
BASIC FEE		
TOTAL CLAIMS	16 minus 20=	*
INDEPENDENT CLAIMS	3 minus 3 =	*
MULTIPLE DEPENDENT CLAIM PRESENT		

* If the difference in column 1 is less than zero, enter "0" in column 2

SMALL ENTITY TYPE ☐		OR	OTHER THAN SMALL ENTITY	
RATE	FEE		RATE	FEE
	380.00	OR	420	~~760.00~~
X$ 9=		OR	X$18=	
X39=		OR	X78=	
+130=		OR	+260=	
TOTAL		OR	TOTAL	420

CLAIMS AS AMENDED - PART II

AMENDMENT A

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA
Total	*	Minus	**	=
Independent	*	Minus	***	=
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM				

SMALL ENTITY		OR	OTHER THAN SMALL ENTITY	
RATE	ADDITIONAL FEE		RATE	ADDITIONAL FEE
X$ 9=		OR	X$18=	
X39=		OR	X78=	
+130=		OR	+260=	
TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	

AMENDMENT B

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA
Total	*	Minus	**	=
Independent	*	Minus	***	=
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM				

RATE	ADDITIONAL FEE		RATE	ADDITIONAL FEE
X$ 9=		OR	X$18=	
X39=		OR	X78=	
+130=		OR	+260=	
TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	

AMENDMENT C

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA
Total	*	Minus	**	=
Independent	*	Minus	***	=
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM				

RATE	ADDITIONAL FEE		RATE	ADDITIONAL FEE
X$ 9=		OR	X$18=	
X39=		OR	X78=	
+130=		OR	+260=	
TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20."
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3."
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

MULTIPLE DEPENDENT CLAIM FEE CALCULATION SHEET

(FOR USE WITH FORM PTO-875)

SERIAL NO. 09/331,002 | FILING DATE

APPLICANT(S)

CLAIMS

	AS FILED		AFTER 1st AMENDMENT		AFTER 2nd AMENDMENT	
	IND.	DEP.	IND.	DEP.	IND.	DEP.
1	1					
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7		1 (A)				
8		(A) 1				
9		1 (A)				
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U.S. DEPARTMENT of COMMERCE
Patent and Trademark Office

Form PTO 1130
(REV 2/94)

U.S. DEPARTMENT OF COMMERCE
Patent and Trademark Office

PACE DATA ENTRY CODING SHEET

1ST EXAMINER	DATE
2ND EXAMINER	DATE

APPLICATION NUMBER	TYPE APPL	FILING DATE (MONTH DAY YEAR)	SPECIAL HANDLING	GROUP ART UNIT	CLASS	SHEETS OF DRAWING
09/331002	1	06 14 99	0	2742	710	002

TOTAL CLAIMS	INDEPENDENT CLAIMS	SMALL ENTITY?	FILING FEE	FOREIGN LICENSE	ATTORNEY DOCKET NUMBER
016	003	1	0420	Y	2055/1011

CONTINUITY DATA

CONT CODE	STATUS CODE	PARENT APPLICATION SERIAL NUMBER	PCT APPLICATION SERIAL NUMBER	PARENT PATENT NUMBER	PARENT FILING DATE (MONTH DAY YEAR)
			PCT/		
			PCT/		
			PCT/		
			PCT/		
			PCT/		

PCT/FOREIGN APPLICATION DATA

FOREIGN PRIORITY CLAIMED	COUNTRY CODE	PCT/FOREIGN APPLICATION SERIAL NUMBER	FOREIGN FILING DATE (MONTH DAY YEAR)
Y	DEX	19708755.8	03 04 97

338

ISSUE SLIP STAPLE AREA (for additional cross references)

POSITION	INITIALS	ID NO.	DATE
FEE DETERMINATION			
O.I.P.E. CLASSIFIER		25	06-25-09
FORMALITY REVIEW			

INDEX OF CLAIMS

✔	..... Rejected	N	..... Non-elected
=	..... Allowed	I	..... Interference
—	(Through numeral)... Canceled	A	..... Appeal
÷	..... Restricted	O	..... Objected

Claim		Date
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Claim		Date
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If more than 150 claims or 10 actions staple additional sheet here

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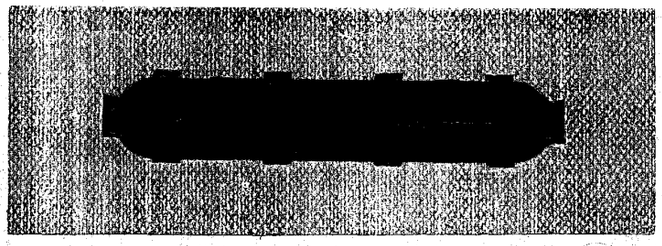

SEARCHED

Class	Sub.	Date	Exmr.
710	15 16 11 12 62 63 64	12/05/01	TD
703	23 24 25		
Search updated		5/14/02	TD
710	11 12 15 16 62 63 64		
703	23 24 25		

INTERFERENCE SEARCHED

Class	Sub.	Date	Exmr.
710	15 16 62 63 64	5/15/02	TD
703	23 24 25		

SEARCH NOTES
(INCLUDING SEARCH STRATEGY)

	Date	Exmr.
EAST	12/05/01	TD
EAST	5/14/02	TD

(RIGHT OUTSIDE)

US006470399B1

(12) **United States Patent**
Tasler

(10) **Patent No.: US 6,470,399 B1**
(45) **Date of Patent: Oct. 22, 2002**

(54) **FLEXIBLE INTERFACE FOR COMMUNICATION BETWEEN A HOST AND AN ANALOG I/O DEVICE CONNECTED TO THE INTERFACE REGARDLESS THE TYPE OF THE I/O DEVICE**

(75) Inventor: **Michael Tasler**, Würzburg (DE)

(73) Assignee: **Labortechnik Tasler GmbH**, Wuerzburg (DE)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **09/331,002**

(22) PCT Filed: **Mar. 3, 1998**

(86) PCT No.: **PCT/EP98/01187**

§ 371 (c)(1),
(2), (4) Date: **Jun. 14, 1999**

(87) PCT Pub. No.: **WO98/39710**

PCT Pub. Date: **Sep. 11, 1998**

(30) **Foreign Application Priority Data**

Mar. 4, 1997 (DE) 197 08 755

(51) **Int. Cl.**[7] **G06F 13/14**
(52) **U.S. Cl.** **710/16**; 710/62; 710/63
(58) **Field of Search** 710/15, 16, 11, 710/12, 62, 63, 64; 703/23, 24, 25

(56) **References Cited**

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WO	WO94/19746		9/1994

OTHER PUBLICATIONS

Steve Martin, "PC–based Data Acquisition in an Industrial Environment," pp. 1–3 (1990).
Payne et al., "High Speed PC–based Data Acquisition Systems," IEEE, pp. 2140–2145 (1995).
National Instruments Corporation, "Dynamic Signal Acquisition and DSP Board for the PC AT," IEEE 488 and VXIbus Control, Data Acquuisition, and Analysis, pp. 3–118–3–123, (1994).
IBM Corporation, "Communication Method between Devices through FDD Interface," IBM Technical Disclosure Bulletin, vol. 38 (No. 05), p. 245 (May, 1995).

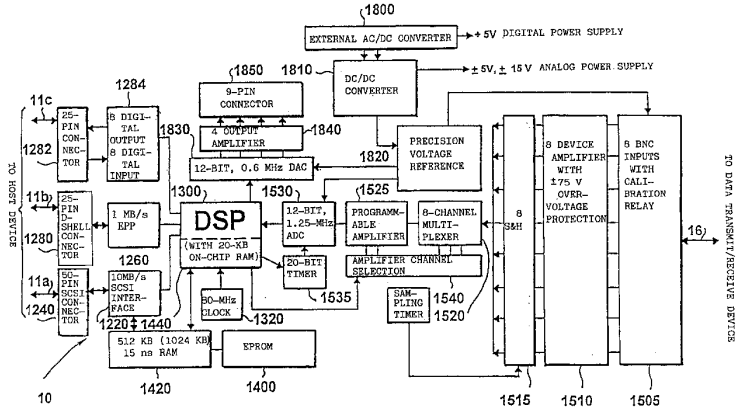
* cited by examiner

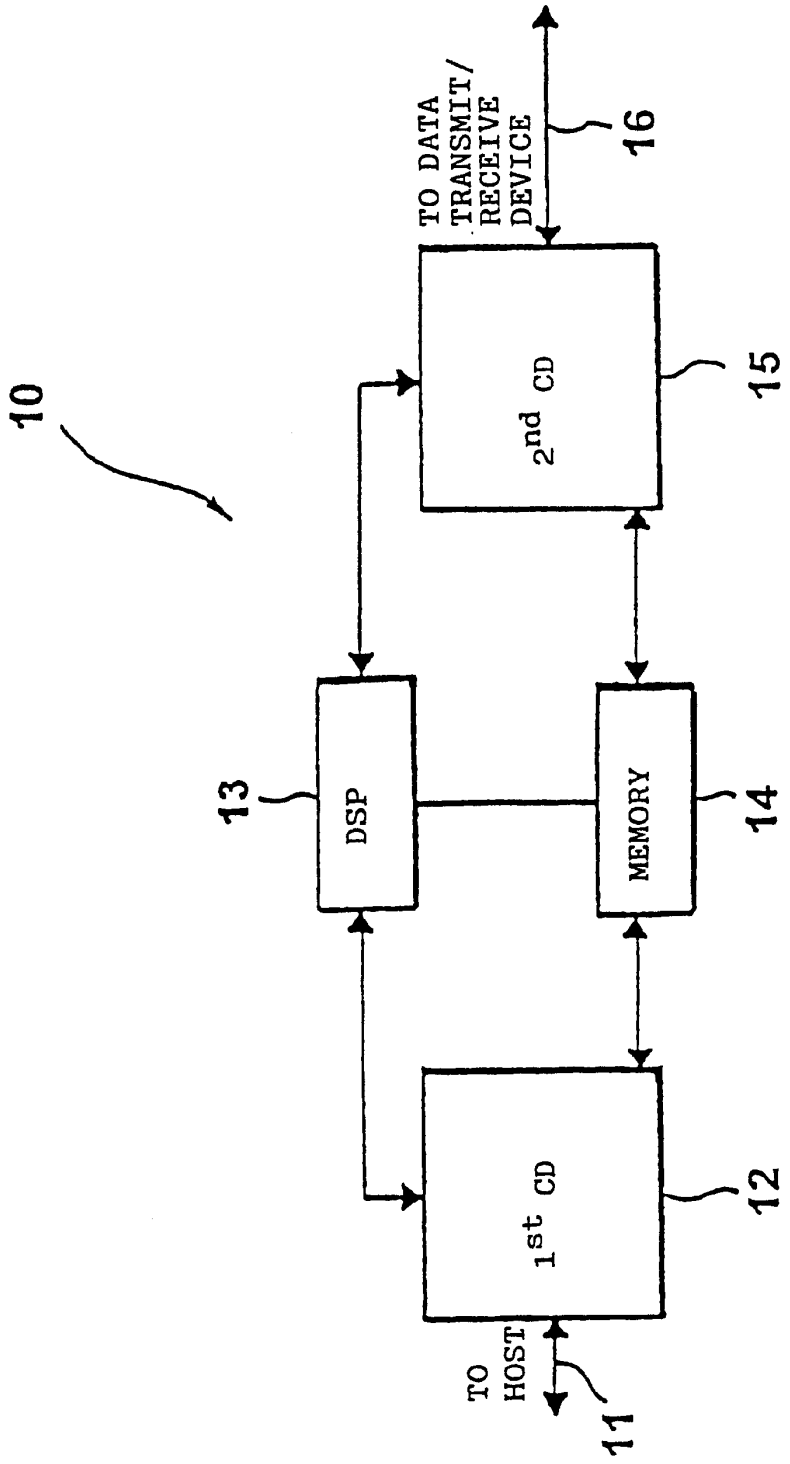
Primary Examiner—Thomas Lee
Assistant Examiner—Thuan Du
(74) *Attorney, Agent, or Firm*—Patton Boggs LLP

(57) **ABSTRACT**

An interface device **(10)** provides fast data communication between a host device with input/output interfaces and a data transmit/receive device, wherein the interface device **(10)** comprises a processor means **(13)**, a memory means **(14)**, a first connecting device **(12)** for interfacing the host device with the interface device, and a second connecting device **(15)** for interfacing the interface device **(10)** with the data transmit/receive device. The interface device **(10)** is configured by the processor means **(13)** and the memory means **(14)** in such a way that, when receiving an inquiry from the host device via the first connecting device **(12)** as to the type of a device attached to the host device, regardless of the type of the data transmit/receive device, the interface device sends a signal to the host device via the first connecting device **(12)** which signals to the host device that it is communicating with an input/output device.

15 Claims, 2 Drawing Sheets




10
TO DATA TRANSMIT/ RECEIVE DEVICE
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2nd CD
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DSP
MEMORY
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1st CD
12
TO HOST
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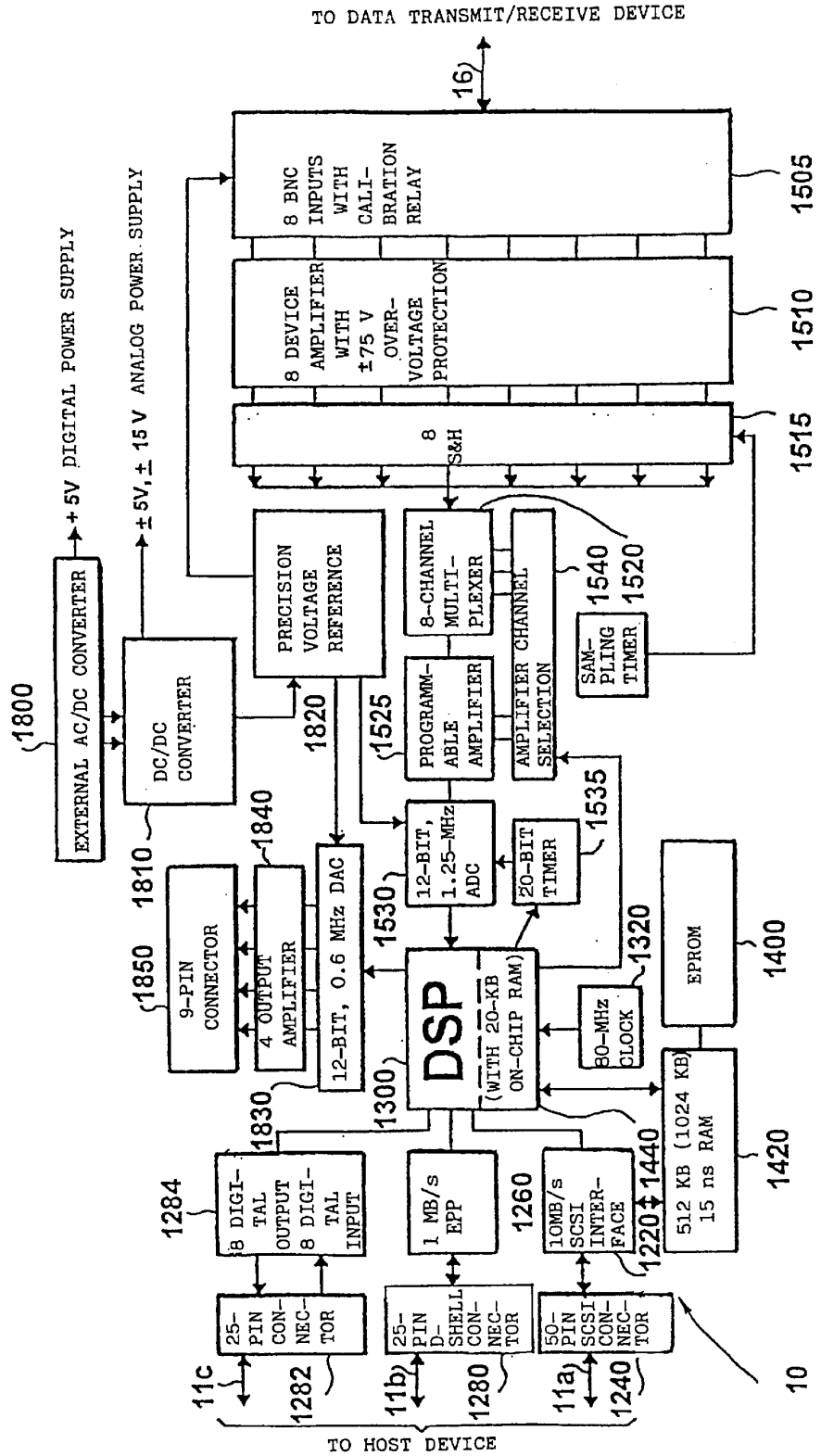
FIG. 1


TO DATA TRANSMIT/RECEIVE DEVICE
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8 BNC INPUTS WITH CALI-BRATION RELAY
1505
8 DEVICE AMPLIFIER WITH ±75 V OVER-VOLTAGE PROTECTION
1510
8 S&H
1515
+5V DIGITAL POWER SUPPLY
±5V, ± 15 V ANALOG POWER SUPPLY
1800
EXTERNAL AC/DC CONVERTER
DC/DC CONVERTER
PRECISION VOLTAGE REFERENCE
1820
8-CHANNEL MULTI-PLEXER
1540
1520
SAM-PLING TIMER
PROGRAMM-ABLE AMPLIFIER
1525
AMPLIFIER CHANNEL SELECTION
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1840
1810
9-PIN CONNECTOR
1850
4 OUTPUT AMPLIFIER
12-BIT, 0.6 MHz DAC
1530
12-BIT, 1.25-MHz ADC
20-BIT TIMER
DSP
(WITH 20-KB ON-CHIP RAM)
1300
80-MHz CLOCK
1320
EPROM
1400
1830
1284
8 DIGI-TAL OUTPUT
8 DIGI-TAL INPUT
1 MB/s EPP
1260
10MB/s SCSI INTER-FACE
1220
1440
512 KB (1024 KB) 15 ns RAM
1420
25-PIN CON-NEC-TOR
1282
25-PIN D-SHELL CON-NEC-TOR
1280
50-PIN SCSI CON-NEC-TOR
1240
11c
11b
11a
10
TO HOST DEVICE

FIG.2

FLEXIBLE INTERFACE FOR COMMUNICATION BETWEEN A HOST AND AN ANALOG I/O DEVICE CONNECTED TO THE INTERFACE REGARDLESS THE TYPE OF THE I/O DEVICE

FIELD OF THE INVENTION

The present invention relates to the transfer of data and in particular to interface devices for communication between a computer or host device and a data transmit/receive device from which data is to be acquired or with which two-way communication is to take place.

BACKGROUND OF THE INVENTION

Existing data acquisition systems for computers are very limited in their areas of application. Generally such systems can be classified into two groups.

In the first group host devices or computer systems are attached by means of an interface to a device whose data is to be acquired. The interfaces of this group are normally standard interfaces which, with specific driver software, can be used with a variety of host systems. An advantage of such interfaces is that they are largely independent of the host device. However, a disadvantage is that they generally require very sophisticated drivers which are prone to malfunction and which limit data transfer rates between the device connected to the interface and the host device and vice versa. Further, it is often very difficult to implement such interfaces for portable systems and they offer few possibilities for adaptation with the result that such systems offer little flexibility.

The devices from which data is to be acquired cover the entire electrical engineering spectrum. In a typical case, it is assumed that a customer who operates, for example, a diagnostic radiology system in a medical engineering environment reports a fault. A field service technician of the system manufacturer visits the customer and reads system log files generated by the diagnostic radiology system by means a portable computer or laptop for example. If the fault cannot be localized or if the fault is intermittent, it will be necessary for the service technician to read not only an error log file but also data from current operation. It is apparent that in this case fast data transfer and rapid data analysis are necessary.

Another case requiring the use of an interface could be, for example, when an electronic measuring device, e.g. a multimeter, is attached to a computer system to transfer the data measured by the multimeter to the computer. Particularly when long-term measurements or large volumes of data are involved is it necessary for the interface to support a high data transfer rate.

From these randomly chosen examples it can be seen that an interface may be put to totally different uses. It is therefore desirable that an interface be sufficiently flexible to permit attachment of very different electrical or electronic systems to a host device by means of the interface. To prevent operator error, it is also desirable that a service technician is not required to operate different interfaces in different ways for different applications but that, if possible, a universal method of operating the interface be provided for a large number of applications.

To increase the data transfer rates across an interface, the route chosen in the second group of data acquisition systems for the interface devices was to specifically match the

interface very closely to individual host systems or computer systems. The advantage of this solution is that high data transfer rates are possible. However, a disadvantage is that the drivers for the interfaces of the second group are very closely matched to a single host system with the result that they generally cannot be used with other host systems or their use is very ineffective. Further, such types of interface have the disadvantage that they must be installed inside the computer casing to achieve maximum data transfer rates as they access the internal host bus system. They are therefore generally not suitable for portable host systems in the form of laptops whose minimum possible size leaves little internal space to plug in an interface card.

DESCRIPTION OF PRIOR ART

A solution to this problem is offered by the interface devices of IOtech (business address: 25971 Cannon Road, Cleveland, Ohio 44146, USA) which are suitable for laptops such as the WaveBook/512 (registered trademark). The interface devices are connected by means of a plug-in card, approximately the size of a credit card, to the PCMCIA interface which is now a standard feature in laptops. The plug-in card converts the PCMCIA interface into an interface known in the art as IEEE 1284. The said plug-in card provides a special printer interface which is enhanced as regards the data transfer rate and delivers a data transfer rate of approximately 2 MBps as compared with a rate of approx. 1 MBps for known printer interfaces. The known interface device generally consists of a driver component, a digital signal processor, a buffer and a hardware module which terminates in a connector to which the device whose data is to be acquired is attached. The driver component is attached directly to the enhanced printer interface thus permitting the known interface device to establish a connection between a computer and the device whose data is to be acquired.

In order to work with the said interface, an interface-specific driver must be installed on the host device so that the host device can communicate with the digital signal processor of the interface card. As described above, the driver must be installed on the host device. If the driver is a driver developed specifically for the host device, a high data transfer rate is achieved but the driver cannot be easily installed on a different host system. However, if the driver is a general driver which is as flexible as possible and which can be used on many host devices, compromises must be accepted with regard to the data transfer rate.

Particularly in an application for multi-tasking systems in which several different tasks such as data acquisition, data display and editing are to be performed quasi-simultaneously, each task is normally assigned a certain priority by the host system. A driver supporting a special task requests the central processing system of the host device for processor resources in order to perform its task. Depending on the particular priority assignment method and on the driver implementation, a particular share of processor resources is assigned to a special task in particular time slots. Conflicts arise if one or more drivers are implemented in such a way that they have the highest priority by default, i.e. they are incompatible, as happens in practice in many applications. It may occur that both drivers are set to highest priority which, in the worst case, can result in a system crash.

EP 0685799 A1 discloses an interface by means of which several peripheral devices can be attached to a bus. An interface is connected between the bus of a host device and various peripheral devices. The interface comprises a finite

state machine and several branches each of which is assigned to a peripheral device. Each branch comprises a data manager, cycle control, user logic and a buffer. This known interface device provides optimal matching between a host device and a specific peripheral device.

The specialist publication IBM Technical Disclosure Bulletin, Vol. 38, No. 05, page 245; "Communication Method between Devices through FDD Interface" discloses an interface which connects a host device to a peripheral device via a floppy disk drive interface. The interface consists in particular of an address generator, an MFM encoder/decoder, a serial/parallel adapter and a format signal generator. The interface makes it possible to attach not only a floppy disk drive but also a further peripheral device to the FDD host controller of a host device. The host device assumes that a floppy disk drive is always attached to its floppy disk drive controller and communication is initiated if the address is correct. However, this document contains no information as to how communication should be possible if the interface is connected to a multi-purpose interface instead of to a floppy disk drive controller.

SUMMARY OF THE INVENTION

It is an object of the present invention to provide an interface device for communication between a host device and a data transmit/receive device whose use is host device-independent and which delivers a high data transfer rate.

In accordance with a first aspect of the present invention, this object is met by an interface device for communication between a host device, which comprises drivers for input/output devices customary in a host device and a multi-purpose interface, and a data transmit/receive device comprising: a processor; a memory; a first connecting device for interfacing the host device with the interface device via the multi-purpose interface of the host device; and a second connecting device for interfacing the interface device with the data transmit/receive device, wherein the interface device is configured by the processor and the memory in such a way that the interface device, when receiving an inquiry from the host device as to the type of a device attached to the multi-purpose interface of the host device, sends a signal, regardless of the type of the data transmit/receive device attached to the second connecting device of the interface device, to the host device which signals to the host device that it is an input/output device customary in a host device, whereupon the host device communicates with the interface device by means of the driver for the input/output device customary in a host device.

In accordance with a second aspect of the present invention, this object is met by an interface device for communication between a host device, which comprises a multi-purpose interface and a specific driver for this interface, and a data transmit/receive device comprising: a processor; a memory; a first connecting device for interfacing the host device with the interface device via the multi-purpose interface of the host device; and a second connecting device for interfacing the interface device with the data transmit/receive device, wherein the interface device is configured using the processor and the memory in such a way that the interface device, when receiving an inquiry from the host device as to the type of a device attached at the multi-purpose interface of the host device, sends a signal, regardless of the type of the data transmit/receive device attached to the second connecting device of the interface device, to the host device which signals to the host device that it is an input/output device customary in a host device, whereupon the host device communicates with the interface device by means of the specific driver for the multi-purpose interface.

In accordance with a third aspect of the present invention, this object is met by a method of communication between a host device, which comprises drivers for input/output devices customary in a host device and a multi-purpose interface, and a data transmit/receive device via an interface device comprising the steps of interfacing of the host device with a first connecting device of the interface device via the multi-purpose interface of the host device; interfacing of the data transmit/receive device with a second connecting device of the interface device; inquiring by the host device at the interface device as to the type of device to which the multi-purpose interface of the host device is attached; regardless of the type of the data transmit/receive device attached to the second connecting device of the interface device, responding to the inquiry from the host device by the interface device in such a way that it is an input/output device customary in a host device, whereupon the host device communicates with the interface device by means of the usual driver for the input/output device.

The present invention is based on the finding that both a high data transfer rate and host device-independent use can be achieved if a driver for an input/output device customary in a host device, normally present in most commercially available host devices, is utilized. Drivers for input/output devices customary in a host device which are found in practically all host devices are, for example, drivers for hard disks, for graphics devices or for printer devices. As however the hard disk interfaces in common host devices which can be, for example, IBM PCs, IBM-compatible PCs, Commodore PCs, Apple computers or even workstations, are the interfaces with the highest data transfer rate, the hard disk driver is utilized in the preferred embodiment of the interface device of the present invention. Drivers for other storage devices such as floppy disk drives, CD-ROM drives or tape drives could also be utilized in order to implement the interface device according to the present invention.

As described in the following, the interface device according to the present invention is to be attached to a host device by means of a multi-purpose interface of the host device which can be implemented, for example, as an SCSI interface or as an enhanced printer interface. Multi-purpose interfaces comprise both an interface card and specific driver software for the interface card. The driver software can be designed so that it can replace the BIOS driver routines. Communication between the host device and the devices attached to the multi-purpose interface then essentially takes place by means of the specific driver software for the multi-purpose interface and no longer primarily by means of BIOS routines of the host device. Recently however drivers for multi-purpose interfaces can also already be integrated in the BIOS system of the host device as, alongside classical input/output interfaces, multi-purpose interfaces are becoming increasingly common in host devices. It is of course also possible to use BIOS routines in parallel with the specific driver software for the multi-purpose interface, if this is desired.

The interface device according to the present invention comprises a processor means, a memory means, a first connecting device for interfacing the host device with the interface device, and a second connecting device for interfacing the interface device with the data transmit/receive device. The interface device is configured by the processor means and the memory means in such a way that the interface device, when receiving an inquiry from the host

device via the first connecting device as to the type of a device attached to the host device, sends a signal, regardless of the type of the data transmit/receive device, to the host device via the first connecting device which signals to the host device that it is communicating with an input/output device. The interface device according to the present invention therefore simulates, both in terms of hardware and software, the way in which a conventional input/output device functions, preferably that of a hard disk drive. As support for hard disks is implemented as standard in all commercially available host systems, the simulation of a hard disk, for example, can provide host device-independent use. The interface device according to the present invention therefore no longer communicates with the host device or computer by means of a specially designed driver but by means of a program which is present in the BIOS system (Basic Input/Output System) and is normally precisely matched to the specific computer system on which it is installed, or by means of a specific program for the multi-purpose interface. Consequently, the interface device according to the present invention combines the advantages of both groups. On the one hand, communication between the computer and the interface takes place by means of a host device-specific BIOS program or by means of a driver program which is matched to the multi-purpose interface and which could be regarded as a "device-specific driver". On the other hand, the BIOS program or a corresponding multi-purpose interface program which operates one of the common input/output interfaces in host systems is therefore present in all host systems so that the interface device according to the present invention is host device-independent.

BRIEF DESCRIPTION OF THE DRAWINGS

In the following, preferred embodiments of the present invention will be explained in more detail with reference to the drawings enclosed, in which:

FIG. **1** shows a general block diagram of the interface device according to the present invention; and

FIG. **2** shows detailed block diagram of an interface device according to a preferred embodiment of the present invention.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

FIG. **1** shows a general block diagram of an interface device **10** according to the present invention. A first connecting device **12** of the interface device **10** can be attached to a host device (not shown) via a host line **11**. The first connecting device is attached both to a digital signal processor **13** and to a memory means **14**. The digital signal processor **13** and the memory means **14** are also attached to a second connecting device **15** by means of bidirectional communication lines (shown for all lines by means of two directional arrows). The second connecting device can be attached by means of an output line **16** to a data transmit/receive device which is to receive data from the host device or from which data is to be read, i.e. acquired, and transferred to the host device. The data transmit/receive device itself can also communicate actively with the host device via the first and second connecting device, as described in more detail in the following.

Communication between the host system or host device and the interface device is based on known standard access commands as supported by all known operating systems (e.g. DOS, Windows, Unix). Preferably, the interface device according to the present invention simulates a hard disk with a root directory whose entries are "virtual" files which can be created for the most varied functions. When the host device system with which the interface device according to the present invention is connected is booted and a data transmit/receive device is also attached to the interface device **10**, usual BIOS routines or multi-purpose interface programs issue an instruction, known by those skilled in the art as the INQUIRY instruction, to the input/output interfaces in the host device. The digital signal processor **13** receives this inquiry instruction via the first connecting device and generates a signal which is sent to the host device (not shown) again via the first connecting device **12** and the host line **11**. This signal indicates to the host device that, for example, a hard disk drive is attached at the interface to which the INQUIRY instruction was sent. Optionally, the host device can send an instruction, known by those skilled in the art as "Test Unit Ready", to the interface device to request more precise details regarding the queried device.

Regardless of which data transmit/receive device at the output line **16** is attached to the second connecting device, the digital signal processor **13** informs the host device that it is communicating with a hard disk drive. If the host device receives the response that a drive is present, it then sends a request to the interface device **10** to read the boot sequence which, on actual hard disks, normally resides on the first sectors of the disk. The digital signal processor **13**, whose operating system in stored in the memory means **14**, responds to this instruction by sending to the host device a virtual boot sequence which, in the case of actual drives, includes the drive type, the starting position and the length of the file allocation table (FAT), the number of sectors, etc., known to those skilled in the art. Once the host device has received this data, it assumes that the interface device **10** according to a preferred embodiment of the present invention is a hard disk drive. In reply to an instruction from the host device to display the directory of the "virtual" hard disk drive simulated by the interface device **10** with respect to the host device, the digital signal processor can respond to the host device in exactly the same way as a conventional hard disk would, namely by reading on request the file allocation table or FAT on a sector specified in the boot sequence, normally the first writable sector, and transferring it to the host device, and subsequently by transferring the directory structure of the virtual hard disk. Further, it is possible that the FAT is not read until immediately prior to reading or storing the data of the "virtual" hard disk and not already at initialization.

In a preferred embodiment of the present invention, the digital signal processor **13**, which need not necessarily be implemented as a digital signal processor but may be any other kind of microprocessor, comprises a first and a second command interpreter. The first command interpreter carries out the steps described above whilst the second command interpreter carries out the read/write assignment to specific functions. If the user now wishes to read data from the data transmit/receive device via the line **16**, the host device sends a command, for example "read file xy", to the interface device. As described above, the interface device appears to the host device as a hard disk. The second command interpreter of the digital signal processor now interprets the read command of the host processor as a data transfer command, by decoding whether "xy" denotes, for example, a "real-time input" file, a "configuration" file or an executable file, whereby the same begins to transfer data from the data transmit/receive device via the second connecting device to the first connecting device and via the line **11** to the host device.

Preferably, the volume of data to be acquired by a data transmit/receive device is specified in a configuration file described in the following by the user specifying in the said configuration file that a measurement is to last, for example, five minutes. To the host device the "real-time input" file then appears as a file whose length corresponds to the anticipated volume of data in those five minutes. Those skilled in the art know that communication between a processor and a hard disk consists of the processor transferring to the hard disk the numbers of the blocks or clusters or sectors whose contents it wishes to read. By reference to the FAT the processor knows which information is contained in which block. In this case, communication between the host device and the interface device according to the present invention therefore consists of the very fast transfer of block numbers and preferably of block number ranges because a virtual "real-time input" file will not be fragmented. If the host device now wants to read the "real-time input" file, it transfers a range of block numbers to the interface device, whereupon data commences to be received via the second connecting device and data commences to be sent to the host device via the first connecting device.

In addition to the digital signal processor instruction memory, which comprises the operating system of the digital signal processor and can be implemented as an EPROM or EEPROM, the memory means **14** can have an additional buffer for purposes of synchronizing data transfer from the data transmit/receive device to the interface device **10** and data transfer from the interface device **10** to the host device.

Preferably, the buffer is implemented as a fast random access memory or RAM buffer.

Further, from the host device the user can also create a configuration file, whose entries automatically set and control various functions of the interface device **10**, on the interface device **10** which appears to the host device as a hard disk. These settings can be, for example, gain, multiplex or sampling rate settings. By creating and editing a configuration file, normally a text file which is simple to understand with little prior knowledge, users of the interface device **10** are able to perform essentially identical operator actions for almost any data transmit/receive devices which can be attached to the second connecting device via the line **16**, thus eliminating a source of error arising from users having to know many different command codes for different applications. In the case of the interface device **10** according to the present invention it is necessary for users to note the conventions of the configuration file once only in order to be able to use the interface device **10** as an interface between a host device and almost any data transmit/receive device.

As a result of the option of storing any files in agreed formats in the memory means **14** of the interface device **10**, taking into account the maximum capacity of the memory means, any enhancements or even completely new functions of the interface device **10** can be quickly implemented. Even files executable by the host device, such as batch files or executable files (BAT or EXE files), and also help files can be implemented in the interface device, thus achieving independence of the interface device **10** from any additional software (with the exception of the BIOS routines) of the host device. On the one hand, this avoids licensing and/or registration problems and, on the other hand, installation of certain routines which can be frequently used, for example an FFT routine to examine acquired time-domain data in the frequency domain, is rendered unnecessary as the EXE files are already installed on the interface device **10** and appear in the virtual root directory, by means of which the host device can access all programs stored on the interface device **10**.

In a preferred embodiment of the present invention in which the interface device **10** simulates a hard disk to the host device, the interface device is automatically detected and readied for operation when the host system is powered up or booted. This corresponds to the plug-and-play standard which is currently finding increasingly widespread use. The user is no longer responsible for installing the interface device **10** on the host device by means of specific drivers which must also be loaded; instead the interface device **10** is automatically readied for operation when the host system is booted.

For persons skilled in the art it is however obvious that the interface device **10** is not necessarily signed on when the computer system is powered up but that a special BIOS routine or a driver for a multi-purpose interface can also be started on the host device during current operation of the computer system in order to sign on or mount the interface device **10** as an additional hard disk. This embodiment is suitable for larger workstation systems which are essentially never powered down as they perform, e.g. mail functions or monitor processes which run continuously, for example, in multi-tasking environments.

In the interface device according to the present invention an enormous advantage is to be gained, as apparent in the embodiment described in the following, in separating the actual hardware required to attach the interface device **10** to the data transmit/receive device from the communication unit, which is implemented by the digital signal processor **13**, the memory means **14** and the first connecting device **12**, as this allows a plurality of dissimilar device types to be operated in parallel in identical manner. Accordingly, many interface devices **10** can be connected to a host device which then sees many different "virtual" hard disks. In addition, any modification of the specific hardware symbolized by the second connecting device **15** can be implemented essentially without changing the operation of the interface device according to the present invention. Further, an experienced user can intervene at any time on any level of the existing second connecting device by making use of the above mentioned option of creating a configuration file or adding or storing new program sections for the second connecting device.

An important advantage of the interface device **10** of the present invention is that it also permits extremely high data transfer rates by using, for data interchange, the host device-own BIOS routines which are optimized for each host device by the host device manufacturer or BIOS system manufacturer, or by using driver programs which are normally optimized and included by the manufacturers of multi-purpose interfaces. Furthermore, due to the simulation of a virtual mass storage device, the data is managed and made available in such a way that it can be transferred directly to other storage media, e.g. to an actual hard disk of the host device without, as it were, intervention of the host device processor. The only limitation to long-term data transfer at high speed is therefore imposed exclusively by the speed and the size of the mass storage device of the host device. This is the case as the digital signal processor **13** already formats the data read by the data transmit/receive device via the second connecting device **15** into block sizes suitable for a hard disk of the host device, whereby the data transfer speed is limited only by the mechanical latency of the hard disk system of the host device. At this point, it should be noted that normally data flow from a host device must be formatted in blocks to permit writing to a hard disk and subsequent reading from a hard disk, as known by those skilled in the art.

The said data transfer rate can be increased further by setting up a direct memory access (DMA) or RAM drive in the host system. As those skilled in the art know, the setting up of a RAM drive requires processor resources of the host device, with the result that the advantage of writing the data to a hard disk drive of the host device essentially without the need for processor resources is lost.

As described above, a data buffer can be implemented in the memory means **14** to permit independence in terms of time of the data transmit/receive device attached to the second connecting device from the host device attached to the first connecting device. This guarantees error-free operation of the interface device **10** even for time-critical applications in multi-tasking host systems.

FIG. **2** shows a detailed block diagram of an interface device **10** according to the present invention.

A digital signal processor (DSP) **1300** is, in a manner of speaking, the heart of the interface device **10**. The DSP can be any DSP but preferably has a 20-MB on-chip random access memory (RAM). Certain instruction sets, for example, can be stored in the RAM already integrated in the DSP. An 80-MHz clock generator is attached to the DSP **1300** in order to synchronize the DSP. The DSP implements a fast Fourier transformation (FFT) in real time and also optional data compression of the data to be transferred from the data transmit/receive device to the host device in order to achieve greater efficiency and to permit interoperation with host devices which have a smaller memory.

In the preferred embodiment of the interface device **10** shown in FIG. **2**, the first connecting device **12** of FIG. **1** contains the following components: an SCSI interface **1220** and a 50-pin SCSI connector **1240** for attachment to an SCSI interface present on most host devices or laptops. The SCSI (small computer system interface) interface **1220** translates the data received via the SCSI connector **1240** into data understood by the DSP **1300**, as known by those skilled in the art. Further, the first connecting device **12** comprises an EPP (enhanced parallel port) with a data transfer rate of approx. 1 MBps which delivers a more moderate data transfer rate of 1 MBps by comparison to the data transfer rate of 10 MBps of the SCSI interface. The EPP **1260** is connected to a 25-pin D-shell connector **1280** to permit attachment to a printer interface of a host device for example. Optionally, the first connecting device **12** also comprises a 25-pin connector **1282** which permits the attachment of 8 digital outputs and 8 digital inputs **1284** at a host device.

Preferably, the second connecting device comprises 8 BNC inputs with the calibration relay **1505**, a block **1510** with 8 device amplifiers with an overvoltage protection of ±75 V, this block being connected in turn to 8 sample/hold (S&H) circuits **1515**. The calibration relays are relays which permit controlled changeover between a test voltage and a calibration reference voltage. Each sample/hold circuit is connected to a corresponding input of an 8-channel multiplexer **1520** which feeds its output signals via a programmable amplifier **1525** into an analog/digital converter (ADC) with 12 bit and 1.25 MHz **1530** and to the DSP **1300**. The ADC **1530** is controlled by means of a 20-bit timer **1535**, as known by persons skilled in the art. The programmable amplifier **1525** and the 8-channel multiplexer **1520** are controlled via an amplifier channel selection circuit **1540** which is in turn controlled by the DSP **1300**.

The complete interface device **10** is supplied with power by an external AC/DC converter **1800** which delivers a digital supply voltage of ±5 V and is attached to a DC/DC converter **1810** which can deliver analog supply voltages of ±5 V and ±15 V as required for the interface device **10**. Further, the DC/DC converter controls a precision voltage reference **1820** which controls the 8 BNC inputs **1505** and the ADC **1530** as well as a digital/analog converter (DAC) **1830** which permits, via an output amplifier block with 4 output amplifiers **1840** and a 9-pin connector **1850**, analog output direct from the DSP **1300** to an output device, e.g. printer device or monitor device, which can be attached via the 9-pin connector **1850**, thus providing the option of monitoring the data transferred to the host device or also, for example, of viewing an FFT to obtain rapid and comprehensive data analysis without using processor time of the host device.

In FIG. **2** the memory means **14** of FIG. **1** is implemented by an EPROM **1400** which, in a preferred embodiment of the present invention, contains the operating system of the digital signal processor **1300**. A random access memory with an access time of 15 ns and a size of 512 KB or optionally 1024 KB **1420** serves as a data buffer to achieve independence in terms of time of the output line **16** from the output lines **11***a*, **11***b* and **11***c* to the data transmit/receive device and to the host device respectively. As described above, in a preferred embodiment of the present invention the digital signal processor **1300** already contains a 20-KB on-chip RAM **1440** which can store certain instruction sets, functions and also smaller application software units.

The connection, symbolized by the line **16**, of the interface device **10** to any data transmit/receive device implements, by means of the blocks 1505–1535, an analog input with a sampling rate of 1.25 MHz and quantization of 12 bits. There are 8 channels with an overvoltage protection of ±75 V. By means of the programmable amplifier **1525** the channels can be programmed independently of each other in voltage ranges up to a maximum of ±10 V. Unused channels can be grounded internally to reduce channel intermodulation. The block **1515** is implemented as a monolithic high-precision, high-speed sample/hold amplifier for simultaneous sampling of all channels. The precision voltage reference **1820** provides a high-precision, temperature-compensated monolithic energy gap voltage reference for auto-calibration of each channel and each gain. Further, offset fine adjustment for each channel is implemented by the same.

The blocks **1830**, **1840** and **1850** implement a direct analog output for the digital signal processor **1300**, and the DAC **1830** provides a data transfer rate of 625 kHz and a quantization of 12 bits. The block **1840** comprises 4 channels with a common output latch.

Further, the interface device **10** comprises a digital input/output device implemented by the blocks **1284** and **1282**. Here there are 8 digital inputs, 8 digital outputs with a common latch, and the digital port can be attached preferably to a side panel of the interface device **10** so that the port itself can easily be accessed.

The digital signal processor **1300** provides on-board digital data processing. In particular, it is a high-performance DSP with a clock speed of 80 MHz and a 20-bit timer **1535**.

As described above, the first connecting device **12** comprises the SCSI interface **1220** with a peak transfer rate of 10 MBps. An optional PCMCIA-to-SCSI adapter permits high-speed communication with laptop computers which are desirable and in widespread use, particularly by mobile service technicians. The EPP **1260** with its associated connector **1280** permits data transfer at a more moderate rate.

As described above, the interface device **10** is supplied with power by means of an external AC/DC adapter which

has a universal power input (85–264 VAC, 47–63 Hz). Interference suppression complies with the standards EN **55022**, curve B and FFC, Class B). Further, it is also in accordance with international safety regulations (TÜV, UL, CSA). The interface device **10** is externally shielded and achieves a value of 55 dB at 30–60 MHz and a value of approximately 40 dB at 1 GHz, and therefore complies with the MILSTD 285-1 standard.

As described above, communication between the host device and the multi-purpose interface can take place not only via drivers for input/output device customary in a host device which reside in the BIOS system of the host device but also via specific interface drivers which, in the case of SCSI interfaces, are known as multi-purpose interface ASPI (advanced SCSI programming interface) drivers. This ASPI driver, which can also be referred to as an ASPI manager, is specific to a special SCSI host adapter, i.e. to a special multi-purpose interface, and is normally included by the manufacturer of the multi-purpose interface. Generally speaking, this multi-purpose interface driver has the task of moving precisely specified SCSI commands from the host system program to the host system SCSI adapter. For this reason, the command set is almost identical to that of the SCSI interface itself. Essentially, only status and reset commands for the host adapter have been added.

The ASPI driver can be used if the hard disk was not already addressable at boot time or if the SCSI-related BIOS routines of the host computer were still disabled. Here too, the steps needed to initialize the interface device, preferably as a virtual hard disk, are similar to the steps taken when initializing at boot time.

In general terms, the ASPI manager comprises two sides. One side is the proprietary, hardware-oriented side. It is responsible for converting all commands into a form required by the corresponding multi-purpose interface. The hardware-oriented side of the ASPI driver is therefore matched to a very specific type of multi-purpose interface or SCSI interface. The other side is known as the user software side. This side is totally independent of the proprietary operating characteristics of the SCSI adapter and is therefore identical for all SCSI interfaces. This permits SCSI programming which is however independent of the individual SCSI adapter types.

In contrast to communication between the host device and the interface device according to the present invention on the basis of a BIOS driver, the use of such an ASPI driver for communication between the host device and the interface device according to the present invention allows various further possibilities of the SCSI multi-purpose interface to be exploited. In the case described above, the interface device which preferably signs on and behaves as a virtual hard disk is detected by the BIOS driver of the host computer at boot time and is configured as a hard disk. This step does not however support active requests sent by the interface device to the host computer. If however the virtual hard disk wishes to write data actively to, for example, a hard disk of the host computer or wishes to initiate communication with the processor of the host computer, the host computer must recognize the request of the virtual hard disk and tolerate a further issuer of instructions on its bus. If the interface device behaves solely like a virtual hard disk, it would always receive and never issue commands. The BIOS has no objections to an additional issuer of commands that actively wishes to place data on the bus of the host device but the BIOS does not support the host device in recognizing corresponding requests of the interface device or in granting the interface device permission to access the bus.

Using the ASPI manager the interface device according to the present invention can now obtain active access to an SCSI hard disk of the host device connected to the same SCSI bus which, in contrast to the interface device, cannot be a virtual but a real SCSI mass storage device or also a further interface device according to the present invention. Thereupon, the interface device according to the present invention can write the desired data to the SCSI hard disk of the host computer totally independently of the host computer or can communicate with the same in some other manner. The interface device according to the present invention therefore initially behaves passively as a virtual hard disk and then, as required and using the driver software for the multi-purpose interface, actively on the same SCSI bus. This means however that the interface device according to the present invention, using a driver software for the multi-purpose interface which comprises the BIOS routines customary in host devices and simultaneously provides the option of active participation, can, regardless of the type of the data transmit/receive device attached to the second connecting device, behave initially as a virtual and at the same time passive hard disk but can, as required, participate actively on the bus so as to be able to initiate communication directly with other SCSI hard disks of the host device by bypassing the processor of the host device.

Using a standard interface of a host device, the interface device according to the present invention permits communication with any host device. By simulating an input/output device to the host device and, in a preferred embodiment, by simulating a virtual mass storage device, the interface device **10** is automatically supported by all known host systems without any additional sophisticated driver software. The simulation of a freely definable file structure on the "virtual" hard disk provides simple operation and expansion options and, through the implementation of any programs, independence from special software implemented on the host device. Help files included on the interface device **10** and plug-and-play support ensure ease of use even in portable, flexible host devices. Despite the very simple user interface, experienced users are free at any time to intervene in the functions of the interface device **10** on system level. The interface device **10** thus provides a universal solution which can cover the entire spectrum of possible data transmit/receive devices.

What is claimed is:

1. An interface device for communication between a host device, which comprises drivers for input/output devices customary in a host device and a multi-purpose interface, and a data transmit/receive device, the data transmit/receive device being arranged for providing analog data, comprising:

a processor;

a memory;

a first connecting device for interfacing the host device with the interface device via the multi-purpose interface of the host device; and

a second connecting device for interfacing the interface device with the data transmit/receive device, the second connecting device including a sampling circuit for sampling the analog data provided by the data transmit/receive device and an analog-to-digital converter for converting data sampled by the sampling circuit into digital data,

wherein the interface device is configured by the processor and the memory to include a first command interpreter and a second command interpreter,

wherein the first command interpreter is configured in such a way that the command interpreter, when receiving an inquiry from the host device as to a type of a device attached to the multi-purpose interface of the

host device, sends a signal, regardless of the type of the data transmit/receive device attached to the second connecting device of the interface device, to the host device which signals to the host device that it is an input/output device customary in a host device, whereupon the host device communicates with the interface device by means of the driver for the input/output device customary in a host device, and

wherein the second command interpreter is configured to interpret a data request command from the host device to the type of input/output device signaled by the first command interpreter as a data transfer command for initiating a transfer of the digital data to the host device.

2. An interface device according to claim **1**,

wherein the drivers for input/output drivers customary in a host device comprise a hard disk driver, and the signal indicates to the host device that the host device is communicating with a hard disk.

3. An interface device according to claim **1**,

wherein the memory means comprises a buffer to buffer data to be transferred between the data transmit/receive device and the host device.

4. An interface device according to claim **1**,

wherein the multi-purpose interface of the host device is an SCSI interface and the first connecting device also comprises an SCSI interface.

5. An interface device according to claim **1**,

wherein the processor is a digital signal processor.

6. An interface device according to claim **2**,

wherein the data to be transferred from the data transmit/receive device to the host device in the interface device is formatted in a suitable format for a hard disk present in the host device.

7. An interface device according to claim **2**,

which further comprises a root directory and virtual files which are present on the signaled hard disk drive and which can be accessed from the host device.

8. An interface device according to claim **7**,

wherein the virtual files comprise a configuration file in text format which are stored in the memory means and using which the user can configure the interface device for a specific data transmit/receive device.

9. An interface device according to claim **7**,

wherein the virtual files comprise batch files or executable files for the microprocessor means which are stored in the interface device in order to perform data processing, independently of the host device, of data received via the second connecting device.

10. An interface device according to claim **7**,

wherein the virtual files comprise batch files or executable files for the host device which are stored in the interface device.

11. An interface device for communication between a host device, which comprises a multi-purpose interface and a specific driver for this interface, and a data transmit/receive device, the data transmit/receive device being arranged for providing analog data, comprising:

a processor;

a memory;

a first connecting device for interfacing the host device with the interface device via the multi-purpose interface of the host device; and

a second connecting device for interfacing the interface device with the data transmit/receive device, the second connecting device including a sampling circuit for sampling the analog data provided by the data transmit/receive device and an analog-to-digital converter for converting data sampled by the sampling circuit into digital data,

where the interface device is configured using the processor and the memory to include a first command interpreter and a second command interpreter,

wherein the first command interpreter is configured in such a way that the interface device, when receiving an inquiry from the host device as to the type of a device attached at the multi-purpose interface of the host device, sends a signal, regardless of the type of the data transmit/receive device attached to the second connecting device of the interface device, to the host device which signals to the host device that it is an input/output device customary in a host device, whereupon the host device communicates with the interface device by means of the specific driver for the multi-purpose interface, and

wherein the second command interpreter is configured to interpret a data request command from the host device to the type of input/output device signaled by the first command interpreter as a data transfer command for initiating a transfer of the digital data to the host device.

12. An interface device according to claim **11**, wherein in addition to the first connecting device of the interface device, there is a further input/output device at the multi-purpose interface of the host device, and wherein the interface device can communicate directly with said further input/output device via the specific driver for the multi-purpose interface.

13. An interface device according to claim **11**,

wherein the multi-purpose interface is an SCSI interface, and wherein the specific driver for the multi-purpose interface is an ASPI manager.

14. A method of communication between a host device, which comprises drivers for input/output devices customary in a host device and a multi-purpose interface, and a data transmit/receive device, the data transmit/receive device being arranged for providing analog data, via an interface device, comprising:

interfacing of the host device with a first connecting device of the interface device via the multi-purpose interface of the host device;

interfacing of the data transmit/receive device with a second connecting device of the interface device, the second connecting device including a sampling circuit for sampling the analog data provided by the data/transmit/receive device and an analog-to-digital converter for converting data sampled by the sampling circuit into digital data;

inquiring by the host device at the interface device as to the type of device to which the multi-purpose interface of the host device is attached;

regardless of the type of the data transmit/receive data attached to the second connecting device of the interface device, responding to the inquiry from the host device by the interface device in such a way that it is an input/output device customary in a host device, whereupon the host device communicates with the interface device by means of the usual driver for the input/output device, and

interpreting a data request command from the host device to the type of input/output device customary in the host device as a data transfer command for initiating a transfer of the digital data to the host device.

15. A method according to claim **14**,

wherein the drivers for input/output devices customary in a host device comprise a driver for a storage device and in particular for a hard disk drive.

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